

# **PROJECT 2**

## **DESIGN AND VERIFICATION OF AN SPI SLAVE WITH SINGLE PORT RAM**

**TEAM MEMBERS**

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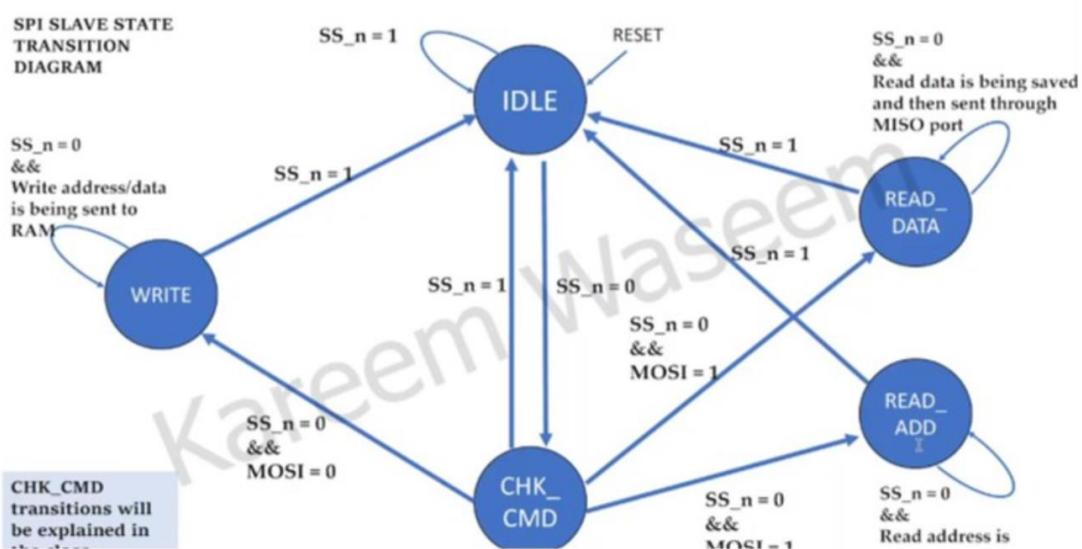
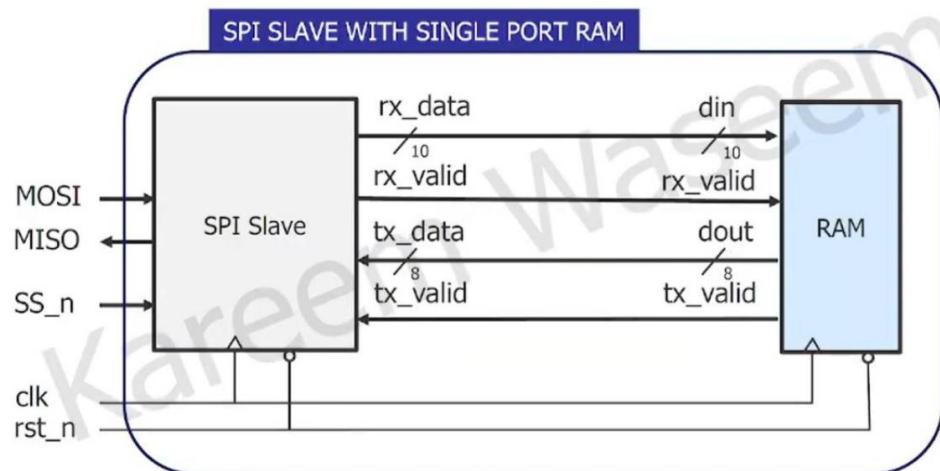
**UNDER THE SUPERVISION OF:**

**ENG. KAREEM WASEEM**

## INTRODUCTION

THIS REPORT COVERS THE DESIGN OF AN SPI SLAVE MODULE WITH A SINGLE-PORT RAM USING VERILOG. THE SPI PROTOCOL IS COMMONLY USED FOR COMMUNICATION BETWEEN A MASTER DEVICE AND PERIPHERALS. IN THIS PROJECT, THE SPI SLAVE RECEIVES DATA AND COMMANDS FROM THE MASTER, STORES THE DATA IN THE RAM, AND ALLOWS READING FROM IT.

THE SINGLE-PORT RAM ACTS AS MEMORY TO SAVE THE DATA SENT OVER SPI. THIS DESIGN DEMONSTRATES HOW SPI COMMUNICATION CAN BE COMBINED WITH MEMORY ACCESS IN A SIMPLE AND EFFECTIVE WAY.



## 1) RTL CODE

### A. SPI SLAVE

```
V SPI.v
1 module SPI (
2     input clk, rst_n, ss_n, MOSI, tx_valid,
3     input[7:0] tx_data,
4     output reg MISO, rx_valid,
5     output reg[9:0] rx_data
6 );
7 parameter IDLE = 3'b000;
8 parameter CHK_CMD = 3'b001;
9 parameter WRITE = 3'b010;
10 parameter READ_ADD = 3'b011;
11 parameter READ_DATA = 3'b100;
12
13 // (* fsm_encoding = "gray" *)
14 reg[2:0] cs, ns;
15 reg rx_type;
16 reg[4:0] cnt;
17
18 always @(posedge clk) begin
19     if(~rst_n) cs <= IDLE;
20     else cs <= ns;
21 end
22
23 always @(*) begin
24     case(cs)
25         IDLE: begin
26             if(~ss_n) ns = CHK_CMD;
27             else ns = IDLE;
28         end
29         CHK_CMD: begin
30             if(ss_n) ns = IDLE;
31             else begin
32                 if(~MOSI) ns = WRITE;
33                 else begin
34                     if(rx_type) ns = READ_DATA;
35                     else ns = READ_ADD;
36                 end
37             end
38         end
39         WRITE: begin
40             if(ss_n) ns = IDLE;
41             else ns = WRITE;
42         end
43         READ_ADD: begin
44             if(ss_n) ns = IDLE;
45             else ns = READ_ADD;
46         end
47         READ_DATA: begin
48             if(ss_n) ns = IDLE;
49             else ns = READ_DATA;
50         end
51         default: ns = IDLE;
52     endcase
53 end
54
```

```

55  always @(posedge clk) begin
56      if(~rst_n) begin
57          MISO <= 0;
58          rx_type <= 0;
59          rx_valid <= 0;
60          rx_data <= 0;
61          cnt <= 0;
62      end
63      else if (cs != IDLE && cs != CHK_CMD) begin
64          cnt <= cnt + 1;
65          rx_data <= {rx_data[8:0], MOSI};
66          if(cs == READ_ADD) rx_type <= 1;
67          else if(cs == READ_DATA) begin
68              rx_type <= 0;
69              if (tx_valid) begin
70                  if (cnt >= 11 && cnt <= 18) MISO <= tx_data[18 - cnt];
71                  else MISO <= 0;
72              end
73          end
74          if(cnt == 9) rx_valid <= 1;
75          else rx_valid <= 0;
76      end
77      else begin
78          cnt<= 0;
79          MISO <= 0;
80          rx_data <=0;
81          rx_valid <= 0;
82      end
83  end
84 endmodule

```

## B. RAM

```

V RAM.v
1  module RAM #(
2      parameter ADDR_SIZE = 8,
3      parameter MEM_DEPTH = 256
4  ) (
5      input clk, rst_n, rx_valid,
6      input[9:0] rx_data,
7      output reg tx_valid,
8      output reg[7:0] tx_data
9  );
10
11 reg[ADDR_SIZE-1:0] mem [MEM_DEPTH-1:0];
12 reg[ADDR_SIZE-1:0] wr_address, rd_address;
13
14 always @(posedge clk) begin
15     if(~rst_n) begin
16         tx_valid <= 0;
17         tx_data <= 0;
18     end
19     else begin
20         if(rx_valid) begin
21             if(rx_data[9:8] == 2'b00) begin
22                 wr_address <= rx_data[7:0];
23                 tx_valid <= 0;
24             end
25             else if(rx_data[9:8] == 2'b01) begin
26                 mem[wr_address] <= rx_data[7:0];
27                 tx_valid <= 0;
28             end
29             else if(rx_data[9:8] == 2'b10) begin
30                 rd_address <= rx_data[7:0];
31                 tx_valid <= 0;
32             end
33             else begin
34                 tx_data <= mem[rd_address];
35                 tx_valid <= 1;
36             end
37         end
38     end
39 end
40 endmodule

```

## D. SPI WRAPPER

```
V SPI_Wrapper.v
1  module SPI_Wrapper (
2    input clk, rst_n, SS_n, MOSI,
3    output MISO
4  );
5
6  wire tx_valid, rx_valid;
7  wire[7:0] tx_data;
8  wire[9:0] rx_data;
9
10 SPI slave(
11   .clk(clk), .rst_n(rst_n), .SS_n(SS_n), .MOSI(MOSI),
12   .tx_valid(tx_valid), .tx_data(tx_data), .MISO(MISO),
13   .rx_valid(rx_valid), .rx_data(rx_data)
14 );
15
16 RAM ram(
17   .clk(clk), .rst_n(rst_n), .rx_valid(rx_valid),
18   .rx_data(rx_data), .tx_valid(tx_valid), .tx_data(tx_data)
19 );
20
21 endmodule
22
```

# TESTEENCH CODE

```
 1 module SPI_Wrapper_tb();
 2   reg clk, rst_n, SS_n, MOSI;
 3   wire MISO;
 4
 5   SPI_Wrapper DUT(
 6     .clk(clk), .rst_n(rst_n), .SS_n(SS_n),
 7     .MOSI(MOSI), .MISO(MISO)
 8   );
 9
10   initial begin
11     clk = 0;
12     forever #1 clk = ~clk;
13   end
14
15   integer i;
16   reg[9:0] data;
17   initial begin
18     $readmem("mem.dat", DUT.ram.mem);
19     rst_n = 0;
20
21     repeat(2) @(negedge clk);
22
23     rst_n = 1;
24     SS_n = 1;
25     repeat(2) @(negedge clk);
26
27     // 1
28     SS_n = 0;
29     @(negedge clk);
30     MOSI = 0;
31     @(negedge clk);
32
33     // 1. Write address (0x35)
34     data = 10'b0_00110101;
```

```

17    initial begin
32        // 1. Write address (0x35)
33        data = 10'b0_00110101;
34        for(i = 9; i >= 0; i = i - 1) begin
35            MOSI = data[i];
36            @(negedge clk);
37        end
38        SS_n = 1;
39        repeat(2) @(negedge clk);
40
41        SS_n = 0;
42        @(negedge clk);
43        MOSI = 0;
44        @(negedge clk);
45
46        // 2. Write data (0xAB)
47        data = 10'b1_01010101;
48        for(i = 9; i >= 0; i = i - 1) begin
49            MOSI = data[i];
50            @(negedge clk);
51        end
52        SS_n = 1;
53        repeat(2) @(negedge clk);
54
55        SS_n = 0;
56        @(negedge clk);
57        MOSI = 1;
58        @(negedge clk);
59
60        // 3. Read address (0x35)
61        data = 10'b10_00110101;
62        for(i = 9; i >= 0; i = i - 1) begin
63            MOSI = data[i];
64            ^

```

```
 17    initial begin
 18
 19        // 3. Read Address (0x35)
 20        data = 16'b10_00110101;
 21        for(i = 9; i >= 0; i = i - 1) begin
 22            MOSI = data[i];
 23            @(negedge clk);
 24        end
 25        SS_n = 1;
 26        repeat(2) @(negedge clk);
 27
 28        SS_n = 0;
 29        @(negedge clk);
 30        MOSI = 1;
 31        @(negedge clk);
 32
 33        // 4. Read Data (0xAB)
 34        data = 16'b11_00000101;
 35        for(i = 9; i >= 0; i = i - 1) begin
 36            MOSI = data[i];
 37            @(negedge clk);
 38        end
 39        repeat(8) @(negedge clk);
 40
 41        SS_n = 1;
 42        repeat(2) @(negedge clk);
 43
 44
 45        // 2
 46        SS_n = 0;
 47        @(negedge clk);
 48        MOSI = 0;
 49        @(negedge clk);
 50
 51
 52        // 1. Write address (0xB3)
 53
```

```

V SPI_Wrapper_tb.v
17  initial begin
105   @ (negedge clk);
106
107   // 2. Write data (0xED)
108   data = 10'b1_1101101;
109   for(i = 9; i >= 0; i = i - 1) begin
110     MOSI = data[i];
111     @(negedge clk);
112   end
113   SS_n = 1;
114   repeat(2) @(negedge clk);
115
116   SS_n = 0;
117   @(negedge clk);
118   MOSI = 1;
119   @(negedge clk);
120
121   // 3. Read address (0xB3)
122   data = 10'b10_10110011;
123   for(i = 9; i >= 0; i = i - 1) begin
124     MOSI = data[i];
125     @(negedge clk);
126   end
127   SS_n = 1;
128   repeat(2) @(negedge clk);
129
130   SS_n = 0;
131   @(negedge clk);
132   MOSI = 1;
133   @(negedge clk);
134
135   // 4. Read Data (0xED)
136   data = 10'b11_00000101;
137   for(i = 9; i >= 0; i = i - 1) begin
138     MOSI = data[i];
139     @(negedge clk);
140
141   repeat(8) @(negedge clk);
142   SS_n = 1;
143
144   repeat(2) @(negedge clk);
145
146   SS_n = 0;
147   @(negedge clk);
148   MOSI = 1;
149   @(negedge clk);
150
151   // 3. Read address (0x55)
152   data = 10'b10_01010101;
153   for(i = 9; i >= 0; i = i - 1) begin
154     MOSI = data[i];
155     @(negedge clk);
156   end
157   SS_n = 1;
158   repeat(2) @(negedge clk);
159
160   SS_n = 0;
161   @(negedge clk);
162   MOSI = 1;
163   @(negedge clk);
164
165   // 4. Read Data (0x55)
166   data = 10'b11_00000101;
167   for(i = 9; i >= 0; i = i - 1) begin
168     MOSI = data[i];
169     @(negedge clk);
170   end
171   repeat(10) @(negedge clk);
172   SS_n = 1;
173
174   $stop;
175 end
176
177 initial begin
178   $monitor("MISO = %b", MISO);
179 end
180
181
182 endmodule

```

```

V SPI_Wrapper_tb.v
17  initial begin
135   // 4. Read Data (0xED)
136   data = 10'b11_00000101;
137   for(i = 9; i >= 0; i = i - 1) begin
138     MOSI = data[i];
139     @(negedge clk);
140   end
141   repeat(8) @(negedge clk);
142   SS_n = 1;
143
144   repeat(2) @(negedge clk);
145
146   SS_n = 0;
147   @(negedge clk);
148   MOSI = 1;
149   @(negedge clk);
150
151   // 3. Read address (0x55)
152   data = 10'b10_01010101;
153   for(i = 9; i >= 0; i = i - 1) begin
154     MOSI = data[i];
155     @(negedge clk);
156   end
157   SS_n = 1;
158   repeat(2) @(negedge clk);
159
160   SS_n = 0;
161   @(negedge clk);
162   MOSI = 1;
163   @(negedge clk);
164
165   // 4. Read Data (0x55)
166   data = 10'b11_00000101;
167   for(i = 9; i >= 0; i = i - 1) begin
168     MOSI = data[i];
169     @(negedge clk);
170   end
171   repeat(10) @(negedge clk);
172   SS_n = 1;
173
174   $stop;
175 end
176
177 initial begin
178   $monitor("MISO = %b", MISO);
179 end
180
181
182 endmodule

```

```

V SPI_Wrapper_tb.v
17  initial begin
150
151   // 3. Read address (0x55)
152   data = 10'b10_01010101;
153   for(i = 9; i >= 0; i = i - 1) begin
154     MOSI = data[i];
155     @(negedge clk);
156   end
157   SS_n = 1;
158   repeat(2) @(negedge clk);
159
160   SS_n = 0;
161   @(negedge clk);
162   MOSI = 1;
163   @(negedge clk);
164
165   // 4. Read Data (0x55)
166   data = 10'b11_00000101;
167   for(i = 9; i >= 0; i = i - 1) begin
168     MOSI = data[i];
169     @(negedge clk);
170   end
171   repeat(10) @(negedge clk);
172   SS_n = 1;
173
174   $stop;
175 end
176
177 initial begin
178   $monitor("MISO = %b", MISO);
179 end
180
181
182 endmodule

```

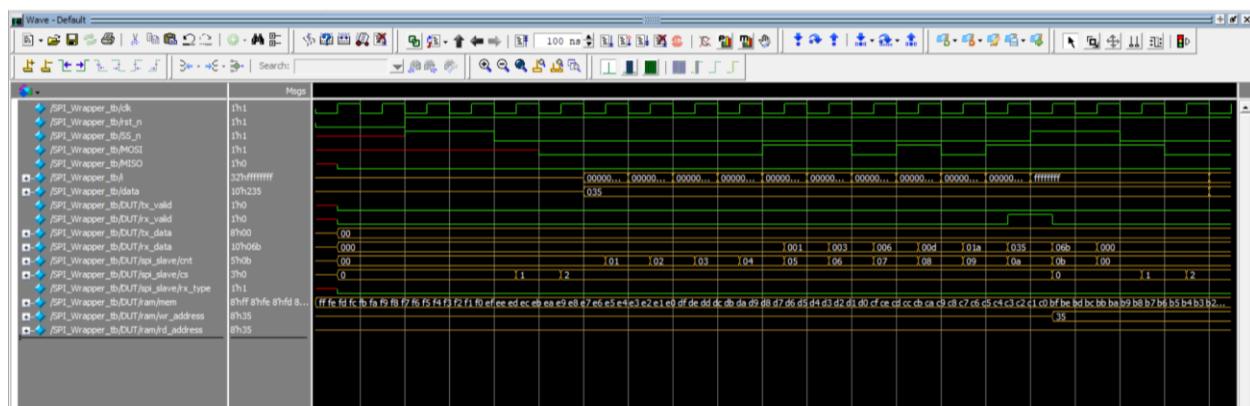
## 3. SIMULATION TOOL

### A. DO FILE

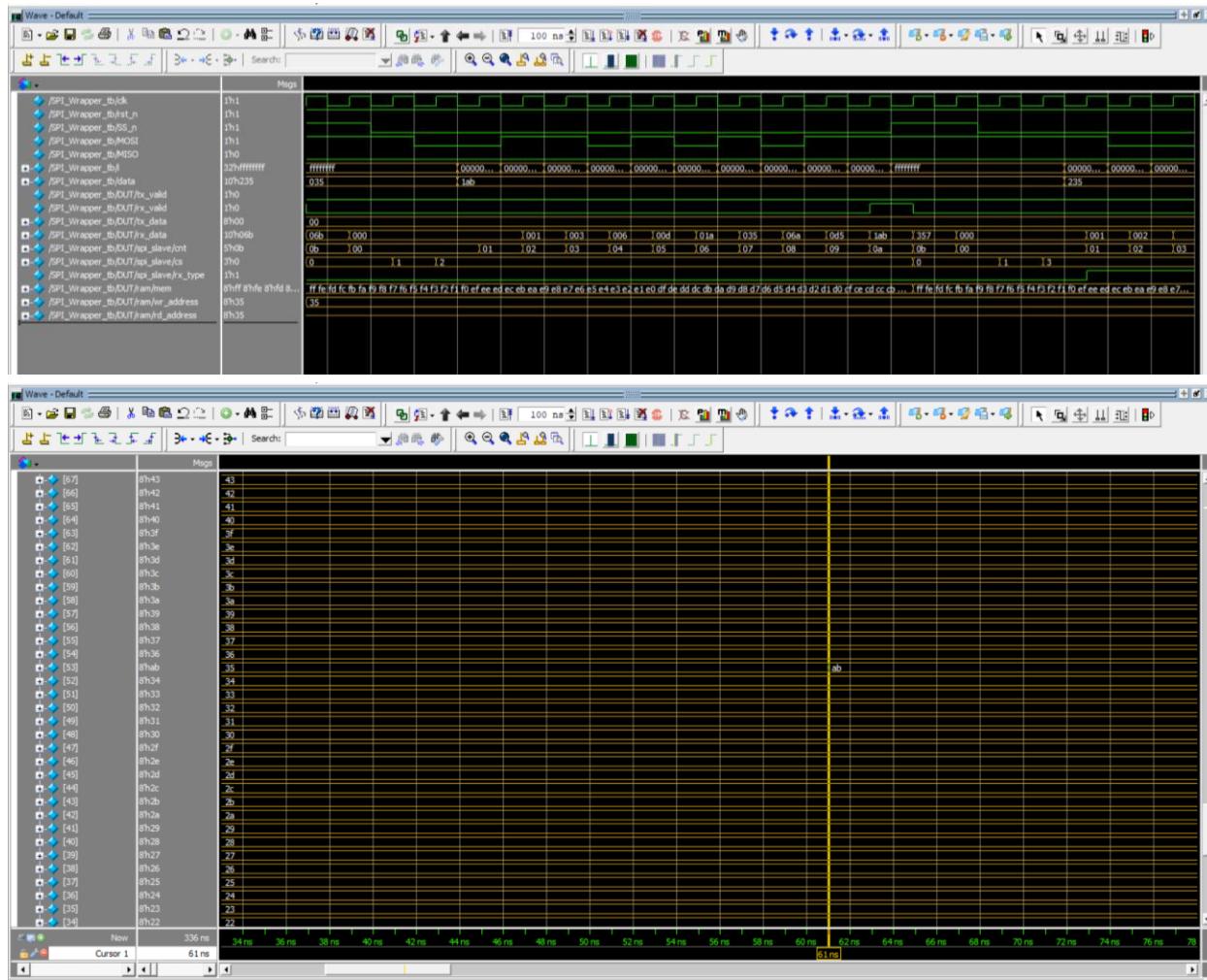
```
# run_spi.do
1 vlib work
2 vlog SPI_Wrapper.v SPI_Wrapper_tb.v SPI.V RAM.V
3 vsim -voptargs=+acc work.SPI_Wrapper_tb
4 add wave *
5 add wave -position insertpoint \
6 sim:/SPI_Wrapper_tb/DUT/tx_valid \
7 sim:/SPI_Wrapper_tb/DUT/rx_valid \
8 sim:/SPI_Wrapper_tb/DUT/tx_data \
9 sim:/SPI_Wrapper_tb/DUT/rx_data
10 add wave -position insertpoint \
11 sim:/SPI_Wrapper_tb/DUT/spi_slave/cnt \
12 sim:/SPI_Wrapper_tb/DUT/spi_slave/cs \
13 sim:/SPI_Wrapper_tb/DUT/spi_slave/rx_type
14 add wave -position insertpoint \
15 sim:/SPI_Wrapper_tb/DUT/ram/mem \
16 sim:/SPI_Wrapper_tb/DUT/ram/wr_address \
17 sim:/SPI_Wrapper_tb/DUT/ram/rd_address
18 run -all
19 #quit -sim
20
```

### B. QUESTA SIM SNIPPETS

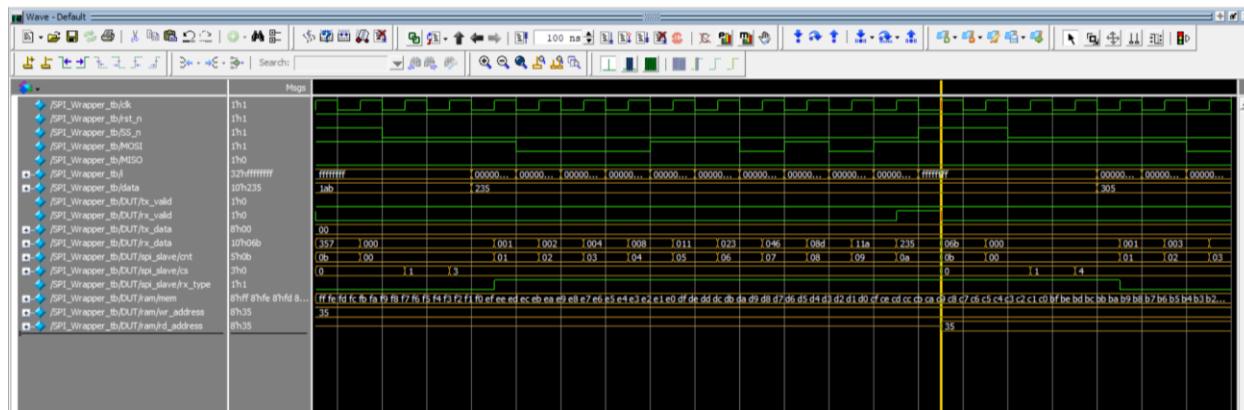
#### I. RESET THEN WRITE ADDRESS => (0x35)



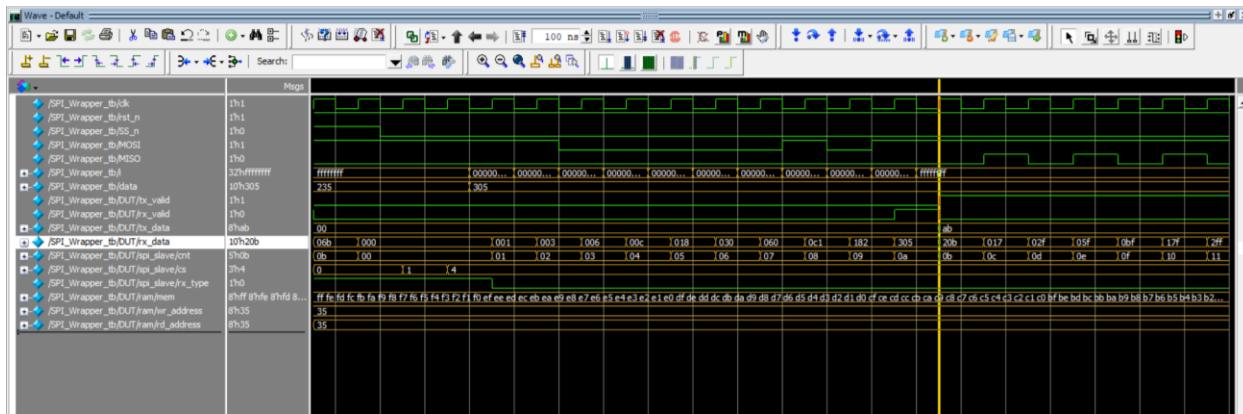
## II. WRITE DATA → (0xAB)



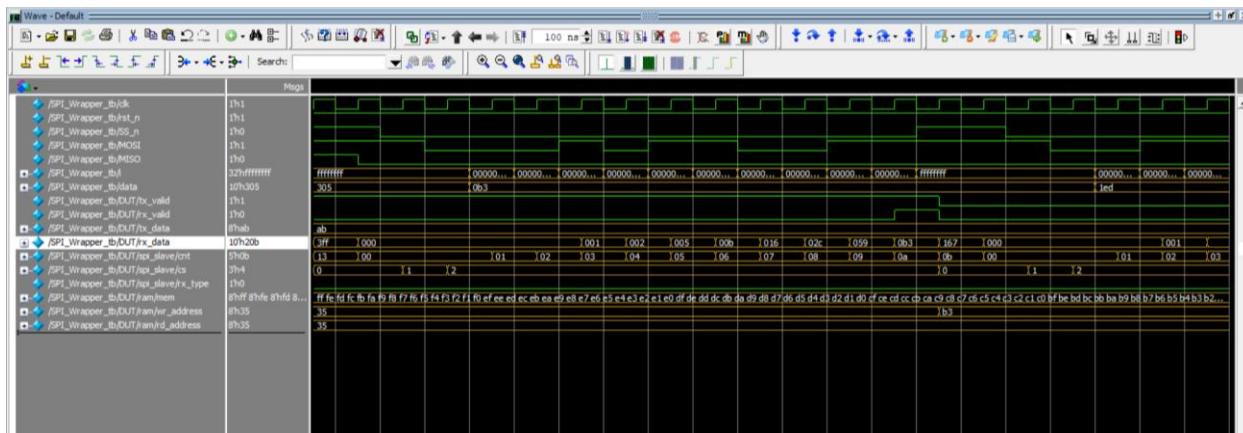
## III. READ ADDRESS → (0x35)



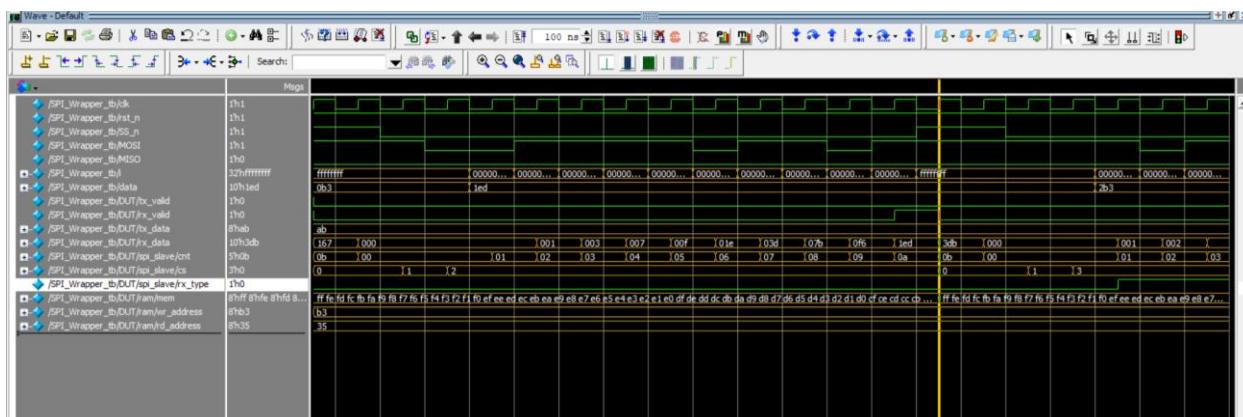
## IV. READ DATA → (0xAB)

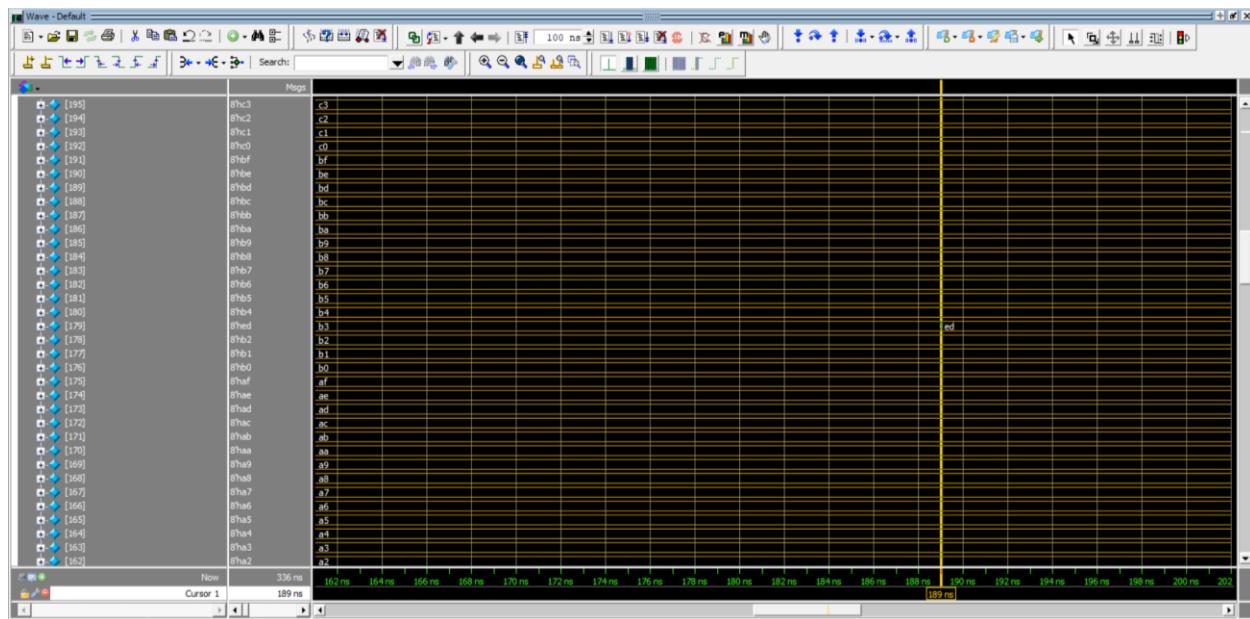


## V. WRITE ADDRESS → (0xB3)

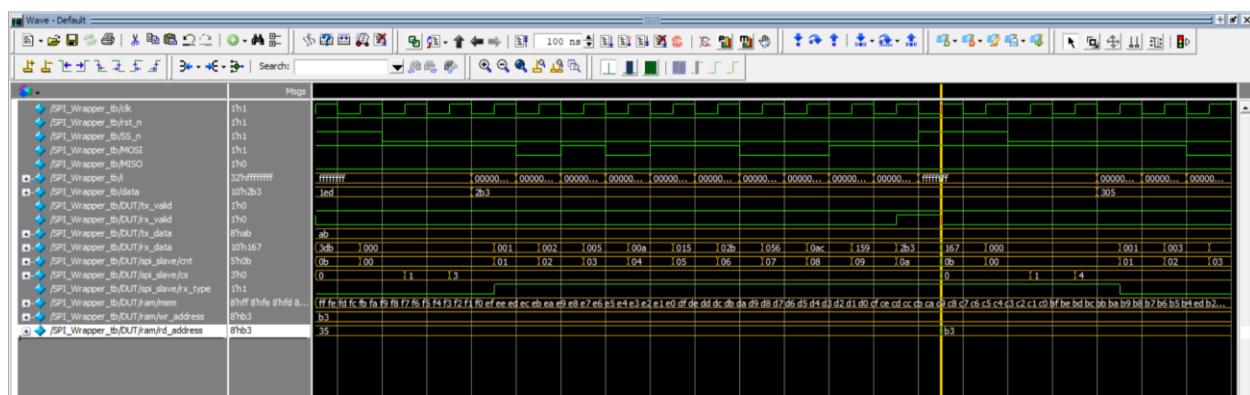


## VI. WRITE DATA → (0xED)

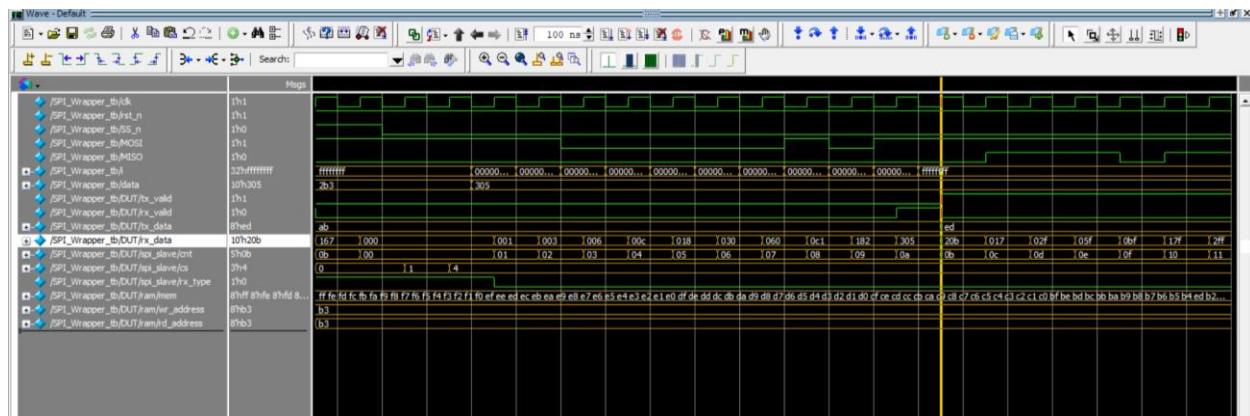




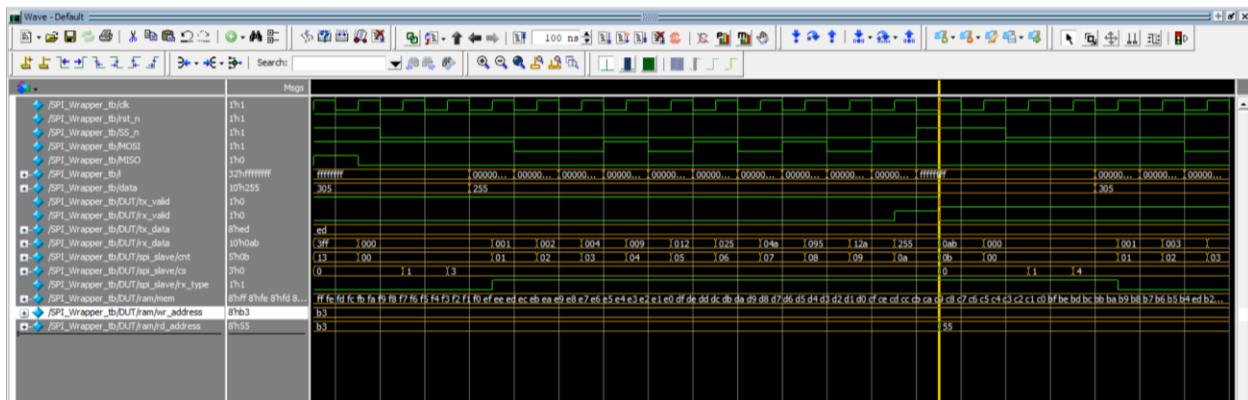
## VII. READ ADDRESS => (0xB3)



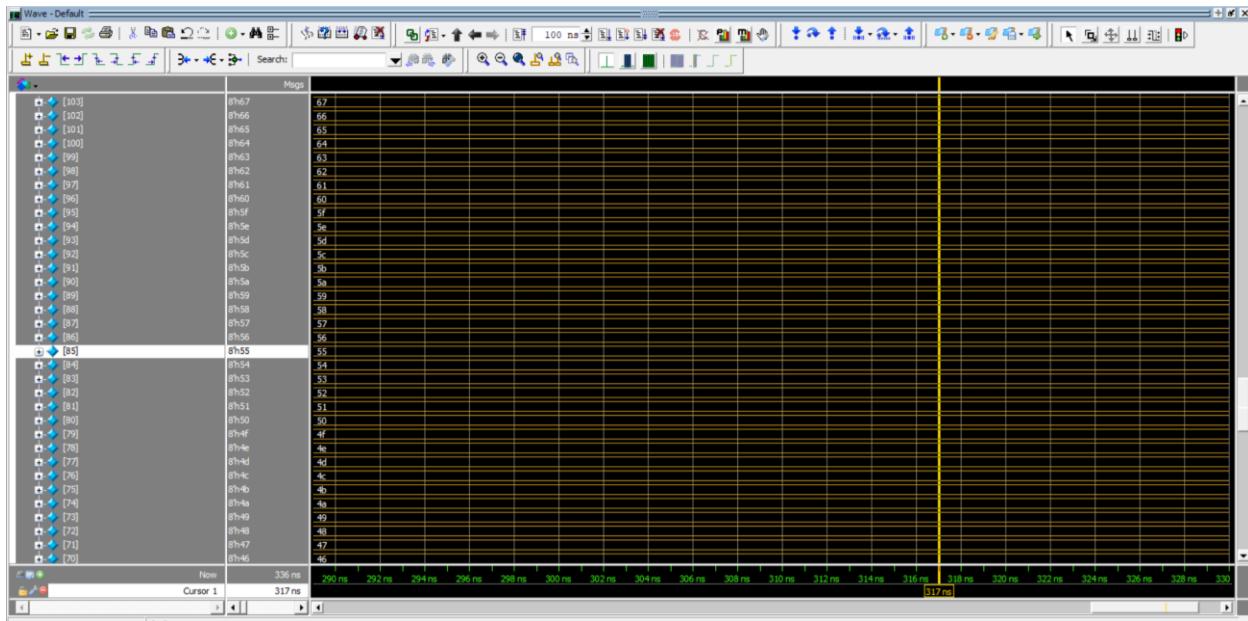
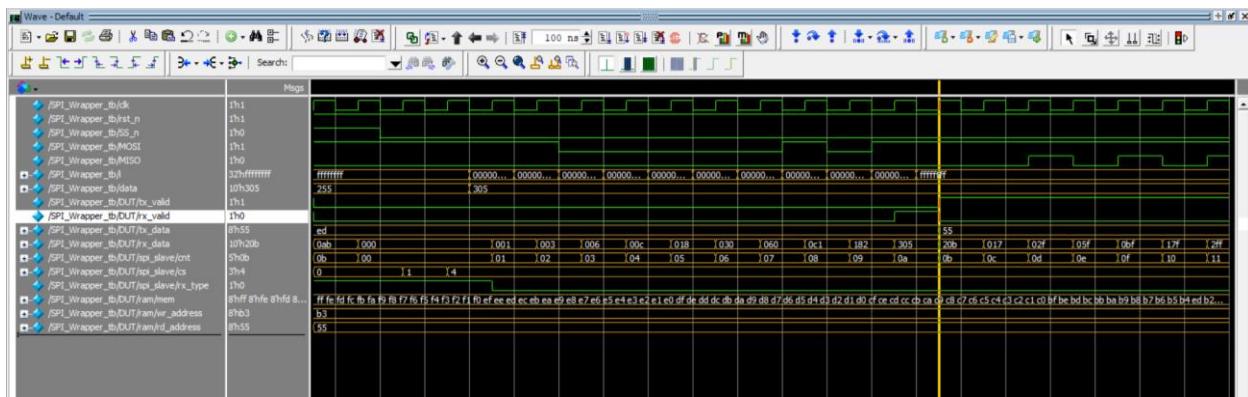
## VIII. READ DATA => (0XED)



## IX. READ ADDRESS => (0x55)



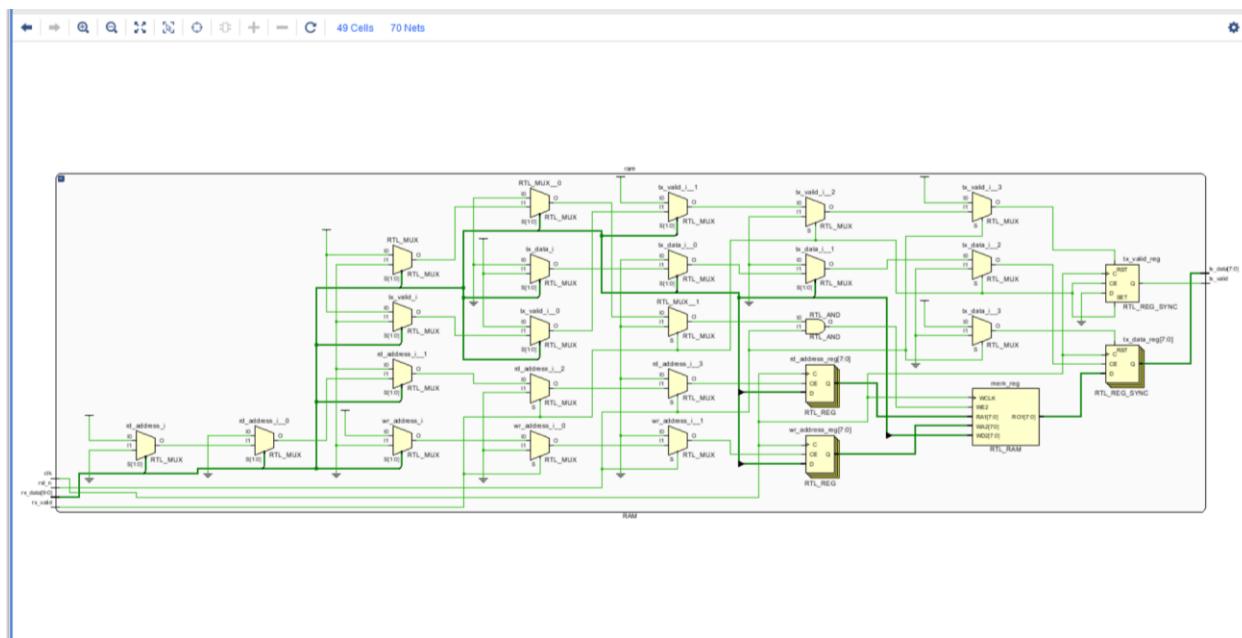
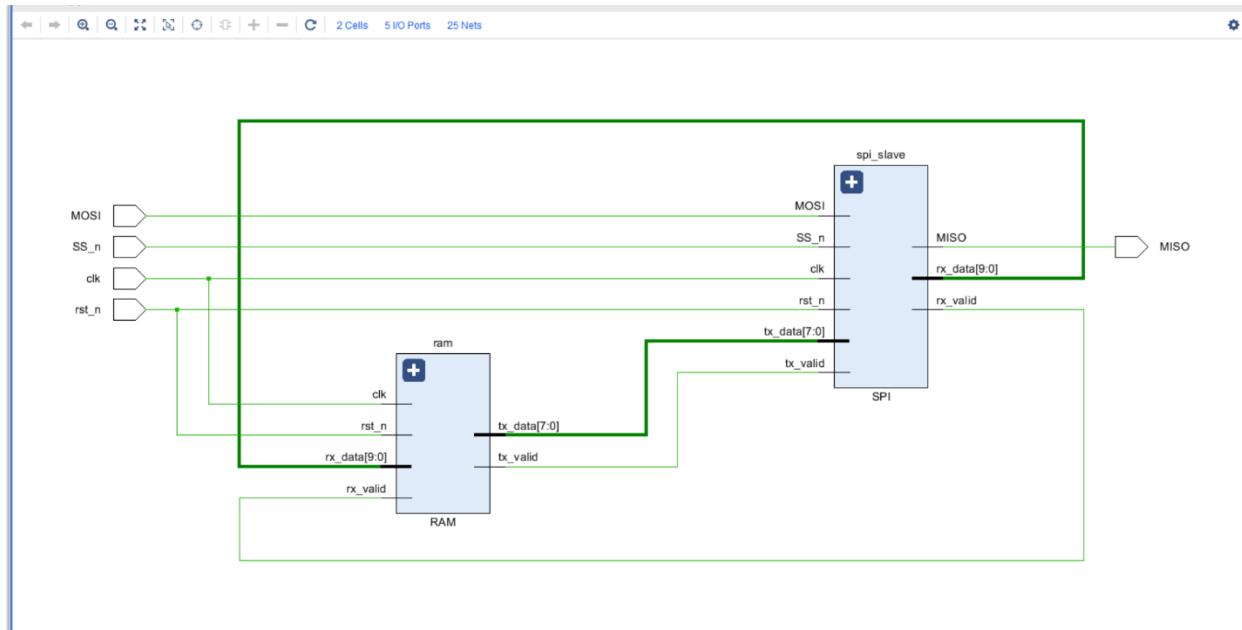
## X. READ DATA

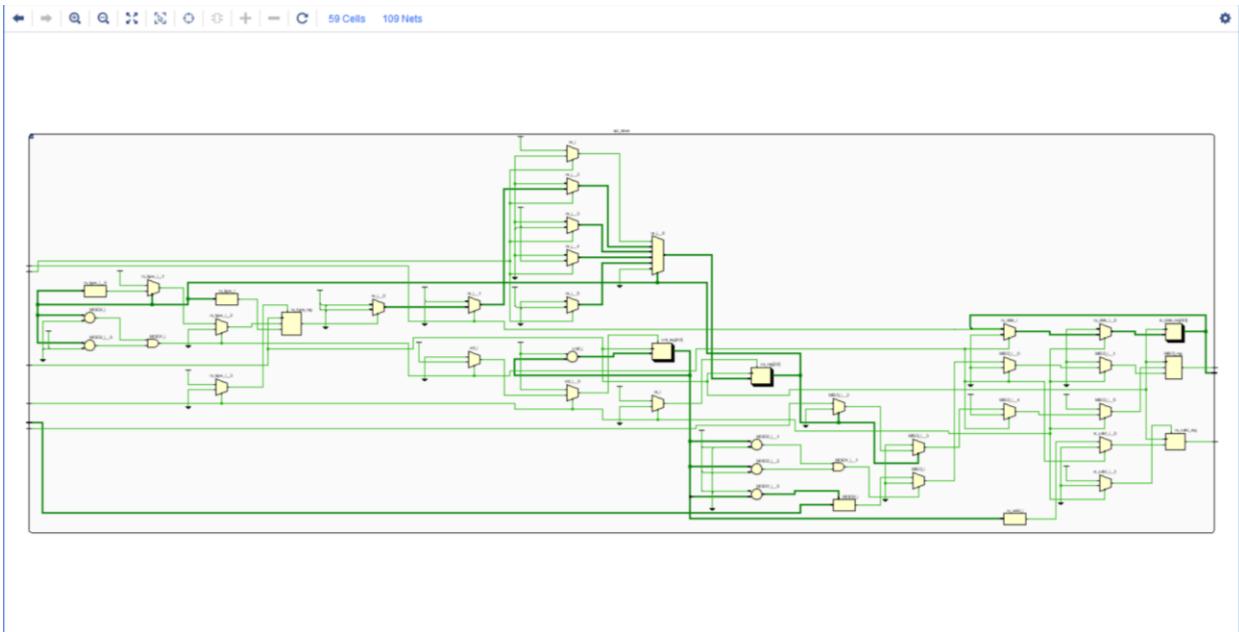


## SYNTHESIS TOOL

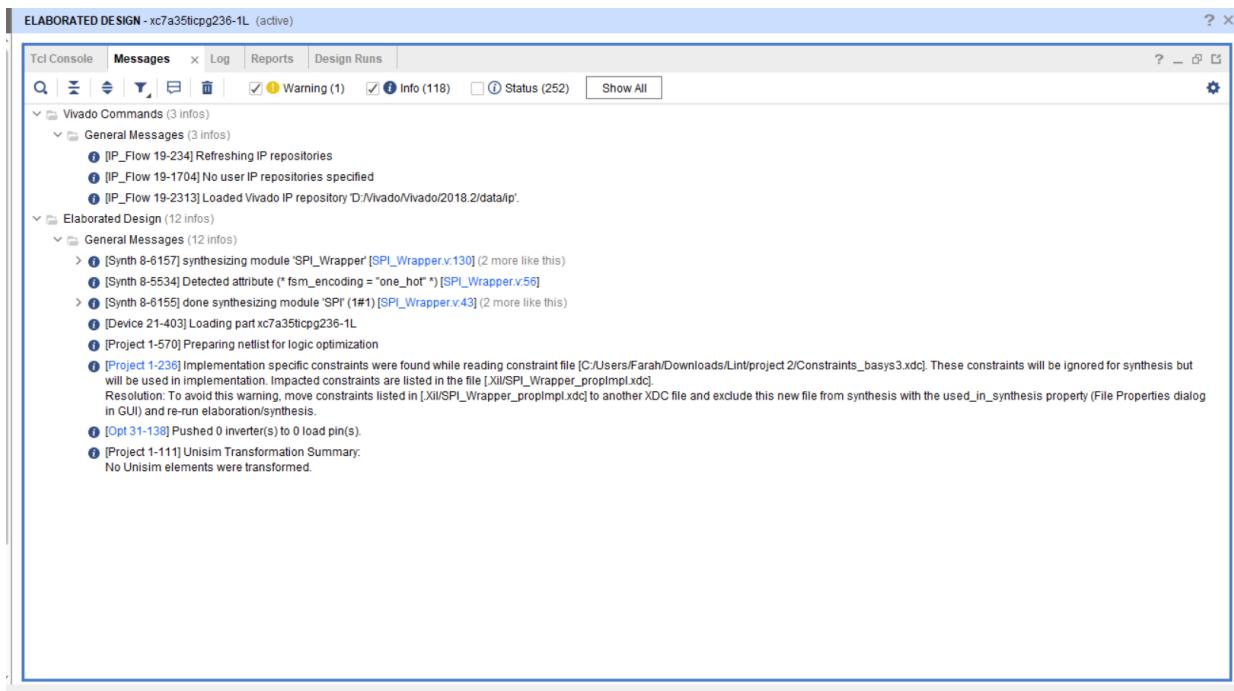
### A. ELABORATION (THE SAME FOR ALL ENCODINGS)

#### I. SCHEMATIC





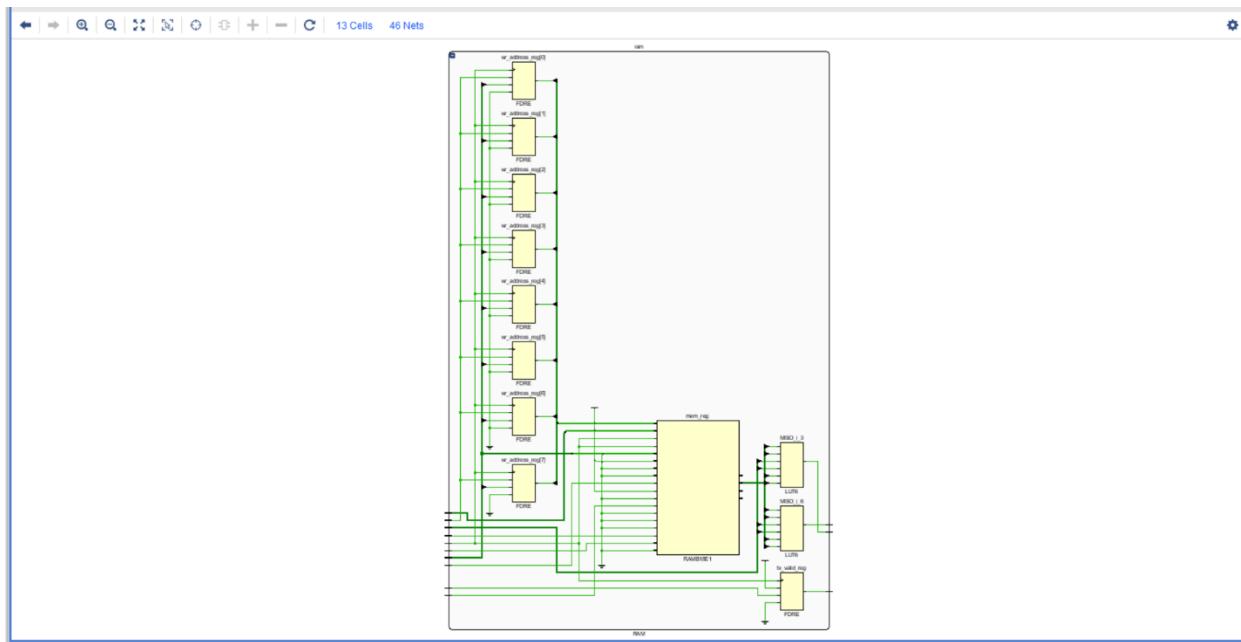
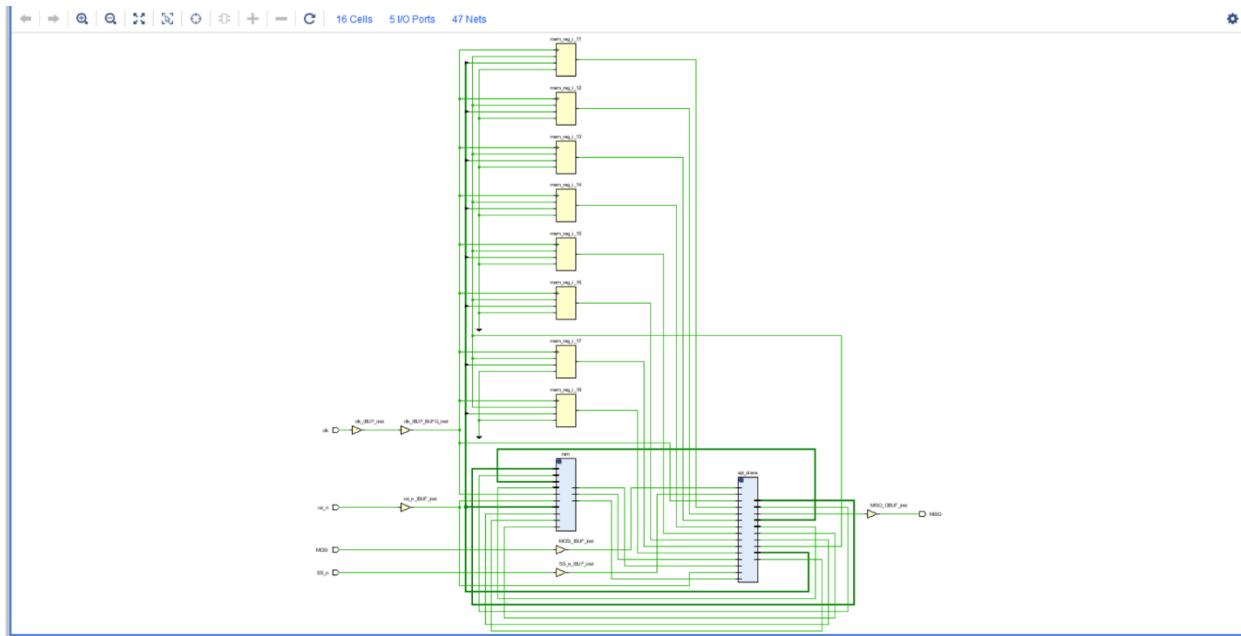
## III. MESSAGES

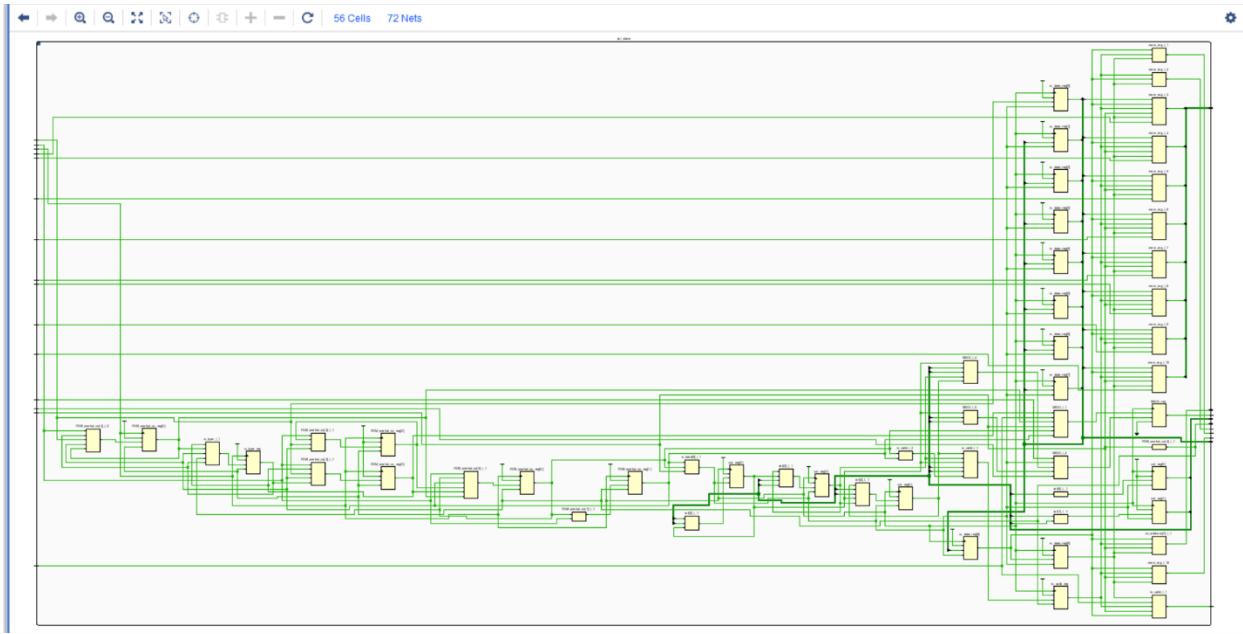


## B. FSM ENCODING = “ONE\_HOT”

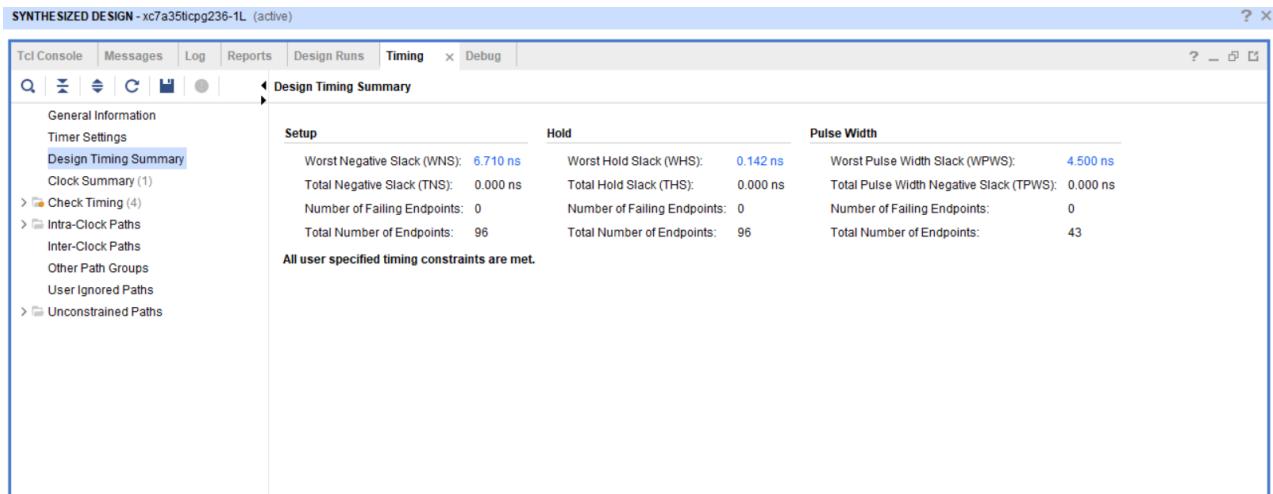
### I. SYNTHESIS

#### 1. SCHEMATIC

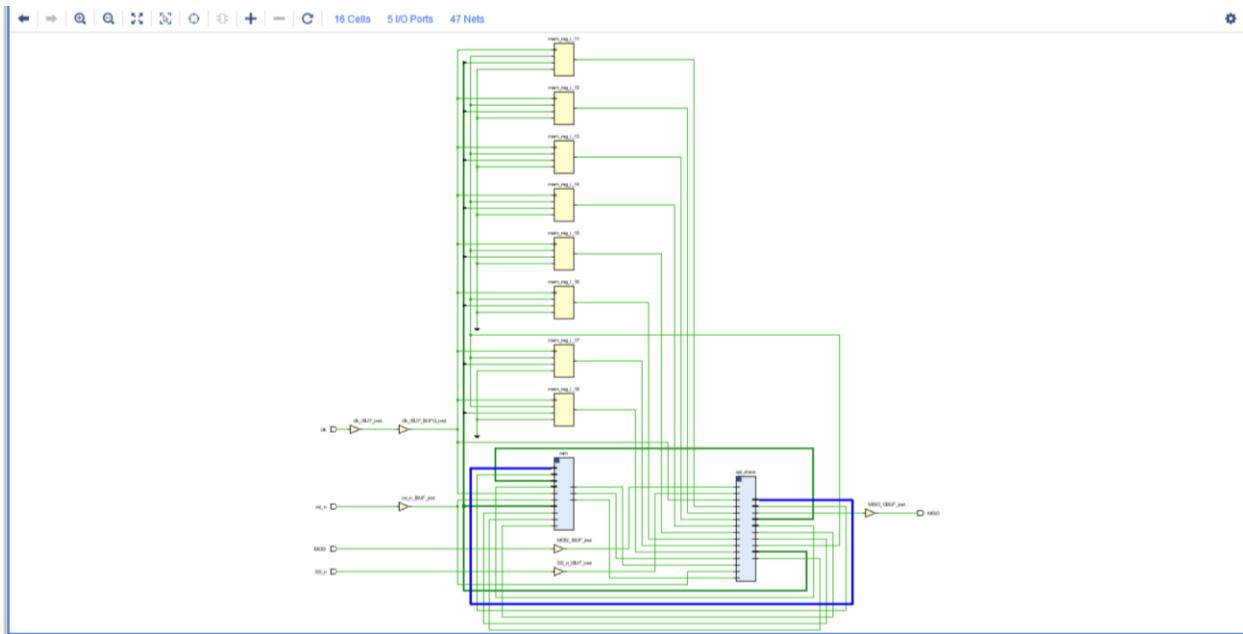




## 2. TIMING



### **3. CRITICAL PATH**



#### **4. UTILIZATION**

SYNTHESIZED DESIGN - xc7a35t-1cpg236-1L (active)

Tcl Console Messages Log Reports Design Runs Utilization x Timing Debug

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPL_Wrapper	30	40	0.5	5	1
ram (RAM)	2	9	0.5	0	0
spi_slave (SPI)	28	23	0	0	0

Summary

Slice Logic

- Slice LUTs (<1%)
- LUT as Logic (<1%)
- Slice Registers (<1%)
- Register as Flip Flop (<1%)

Memory

- Block RAM Tile (1%)
- RAMB18 (1%)
- RAMB18E1 only

DSP

## 5. MESSAGES

A screenshot of a software interface titled "SYNTHESIZED DESIGN - xc7a35tccpg236-1L (active)". The top menu bar includes "Tcl Console", "Messages" (selected), "Log", "Reports", "Design Runs", "Utilization", "Timing", and "Debug". Below the menu is a toolbar with search, filter, and other icons. A status bar at the bottom shows "Synthesis (1 warning)" and "[Constraints 18-5210] No constraint will be written out.".

## **6. REPORT**

```
synth_1_synth_synthesis_report_0 - synth_1

C:/Users/Farah/Downloads/Lint/project_2/project_1/project_1.runs/synth_1/SPI_Wrapper.vds

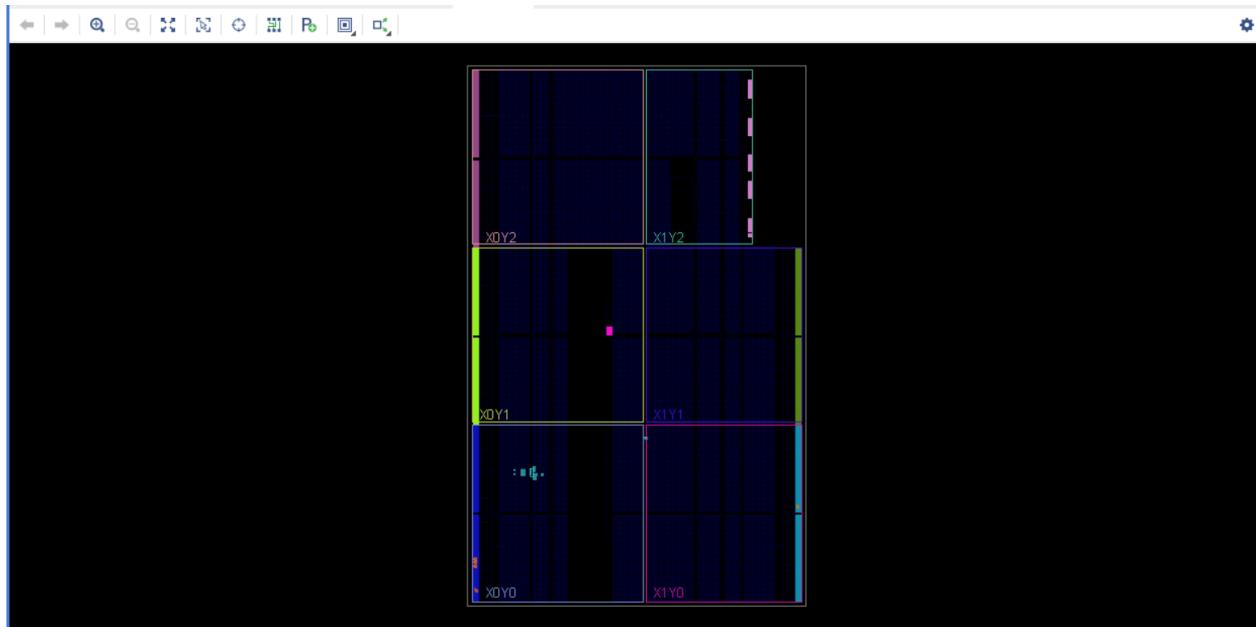
Q |          x

Read-only

99 -----
100 -----
101 Start Applying 'set_property' XDC Constraints
102 -----
103 -----
104 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:22 . Memory (MB): peak = 757.758 ; gain = 500.258
105 -----
106 INFO: [Synth 0-802] inferred FSM for state register 'cg_reg' in module 'SPI'
107 INFO: [Synth 0-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse
108 INFO: [Synth 0-5544] ROM "rx_type" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
109 INFO: [Synth 0-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
110 INFO: [Synth 0-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
111 INFO: [Synth 0-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
112 INFO: [Synth 0-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
113 INFO: [Synth 0-5544] ROM "tx_valid" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
114 INFO: [Synth 0-5544] ROM "wr_address" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
115 -----
116 State | New Encoding | Previous Encoding
117 -----
118 IDLE | 00001 | 000
119 CHK_CMD | 00010 | 001
120 WRITE | 00100 | 010
121 READ_DATA | 01000 | 100
122 READ_ADD | 10000 | 011
123 -----
124 INFO: [Synth 0-354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'
125 INFO: [Synth 0-4430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "yes" *) to avoid collision
126 -----
127 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:22 . Memory (MB): peak = 757.758 ; gain = 500.258
128 -----
129 -----
```

## **II. IMPLEMENTATION**

## 1. DEVICE



## 2. TIMING

IMPLEMENTED DESIGN - xc7a35tci/pg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Timing** x

Design Timing Summary

General Information  
Timer Settings  
Design Timing Summary  
Clock Summary (1)  
Check Timing (4)  
Intra-Clock Paths  
Inter-Clock Paths  
Other Path Groups  
User Ignored Paths  
Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.694 ns	Worst Hold Slack (WHS): 0.108 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 97	Total Number of Endpoints: 97	Total Number of Endpoints: 43

All user specified timing constraints are met.

## 3. UTILIZATION

Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	31	40	14	31	15	0.5	5	1
ram (RAM)	3	9	3	3	0	0.5	0	0
spi_slave (SPI)	28	23	12	28	14	0	0	0

## 4. MESSAGES

IMPLEMENTED DESIGN - xc7a35tci/pg236-1L (active)

Tcl Console | **Messages** x | Log | Reports | Design Runs | Power | Methodology | Timing | Utilization |

Warning (1) Info (244) Status (480) Show All

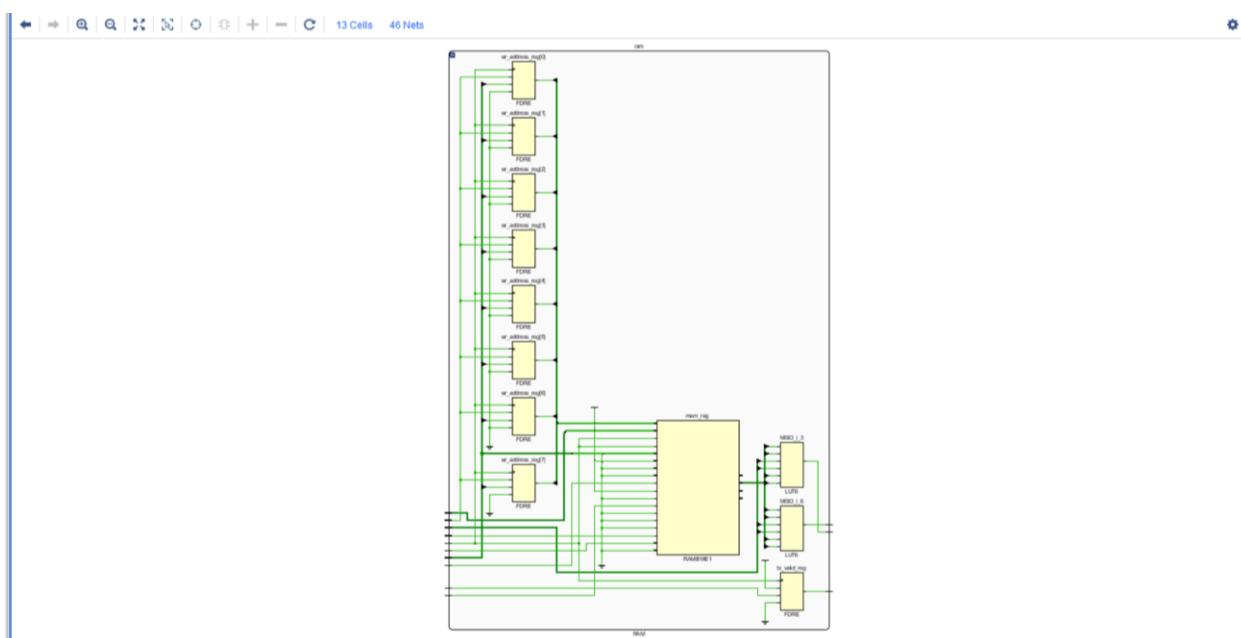
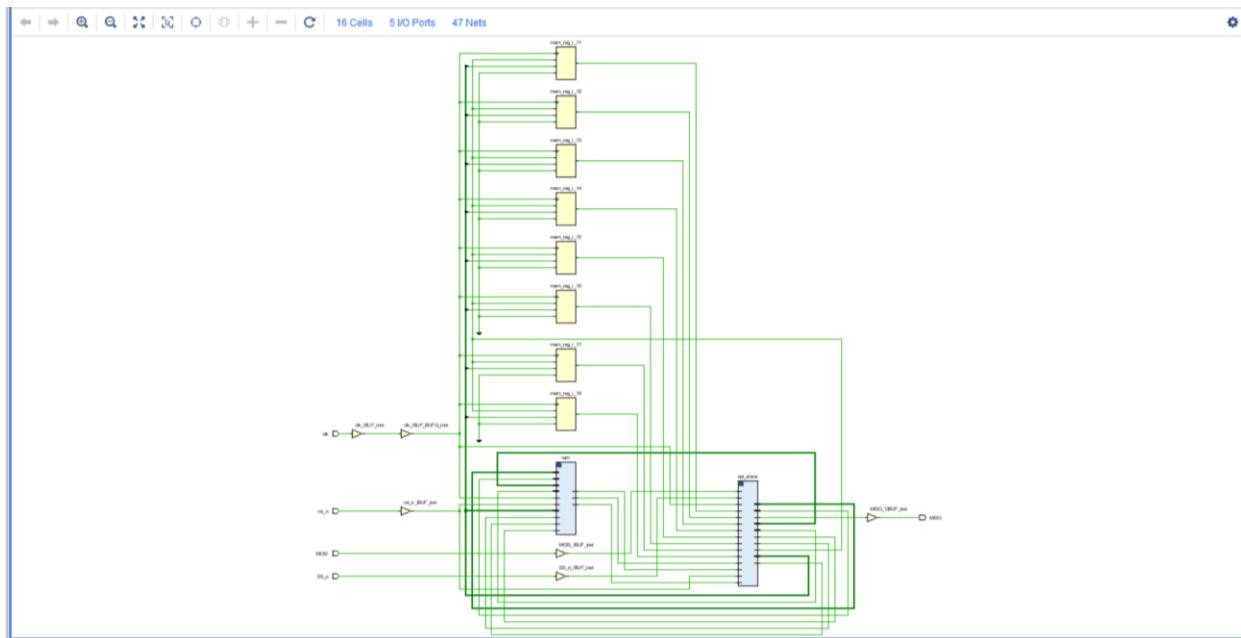
Implementation (98 infos)

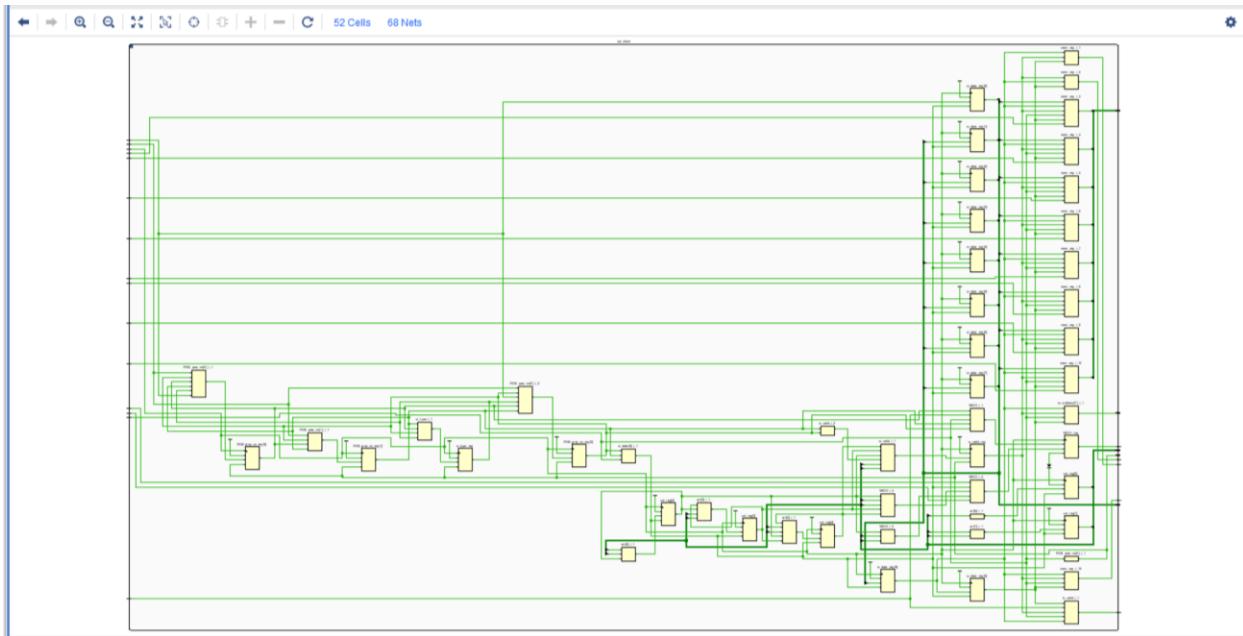
- Design Initialization (11 infos)
  - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-479] Netlist was created with Vivado 2018.2
  - [Device 21-403] Loading part xc7a35tci/pg236-1L
  - [Project 1-570] Preparing netlist for logic optimization
  - [Timing 38-478] Restoring timing data from binary archive.
  - [Timing 38-479] Binary timing data restore complete.
  - [Project 1-856] Restoring constraints from binary archive.
  - [Project 1-853] Binary constraint restore complete.
  - [Project 1-111] Unisim Transformation Summary:  
No Unisim elements were transformed.
  - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- Opt Design (30 infos)
  - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
  - [Project 1-481] DRC finished with 0 Errors
  - [Project 1-462] Please refer to the DRC report (report\_drc) for more information.
  - [Opt 31-49] Retargeted 0 cell(s).
  - [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
  - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
  - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
  - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
  - [Pwropt 34-9] Applying IDT optimizations ...
  - [Pwropt 34-10] Applying ODC optimizations ...
  - [Physopt 32-619] Estimated Timing Summary | WNS=6.710 | TNS=0.000 |
  - [Pwropt 34-162] WRITE\_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report\_power\_opt to get a complete listing of the BRAMs updated.

## **C. FSM ENCODING = "GRAY"**

### **I. SYNTHESIS**

#### **1. SCHEMATIC**





## 2. TIMING

**SYNTHESIZED DESIGN - xc7a35lccpg236-1L (active)**

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Debug | ? x

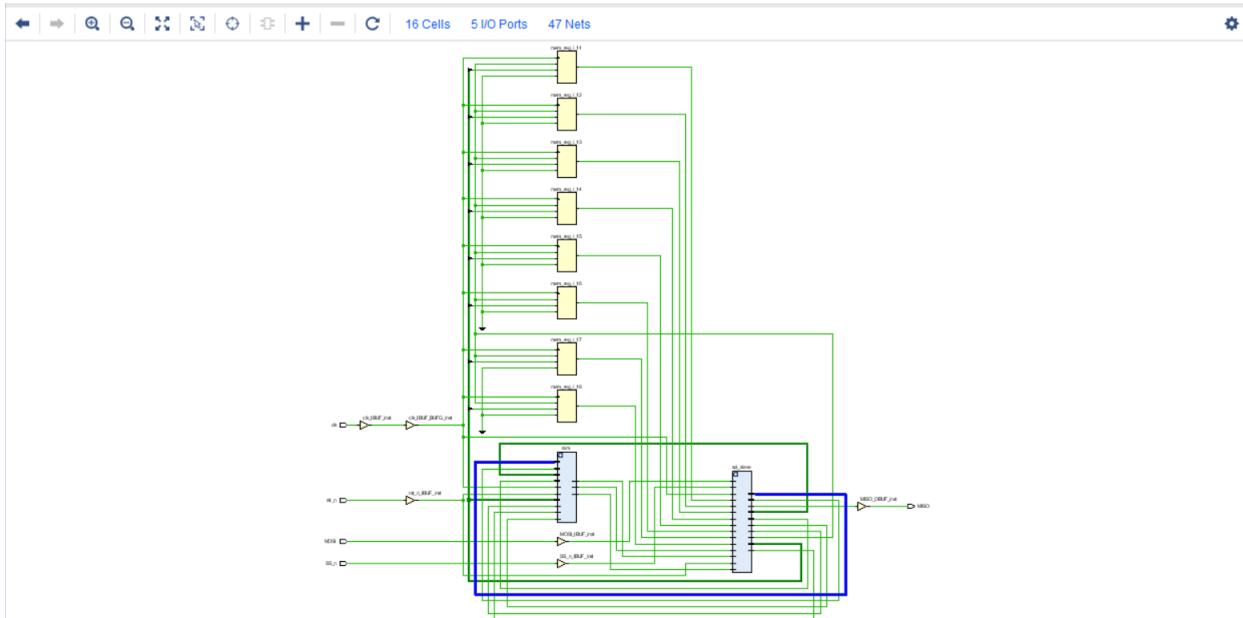
Q | X | C | L | S | D | Design Timing Summary

- General Information
- Timer Settings
- Design Timing Summary**
- Clock Summary (1)
- > Check Timing (4)
- > Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- > Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <b>6.710 ns</b>	Worst Hold Slack (WHS): <b>0.142 ns</b>	Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>
Total Negative Slack (TNS): <b>0.000 ns</b>	Total Hold Slack (THS): <b>0.000 ns</b>	Total Pulse Width Negative Slack (TPWS): <b>0.000 ns</b>
Number of Failing Endpoints: <b>0</b>	Number of Failing Endpoints: <b>0</b>	Number of Failing Endpoints: <b>0</b>
Total Number of Endpoints: <b>94</b>	Total Number of Endpoints: <b>94</b>	Total Number of Endpoints: <b>41</b>

All user specified timing constraints are met.

### **3. CRITICAL PATH**



#### **4. UTILIZATION**

**SYNTHESIZED DESIGN - xc7a35tci2g236-1L (active)**

The screenshot shows the Utilization tab in the Vivado interface. The left sidebar displays a tree view of the design hierarchy, including Summary, Slice Logic (with sub-items for Slice LUTs, Slice Registers, and Memory), and DSP. The main area shows utilization statistics for various components:

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper	28	38	0.5	5	1
ram (RAM)	2	9	0.5	0	0
spi_slave (SPI)	26	21	0	0	0

## **5. MESSAGES**

A screenshot of the Xilinx Vivado IDE interface. The title bar reads "SYNTHESIZED DESIGN - xc7a35tci236-1L (active)". The menu bar includes "File", "Edit", "Project", "Run", "Design", "Tools", "Help". Below the menu is a toolbar with icons for "Tcl Console", "Messages", "Log", "Reports", "Design Runs", "Utilization", "Timing", and "Debug". The "Messages" tab is selected. A search bar and filter buttons for "Warning (1)", "Info (50)", and "Status (35)" are present. A "Show All" button is also available. The main pane shows a single warning under the "Synthesis" category: "[Constraints 18-5210] No constraint will be written out.".

## 6. REPORT

SYNTHESIZED DESIGN - xc7a35tcipg236-1L (active)

Schematic | SPI\_Wrapper.v | Schematic (2) | synth\_1\_synth\_synthesis\_report\_0 - synth\_1 | X

C:/Users/Farahi/Downloads/Lint/project\_2/project\_1/runs/synth\_1/SPI\_Wrapper.vds

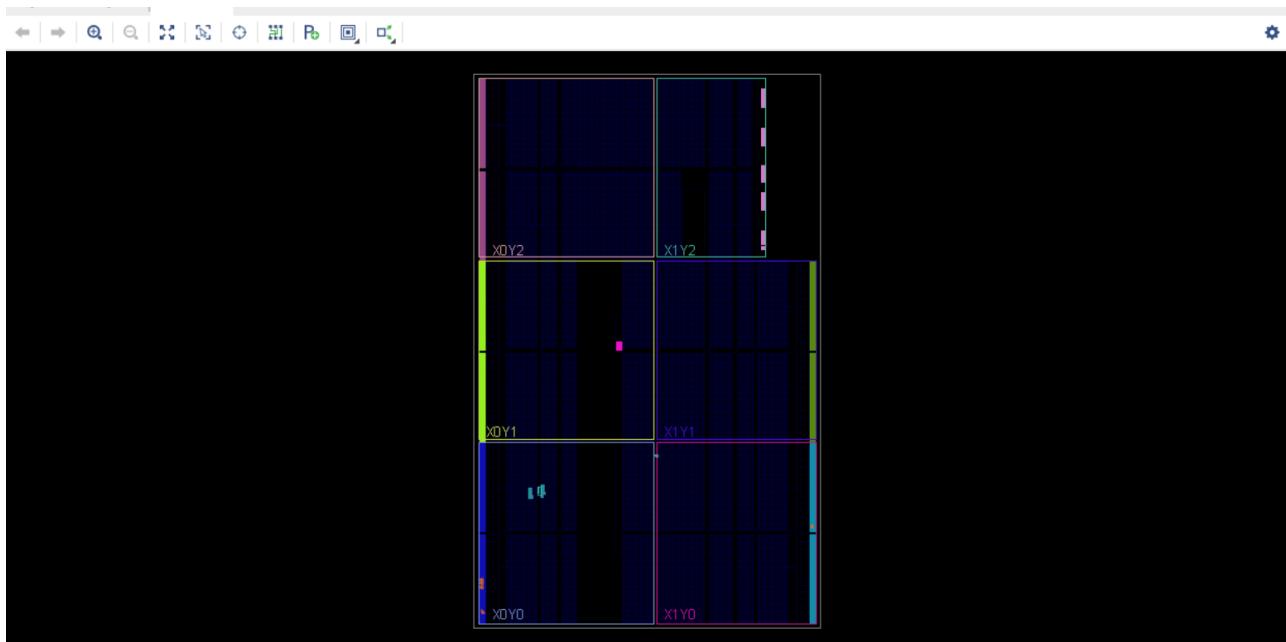
Read-only

Netlist | Cell Properties

```
79 -----
80 -----
81 Start Applying 'set_property' XDC Constraints
82 -----
83 -----
84 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:23 . Memory (MB): peak = 759.270 ; gain = 502.516
85 -----
86 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
87 INFO: [Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse
88 INFO: [Synth 8-5544] ROM "rx_type" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
89 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
90 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
91 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "tx_valid" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "wr_address" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
95 -----
96 State | New Encoding | Previous Encoding
97 -----
98 IDLE | 000 | 000
99 CHK_CMD | 001 | 001
100 WRITE | 011 | 010
101 READ_DATA | 010 | 100
102 READ_ADD | 111 | 011
103 -----
104 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
105 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "yes" *) to avoid collis
106 -----
107 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:23 . Memory (MB): peak = 759.270 ; gain = 502.516
108 -----
109 < ----->
```

## II. IMPLEMENTATION

### 1. DEVICE



## 2. TIMING

IMPLEMENTED DESIGN - xc7a35tclcp236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Timing** | x

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Setup Hold Pulse Width

Worst Negative Slack (WNS):	0.6754 ns	Worst Hold Slack (WHS):	0.090 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	95	Total Number of Endpoints:	95	Total Number of Endpoints:	41

All user specified timing constraints are met.

## 3. UTILIZATION

IMPLEMENTED DESIGN - xc7a35tclcp236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Utilization** | x

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N_SPL_Wrapper	29	38	13	29	8	0.5	5	1
ram (RAM)	3	9	5	3	0	0.5	0	0
spi_slave (SPI)	26	21	13	26	8	0	0	0

## 4. MESSAGES

IMPLEMENTED DESIGN - xc7a35tclcp236-1L (active)

Tcl Console | **Messages** | x | Log | Reports | Design Runs | Power | Methodology | Timing | Utilization |

Warning (1) Info (242) Status (484) Show All

Synthesis (1 warning, 34 infos)

Implementation (98 infos)

  Design Initialization (11 infos)

- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a35tclcp236-1L
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:  
      No Unisim elements were transformed.
- [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

  Opt Design (30 infos)

- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
- [Project 1-461] DRC finished with 0 Errors
- [Project 1-462] Please refer to the DRC report (report\_drc) for more information.
- [Opt 31-49] Retargeted 0 cell(s).

  | [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)

  | [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)

  | [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

  | [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

  | [Pwropt 34-9] Applying IDT optimizations ...

  | [Pwropt 34-10] Applying ODC optimizations ...

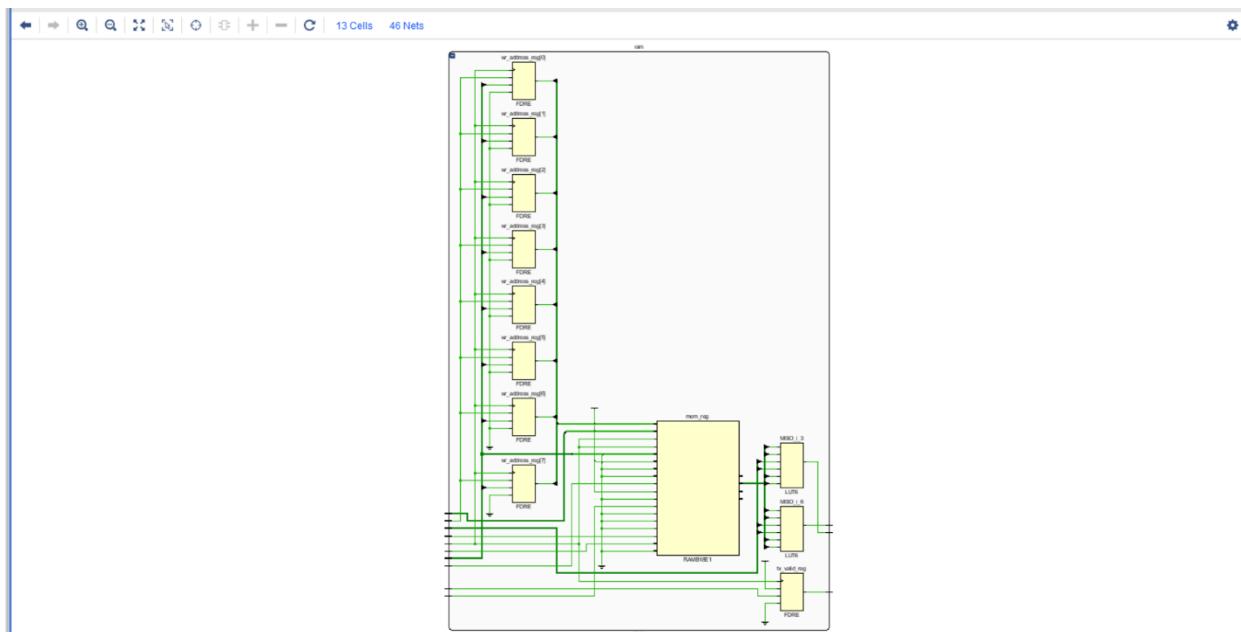
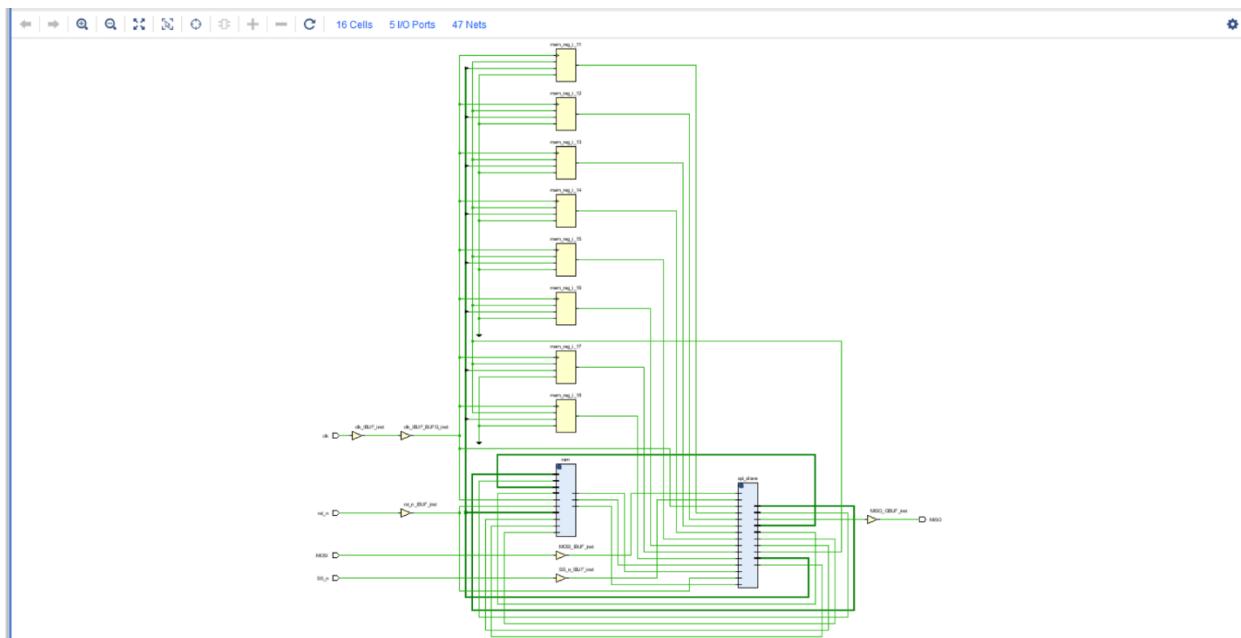
  | [Physopt 32-619] Estimated Timing Summary | WNS=6.710 | TNS=0.000 |

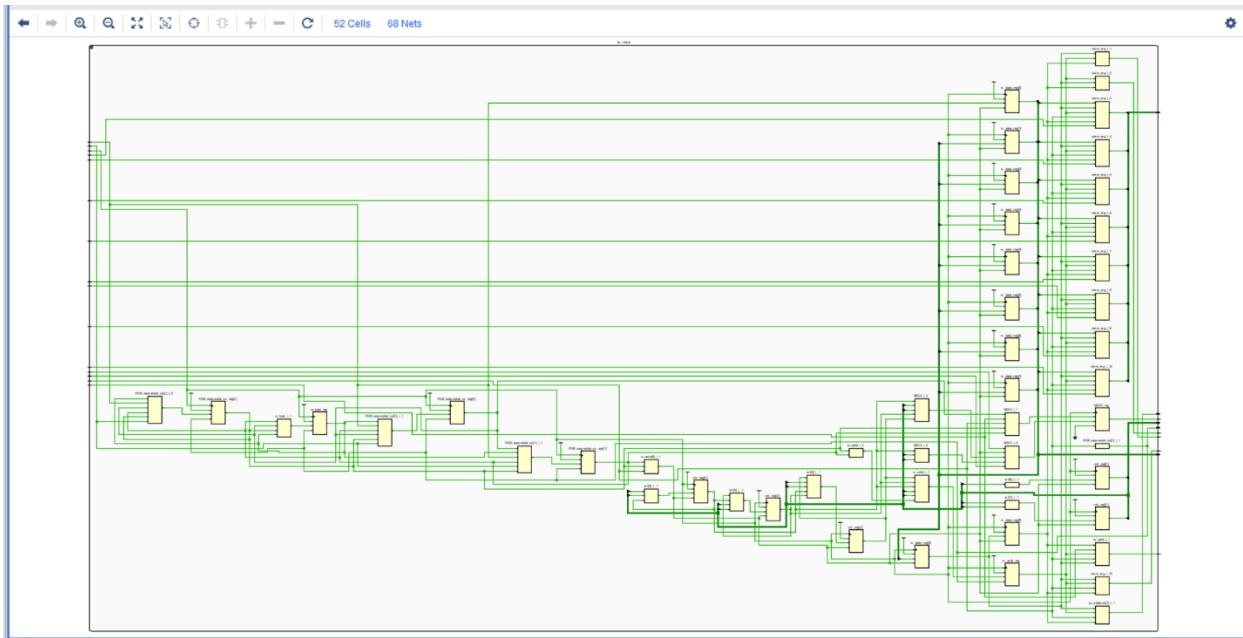
  | [Pwropt 34-162] WRITE\_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report\_power\_opt to get a complete listing of the BRAMs updated.

## D.FSM ENCODING = "SEQUENTIAL"

### I. SYNTHESIS

#### 1. SCHEMATIC





## 2. TIMING

**SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)**

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** | Debug | ? - ×

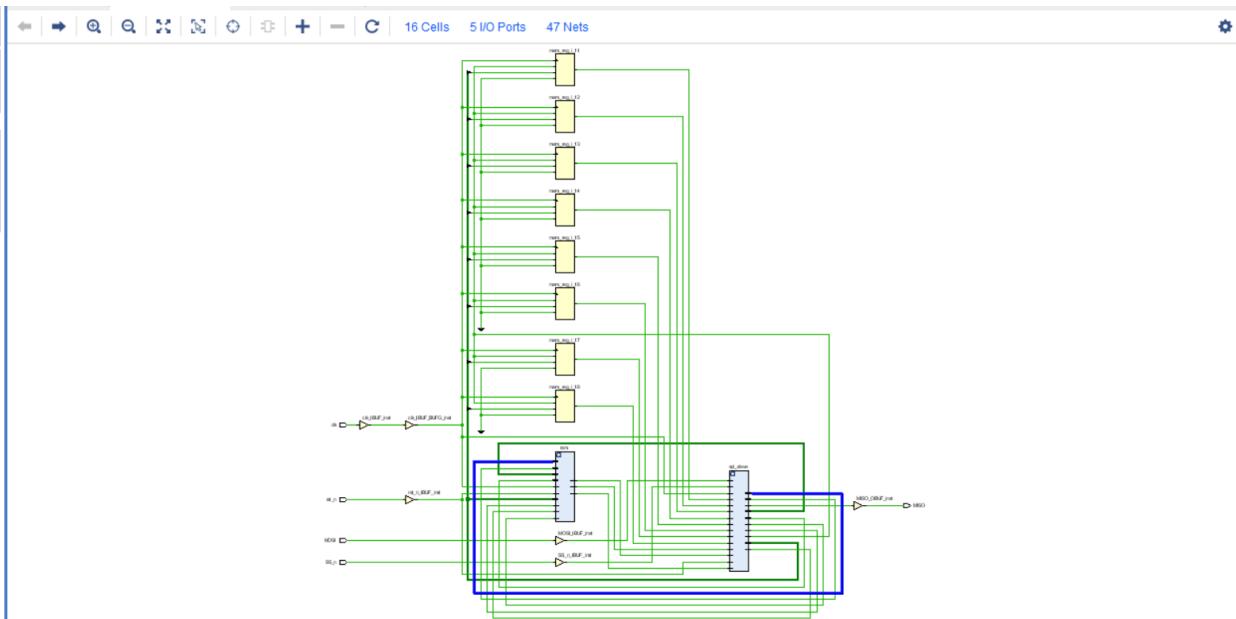
**Design Timing Summary**

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	<b>6.710 ns</b>	Worst Hold Slack (WHS):	<b>0.144 ns</b>	Worst Pulse Width Slack (WPWS):	<b>4.500 ns</b>
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	94	Total Number of Endpoints:	94	Total Number of Endpoints:	41

All user specified timing constraints are met.

- General Information
- Timer Settings
- Design Timing Summary**
- Clock Summary (1)
  - Check Timing (4)
  - Intra-Clock Paths
  - Inter-Clock Paths
  - Other Path Groups
  - User Ignored Paths
  - Unconstrained Paths

## 3. CRITICAL PATH



## 4. UTILIZATION

SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)					
Utilization					
	Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)
	N SPI_Wrapper	28	38	0.5	5
	ram (RAM)	2	9	0.5	0
	spi_slave (SPI)	26	21	0	0

## 5. MESSAGES

SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)					
Messages					
	Warning (1)	Info (46)	Status (32)	Show All	
Synthesis (1 warning)					
	! [Constraints 18-5210] No constraint will be written out.				

## **6. REPORT**

SYNTHESIZED DESIGN - xc7a35t-1cpg236-1L (active)

Schematic | SPI\_Wrapper.v | Path 2 - timing\_1 | Schematic (2) | synth\_1\_synth\_synthesis\_report\_0 - synth\_1 |

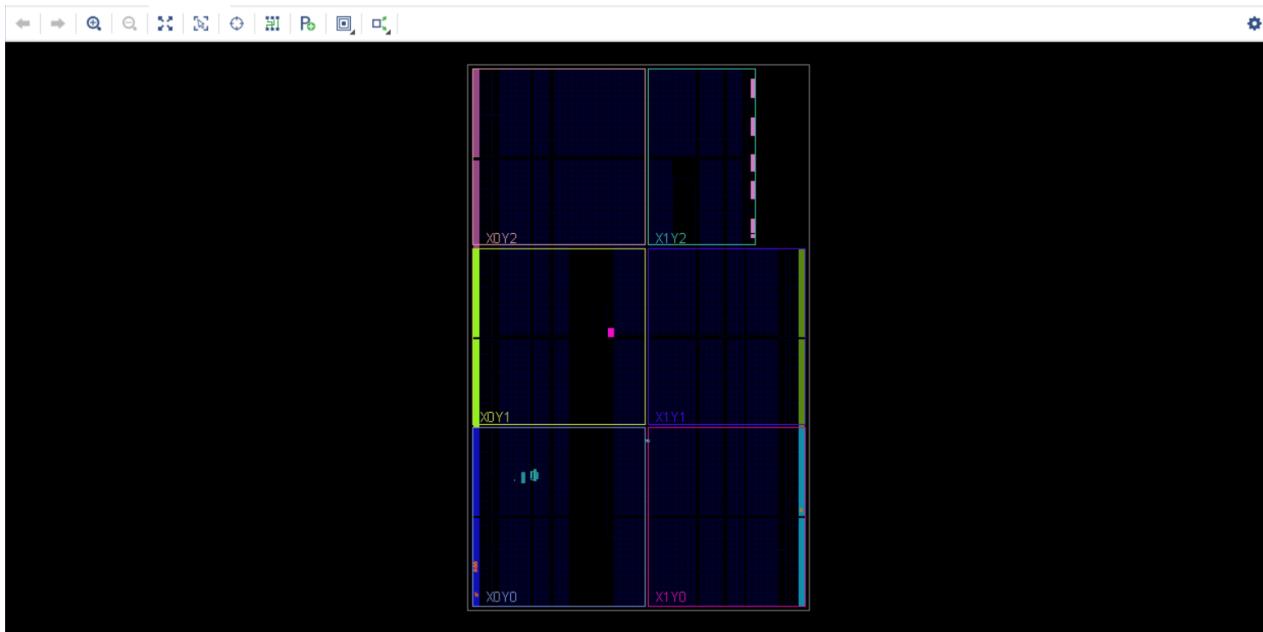
C:/Users/Farah/Downloads/Lint/project 2/project\_1/runs/synth\_1/SPI\_Wrapper.vds

Read-only |

```
79 -----
80 -----
81 Start Applying 'set_property' XDC Constraints
82 -----
83 -----
84 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:11 ; elapsed = 00:00:20 . Memory (MB): peak = 758.074 ; gain = 500.832
85 -----
86 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
87 INFO: [Synth 8-5546] ROM "rx_valid" won't be mapped to RAM because it is too sparse
88 INFO: [Synth 8-5544] ROM "rx_type" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
89 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
90 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
91 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "tx_valid" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "wr_address" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
95 -----
96          State |           New Encoding |           Previous Encoding
97 -----
98          IDLE |             000 |             000
99          CHK_CMD |            001 |             001
100         WRITE |            010 |             010
101        READ_DATA |            011 |             100
102       READ_ADD |            100 |             011
103 -----
104 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'
105 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "yes" *) to avoid collis
106 -----
107 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:11 ; elapsed = 00:00:20 . Memory (MB): peak = 758.074 ; gain = 500.832
108 -----
109 -----
```

## **II. IMPLEMENTATION**

## **1. DEVICE**



## 2. TIMING

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Timing** | x

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> **Check Timing (4)**

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Setup Hold Pulse Width

Worst Negative Slack (WNS): 6.609 ns	Worst Hold Slack (WHS): 0.090 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 95	Total Number of Endpoints: 95	Total Number of Endpoints: 41

All user specified timing constraints are met.

## 3. UTILIZATION

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Utilization** | x

Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
N SPI_Wrapper		29	38	14	29		8	0.5	5	1
ram (RAM)		3	9	5	3		0	0.5	0	0
spi_slave (SPI)		26	21	14	26		8	0	0	0

Hierarchy

Summary

slice Logic

  slice LUTs (<1%)

    LUT as Logic (<1%)

  slice Registers (<1%)

  Register as Flip Flop (

slice Logic Distribution

  slice (<1%)

    SLICEM

    SLICEL

## 4. MESSAGES

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | **Messages** | x | Log | Reports | Design Runs | Power | Methodology | Timing | Utilization |

Q | X | D | T | M | B | W | I | S | Show All

Implementation (98 infos)

  Design Initialization (11 infos)

- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds*
- [Project 1-479] Netlist was created with Vivado 2018.2*
- [Device 21-403] Loading part xc7a35ticpg236-1L*
- [Project 1-570] Preparing netlist for logic optimization*
- [Timing 38-478] Restoring timing data from binary archive.*
- [Timing 38-479] Binary timing data restore complete.*
- [Project 1-856] Restoring constraints from binary archive.*
- [Project 1-853] Binary constraint restore complete.*
- [Project 1-111] Unisim Transformation Summary:*  
      No Unisim elements were transformed.
- [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646*

  Opt Design (30 infos)

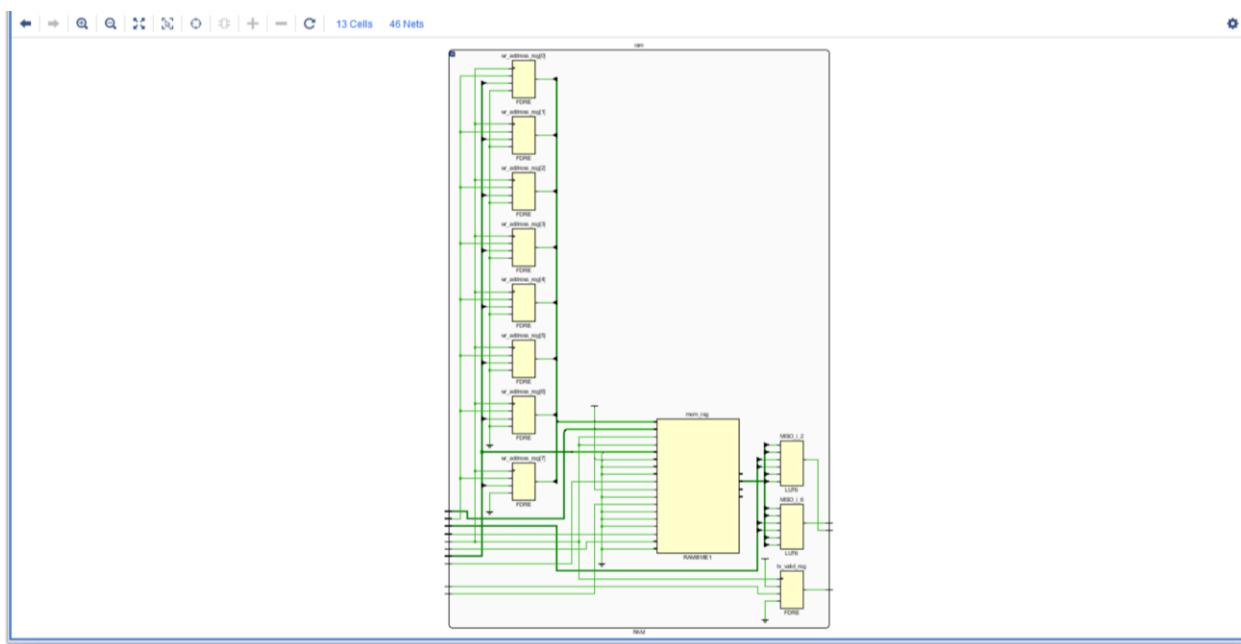
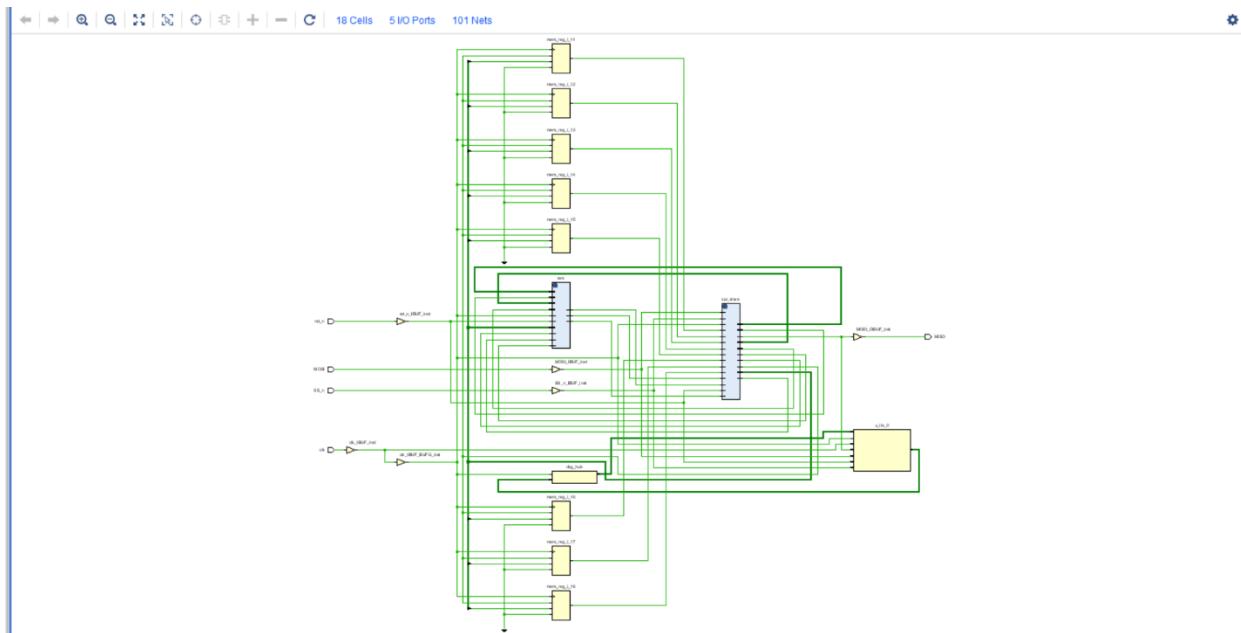
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'*
- [Project 1-461] DRC finished with 0 Errors*
- [Project 1-462] Please refer to the DRC report (report\_drc) for more information.*
- [Opt 31-49] Retargeted 0 cell(s).*
- [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)*
- [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)*
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.*
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.*
- [Pwropt 34-9] Applying IDT optimizations ...*
- [Pwropt 34-10] Applying ODC optimizations ...*
- [Physopt 32-619] Estimated Timing Summary | WNS=6.710 | TNS=0.000 |*
- [Pwropt 34-162] WRITE\_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report\_power\_opt to get a complete listing of the BRAMs updated.*
- [Parent 24-2011] Structural ODC has moved 0 WLF to FN ports*

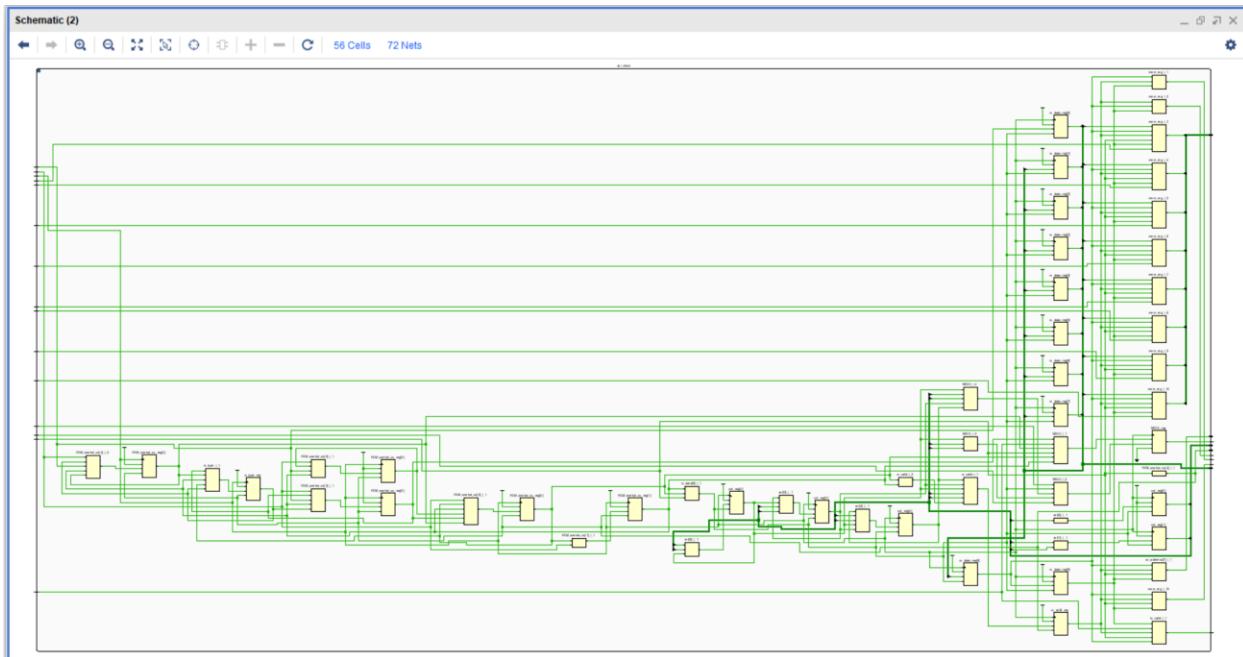
## E. CONCLUSION

ONE-HOT ENCODING IS FOUND TO BE THE BEST ENCODING

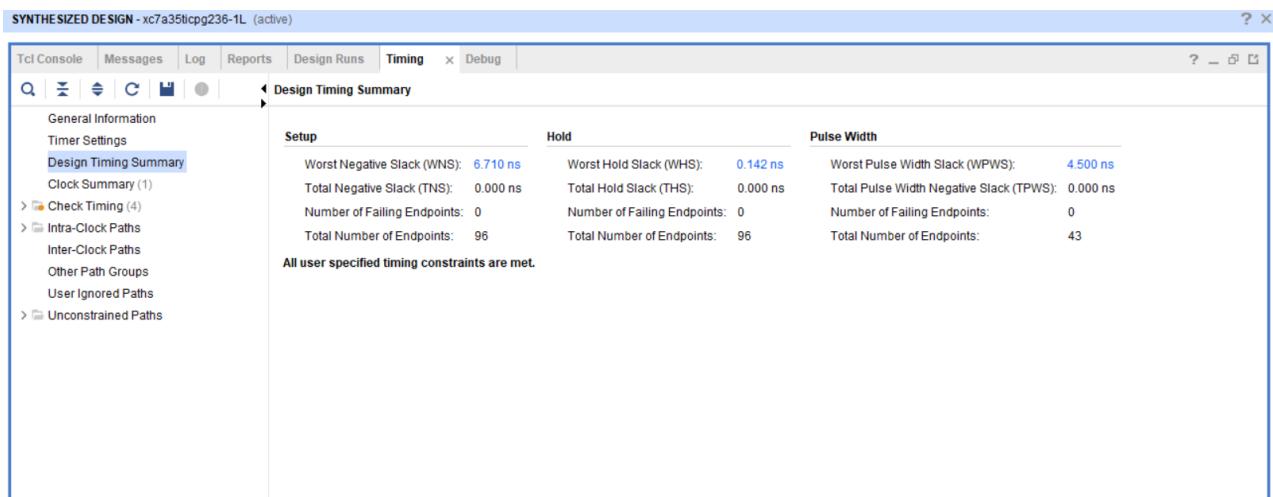
## I. SYNTHESIS POST-DEBUGGING

### 1. SCHEMATIC

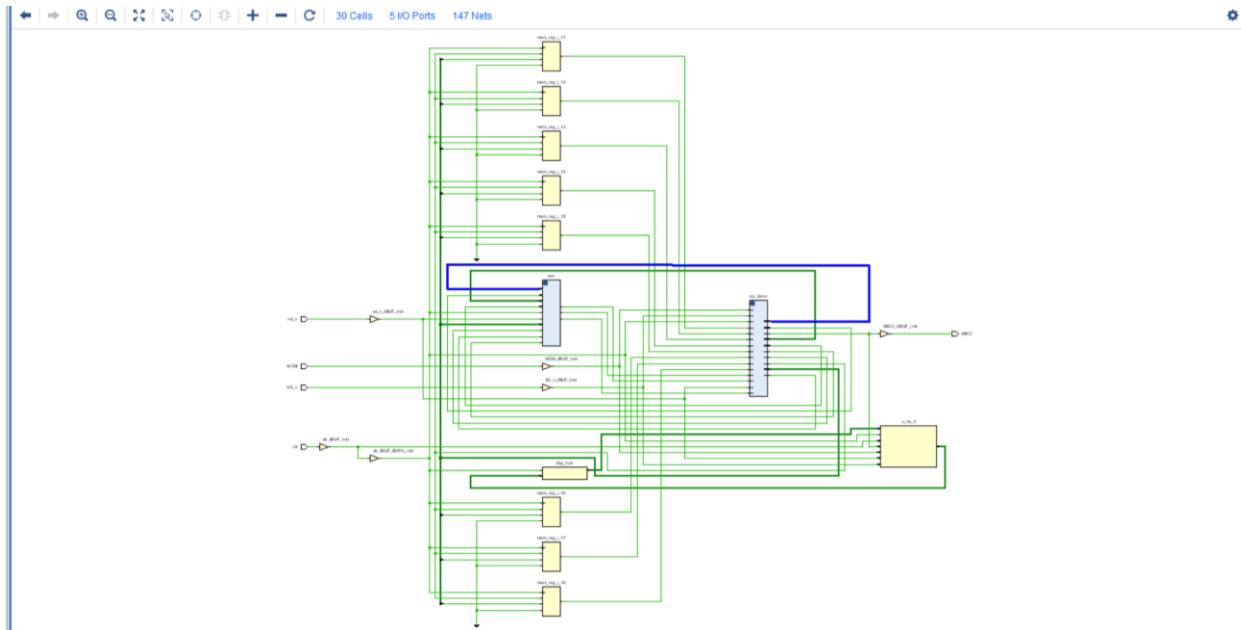




## 2. TIMING



## 3. CRITICAL PATH



## 4. UTILIZATION

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	30	40	0.5	5	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
ram (RAM)	2	9	0.5	0	0
spi_slave (SPI)	28	23	0	0	0
u_ilia_0 (u_ilia_0_CV)	0	0	0	0	0

## 5. MESSAGES

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Message Type	Count
Warning	1
Info	59
Status	39

Details:

- Synthesis (1 warning)  
[Constraints 18-5210] No constraint will be written out.

6. REPORT

```
synth_1_synth_synthesis_report_0 - synth_1

C:/Users/Farah/Downloads/Lint/project_2/project_1/project_1.runs/synth_1/SPI_Wrapper.vds

Q |          x

Read-only

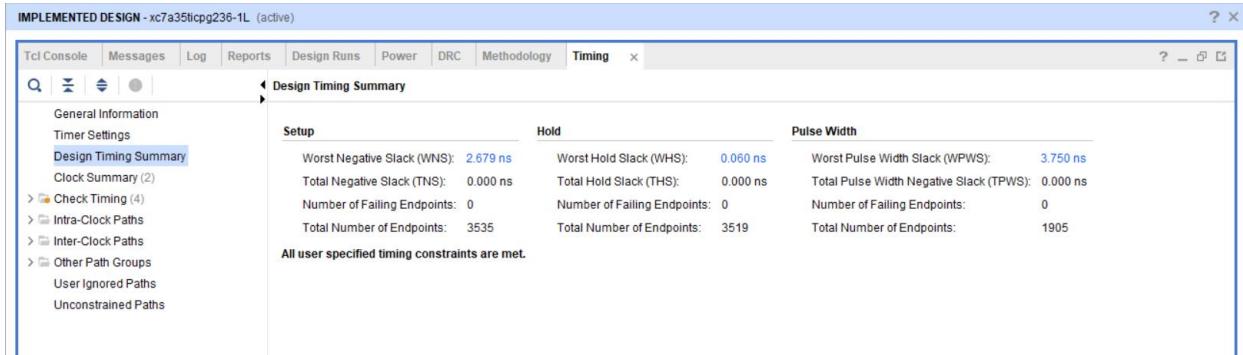
99 -----
100 -----
101 -----
102 -----
103 -----
104 -----
105 -----
106 -----
107 -----
108 -----
109 -----
```

## **II. IMPLEMENTATION POST-DEBUGGING**

## 1. DEVICE

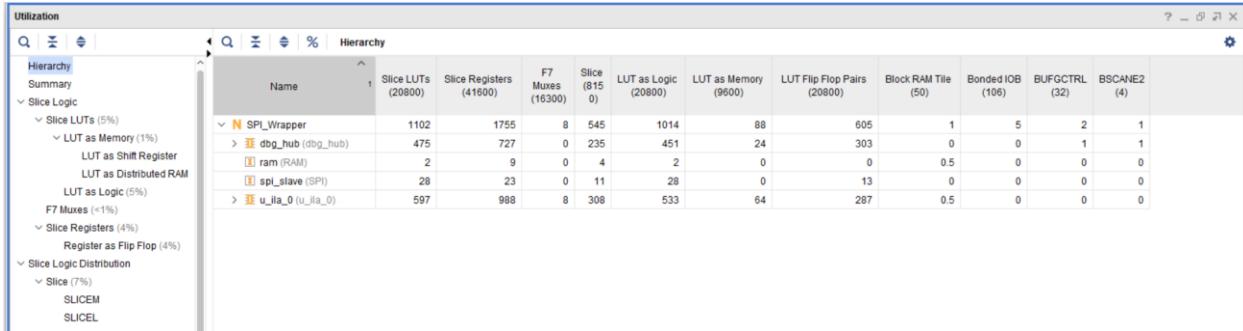


## 2. TIMING



The screenshot shows the 'Design Timing Summary' report for an implemented design. The report is divided into three main sections: Setup, Hold, and Pulse Width. Under Setup, it lists Worst Negative Slack (WNS) as 2.679 ns, Total Negative Slack (TNS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 3535. Under Hold, it lists Worst Hold Slack (WHS) as 0.060 ns, Total Hold Slack (THS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 3519. Under Pulse Width, it lists Worst Pulse Width Slack (WPWS) as 3.750 ns, Total Pulse Width Negative Slack (TPWS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 1905. A note at the bottom states: "All user specified timing constraints are met."

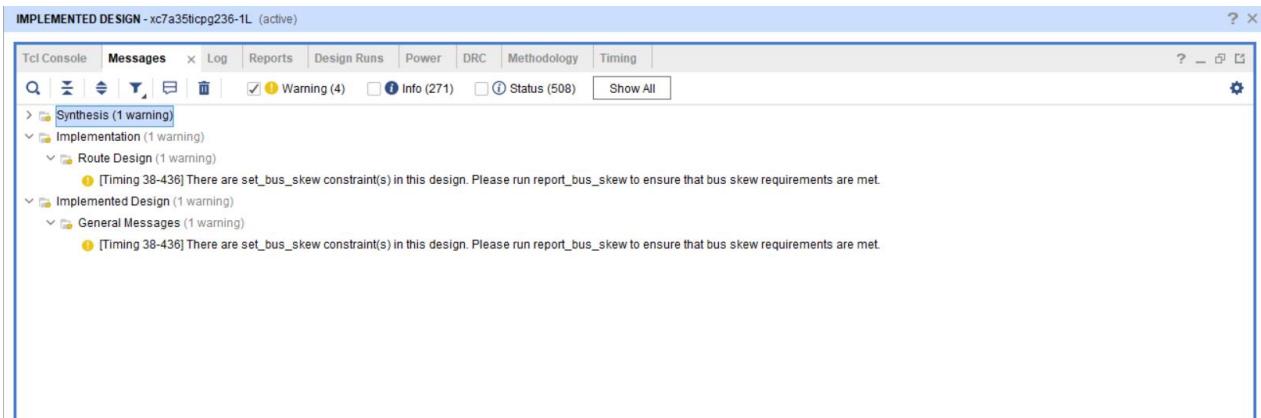
## 3. UTILIZATION



The screenshot shows the Utilization report. On the left, there is a hierarchical tree view of logic elements: Slice Logic (5%), Slice Registers (4%), and Slice (7%). The main pane displays utilization statistics for various components. The table includes columns for Name, Slice LUTs (20800), Slice Registers (41600), F7 Muxes (16300), Slice (8150), LUT as Logic (20800), LUT as Memory (9600), LUT Flip Flop Pairs (20800), Block RAM Tile (50), Bonded IOB (106), BUFGCTRL (32), and BSCANE2 (4). Key entries include SPI\_Wrapper, dbg\_hub, ram, spi\_slave, and u\_llla\_0.

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
N SPI_Wrapper	1102	1755	8	545	1014	88	605	1	5	2	1
> dbg_hub (dbg_hub)	475	727	0	235	451	24	303	0	0	1	1
ram (RAM)	2	9	0	4	2	0	0	0.5	0	0	0
spi_slave (SPI)	28	23	0	11	28	0	13	0	0	0	0
> u_llla_0 (u_llla_0)	597	988	8	308	533	64	287	0.5	0	0	0

## 4. MESSAGES



The screenshot shows the Messages report. The top navigation bar includes tabs for Tcl Console, Messages, Log, Reports, Design Runs, Power, DRC, Methodology, and Timing. The 'Messages' tab is active. The main pane displays a tree view of messages categorized by source: Synthesis (1 warning), Implementation (1 warning), Route Design (1 warning), Implemented Design (1 warning), and General Messages (1 warning). A note under Route Design states: "[Timing 38-436] There are set\_bus\_skew constraint(s) in this design. Please run report\_bus\_skew to ensure that bus skew requirements are met." A note under General Messages states: "[Timing 38-436] There are set\_bus\_skew constraint(s) in this design. Please run report\_bus\_skew to ensure that bus skew requirements are met."

## S-CONSTRAINT FILE

```
Constraints_basys3.xdc
1  ## This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6  ## Clock signal
7  set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
8  create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]
9
10
11  ## Switches
12  set_property -dict {PACKAGE_PIN V17 IOSTANDARD LVCMOS33} [get_ports MOSI]
13  set_property -dict {PACKAGE_PIN V16 IOSTANDARD LVCMOS33} [get_ports SS_n]
14  set_property -dict {PACKAGE_PIN W16 IOSTANDARD LVCMOS33} [get_ports rst_n]
15  # set_property -dict {PACKAGE_PIN W17 IOSTANDARD LVCMOS33} [get_ports {A[0]}]
16  # set_property -dict {PACKAGE_PIN W15 IOSTANDARD LVCMOS33} [get_ports {A[1]}]
17  # set_property -dict {PACKAGE_PIN V15 IOSTANDARD LVCMOS33} [get_ports {A[2]}]
18  # set_property -dict {PACKAGE_PIN W14 IOSTANDARD LVCMOS33} [get_ports {B[0]}]
19  # set_property -dict {PACKAGE_PIN W13 IOSTANDARD LVCMOS33} [get_ports {B[1]}]
20  # set_property -dict {PACKAGE_PIN V2 IOSTANDARD LVCMOS33} [get_ports {B[2]}]
21  # set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVCMOS33} [get_ports cin]
22  # set_property -dict {PACKAGE_PIN T2 IOSTANDARD LVCMOS33} [get_ports red_op_A]
23  # set_property -dict {PACKAGE_PIN R3 IOSTANDARD LVCMOS33} [get_ports red_op_B]
24  # set_property -dict {PACKAGE_PIN W2 IOSTANDARD LVCMOS33} [get_ports bypass_A]
25  # set_property -dict {PACKAGE_PIN U1 IOSTANDARD LVCMOS33} [get_ports bypass_B]
26  # set_property -dict {PACKAGE_PIN T1 IOSTANDARD LVCMOS33} [get_ports direction]
27  # set_property -dict {PACKAGE_PIN R2 IOSTANDARD LVCMOS33} [get_ports serial_in]
28
29
30  ## LEDs
31  set_property -dict {PACKAGE_PIN U16 IOSTANDARD LVCMOS33} [get_ports MISO]
32  # set_property -dict {PACKAGE_PIN E19 IOSTANDARD LVCMOS33} [get_ports {leds[1]}]
33  # set_property -dict {PACKAGE_PIN U19 IOSTANDARD LVCMOS33} [get_ports {leds[2]}]
34  # set_property -dict {PACKAGE_PIN V19 IOSTANDARD LVCMOS33} [get_ports {leds[3]}]
35  # set_property -dict {PACKAGE_PIN W18 IOSTANDARD LVCMOS33} [get_ports {leds[4]}]
36  # set_property -dict {PACKAGE_PIN U15 IOSTANDARD LVCMOS33} [get_ports {leds[5]}]
37  # set_property -dict {PACKAGE_PIN U14 IOSTANDARD LVCMOS33} [get_ports {leds[6]}]
38  # set_property -dict {PACKAGE_PIN V14 IOSTANDARD LVCMOS33} [get_ports {leds[7]}]

Constraints.basys3.xdc
39  # set_property -dict {PACKAGE_PIN V14 IOSTANDARD LVCMOS33} [get_ports {leds[7]}]
40  # set_property -dict {PACKAGE_PIN V13 IOSTANDARD LVCMOS33} [get_ports {leds[8]}]
41  # set_property -dict {PACKAGE_PIN V3 IOSTANDARD LVCMOS33} [get_ports {leds[9]}]
42  # set_property -dict {PACKAGE_PIN W3 IOSTANDARD LVCMOS33} [get_ports {leds[10]}]
43  # set_property -dict {PACKAGE_PIN U3 IOSTANDARD LVCMOS33} [get_ports {leds[11]}]
44  # set_property -dict {PACKAGE_PIN P3 IOSTANDARD LVCMOS33} [get_ports {leds[12]}]
45  # set_property -dict {PACKAGE_PIN N3 IOSTANDARD LVCMOS33} [get_ports {leds[13]}]
46  # set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVCMOS33} [get_ports {leds[14]}]
47  # set_property -dict {PACKAGE_PIN L1 IOSTANDARD LVCMOS33} [get_ports {leds[15]}]
48
49  ### Segment Display
50  #set_property -dict { PACKAGE_PIN W7 IOSTANDARD LVCMOS33 } [get_ports {seg[0]}]
51  #set_property -dict { PACKAGE_PIN W6 IOSTANDARD LVCMOS33 } [get_ports {seg[1]}]
52  #set_property -dict { PACKAGE_PIN U8 IOSTANDARD LVCMOS33 } [get_ports {seg[2]}]
53  #set_property -dict { PACKAGE_PIN V8 IOSTANDARD LVCMOS33 } [get_ports {seg[3]}]
54  #set_property -dict { PACKAGE_PIN U5 IOSTANDARD LVCMOS33 } [get_ports {seg[4]}]
55  #set_property -dict { PACKAGE_PIN V5 IOSTANDARD LVCMOS33 } [get_ports {seg[5]}]
56  #set_property -dict { PACKAGE_PIN U7 IOSTANDARD LVCMOS33 } [get_ports {seg[6]}]
57
58  #set_property -dict { PACKAGE_PIN V7 IOSTANDARD LVCMOS33 } [get_ports dp]
59
60  #set_property -dict { PACKAGE_PIN U2 IOSTANDARD LVCMOS33 } [get_ports {an[0]}]
61  #set_property -dict { PACKAGE_PIN U4 IOSTANDARD LVCMOS33 } [get_ports {an[1]}]
62  #set_property -dict { PACKAGE_PIN V4 IOSTANDARD LVCMOS33 } [get_ports {an[2]}]
63  #set_property -dict { PACKAGE_PIN W4 IOSTANDARD LVCMOS33 } [get_ports {an[3]}]
64
65  ##Buttons
66  #set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVCMOS33 } [get_ports btnU]
67  #set_property -dict { PACKAGE_PIN W19 IOSTANDARD LVCMOS33 } [get_ports btnL]
68  #set_property -dict { PACKAGE_PIN T17 IOSTANDARD LVCMOS33 } [get_ports btnR]
69  #set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVCMOS33 } [get_ports btnD]
70
71
72  ##Pmod Header JA
73  #set_property -dict { PACKAGE_PIN J1 IOSTANDARD LVCMOS33 } [get_ports {JA[0]}];#Sch name = JA1
74  #set_property -dict { PACKAGE_PIN L2 IOSTANDARD LVCMOS33 } [get_ports {JA[1]}];#Sch name = JA2
75  #set_property -dict { PACKAGE_PIN J2 IOSTANDARD LVCMOS33 } [get_ports {JA[2]}];#Sch name = JA3
76  #set_property -dict { PACKAGE_PIN G2 IOSTANDARD LVCMOS33 } [get_ports {JA[3]}];#Sch name = JA4
```

```

    Constraints_basys3.xdc
17  #set_property -dict { PACKAGE_PIN H1 IOSTANDARD LVCMS33 } [get_ports {A[4]}];#Sch name = JA7
18  #set_property -dict { PACKAGE_PIN K2 IOSTANDARD LVCMS33 } [get_ports {A[5]}];#Sch name = JA8
19  #set_property -dict { PACKAGE_PIN H2 IOSTANDARD LVCMS33 } [get_ports {A[6]}];#Sch name = JA9
20  #set_property -dict { PACKAGE_PIN G3 IOSTANDARD LVCMS33 } [get_ports {A[7]}];#Sch name = JA10
21
22  ##Pmod Header JB
23  #set_property -dict { PACKAGE_PIN A14 IOSTANDARD LVCMS33 } [get_ports {JB[0]}];#Sch name = JB1
24  #set_property -dict { PACKAGE_PIN A16 IOSTANDARD LVCMS33 } [get_ports {JB[1]}];#Sch name = JB2
25  #set_property -dict { PACKAGE_PIN B15 IOSTANDARD LVCMS33 } [get_ports {JB[2]}];#Sch name = JB3
26  #set_property -dict { PACKAGE_PIN B16 IOSTANDARD LVCMS33 } [get_ports {JB[3]}];#Sch name = JB4
27  #set_property -dict { PACKAGE_PIN A15 IOSTANDARD LVCMS33 } [get_ports {JB[4]}];#Sch name = JB7
28  #set_property -dict { PACKAGE_PIN A17 IOSTANDARD LVCMS33 } [get_ports {JB[5]}];#Sch name = JB8
29  #set_property -dict { PACKAGE_PIN C15 IOSTANDARD LVCMS33 } [get_ports {JB[6]}];#Sch name = JB9
30  #set_property -dict { PACKAGE_PIN C16 IOSTANDARD LVCMS33 } [get_ports {JB[7]}];#Sch name = JB10
31
32  ##Pmod Header JC
33  #set_property -dict { PACKAGE_PIN K17 IOSTANDARD LVCMS33 } [get_ports {JC[0]}];#Sch name = JC1
34  #set_property -dict { PACKAGE_PIN M18 IOSTANDARD LVCMS33 } [get_ports {JC[1]}];#Sch name = JC2
35  #set_property -dict { PACKAGE_PIN N17 IOSTANDARD LVCMS33 } [get_ports {JC[2]}];#Sch name = JC3
36  #set_property -dict { PACKAGE_PIN P18 IOSTANDARD LVCMS33 } [get_ports {JC[3]}];#Sch name = JC4
37  #set_property -dict { PACKAGE_PIN L17 IOSTANDARD LVCMS33 } [get_ports {JC[4]}];#Sch name = JC7
38  #set_property -dict { PACKAGE_PIN M19 IOSTANDARD LVCMS33 } [get_ports {JC[5]}];#Sch name = JC8
39  #set_property -dict { PACKAGE_PIN P17 IOSTANDARD LVCMS33 } [get_ports {JC[6]}];#Sch name = JC9
40  #set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVCMS33 } [get_ports {JC[7]}];#Sch name = JC10
41
42  ##Pmod Header JXADC
43  #set_property -dict { PACKAGE_PIN J3 IOSTANDARD LVCMS33 } [get_ports {JXADC[0]}];#Sch name = XA1_P
44  #set_property -dict { PACKAGE_PIN L3 IOSTANDARD LVCMS33 } [get_ports {JXADC[1]}];#Sch name = XA2_P
45  #set_property -dict { PACKAGE_PIN M2 IOSTANDARD LVCMS33 } [get_ports {JXADC[2]}];#Sch name = XA3_P
46  #set_property -dict { PACKAGE_PIN N2 IOSTANDARD LVCMS33 } [get_ports {JXADC[3]}];#Sch name = XA4_P
47  #set_property -dict { PACKAGE_PIN K3 IOSTANDARD LVCMS33 } [get_ports {JXADC[4]}];#Sch name = XA1_N
48  #set_property -dict { PACKAGE_PIN M3 IOSTANDARD LVCMS33 } [get_ports {JXADC[5]}];#Sch name = XA2_N
49  #set_property -dict { PACKAGE_PIN M1 IOSTANDARD LVCMS33 } [get_ports {JXADC[6]}];#Sch name = XA3_N
50  #set_property -dict { PACKAGE_PIN N1 IOSTANDARD LVCMS33 } [get_ports {JXADC[7]}];#Sch name = XA4_N
51
52
53  Constraints_basys3.xdc
121  #set_property -dict { PACKAGE_PIN J18 IOSTANDARD LVCMS33 } [get_ports {vgaBlue[3]}]
122  #set_property -dict { PACKAGE_PIN J17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[0]}]
123  #set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[1]}]
124  #set_property -dict { PACKAGE_PIN G17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[2]}]
125  #set_property -dict { PACKAGE_PIN D17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[3]}]
126  #set_property -dict { PACKAGE_PIN P19 IOSTANDARD LVCMS33 } [get_ports Hsync]
127  #set_property -dict { PACKAGE_PIN R19 IOSTANDARD LVCMS33 } [get_ports Vsync]
128
129
130  ##USB-RS232 Interface
131  #set_property -dict { PACKAGE_PIN B18 IOSTANDARD LVCMS33 } [get_ports RsRx]
132  #set_property -dict { PACKAGE_PIN A18 IOSTANDARD LVCMS33 } [get_ports RsTx]
133
134
135  ##USB HID (PS/2)
136  #set_property -dict { PACKAGE_PIN C17 IOSTANDARD LVCMS33 PULLUP true } [get_ports PS2Clk]
137  #set_property -dict { PACKAGE_PIN B17 IOSTANDARD LVCMS33 PULLUP true } [get_ports PS2Data]
138
139
140  ##Quad SPI Flash
141  ##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
142  ##STARTUPE2 primitive.
143  #set_property -dict { PACKAGE_PIN D18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[0]}]
144  #set_property -dict { PACKAGE_PIN D19 IOSTANDARD LVCMS33 } [get_ports {QspiDB[1]}]
145  #set_property -dict { PACKAGE_PIN G18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[2]}]
146  #set_property -dict { PACKAGE_PIN F18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[3]}]
147  #set_property -dict { PACKAGE_PIN K19 IOSTANDARD LVCMS33 } [get_ports QspicSn]
148
149
150  ## Configuration options, can be used for all designs
151  set_property CONFIG_VOLTAGE 3.3 [current_design]
152  set_property CFGBVS VCCO [current_design]
153
154  ## SPI configuration mode options for QSPI boot, can be used for all designs
155  set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
156  set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
157  set_property CONFIG_MODE SPIx4 [current_design]
158

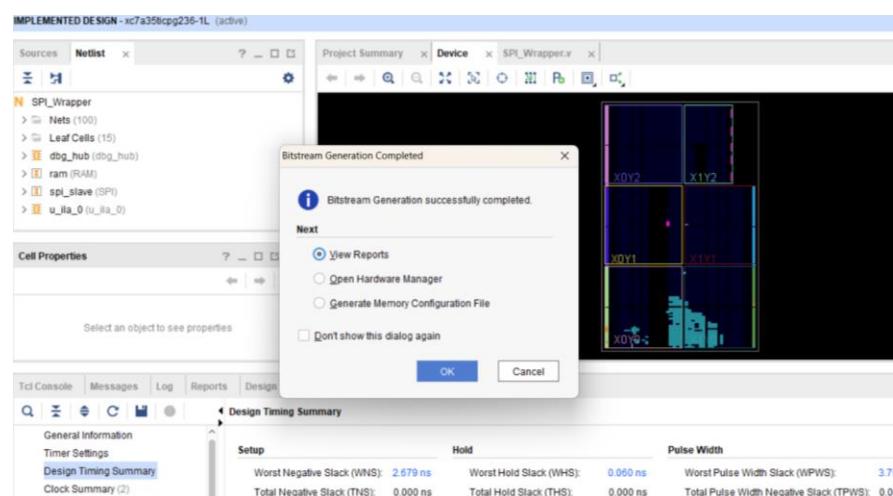
```

```

Constraints_basys3.xdc
158
159  create_debug_core u_il_0 ila
160  set_property ALL_PROBE_SAME_MU true [get_debug_cores u_il_0]
161  set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_il_0]
162  set_property C_ADV_TRIGGER false [get_debug_cores u_il_0]
163  set_property C_DATA_DEPTH 1024 [get_debug_cores u_il_0]
164  set_property C_EN_STRG_QUAL false [get_debug_cores u_il_0]
165  set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_il_0]
166  set_property C_TRIGIN_EN false [get_debug_cores u_il_0]
167  set_property C_TRIGOUT_EN false [get_debug_cores u_il_0]
168  set_property port_width 1 [get_debug_ports u_il_0/clk]
169  connect_debug_port u_il_0/clk [get_nets [list clk_IBUF_BUFG]]
170  set_property PROBE_TYPE TRIGGER [get_debug_ports u_il_0/probe0]
171  set_property port_width 1 [get_debug_ports u_il_0/probe0]
172  connect_debug_port u_il_0/probe0 [get_nets [list clk_IBUF]]
173  create_debug_port u_il_0 probe
174  set_property PROBE_TYPE DATA [get_debug_ports u_il_0/probe1]
175  set_property port_width 1 [get_debug_ports u_il_0/probe1]
176  connect_debug_port u_il_0/probe1 [get_nets [list MISO_OBUF]]
177  create_debug_port u_il_0 probe
178  set_property PROBE_TYPE DATA [get_debug_ports u_il_0/probe2]
179  set_property port_width 1 [get_debug_ports u_il_0/probe2]
180  connect_debug_port u_il_0/probe2 [get_nets [list MOSI_IBUF]]
181  create_debug_port u_il_0 probe
182  set_property PROBE_TYPE DATA [get_debug_ports u_il_0/probe3]
183  set_property port_width 1 [get_debug_ports u_il_0/probe3]
184  connect_debug_port u_il_0/probe3 [get_nets [list rst_n_IBUF]]
185  create_debug_port u_il_0 probe
186  set_property PROBE_TYPE DATA [get_debug_ports u_il_0/probe4]
187  set_property port_width 1 [get_debug_ports u_il_0/probe4]
188  connect_debug_port u_il_0/probe4 [get_nets [list SS_n_IBUF]]
189  set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
190  set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
191  set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
192  connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
193

```

## 6-BITSTREAM FILE



IMPLEMENTED DESIGN - xc7a35tcipg236-1L (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing

Warning (9) Info (434) Status (833) Show All

- Write Bitstream (1 warning, 22 infos)
  - [Netlist 29-17] Analyzing 77 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-479] Netlist was created with Vivado 2018.2
  - [Device 21-403] Loading part xc7a35tcipg236-1L
  - [Project 1-570] Preparing netlist for logic optimization
  - [Timing 38-478] Restoring timing data from binary archive.
  - [Timing 38-479] Binary timing data restore complete.
  - [Project 1-856] Restoring constraints from binary archive.
  - [Project 1-853] Binary constraint restore complete.
  - [Project 1-111] Unisim Transformation Summary:  
A total of 38 instances were transformed.  
CFG GLUTS => CFG GLUTS (SRLC32E, SRL16E): 32 instances  
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
  - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
  - [IP\_Flow 19-234] Refreshing IP repositories
  - [IP\_Flow 19-1704] No user IP repositories specified
  - [IP\_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/Vivado/2018.2/data/ip'.
  - [DRC 23-27] Running DRC with 2 threads
- DRC (1 warning)
  - [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
  - [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.
  - [Designutils 20-2272] Running write\_bitstream with 2 threads.
  - [Vivado 12-1842] Bitgen Completed Successfully.
  - [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.
  - [Common 17-83] Releasing license: Implementation

## F-LINT TOOL SNIPPETS

Questa Lint 2021.1 .../Users/Lenovo/Desktop/Final/lint.db

File Edit View Objects Window Help

Objects C:/Users/Lenovo/Desktop/Final/SPI/SPI/SPI\_Wrapper.v [SPI\_Wrapper]

Show Collated View

Search: Type Search Text ... Exact »

Name	Clock Group	Reset Group	Kind
clk	Unspecified	Unspecified	Port
MISO	Unspecified	Unspecified	Port
MOSI	Unspecified	Unspecified	Port
rst_n	Unspecified	Unspecified	Port
rx_data	Unspecified	Unspecified	Net
rx_valid	Unspecified	Unspecified	Net
SS_n	Unspecified	Unspecified	Port
tx_data	Unspecified	Unspecified	Net
tx_valid	Unspecified	Unspecified	Net

```

1 module SPI_Wrapper (
2     input clk, rst_n, SS_n, MOSI,
3     output MISO
4 );
5
6     wire tx_valid, rx_valid;
7     wire[7:0] tx_data;
8     wire[9:0] rx_data;
9
10    SPI spi_slave(
11        .clk(clk), .rst_n(rst_n), .SS_n(SS_n), .MOSI(MOSI),
12        .tx_valid(tx_valid), .tx_data(tx_data), .MISO(MISO),
13        .rx_valid(rx_valid), .rx_data(rx_data)
14    );
15
16    RAM ram(
17        .clk(clk), .rst_n(rst_n), .rx_valid(rx_valid),
18        .rx_data(rx_data), .tx_valid(tx_valid), .tx_data(tx_data)
19    );
20
21 endmodule

```

Flow Navigator Design Objects Lint Checks

Filter: Type here Severity Status Check Alias Message

Severity	Status	Check	Alias	Message
Info	Waived	multi_ports_in_single_line		Multiple ports are declared in one line. Module RAM, File C:/Users/Lenovo/Desktop/Final/SPI/RAM.v, Line 5.
Info	Fixed	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI, File C:/Users/Lenovo/Desktop/Final/SPI/SPI.v, Line 2.
Info	Pending	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_Wrapper, File C:/Users/Lenovo/Desktop/Final/SPI/SPI_Wrapper.v, ...

Transcript Message Viewer Lint Checks Design Metrics Design Information Status History Lint Dashboard

C:/Users/Lenovo/Desktop/Final/SPI/SPI/SPI\_Wrapper.v [SPI\_Wrapper]