

PROJECT 1

Spartan6 - DSP48A1

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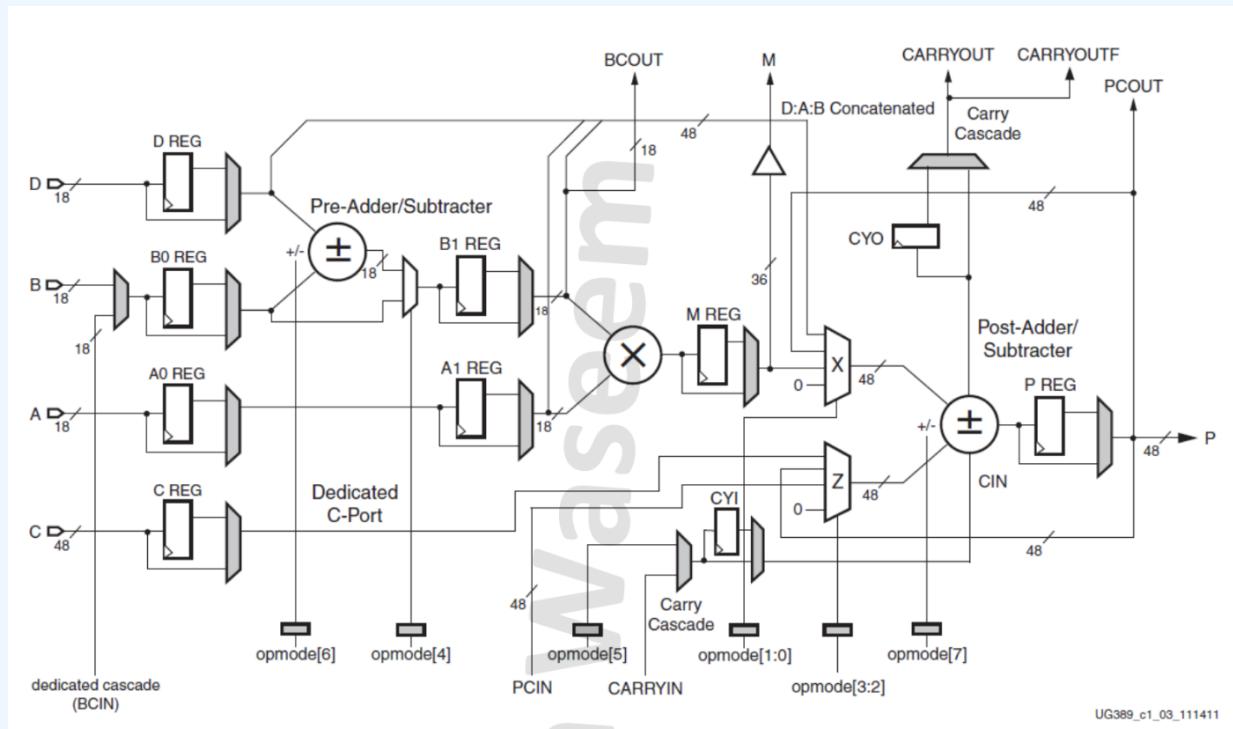
INTRODUCTION

The DSP48A1 is a dedicated Digital Signal Processing (DSP) block available in the Xilinx Spartan-6 FPGA family. It is designed for high-performance and low-power arithmetic operations, making it ideal for computationally intensive tasks in digital systems.

This block is widely used for:

- Multiply-Accumulate (MAC) operations
- Multiply-Add (MAD) computations
- Complex digital filters
- High-speed signal processing pipelines

By integrating the DSP48A1 slice, designers can achieve efficient and optimized hardware implementations for applications such as communication systems, image processing, and control systems.



RTL CODE

```
D: > Digital Design > Project 1 > mux_ff.v
 1  module mux_ff#(
 2    parameter N = 18,
 3    parameter RSTTYPE = "SYNC"
 4  ) (
 5    input clk, rst, en, REG,
 6    input[N-1:0] d,
 7    output[N-1:0] q
 8  );
 9  reg[N-1:0] out;
10
11 generate
12   if (RSTTYPE == "SYNC") begin
13     always @ (posedge clk) begin
14       if(rst) out <= {N{1'b0}};
15       else if(en) out <= d;
16     end
17   end
18   else begin
19     always @ (posedge clk, posedge rst) begin
20       if(rst) out <= {N{1'b0}};
21       else if(en) out <= d;
22     end
23   end
24 endgenerate
25
26 assign q = (REG) ? out : d;
27
28 endmodule
```

```
V DSP48A1.v
 1  module DSP48A1 #(
 2    parameter A0REG = 0,
 3    parameter A1REG = 1,
 4    parameter B0REG = 0,
 5    parameter B1REG = 1,
 6    parameter CREG = 1,
 7    parameter DREG = 1,
 8    parameter MREG = 1,
 9    parameter PREG = 1,
10    parameter CARRYINREG = 1,
11    parameter CARRYOUTREG = 1,
12    parameter OPMODEREG = 1,
13    parameter CARRYINSEL = "OPMODE5",
14    parameter B_INPUT = "DIRECT",
15    parameter RSTTYPE = "SYNC"
16  ) (
17    input CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP,
18    CARRYIN, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP,
19    input[7:0] OPMODE,
20    input[17:0] A, B, D, BCIN,
21    input[47:0] C, PCIN,
22    output CARRYOUT, CARRYOUTF,
23    output[17:0] BOUT,
24    output[35:0] M,
25    output[47:0] P, POUT
26  );
27
```

```

27
28     wire[7:0] OPMODE_reg;
29     wire[17:0] A0_reg, B0_reg, B_sel_wire, D_reg;
30     wire[47:0] C_reg;
31     assign B_sel_wire = (B_INPUT == "DIRECT") ? B : (B_INPUT == "CASCADE") ? BCIN : 0;
32
33     mux_ff #(N(18), .RSTTYPE(RSTTYPE)) mA0(
34         .clk(CLK), .rst(RSTA), .en(CEA), .REG(A0REG), .d(A), .q(A0_reg)
35     );
36     mux_ff #(N(18), .RSTTYPE(RSTTYPE)) mB0(
37         .clk(CLK), .rst(RSTB), .en(CEB), .REG(B0REG), .d(B_sel_wire), .q(B0_reg)
38     );
39     mux_ff #(N(48), .RSTTYPE(RSTTYPE)) mC(
40         .clk(CLK), .rst(RSTC), .en(CEC), .REG(CREG), .d(C), .q(C_reg)
41     );
42     mux_ff #(N(18), .RSTTYPE(RSTTYPE)) mD(
43         .clk(CLK), .rst(RSTD), .en(CED), .REG(DREG), .d(D), .q(D_reg)
44     );
45     mux_ff #(N(8), .RSTTYPE(RSTTYPE)) mOP(
46         .clk(CLK), .rst(RSTOPMODE), .en(CEOPMODE), .REG(OPMODEREG), .d(OPMODE), .q(OPMODE_reg)
47     );
48

```

```

48
49     wire[17:0] add_sub1_wire, A1_reg, B1_reg, B_mux_wire;
50     assign add_sub1_wire = (OPMODE_reg[6]) ? D_reg - B0_reg : D_reg + B0_reg;
51     assign B_mux_wire = (OPMODE_reg[4]) ? add_sub1_wire : B0_reg;
52
53     mux_ff #(N(18), .RSTTYPE(RSTTYPE)) mA1(
54         .clk(CLK), .rst(RSTA), .en(CEA), .REG(A1REG), .d(A0_reg), .q(A1_reg)
55     );
56     mux_ff #(N(18), .RSTTYPE(RSTTYPE)) mB1(
57         .clk(CLK), .rst(RSTB), .en(CEB), .REG(B1REG), .d(B_mux_wire), .q(B1_reg)
58     );
59
60     assign BOUT = B1_reg;
61
62     wire[35:0] mul_wire, mul_reg;
63     assign mul_wire = A1_reg*B1_reg;
64
65     mux_ff #(N(36), .RSTTYPE(RSTTYPE)) mM(
66         .clk(CLK), .rst(RSTM), .en(CEM), .REG(MREG), .d(mul_wire), .q(mul_reg)
67     );
68     assign M = mul_reg;
69

```

```

70  // mux x
71  reg[47:0] mux_x_wire;
72  wire[47:0] conc_wire = {D_reg[11:0], A1_reg, B1_reg};
73  always @(*) begin
74      case(OPMODE_reg[1:0])
75      2'b00: mux_x_wire = 0;
76      2'b01: mux_x_wire = mul_reg;
77      2'b10: mux_x_wire = P;
78      default: mux_x_wire = conc_wire;
79  endcase
80 end
81
82 //mux z
83 reg[47:0] mux_z_wire;
84 always @(*) begin
85     case(OPMODE_reg[3:2])
86     2'b00: mux_z_wire = 0;
87     2'b01: mux_z_wire = PCIN;
88     2'b10: mux_z_wire = P;
89     default: mux_z_wire = C_reg;
90 endcase
91 end
92

```

```

94
95 wire CARRY.Cascade_wire, CARRYIN_reg;
96 assign CARRY.Cascade_wire = (CARRYINSEL == "OPMDES") ? OPMODE_reg[5] : (CARRYINSEL == "CARRYIN") ? CARRYIN : 0;
97
98 mux_ff #(N(1), .RSTTYPE(RSTTYPE)) mCI(
99     .clk(CLK), .rst(RSTCARRYIN), .en(CECARRYIN), .REG(CARRYINREG), .d(CARRY.Cascade_wire), .q(CARRYIN_reg)
100 );
101
102 wire CARRYOUT_wire;
103 wire[47:0] add_sub2_wire;
104
105 assign {CARRYOUT_wire, add_sub2_wire} = (OPMODE_reg[7]) ? mux_z_wire - mux_x_wire - CARRYIN_reg : mux_z_wire + mux_x_wire + CARRYIN_reg;
106
107 mux_ff #(N(1), .RSTTYPE(RSTTYPE)) mCO(
108     .clk(CLK), .rst(RSTCARRYIN), .en(CECARRYIN), .REG(CARRYOUTREG), .d(CARRYOUT_wire), .q(CARRYOUT)
109 );
110
111 assign CARRYOUTF = CARRYOUT;
112
113 mux_ff #(N(48), .RSTTYPE(RSTTYPE)) mP(
114     .clk(CLK), .rst(RSTP), .en(CEP), .REG(PREG), .d(add_sub2_wire), .q(P)
115 );
116
117 assign POUT = P;
118
119 endmodule

```

TESTBENCH CODE

```
▼ DSP48A1_tb.v
 1  module DSP48A1_tb();
 2    reg CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, CARRYIN;
 3    reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
 4    reg[7:0] OPMODE;
 5    reg[17:0] A, B, D, BCIN;
 6    reg[47:0] C, PCIN;
 7    wire CARRYOUT, CARRYOUTF;
 8    wire[17:0] BOUT;
 9    wire[35:0] M;
10    wire[47:0] P, POUT;
11
12    DSP48A1 D1(
13      .CLK(CLK), .CEA(CEA), .CEB(CEB), .CEC(CEC), .CECARRYIN(CECARRYIN),
14      .CED(CED), .CEM(CEM), .CEOPMODE(CEOPMODE), .CEP(CEP), .CARRYIN(CARRYIN),
15      .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC), .RSTCARRYIN(RSTCARRYIN), .RSTD(RSTD),
16      .RSTM(RSTM), .RSTOPMODE(RSTOPMODE), .RSTP(RSTP), .OPMODE(OPMODE),
17      .A(A), .B(B), .D(D), .BCIN(BCIN), .C(C), .PCIN(PCIN), .CARRYOUT(CARRYOUT),
18      .CARRYOUTF(CARRYOUTF), .BOUT(BOUT), .M(M), .P(P), .POUT(POUT)
19  );
20
21  initial begin
22    CLK = 0;
23    forever #1 CLK = ~CLK;
24  end
25
26  initial begin
27    RSTA=1; RSTB=1; RSTC=1; RSTCARRYIN=1; RSTD=1; RSTM=1; RSTOPMODE=1; RSTP=1;
28    CEA = $random; CEB = $random; CEC = $random; CECARRYIN = $random; CED = $random;
29    CEM = $random; CEOPMODE = $random; CEP = $random; CARRYIN = $random; OPMODE = $random;
30    A = $random; B = $random; C = $random; D = $random; PCIN = $random; BCIN = $random;
31    @(negedge CLK);
32
33    RSTA=0; RSTB=0; RSTC=0; RSTCARRYIN=0; RSTD=0; RSTM=0; RSTOPMODE=0; RSTP=0;
34    CEA = 1; CEB = 1; CEC = 1; CECARRYIN = 1; CED = 1; CEM = 1; CEOPMODE = 1; CEP = 1;
35  
```

```

36 OPMODE = 8'b11011101; A = 20; B = 10; C = 350; D = 25;
37 CARRYIN = $random; PCIN = $random; BCIN = $random;
38 repeat(4) @ (negedge CLK);
39 if(BOUT != 18'hf || M != 36'h12c || P != 48'h32 || POUT != 48'h32 || CARRYOUT != 0 || CARRYOUTF != 0) begin
40     $display("ERROR - BOUT= %h, M = %h, P = %h, POUT = %h, CARRYOUT = %h, CARRYOUTF = %h",BOUT, M, P, POUT, CARRYOUT, CARRYOUTF);
41     $display("EXPECTED- BOUT= 18'hf, M = 36'h12c, P = 48'h32, POUT = 48'h32, CARRYOUT = 0, CARRYOUTF = 0");
42     $stop;
43 end
44 OPMODE = 8'b00010000;
45 CARRYIN = $random; PCIN = $random; BCIN = $random;
46 repeat(3) @ (negedge CLK);
47 if(BOUT != 18'h23 || M != 36'h2bc || P != 48'h0 || POUT != 48'h0 || CARRYOUT != 0 || CARRYOUTF != 0) begin
48     $display("ERROR - BOUT= %h, M = %h, P = %h, POUT = %h, CARRYOUT = %h, CARRYOUTF = %h",BOUT, M, P, POUT, CARRYOUT, CARRYOUTF);
49     $display("EXPECTED- BOUT= 18'h23, M = 36'h2bc, P = 48'h0, POUT = 48'h0, CARRYOUT = 0, CARRYOUTF = 0");
50     $stop;
51 end
52 OPMODE = 8'b00001010;
53 CARRYIN = $random; PCIN = $random; BCIN = $random;
54 repeat(3) @ (negedge CLK);
55 if(BOUT != 18'ha || M != 36'hc8 || P != 48'h0 || POUT != 48'h0 || CARRYOUT != 0 || CARRYOUTF != 0) begin
56     $display("ERROR - BOUT= %h, M = %h, P = %h, POUT = %h, CARRYOUT = %h, CARRYOUTF = %h",BOUT, M, P, POUT, CARRYOUT, CARRYOUTF);
57     $display("EXPECTED- BOUT= 18'ha, M = 36'hc8, P = 48'h0, POUT = 48'h0, CARRYOUT = 0, CARRYOUTF = 0");
58     $stop;
59 end
60 OPMODE = 8'b10100111; A = 5; B = 6; C = 350; D = 25; PCIN = 3000;
61 CARRYIN = $random; BCIN = $random;
62 repeat(4) @ (negedge CLK);
63 if(BOUT != 18'h6 || M != 36'h1e || P != 48'hfe6ffffec0bb1 || POUT != 48'hfe6ffffec0bb1 || CARRYOUT != 1 || CARRYOUTF != 1) begin
64     $display("ERROR - BOUT= %h, M = %h, P = %h, POUT = %h, CARRYOUT = %h, CARRYOUTF = %h",BOUT, M, P, POUT, CARRYOUT, CARRYOUTF);
65     $display("EXPECTED- BOUT= 18'h6, M = 36'h1e, P = 48'hfe6ffffec0bb1, POUT = 48'hfe6ffffec0bb1, CARRYOUT = 1, CARRYOUTF = 1");
66     $stop;
67 end
68 $stop;
69 end

```

```

70
71 initial begin
72     $monitor("BOUT= %h, M = %h, P = %h, POUT = %h, CARRYOUT = %h, CARRYOUTF = %h",BOUT, M, P, POUT, CARRYOUT, CARRYOUTF);
73 end
74
75 endmodule
76

```

DO FILE

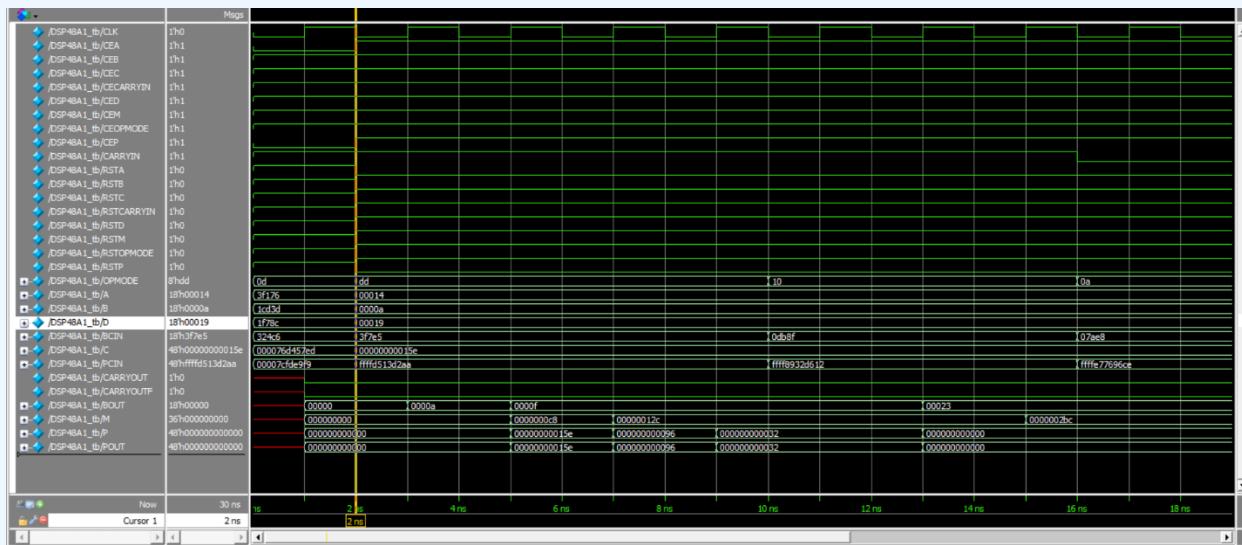
```

run_dsp.do
1 vlib work
2 vlog DSP48A1.v DSP48A1_tb.v
3 vsim -voptargs=+acc work.DSP48A1_tb
4 add wave *
5 run -all
6 #quit -sim
7

```

WAVEFORM

- Reset



- Path 1

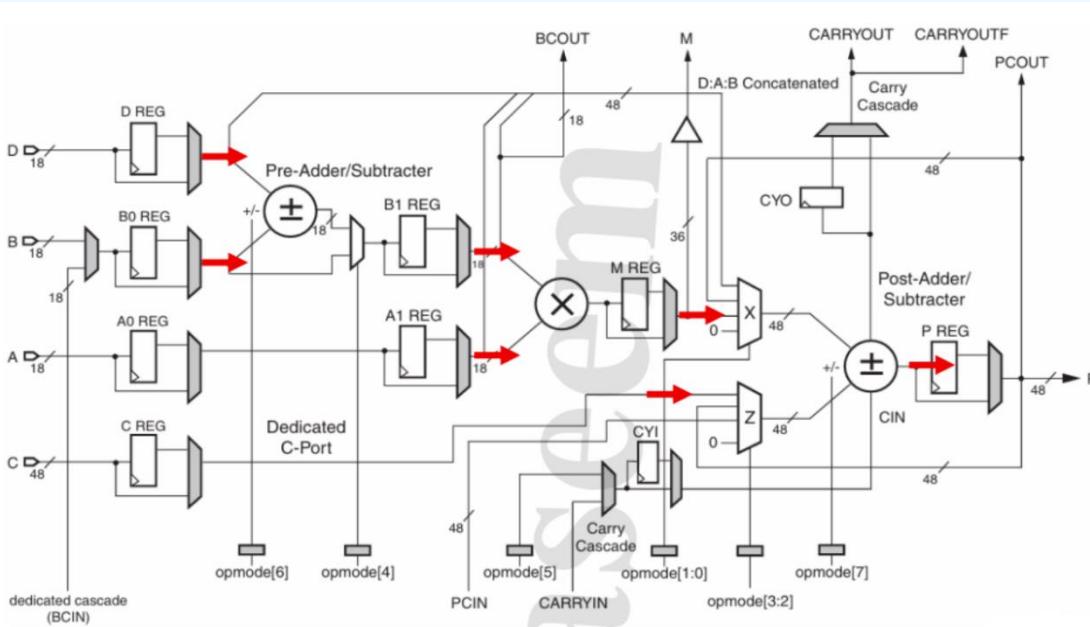
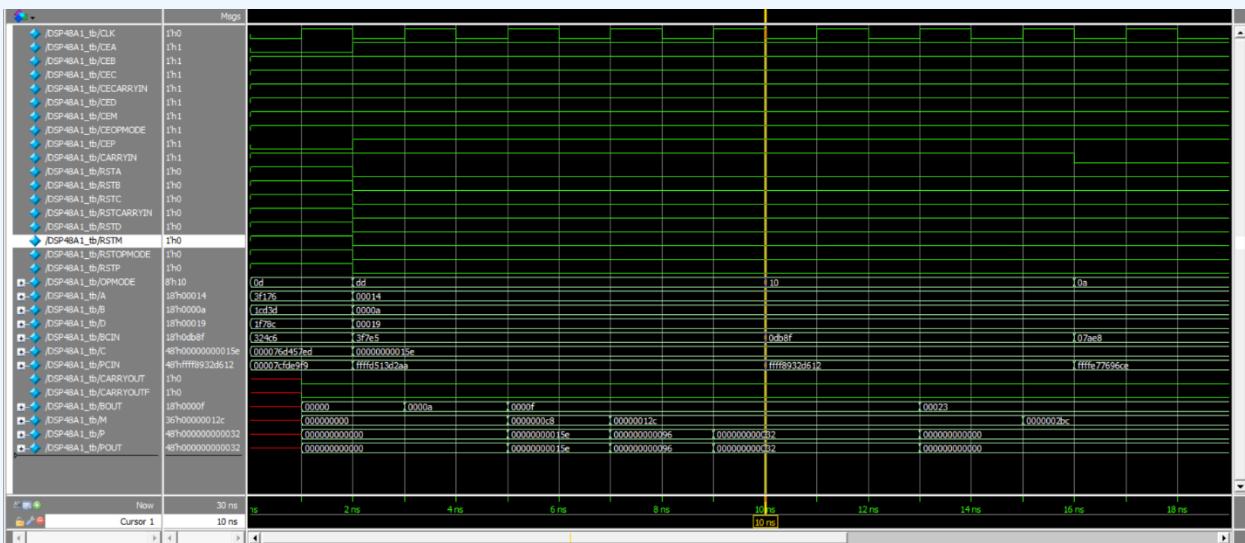


Figure 1: Path 1 Data Flow



- Path 2

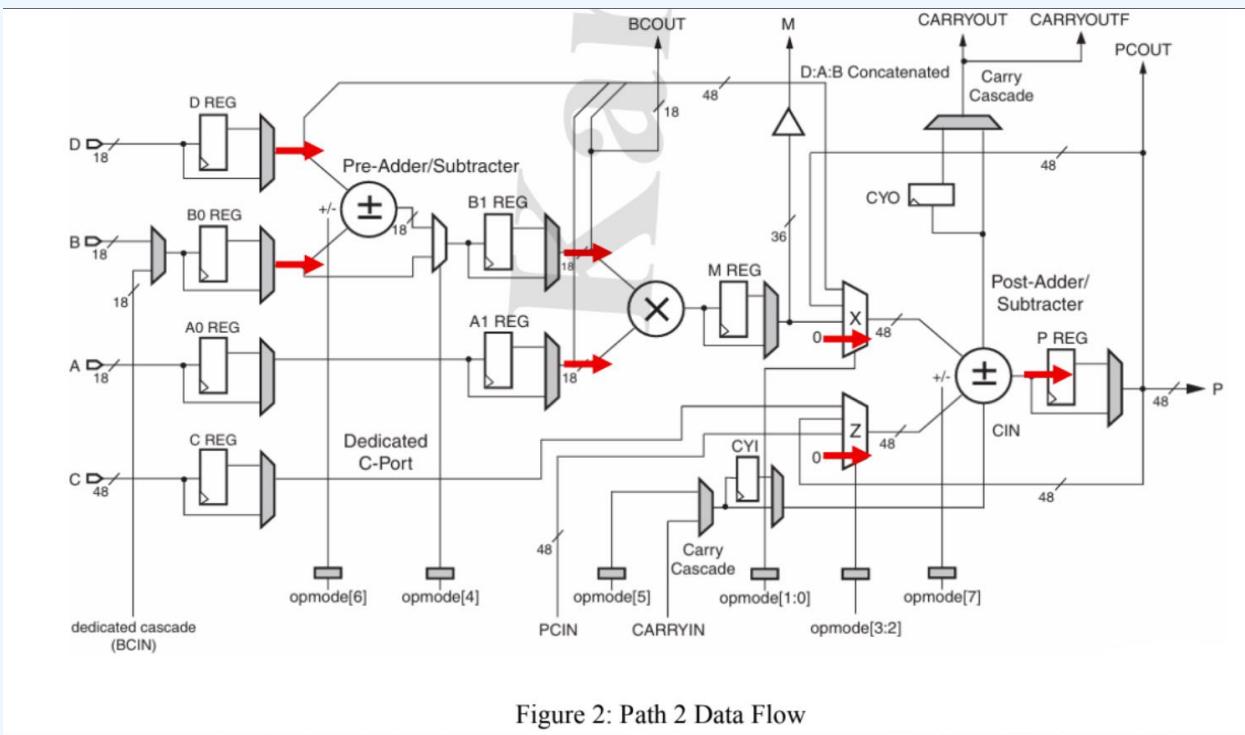
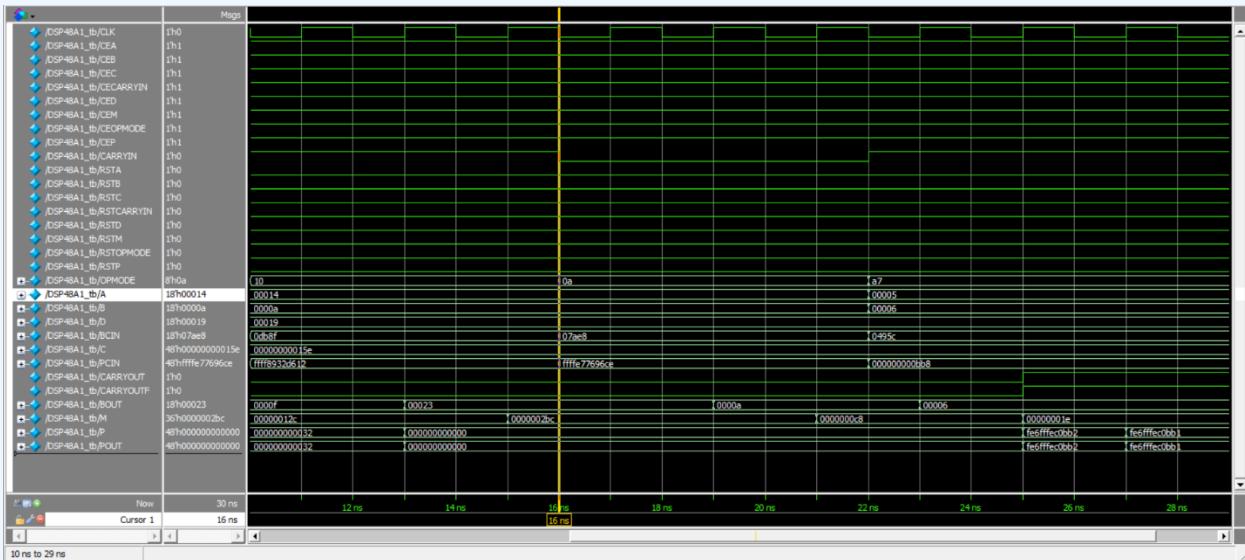
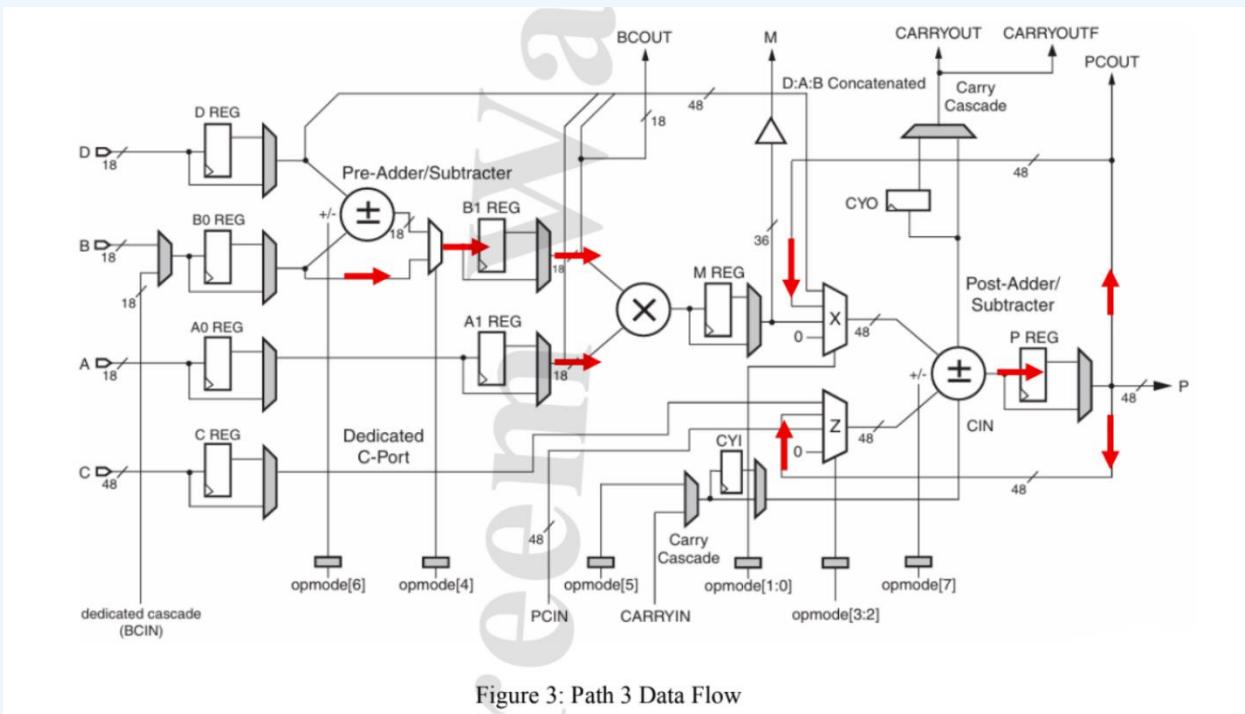
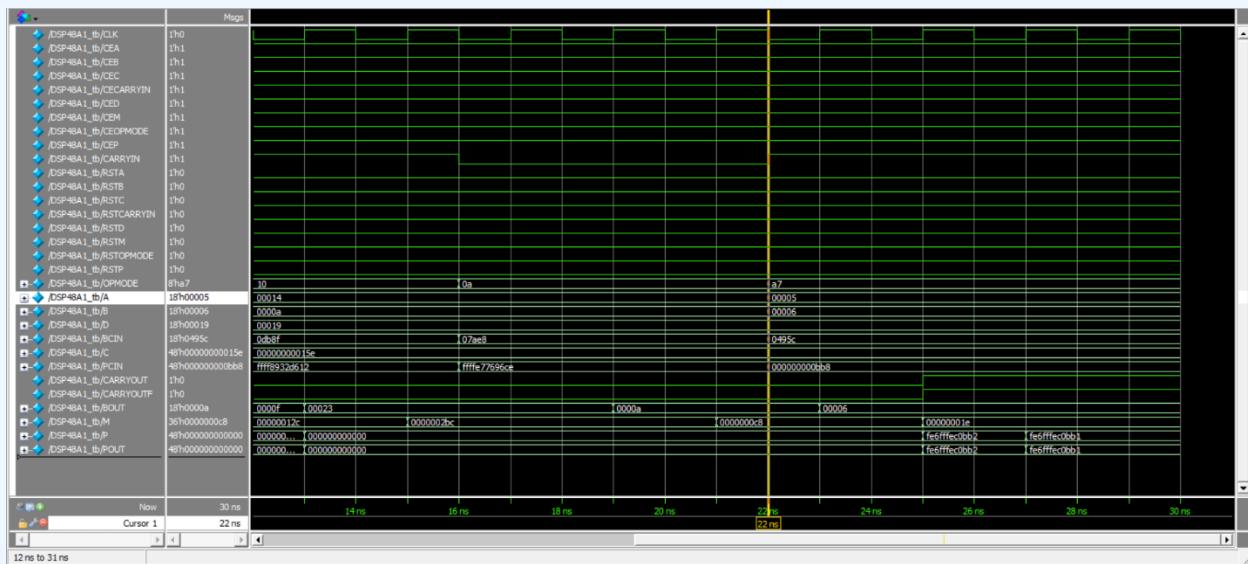


Figure 2: Path 2 Data Flow

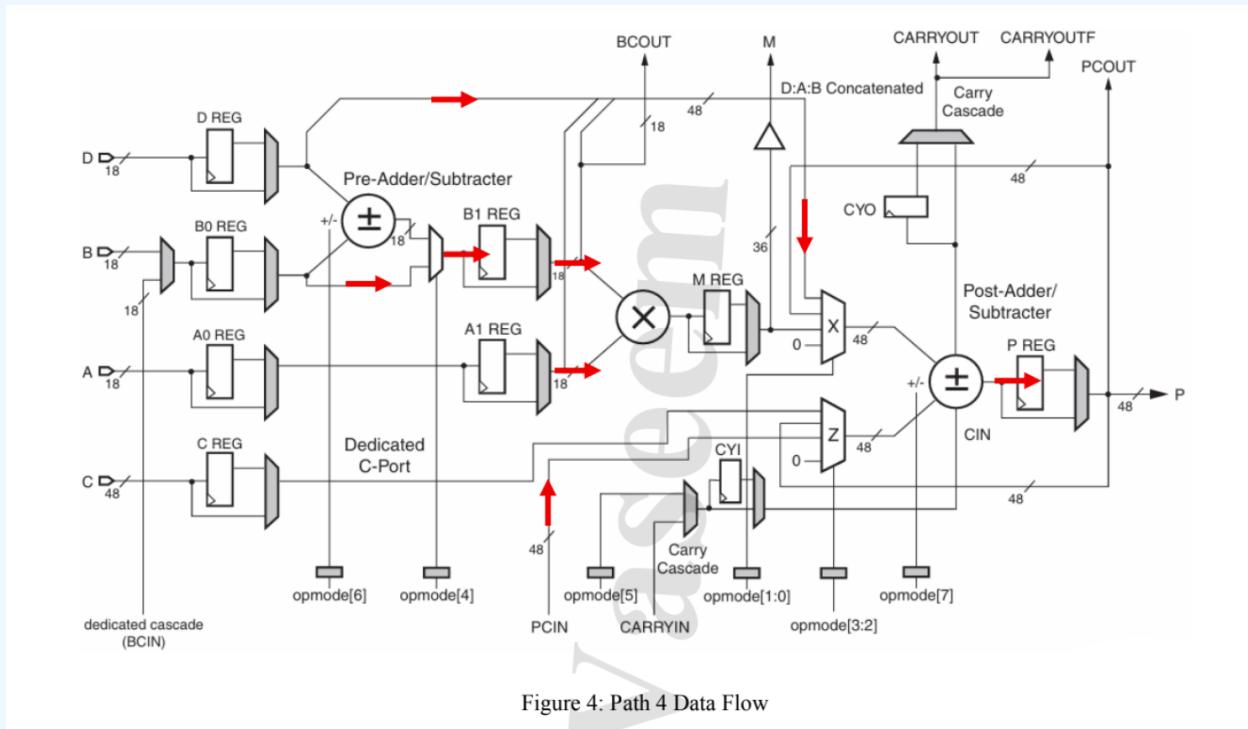


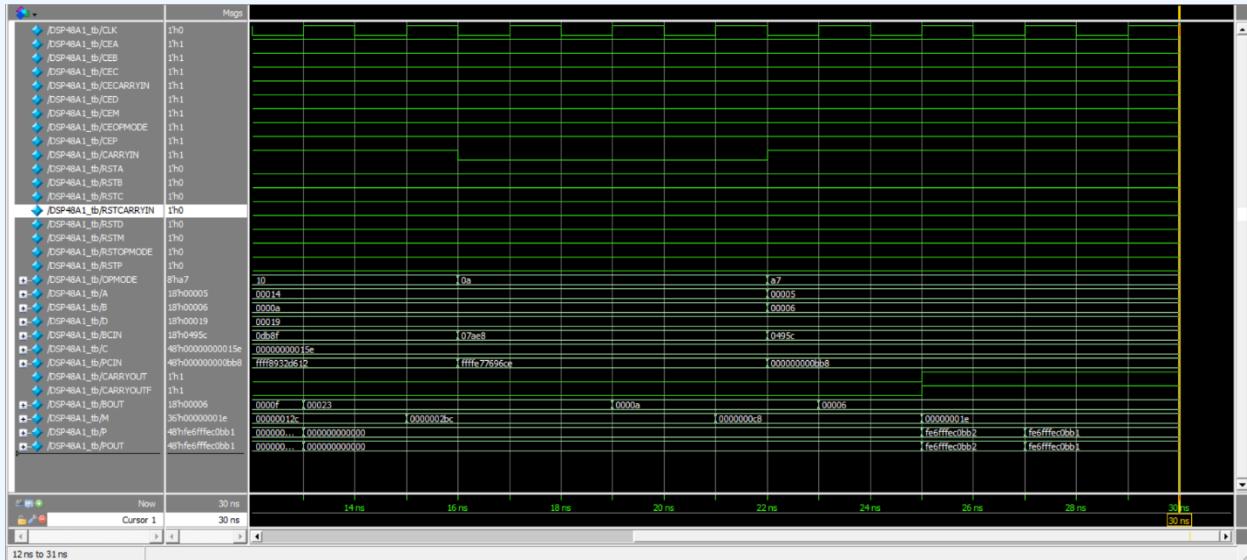
- Path 3





● Path 4





CONSTRAINT FILE

```
D: > Spartan6-DSP48A1 > constraints > Constraints_basys3.xdc
1  # This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVC MOS33 } [get_ports CLK]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
9
10
11 ## Switches
12 # set_property -dict {PACKAGE_PIN V17 IOSTANDARD LVC MOS33} [get_ports {opcode[0]}]
13 # set_property -dict {PACKAGE_PIN V16 IOSTANDARD LVC MOS33} [get_ports {opcode[1]}]
14 # set_property -dict {PACKAGE_PIN W16 IOSTANDARD LVC MOS33} [get_ports {opcode[2]}]
15 # set_property -dict {PACKAGE_PIN W17 IOSTANDARD LVC MOS33} [get_ports {A[0]}]
16 # set_property -dict {PACKAGE_PIN W15 IOSTANDARD LVC MOS33} [get_ports {A[1]}]
17 # set_property -dict {PACKAGE_PIN V15 IOSTANDARD LVC MOS33} [get_ports {A[2]}]
18 # set_property -dict {PACKAGE_PIN W14 IOSTANDARD LVC MOS33} [get_ports {B[0]}]
19 # set_property -dict {PACKAGE_PIN W13 IOSTANDARD LVC MOS33} [get_ports {B[1]}]
20 # set_property -dict {PACKAGE_PIN V2 IOSTANDARD LVC MOS33} [get_ports {B[2]}]
21 # set_property -dict {PACKAGE_PIN T3 IOSTANDARD LVC MOS33} [get_ports cin]
22 # set_property -dict {PACKAGE_PIN T2 IOSTANDARD LVC MOS33} [get_ports red_op_A]
23 # set_property -dict {PACKAGE_PIN R3 IOSTANDARD LVC MOS33} [get_ports red_op_B]
24 # set_property -dict {PACKAGE_PIN W2 IOSTANDARD LVC MOS33} [get_ports bypass_A]
25 # set_property -dict {PACKAGE_PIN U1 IOSTANDARD LVC MOS33} [get_ports bypass_B]
26 # set_property -dict {PACKAGE_PIN T1 IOSTANDARD LVC MOS33} [get_ports direction]
27 # set_property -dict {PACKAGE_PIN R2 IOSTANDARD LVC MOS33} [get_ports serial_in]
28
29
30 ## LEDs
31 # set_property -dict {PACKAGE_PIN U16 IOSTANDARD LVC MOS33} [get_ports {leds[0]}]
32 # set_property -dict {PACKAGE_PIN E19 IOSTANDARD LVC MOS33} [get_ports {leds[1]}]
33 # set_property -dict {PACKAGE_PIN U19 IOSTANDARD LVC MOS33} [get_ports {leds[2]}]
34 # set_property -dict {PACKAGE_PIN V19 IOSTANDARD LVC MOS33} [get_ports {leds[3]}]
35 # set_property -dict {PACKAGE_PIN W18 IOSTANDARD LVC MOS33} [get_ports {leds[4]}]
36 # set_property -dict {PACKAGE_PIN U15 IOSTANDARD LVC MOS33} [get_ports {leds[5]}]
37 # set_property -dict {PACKAGE_PIN U14 IOSTANDARD LVC MOS33} [get_ports {leds[6]}]
38 # set_property -dict {PACKAGE_PIN V14 IOSTANDARD LVC MOS33} [get_ports {leds[7]}]
```

```

D:> Spartan6-DSP48A1 > constraints > Constraints_basys3.xdc
39 # set_property -dict {PACKAGE_PIN V13 IOSTANDARD LVC MOS33} [get_ports {leds[8]}]
40 # set_property -dict {PACKAGE_PIN V3 IOSTANDARD LVC MOS33} [get_ports {leds[9]}]
41 # set_property -dict {PACKAGE_PIN W3 IOSTANDARD LVC MOS33} [get_ports {leds[10]}]
42 # set_property -dict {PACKAGE_PIN U3 IOSTANDARD LVC MOS33} [get_ports {leds[11]}]
43 # set_property -dict {PACKAGE_PIN P3 IOSTANDARD LVC MOS33} [get_ports {leds[12]}]
44 # set_property -dict {PACKAGE_PIN N3 IOSTANDARD LVC MOS33} [get_ports {leds[13]}]
45 # set_property -dict {PACKAGE_PIN P1 IOSTANDARD LVC MOS33} [get_ports {leds[14]}]
46 # set_property -dict {PACKAGE_PIN L1 IOSTANDARD LVC MOS33} [get_ports {leds[15]}]
47
48 ###7 Segment Display
49 #set_property -dict { PACKAGE_PIN W7 IOSTANDARD LVC MOS33 } [get_ports {seg[0]}]
50 #set_property -dict { PACKAGE_PIN W6 IOSTANDARD LVC MOS33 } [get_ports {seg[1]}]
51 #set_property -dict { PACKAGE_PIN U8 IOSTANDARD LVC MOS33 } [get_ports {seg[2]}]
52 #set_property -dict { PACKAGE_PIN V8 IOSTANDARD LVC MOS33 } [get_ports {seg[3]}]
53 #set_property -dict { PACKAGE_PIN U5 IOSTANDARD LVC MOS33 } [get_ports {seg[4]}]
54 #set_property -dict { PACKAGE_PIN V5 IOSTANDARD LVC MOS33 } [get_ports {seg[5]}]
55 #set_property -dict { PACKAGE_PIN U7 IOSTANDARD LVC MOS33 } [get_ports {seg[6]}]
56
57 #set_property -dict { PACKAGE_PIN V7 IOSTANDARD LVC MOS33 } [get_ports dp]
58
59 #set_property -dict { PACKAGE_PIN U2 IOSTANDARD LVC MOS33 } [get_ports {an[0]}]
60 #set_property -dict { PACKAGE_PIN U4 IOSTANDARD LVC MOS33 } [get_ports {an[1]}]
61 #set_property -dict { PACKAGE_PIN V4 IOSTANDARD LVC MOS33 } [get_ports {an[2]}]
62 #set_property -dict { PACKAGE_PIN W4 IOSTANDARD LVC MOS33 } [get_ports {an[3]}]
63
64
65 ##Buttons
66 # set_property -dict { PACKAGE_PIN U18 IOSTANDARD LVC MOS33 } [get_ports rst]
67 #set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVC MOS33 } [get_ports btnU]
68 #set_property -dict { PACKAGE_PIN W19 IOSTANDARD LVC MOS33 } [get_ports btnL]
69 #set_property -dict { PACKAGE_PIN T17 IOSTANDARD LVC MOS33 } [get_ports btnR]
70 #set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVC MOS33 } [get_ports btnD]
71
72
73 ##Pmod Header JA
74 #set_property -dict { PACKAGE_PIN J1 IOSTANDARD LVC MOS33 } [get_ports {JA[0]}];#Sch name = JA1
75 #set_property -dict { PACKAGE_PIN L2 IOSTANDARD LVC MOS33 } [get_ports {JA[1]}];#Sch name = JA2
76 #set_property -dict { PACKAGE_PIN J2 IOSTANDARD LVC MOS33 } [get_ports {JA[2]}];#Sch name = JA3

```

```

D:> Spartan6-DSP48A1 > constraints > Constraints_basys3.xdc
77 #set_property -dict { PACKAGE_PIN G2 IOSTANDARD LVC MOS33 } [get_ports {JA[3]}];#Sch name = JA4
78 #set_property -dict { PACKAGE_PIN H1 IOSTANDARD LVC MOS33 } [get_ports {JA[4]}];#Sch name = JA7
79 #set_property -dict { PACKAGE_PIN K2 IOSTANDARD LVC MOS33 } [get_ports {JA[5]}];#Sch name = JA8
80 #set_property -dict { PACKAGE_PIN H2 IOSTANDARD LVC MOS33 } [get_ports {JA[6]}];#Sch name = JA9
81 #set_property -dict { PACKAGE_PIN G3 IOSTANDARD LVC MOS33 } [get_ports {JA[7]}];#Sch name = JA10
82
83 ##Pmod Header JB
84 #set_property -dict { PACKAGE_PIN A14 IOSTANDARD LVC MOS33 } [get_ports {JB[0]}];#Sch name = JB1
85 #set_property -dict { PACKAGE_PIN A16 IOSTANDARD LVC MOS33 } [get_ports {JB[1]}];#Sch name = JB2
86 #set_property -dict { PACKAGE_PIN B15 IOSTANDARD LVC MOS33 } [get_ports {JB[2]}];#Sch name = JB3
87 #set_property -dict { PACKAGE_PIN B16 IOSTANDARD LVC MOS33 } [get_ports {JB[3]}];#Sch name = JB4
88 #set_property -dict { PACKAGE_PIN A15 IOSTANDARD LVC MOS33 } [get_ports {JB[4]}];#Sch name = JB7
89 #set_property -dict { PACKAGE_PIN A17 IOSTANDARD LVC MOS33 } [get_ports {JB[5]}];#Sch name = JB8
90 #set_property -dict { PACKAGE_PIN C15 IOSTANDARD LVC MOS33 } [get_ports {JB[6]}];#Sch name = JB9
91 #set_property -dict { PACKAGE_PIN C16 IOSTANDARD LVC MOS33 } [get_ports {JB[7]}];#Sch name = JB10
92
93 ##Pmod Header JC
94 #set_property -dict { PACKAGE_PIN K17 IOSTANDARD LVC MOS33 } [get_ports {JC[0]}];#Sch name = JC1
95 #set_property -dict { PACKAGE_PIN M18 IOSTANDARD LVC MOS33 } [get_ports {JC[1]}];#Sch name = JC2
96 #set_property -dict { PACKAGE_PIN N17 IOSTANDARD LVC MOS33 } [get_ports {JC[2]}];#Sch name = JC3
97 #set_property -dict { PACKAGE_PIN P18 IOSTANDARD LVC MOS33 } [get_ports {JC[3]}];#Sch name = JC4
98 #set_property -dict { PACKAGE_PIN L17 IOSTANDARD LVC MOS33 } [get_ports {JC[4]}];#Sch name = JC7
99 #set_property -dict { PACKAGE_PIN M19 IOSTANDARD LVC MOS33 } [get_ports {JC[5]}];#Sch name = JC8
100 #set_property -dict { PACKAGE_PIN P17 IOSTANDARD LVC MOS33 } [get_ports {JC[6]}];#Sch name = JC9
101 #set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVC MOS33 } [get_ports {JC[7]}];#Sch name = JC10
102
103 ##Pmod Header JXADC
104 #set_property -dict { PACKAGE_PIN J3 IOSTANDARD LVC MOS33 } [get_ports {JXADC[0]}];#Sch name = XA1_P
105 #set_property -dict { PACKAGE_PIN L3 IOSTANDARD LVC MOS33 } [get_ports {JXADC[1]}];#Sch name = XA2_P
106 #set_property -dict { PACKAGE_PIN M2 IOSTANDARD LVC MOS33 } [get_ports {JXADC[2]}];#Sch name = XA3_P
107 #set_property -dict { PACKAGE_PIN N2 IOSTANDARD LVC MOS33 } [get_ports {JXADC[3]}];#Sch name = XA4_P
108 #set_property -dict { PACKAGE_PIN K3 IOSTANDARD LVC MOS33 } [get_ports {JXADC[4]}];#Sch name = XA1_N
109 #set_property -dict { PACKAGE_PIN M3 IOSTANDARD LVC MOS33 } [get_ports {JXADC[5]}];#Sch name = XA2_N
110 #set_property -dict { PACKAGE_PIN M1 IOSTANDARD LVC MOS33 } [get_ports {JXADC[6]}];#Sch name = XA3_N
111 #set_property -dict { PACKAGE_PIN N1 IOSTANDARD LVC MOS33 } [get_ports {JXADC[7]}];#Sch name = XA4_N
112

```

```

114 ##VGA Connector
115 #set_property -dict { PACKAGE_PIN G19 IOSTANDARD LVCMS33 } [get_ports {vgaRed[0]}]
116 #set_property -dict { PACKAGE_PIN H19 IOSTANDARD LVCMS33 } [get_ports {vgaRed[1]}]
117 #set_property -dict { PACKAGE_PIN J19 IOSTANDARD LVCMS33 } [get_ports {vgaRed[2]}]
118 #set_property -dict { PACKAGE_PIN N19 IOSTANDARD LVCMS33 } [get_ports {vgaRed[3]}]
119 #set_property -dict { PACKAGE_PIN N18 IOSTANDARD LVCMS33 } [get_ports {vgaBlue[0]}]
120 #set_property -dict { PACKAGE_PIN L18 IOSTANDARD LVCMS33 } [get_ports {vgaBlue[1]}]
121 #set_property -dict { PACKAGE_PIN K18 IOSTANDARD LVCMS33 } [get_ports {vgaBlue[2]}]
122 #set_property -dict { PACKAGE_PIN J18 IOSTANDARD LVCMS33 } [get_ports {vgaBlue[3]}]
123 #set_property -dict { PACKAGE_PIN J17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[0]}]
124 #set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[1]}]
125 #set_property -dict { PACKAGE_PIN G17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[2]}]
126 #set_property -dict { PACKAGE_PIN D17 IOSTANDARD LVCMS33 } [get_ports {vgaGreen[3]}]
127 #set_property -dict { PACKAGE_PIN P19 IOSTANDARD LVCMS33 } [get_ports Hsync]
128 #set_property -dict { PACKAGE_PIN R19 IOSTANDARD LVCMS33 } [get_ports Vsync]
129
130
131 ##USB-RS232 Interface
132 #set_property -dict { PACKAGE_PIN B18 IOSTANDARD LVCMS33 } [get_ports RsRX]
133 #set_property -dict { PACKAGE_PIN A18 IOSTANDARD LVCMS33 } [get_ports RSTX]
134
135
136 ##USB HID (PS/2)
137 #set_property -dict { PACKAGE_PIN C17 IOSTANDARD LVCMS33 PULLUP true } [get_ports PS2Clk]
138 #set_property -dict { PACKAGE_PIN B17 IOSTANDARD LVCMS33 PULLUP true } [get_ports PS2Data]
139
140
141 ##Quad SPI Flash
142 ##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
143 ##STARTUP2 primitive.
144 #set_property -dict { PACKAGE_PIN D18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[0]}]
145 #set_property -dict { PACKAGE_PIN D19 IOSTANDARD LVCMS33 } [get_ports {QspiDB[1]}]
146 #set_property -dict { PACKAGE_PIN G18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[2]}]
147 #set_property -dict { PACKAGE_PIN F18 IOSTANDARD LVCMS33 } [get_ports {QspiDB[3]}]
148 #set_property -dict { PACKAGE_PIN K19 IOSTANDARD LVCMS33 } [get_ports QspiCSn]
149

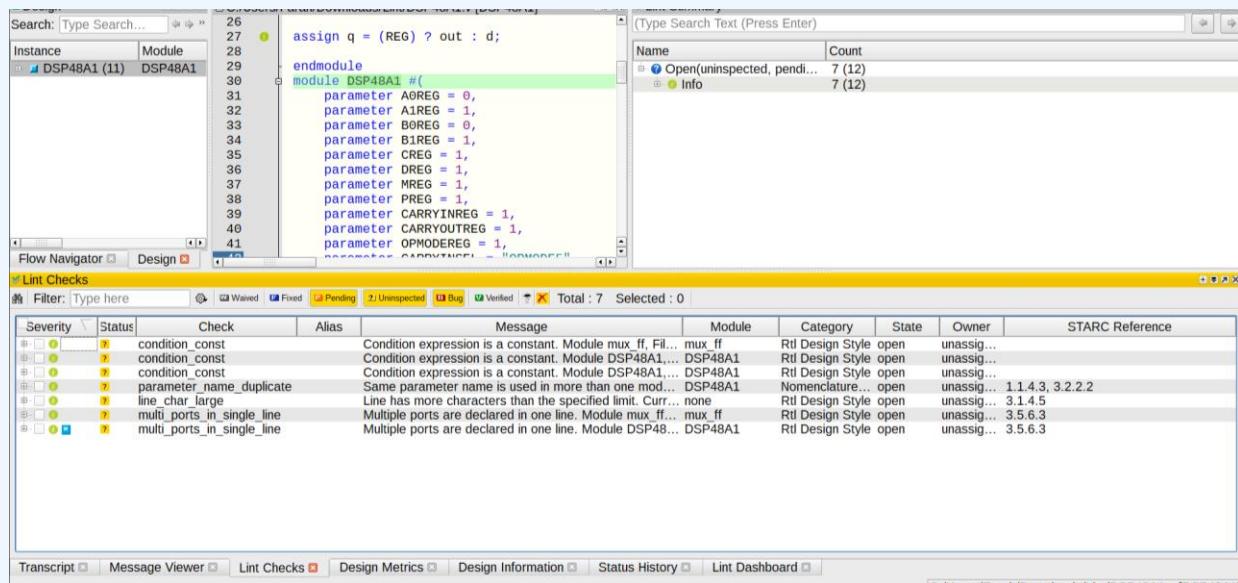
```

```

150
151 ## Configuration options, can be used for all designs
152 set_property CONFIG_VOLTAGE 3.3 [current_design]
153 set_property CFGBVS VCCO [current_design]
154
155 ## SPI configuration mode options for QSPI boot, can be used for all designs
156 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
157 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
158 set_property CONFIG_MODE SPIx4 [current_design]

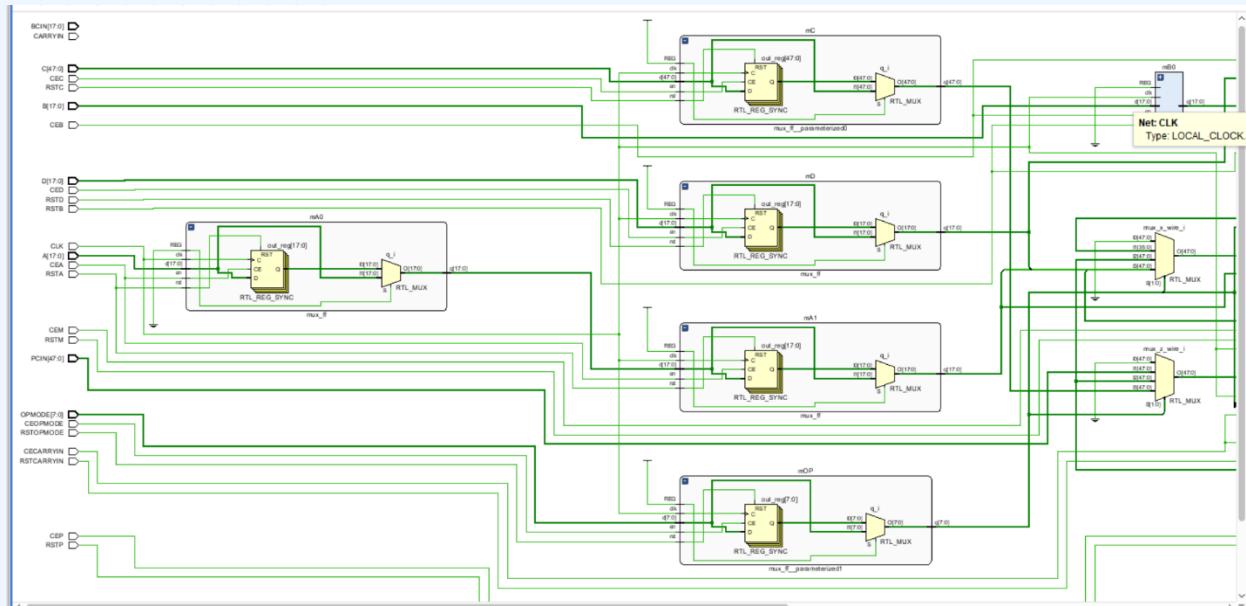
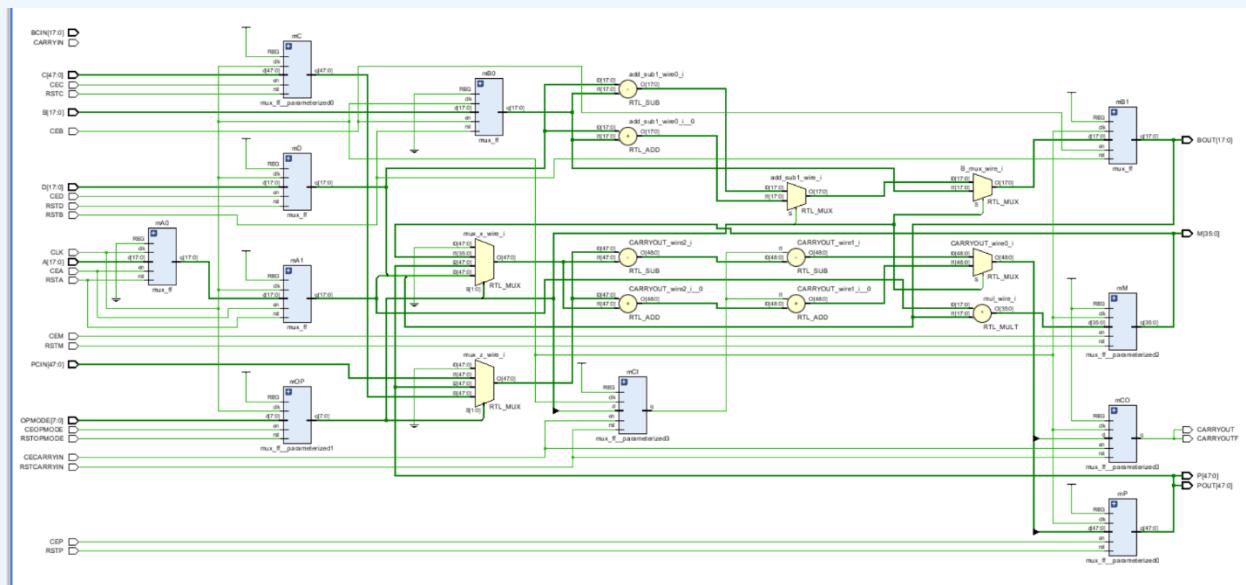
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LINTING

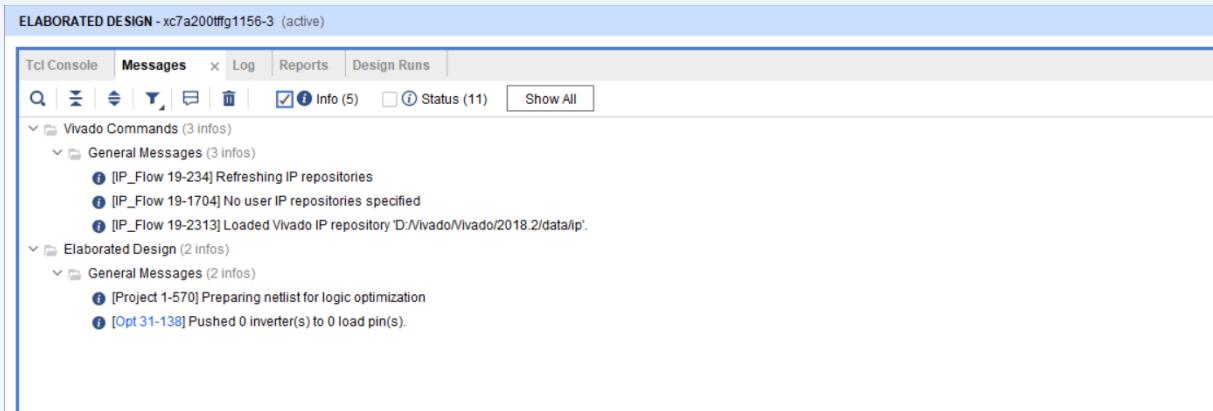


ELABORATION

SCHEMATIC

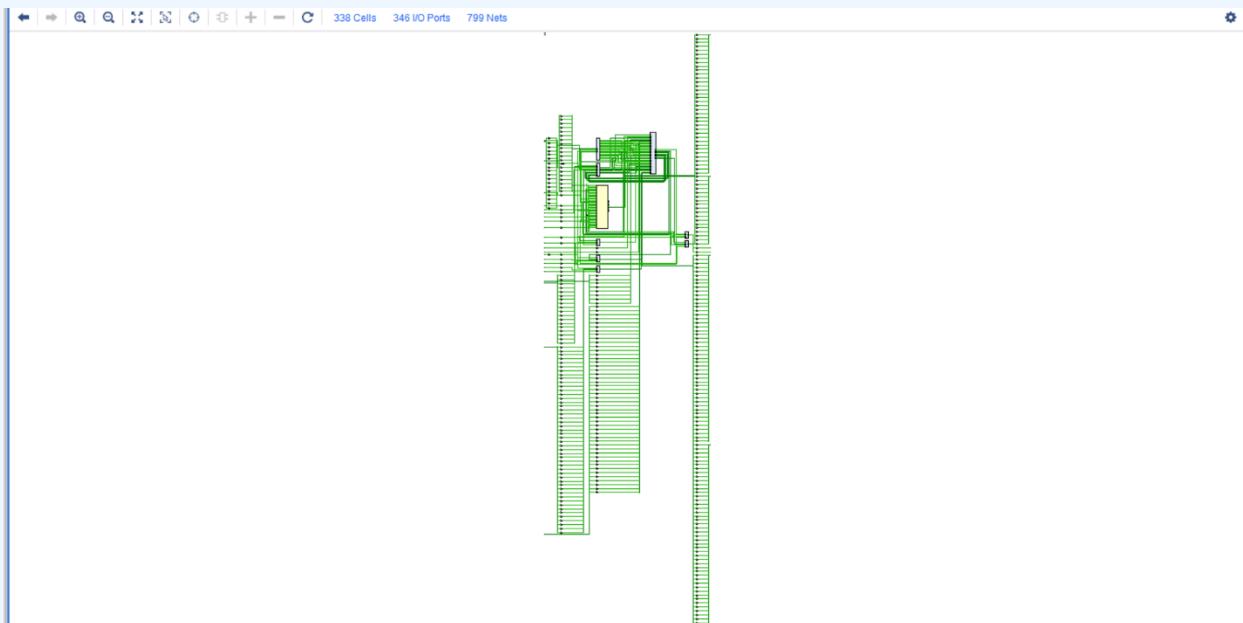


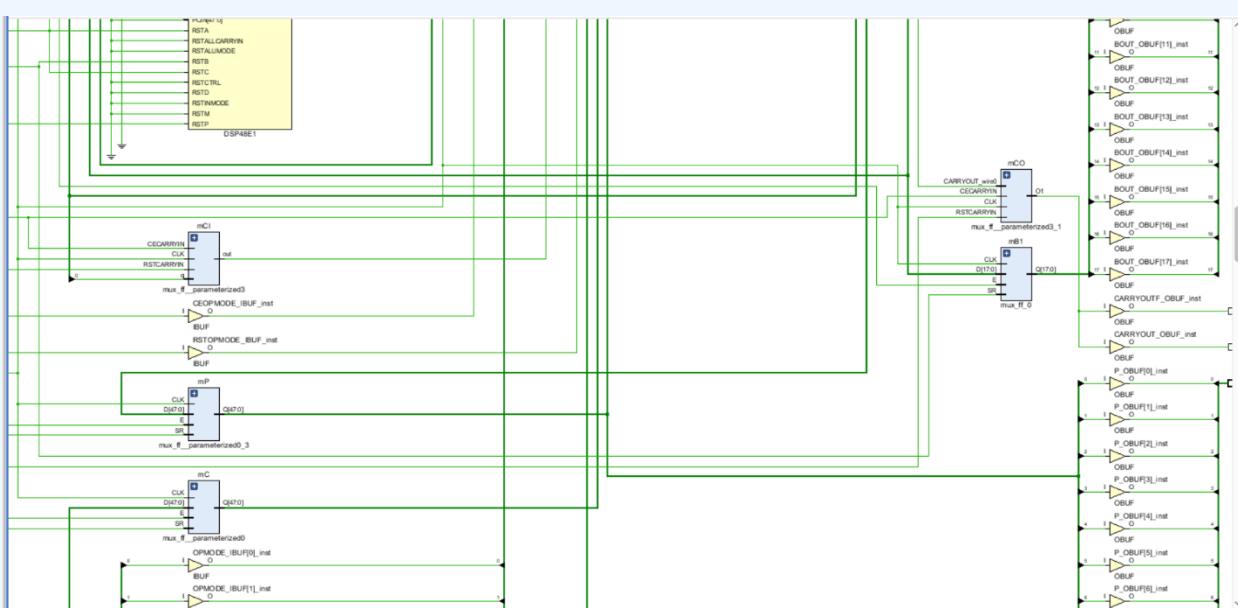
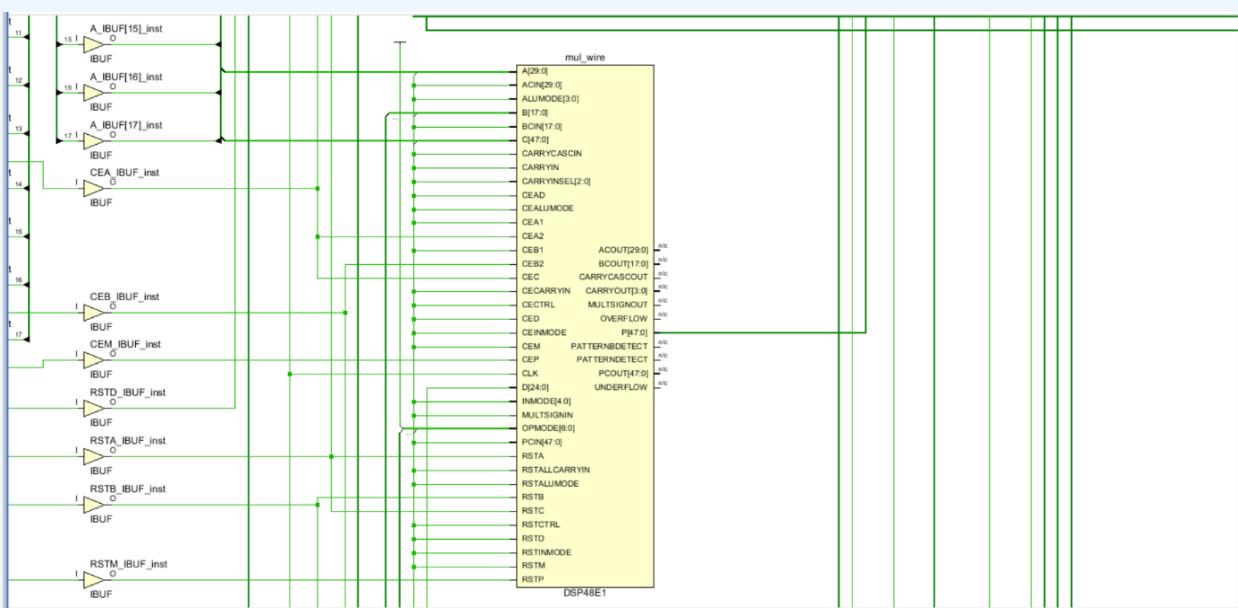
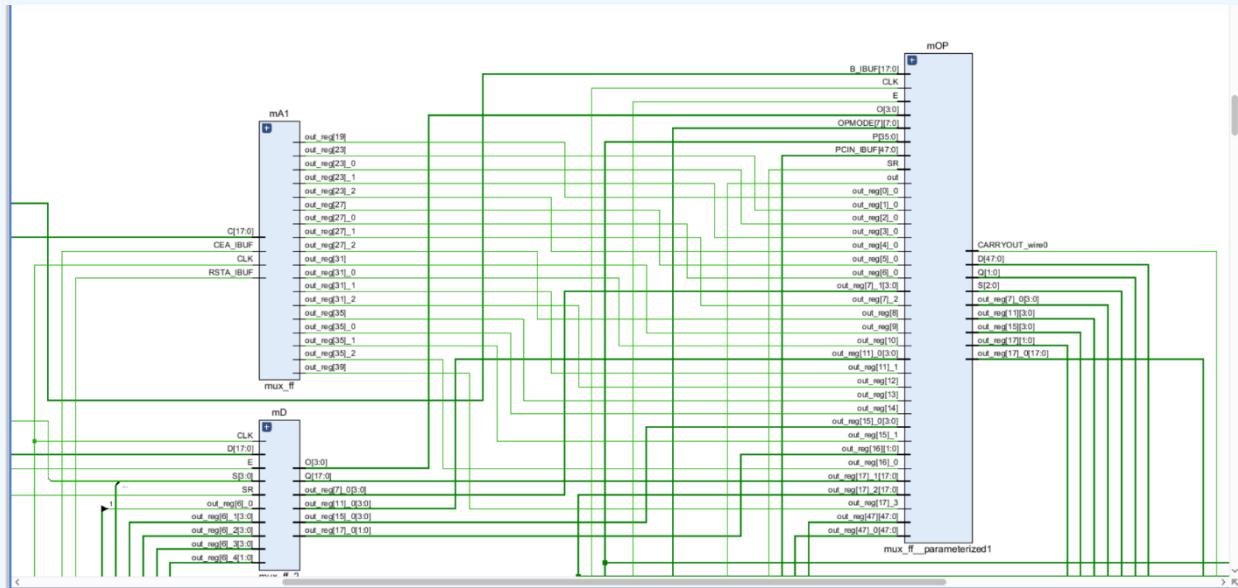
MESSAGES



SYNTHESIS

SCHEMATIC





MESSAGES

SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Debug

Q | X | D | T | M | B | Warning (58) Info (59) Status (28) Show All

▼ Synthesis (58 warnings)

- ⌚ [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:30]
- >⌚ [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (37 more like this)
- >⌚ [Synth 8-3332] Sequential element (mB0/out_reg[17]) is unused and will be removed from module DSP48A1. (17 more like this)
- ⌚ [Constraints 18-5210] No constraint will be written out.

TIMING REPORT

Tcl Console Messages Log Reports Design Runs Timing Debug

Q | X | D | C | B | General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (326)

> Intra-Clock Paths

 Inter-Clock Paths

 Other Path Groups

 User Ignored Paths

> Unconstrained Paths

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.963 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 162

All user specified timing constraints are met.

UTILIZATION REPORT

Tcl Console Messages Log Reports Design Runs Utilization Timing Debug

Q | X | D | % Hierarchy

Hierarchy

Summary

▼ Slice Logic

- ▼ Slice LUTs (<1%)
- LUT as Logic (<1%)
- ▼ Slice Registers (<1%)
- Register as Flip Flop (<1%)

Memory

▼ DSP

- ▼ DSPs (<1%)
- DSP48E1 only

▼ IO and GT Specific

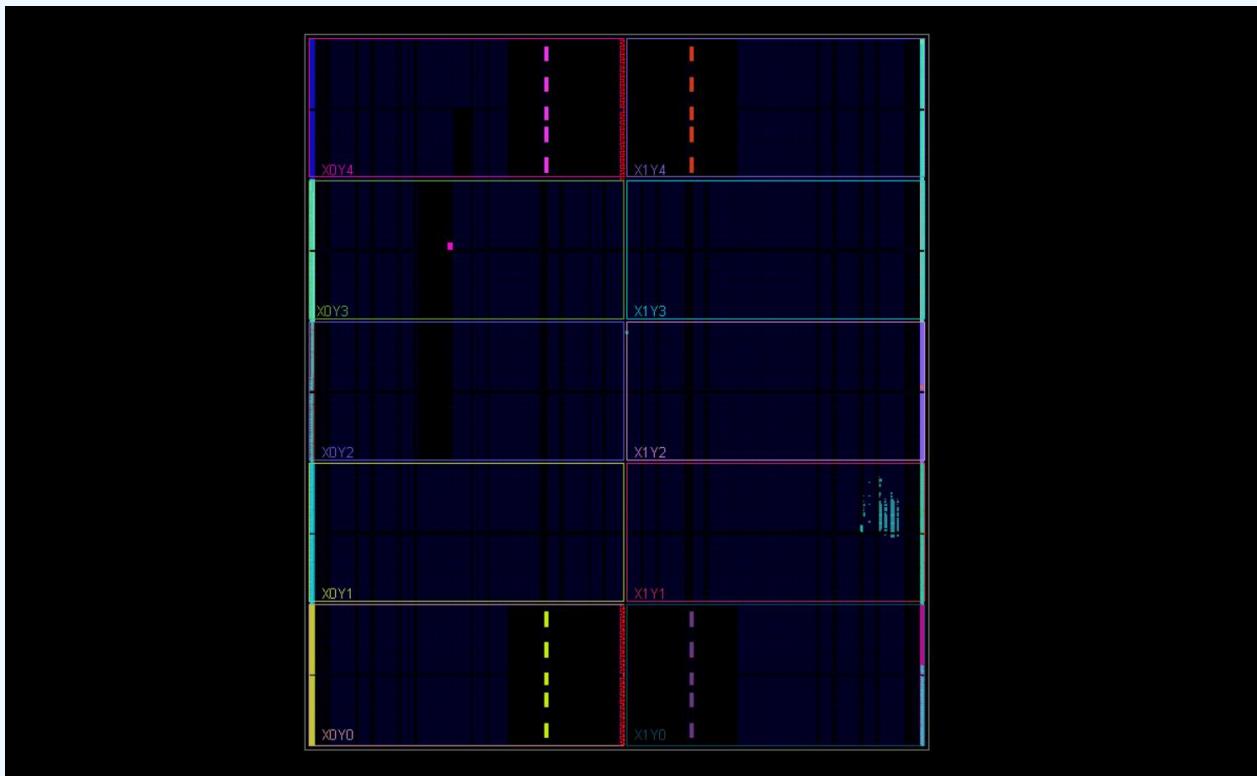
- ▼ Bonded IOB (65%)
- IOB Master Pads

▼ Clocking

Name	1	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
⌚ DSP48A1	275	160	1	327	1	0
⌚ mA1 (mux_ff)	0	18	0	0	0	0
⌚ mb1 (mux_ff_0)	0	18	0	0	0	0
⌚ mC (mux_ff_paramet...)	0	48	0	0	0	0
⌚ mCl (mux_ff_paramet...)	1	1	0	0	0	0
⌚ mCO (mux_ff_paramet...)	0	1	0	0	0	0
⌚ mD (mux_ff_2)	0	18	0	0	0	0
⌚ mOP (mux_ff_paramet...)	273	8	0	0	0	0
⌚ mP (mux_ff_paramet...)	0	48	0	0	0	0

IMPLEMENTATION

DEVICE



MESSAGES



TIMING REPORT

IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing

Design Timing Summary

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Setup Hold Pulse Width

Worst Negative Slack (WNS):	3.558 ns	Worst Hold Slack (WHS):	0.261 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	181

All user specified timing constraints are met.

UTILIZATION REPORT

IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	274	179	114	274	50	1	327	1
mA1 (mux_ff)	0	18	7	0	0	0	0	0
mB1 (mux_ff_0)	0	36	13	0	0	0	0	0
mC (mux_ff_paramet...)	0	48	11	0	0	0	0	0
mCl (mux_ff_paramet...)	1	1	1	1	1	0	0	0
mCO (mux_ff_paramet...)	0	2	2	0	0	0	0	0
mD (mux_ff_2)	0	18	9	0	0	0	0	0
mOP (mux_ff_paramet...)	273	8	86	273	0	0	0	0
mP (mux_ff_paramet...)	0	48	12	0	0	0	0	0