

The screenshot displays the Quartus Prime Lite Edition IDE interface during a compilation process. The title bar indicates the project path: `/home/parsa/intelFPGA_lite/Projects/SingleCycle/SingleCycle - SingleCycle`.

Project Navigator: Shows the project hierarchy with `SingleCycle` selected.

Entity/Instance: Lists the entity `Cyclone IV E: EP4CE115F29C7` and its associated components: `armarm`, `dmem2dmem`, and `inmem2dmem`.

Table of Contents: Displays the project structure, including `Flow Summary`, `Flow Settings`, `Flow Non-Default Global Settings`, `Flow Elapsed Time`, `Flow OS Summary`, `Flow Log`, `Analysis & Synthesis`, `Filter`, `Assembler`, `Timing Analyzer`, `EDA Netlist Writer`, `Flow Messages`, `Flow Suppressed Messages`, and `Timing Analyzer GUI`.

Flow Summary: Provides a detailed overview of the compilation process, including the status (Successful), date and time (Fri May 7 20:58:17 2021), Quartus Prime Version (20.1.1 Build 720 11/11/2020 SJ Lite Edition), Revision Name (SingleCycle), Top-level Entity Name (top), Family (Cyclone IV E), Device (EP4CE115F29C7), Timing Models (Final), Total logic elements (3,704 / 114,480 (3 %)), Total registers (2563), Total pins (67 / 529 (13 %)), Total virtual pins (0), Total memory bits (0 / 3,981,312 (0 %)), Embedded Multiplier 9-bit elements (0 / 532 (0 %)), and Total PLLs (0 / 4 (0 %)).

Tasks: Lists the compilation tasks, including `Compile Design`, `Generate Hardware`, `Place and Route Design`, `Assembler Generate programming file`, `Timing Analyzer`, `EDA Netlist Writer`, and `Edit Settings`.

Messages: Displays the compilation messages, including warnings and errors. The messages indicate that some warnings were suppressed due to user configuration and that the compilation was successful.

Timing Analyzer - /home/parisa/intelFPGA_lite/Projects/SingleCycle/SingleCycle

FileViewNetlistConstraintsReportsScriptToolsWindowHelp

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Set Operating Conditions

Slow 1200mV 85C Model

Slow 1200mV 0C Model

Fast 1200mV 0C Model

Command Info

Summary of Paths

	Delay	From Node	To Node
1	20.545	armarm[datapathdpdfflop:pcreg[q]2]	DataAddr[26]

Path #1: Delay is 20.545

Path Summary	Statistics	Data Path					
Total	Incr	RF	Type	Fanout	Location	Element	
1	20.545	20.545				data path	
1	0.000	0.000		1	FF_X55_Y38_N7	armarm[datapathdpdfflop:	
2	0.000	0.000	FF	CELL	49	FF_X55_Y38_N7	armdp[pcreg[q]2]q
3	0.513	0.513	FF	IC	1	LCCOMB_X55_Y38_N8	inmem[RAM-11]dataa
4	0.917	0.404	FF	CELL	3	LCCOMB_X55_Y38_N8	inmem[RAM-11]combout
5	1.347	0.430	FF	IC	1	LCCOMB_X54_Y38_N6	inmem[RAM-12]datac
6	1.628	0.281	FF	CELL	3	LCCOMB_X54_Y38_N6	inmem[RAM-12]combout
7	1.930	0.302	FF	IC	1	LCCOMB_X54_Y38_N30	armdp[ra2mux[y]1]-1]dat
8	2.334	0.404	FF	CELL	110	LCCOMB_X54_Y38_N30	armdp[ra2mux[y]1]-1]con
9	3.826	1.492	FF	IC	1	LCCOMB_X61_Y35_N18	armdp[rlfrf-663]dataa
10	4.238	0.412	FR	CELL	1	LCCOMB_X61_Y35_N18	armdp[rlfrf-663]combout
11	5.503	1.265	RR	IC	1	LCCOMB_X55_Y37_N12	armdp[rlfrf-664]datac
12	5.790	0.287	RR	CELL	1	LCCOMB_X55_Y37_N12	armdp[rlfrf-664]combout
13	6.532	0.742	RR	IC	1	LCCOMB_X56_Y34_N6	armdp[rlfrf-665]datac
14	6.819	0.287	RR	CELL	1	LCCOMB_X56_Y34_N6	armdp[rlfrf-665]combout
15	7.023	0.204	RR	IC	1	LCCOMB_X56_Y34_N14	armdp[rlfrf-668]datac
16	7.178	0.155	RR	CELL	1	LCCOMB_X56_Y34_N14	armdp[rlfrf-668]combout

Path #1: Delay is 20.545

Path Summary	Statistics	Data Path					
Total	Incr	RF	Type	Fanout	Location	Element	
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1	0.000	0.000		1	FF_X55_Y38_N7	armarm[datapathdpdfflop:	
2	0.000	0.000	FF	CELL	49	FF_X55_Y38_N7	armdp[pcreg[q]2]q
3	0.513	0.513	FF	IC	1	LCCOMB_X55_Y38_N8	inmem[RAM-11]dataa
4	0.917	0.404	FF	CELL	3	LCCOMB_X55_Y38_N8	inmem[RAM-11]combout
5	1.347	0.430	FF	IC	1	LCCOMB_X54_Y38_N6	inmem[RAM-12]datac
6	1.628	0.281	FF	CELL	3	LCCOMB_X54_Y38_N6	inmem[RAM-12]combout
7	1.930	0.302	FF	IC	1	LCCOMB_X54_Y38_N30	armdp[ra2mux[y]1]-1]dat
8	2.334	0.404	FF	CELL	110	LCCOMB_X54_Y38_N30	armdp[ra2mux[y]1]-1]con
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Report

Set Operating Conditions

Tasks

Custom Reports

Report Timing...

Report Timing Tree...

Report Minimum Pulse Wl

Report False Path...

Report Path...

Report Exceptions...

Report Bottlenecks...

Report Net Timing...

Report Skew...

Report Max Skew...

Report Net Delay...

Report Path...

Report Exceptions...

Report Bottlenecks...

Report Net Timing...

Report Skew...

Report Max Skew...

Report Net Delay...

Report Path...

Report Exceptions...

Report Bottlenecks...

Report Net Timing...

Report Skew...

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Report Net Delay...

Report Path...

Report Exceptions...

Report Bottlenecks...

Report Net Timing...

Report Skew...

Report Max Skew...

Report Net Delay...

Report Path...

Timing Analyzer - /home/parsa/intelFPGA_lite/Projects/SingleCycle/SingleCycle - SingleCycle

File View Netlist Constraints Reports Script Tools Window Help

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Set Operating Conditions

Slow 1200mV 85C Model

Slow 1200mV OC Model

Fast 1200mV OC Model

Command Info Summary of Paths

Delay	From Node	To Node
20.545	armarmjdatapathdpjflopprcreg[q[2]	DataAdr[26]

Path #1: Delay is 20.545

Path Summary	Statistics	Data Path
Property	Value	
1 From Node	armarmjdatapathdpjflopprcreg[q[2]	
2 To Node	DataAdr[26]	
3 Delay	20.545	

Report Set Operating Conditions

Tasks

- Custom Reports
 - Report Timing...
 - Report Timing Tree...
 - Report Minimum Pulse Wi
 - Report False Path...
 - Report Paths...
 - Report Exceptions...
 - Report Bottlenecks...
 - Report Net Timing...
 - Report Skew...
 - Report Max Skew...
 - Report Net Delay...

Path #1: Delay is 20.545

Path Summary	Statistics	Data Path
Total	Incr	RF Type Fanout Location Element
1 20.545	20.545	
1 0.000	0.000	
2 0.000	0.000	FF CELL 49 FF_X55_Y38_N7 armarmjdatapathdpjflopprc
3 0.513	0.513	FF IC 1 LCCOMB_X55_Y38_N8 armjdpjpcreg[q[2]]q
4 0.917	0.404	FF CELL 3 LCCOMB_X55_Y38_N8 inemj(RAM-11)combout
5 1.347	0.430	FF IC 1 LCCOMB_X54_Y38_N6 inemj(RAM-12)dat
6 1.628	0.281	FF CELL 3 LCCOMB_X54_Y38_N6 inemj(RAM-12)combout
7 1.930	0.302	FF IC 1 LCCOMB_X54_Y38_N30 armjdpjra2muxj(1)-1dat
8 2.334	0.404	FF CELL 110 LCCOMB_X54_Y38_N30 armjdpjra2muxj(1)-1con
9 3.826	1.492	FF IC 1 LCCOMB_X61_Y35_N18 armjdpjrfjrf-663]dataa
10 4.238	0.412	FR CELL 1 LCCOMB_X61_Y35_N18 armjdpjrfjrf-663]combout
11 5.503	1.265	RR IC 1 LCCOMB_X55_Y37_N12 armjdpjrfjrf-664]dataa
12 5.790	0.287	RR CELL 1 LCCOMB_X55_Y37_N12 armjdpjrfjrf-664]combout
13 6.532	0.742	RR IC 1 LCCOMB_X56_Y34_N6 armjdpjrfjrf-665]dataa
14 6.819	0.287	RR CELL 1 LCCOMB_X56_Y34_N6 armjdpjrfjrf-665]combout
15 7.023	0.204	RR IC 1 LCCOMB_X56_Y34_N14 armjdpjrfjrf-668]dataa
16 7.178	0.155	RR CELL 1 LCCOMB_X56_Y34_N14 armjdpjrfjrf-668]combout

report_path -npaths 1 -panel_name {Report Path} -multi_corner

1 20.545

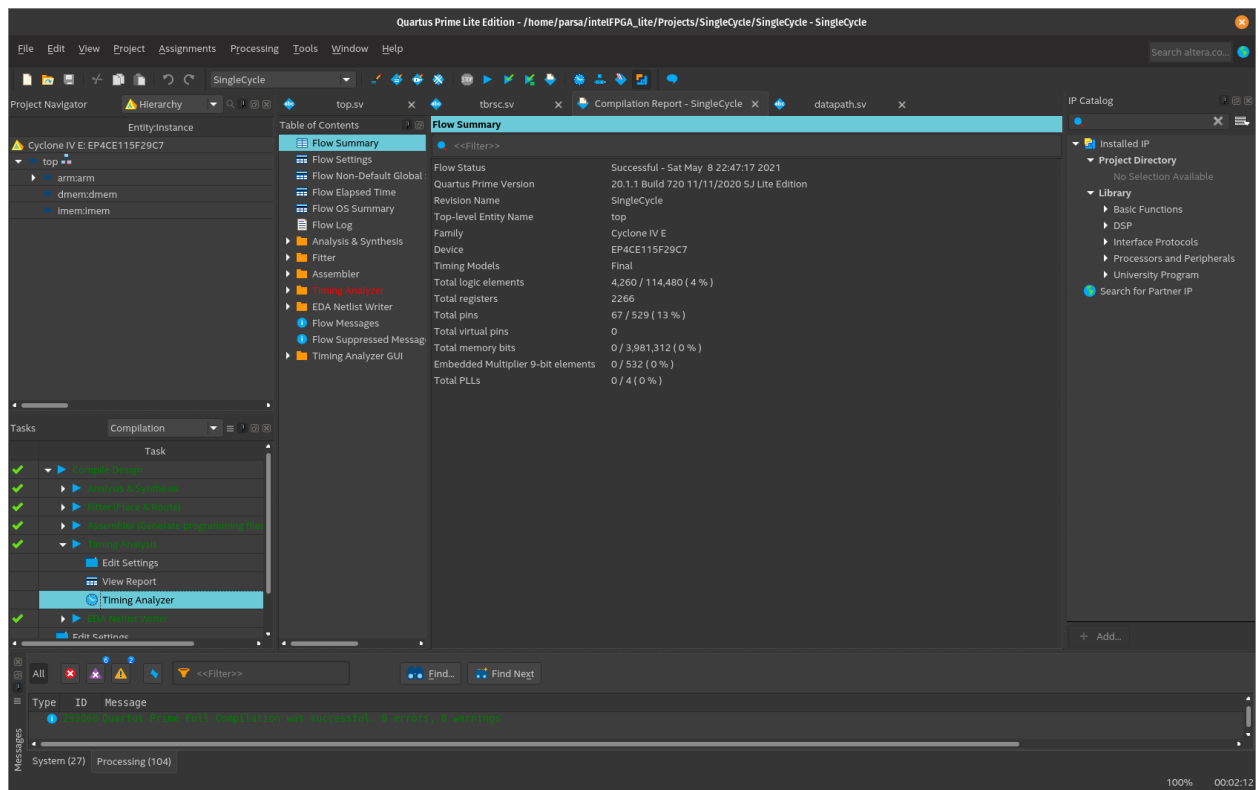
10

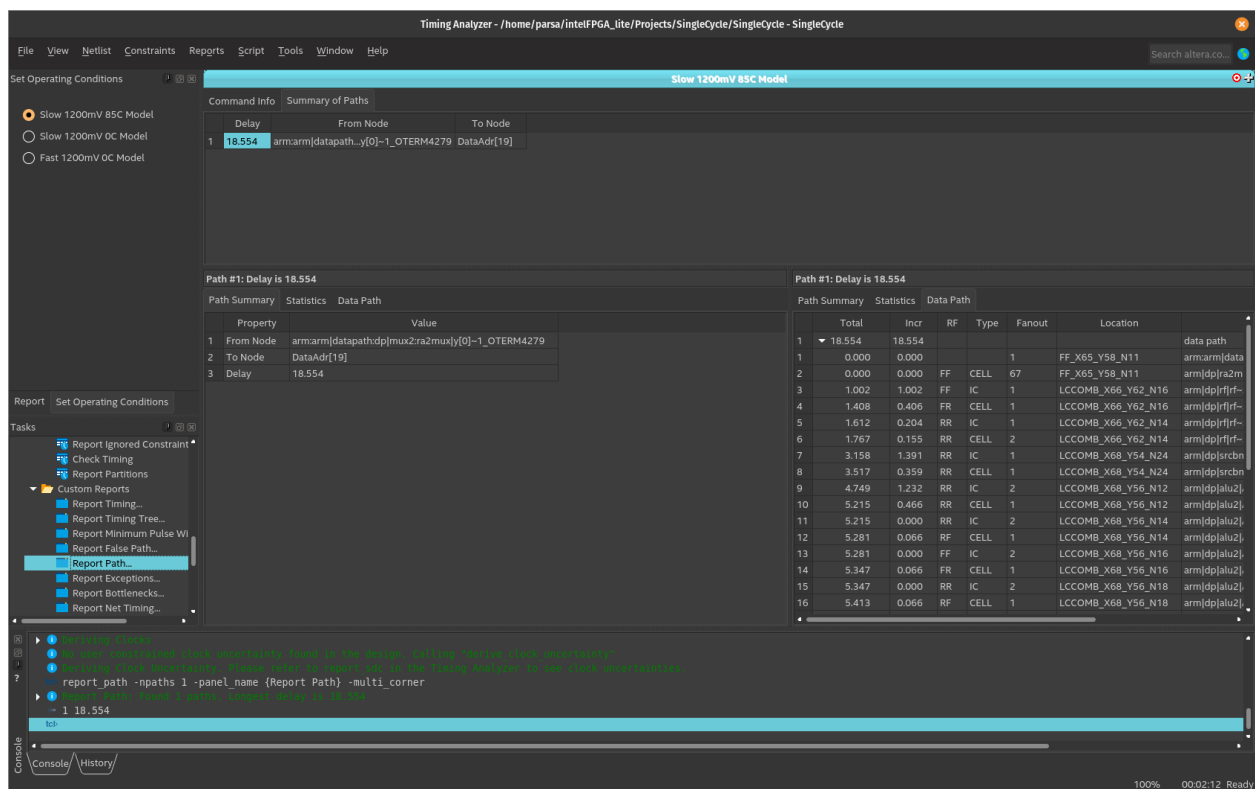
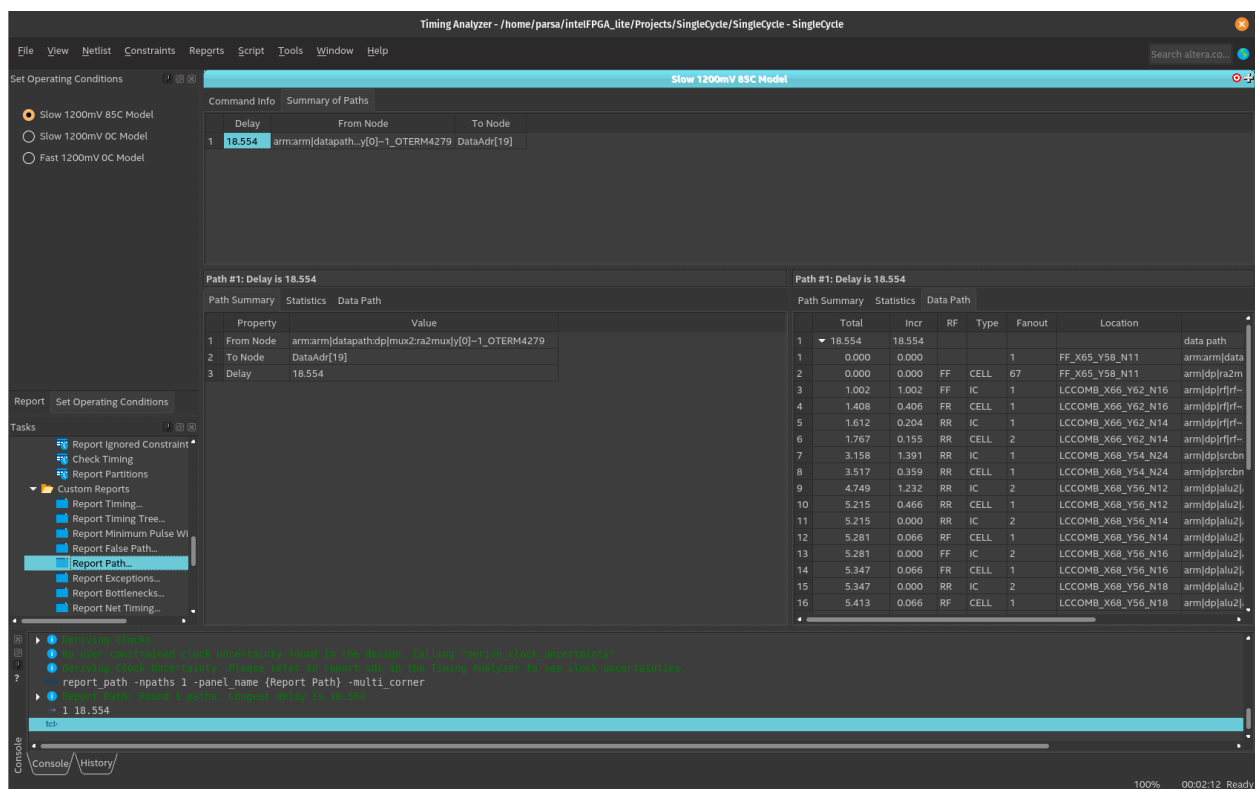
Console History

0% 00:00:00 Ready

این مسیر واقعی نیست است زیرا به regfile نرسیده و در نتیجه بیانگر مسیر بحرانی است.

۱. ب)





تعداد Logic Element ها از ۳۷۰۴ به ۴۲۶۰ رسیده که یعنی مساحت افزایش یافته. و تاخیر مسیر بحرانی از ۲۰.۵ به ۱۸.۵ رسیده.

(ج. ۱)

ماشین کد زیر را ران کرده و هنگام اجرای STR صحت عملکرد را می‌سنجیم.

```
SUB R0, R15, R15
ADD R2,R0,#90
SUB R1,R2,#30
RSC R3,R1,R2
STR R3,[R0,#100]
```

صحت عملکرد:

