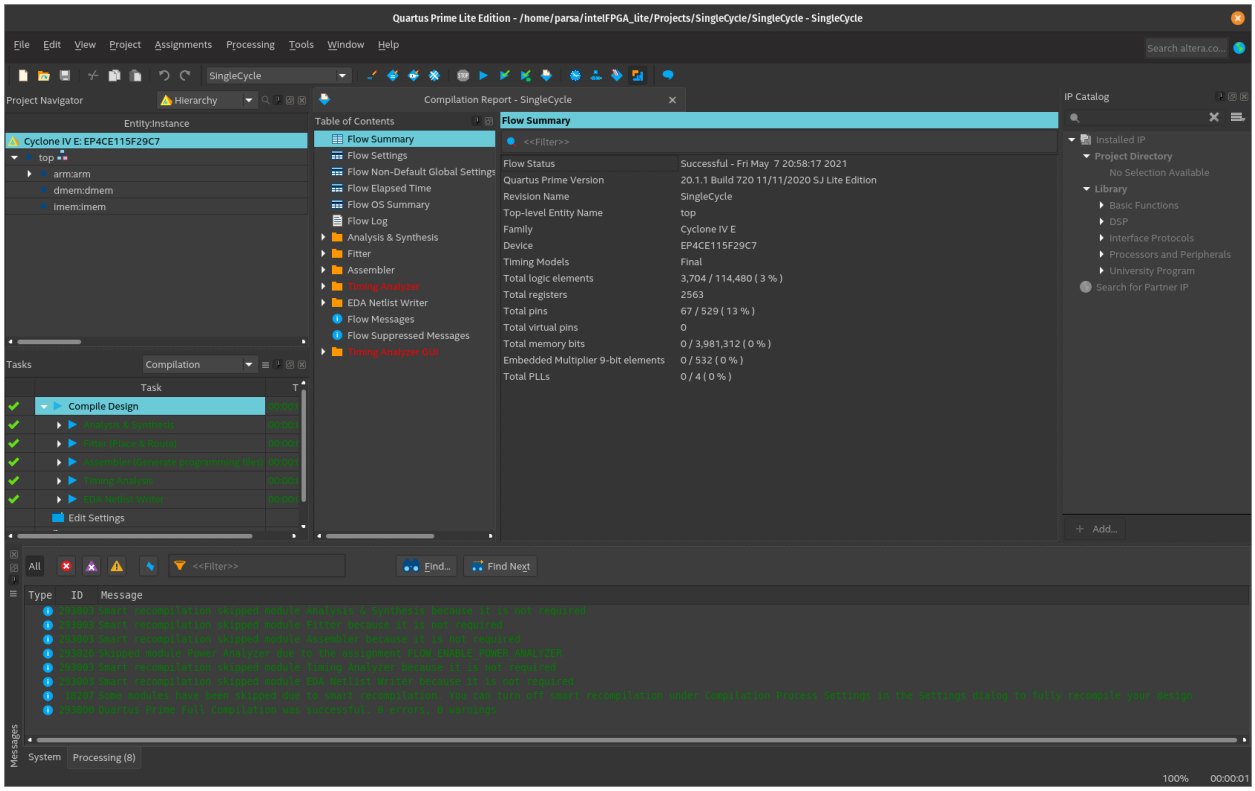
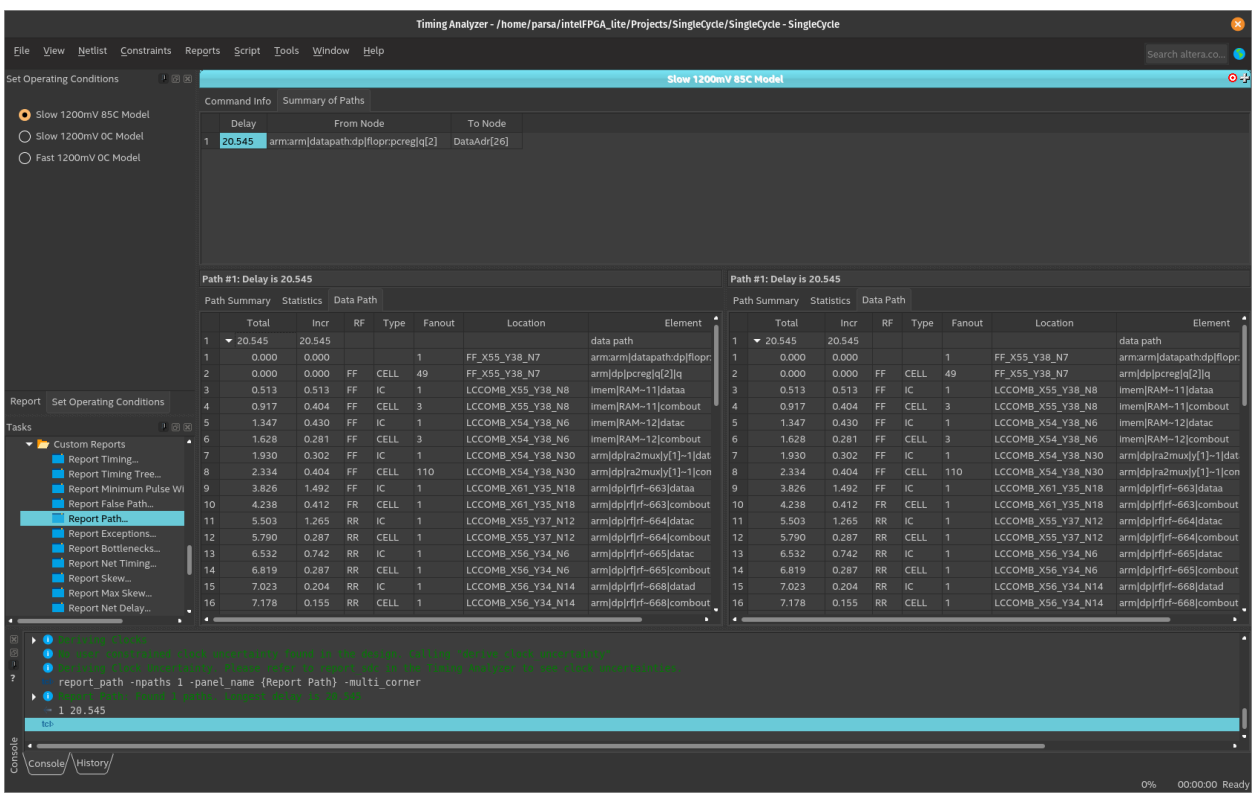
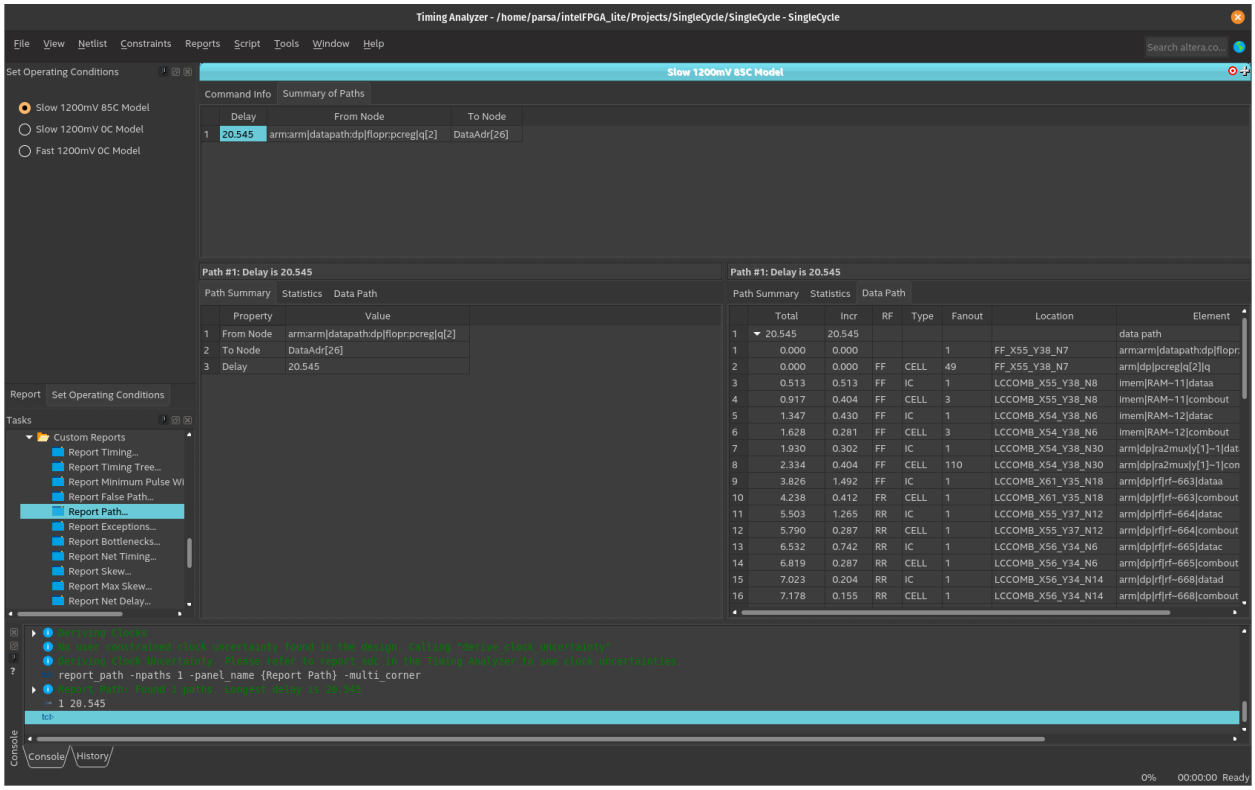
۱. الف)


Quartus Prime Lite Edition - /home/parsa/intelFPGA_lite/Projects/SingleCycle/SingleCycle - SingleCycle
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
top
arm:arm
dmem:dmem
imem:imem
Compilation Report - SingleCycle
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Timing Analyzer GUI
Flow Summary
Flow Status Successful - Fri May 7 20:58:17 2021
Quartus Prime Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name SingleCycle
Top-level Entity Name top
Family Cyclone IV E
Device EP4CE115F29C7
Timing Models Final
Total logic elements 3,704 / 114,480 (3 %)
Total registers 2563
Total pins 67 / 529 (13 %)
Total virtual pins 0
Total memory bits 0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements 0 / 532 (0 %)
Total PLLs 0 / 4 (0 %)
IP Catalog
Installed IP
Project Directory
Library
Tasks
Compilation
Compile Design
Edit Settings
Messages
System
Processing (8)
100%
00:00:01


Timing Analyzer - /home/parsa/intelFPGA_lite/Projects/SingleCycle/SingleCycle - SingleCycle
File View Netlist Constraints Reports Script Tools Window Help
Set Operating Conditions
Slow 1200mV 85C Model
Slow 1200mV 0C Model
Fast 1200mV 0C Model
Command Info
Summary of Paths
Delay From Node To Node
1 20.545 arm:arm|datapath:dp|flopr:pcreg|q[2] DataAdr[26]
Path #1: Delay is 20.545
Path Summary Statistics Data Path
Total Incr RF Type Fanout Location Element
1 20.545 20.545 data path
1 0.000 0.000 1 FF_X55_Y38_N7 arm:arm|datapath:dp|flopr:
2 0.000 0.000 FF CELL 49 FF_X55_Y38_N7 arm|dp|pcreg|q[2]|q
3 0.513 0.513 FF IC 1 LCCOMB_X55_Y38_N8 imem|RAM~11|dataa
4 0.917 0.404 FF CELL 3 LCCOMB_X55_Y38_N8 imem|RAM~11|combout
5 1.347 0.430 FF IC 1 LCCOMB_X54_Y38_N6 imem|RAM~12|datac
6 1.628 0.281 FF CELL 3 LCCOMB_X54_Y38_N6 imem|RAM~12|combout
7 1.930 0.302 FF IC 1 LCCOMB_X54_Y38_N30 arm|dp|ra2mux|y[1]~1|dat
8 2.334 0.404 FF CELL 110 LCCOMB_X54_Y38_N30 arm|dp|ra2mux|y[1]~1|con
9 3.826 1.492 FF IC 1 LCCOMB_X61_Y35_N18 arm|dp|rf|rf~663|dataa
10 4.238 0.412 FR CELL 1 LCCOMB_X61_Y35_N18 arm|dp|rf|rf~663|combout
11 5.503 1.265 RR IC 1 LCCOMB_X55_Y37_N12 arm|dp|rf|rf~664|datac
12 5.790 0.287 RR CELL 1 LCCOMB_X55_Y37_N12 arm|dp|rf|rf~664|combout
13 6.532 0.742 RR IC 1 LCCOMB_X56_Y34_N6 arm|dp|rf|rf~665|datac
14 6.819 0.287 RR CELL 1 LCCOMB_X56_Y34_N6 arm|dp|rf|rf~665|combout
15 7.023 0.204 RR IC 1 LCCOMB_X56_Y34_N14 arm|dp|rf|rf~668|datad
16 7.178 0.155 RR CELL 1 LCCOMB_X56_Y34_N14 arm|dp|rf|rf~668|combout
Report Set Operating Conditions
Tasks
Custom Reports
Report Timing...
Report Timing Tree...
Report Minimum Pulse Wi
Report False Path...
Report Path...
Report Exceptions...
Report Bottlenecks...
Report Net Timing...
Report Skew...
Report Max Skew...
Report Net Delay...
report_path -npaths 1 -panel_name {Report Path} -multi_corner
1 20.545
Console
History
0%
00:00:00 Ready



این مسیر واقعی نیست است زیرا به regfile نرسیده و در نتیجه بیانگر مسیر بحرانی است.

۱. ب)

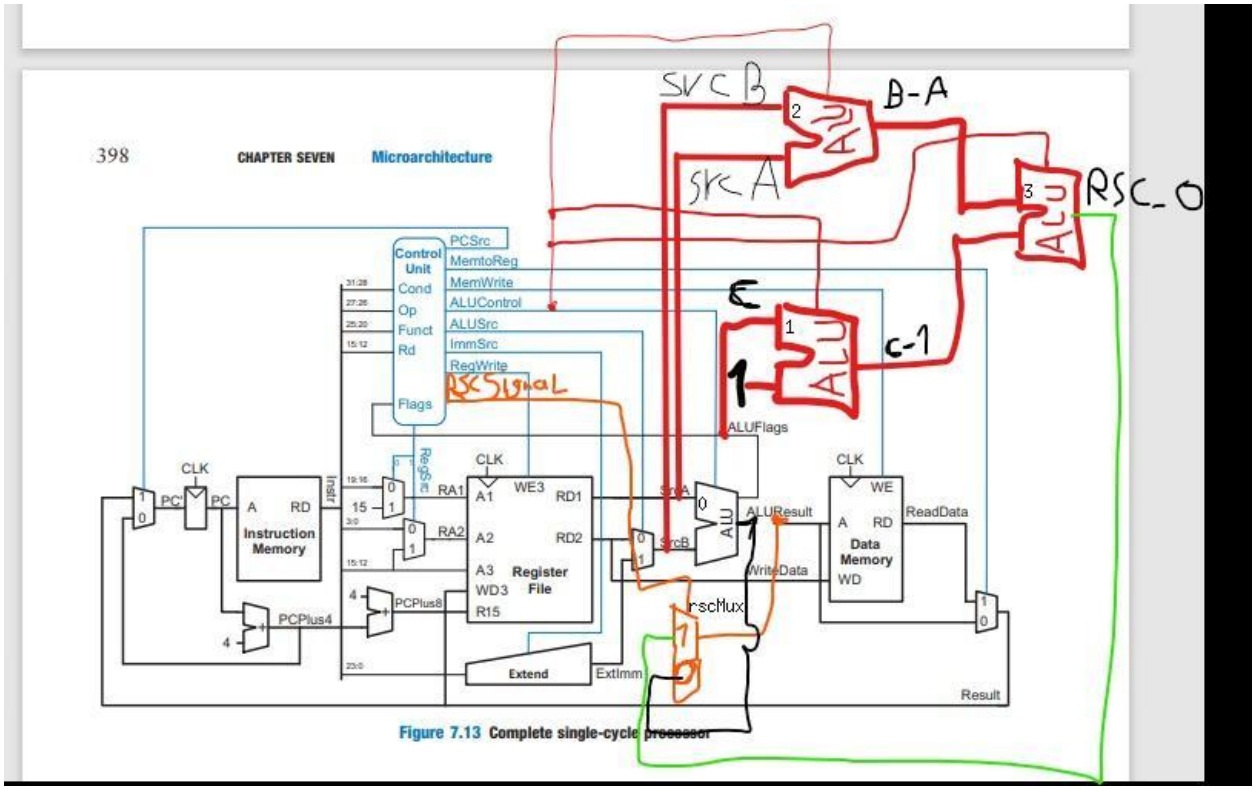
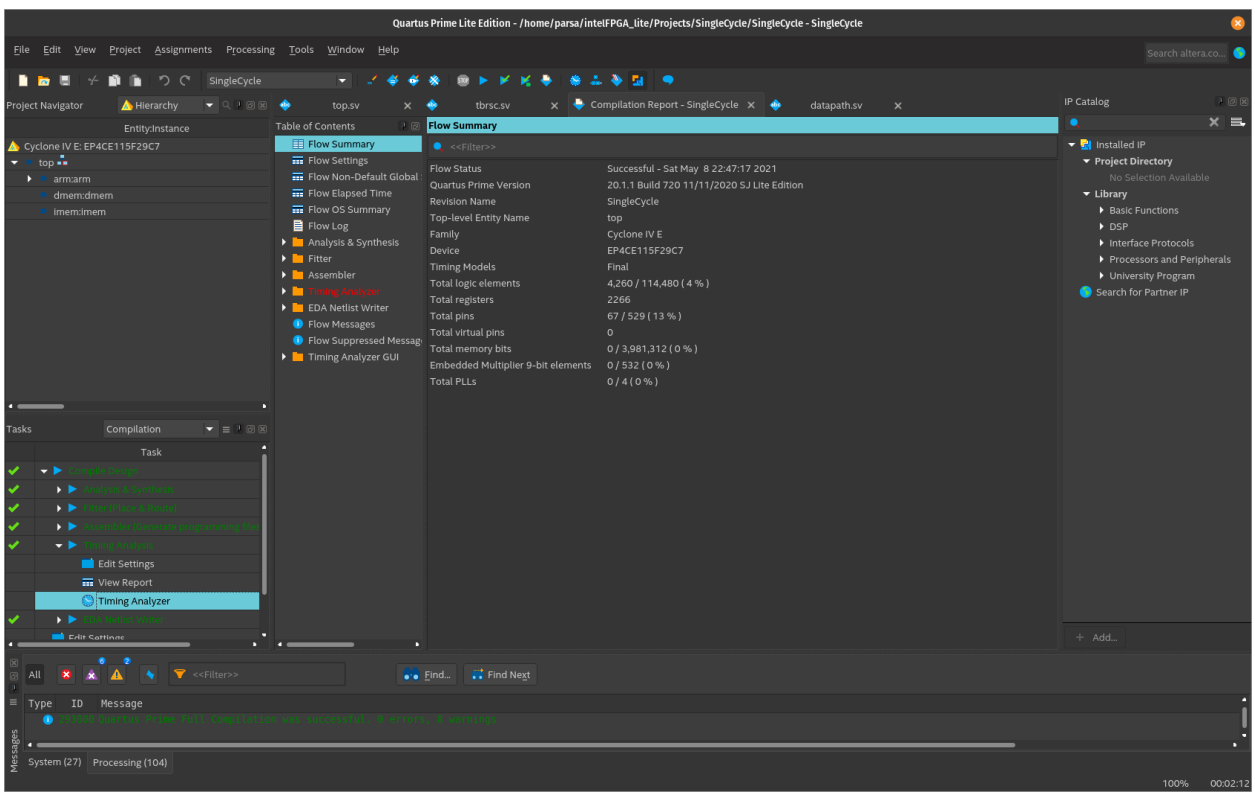
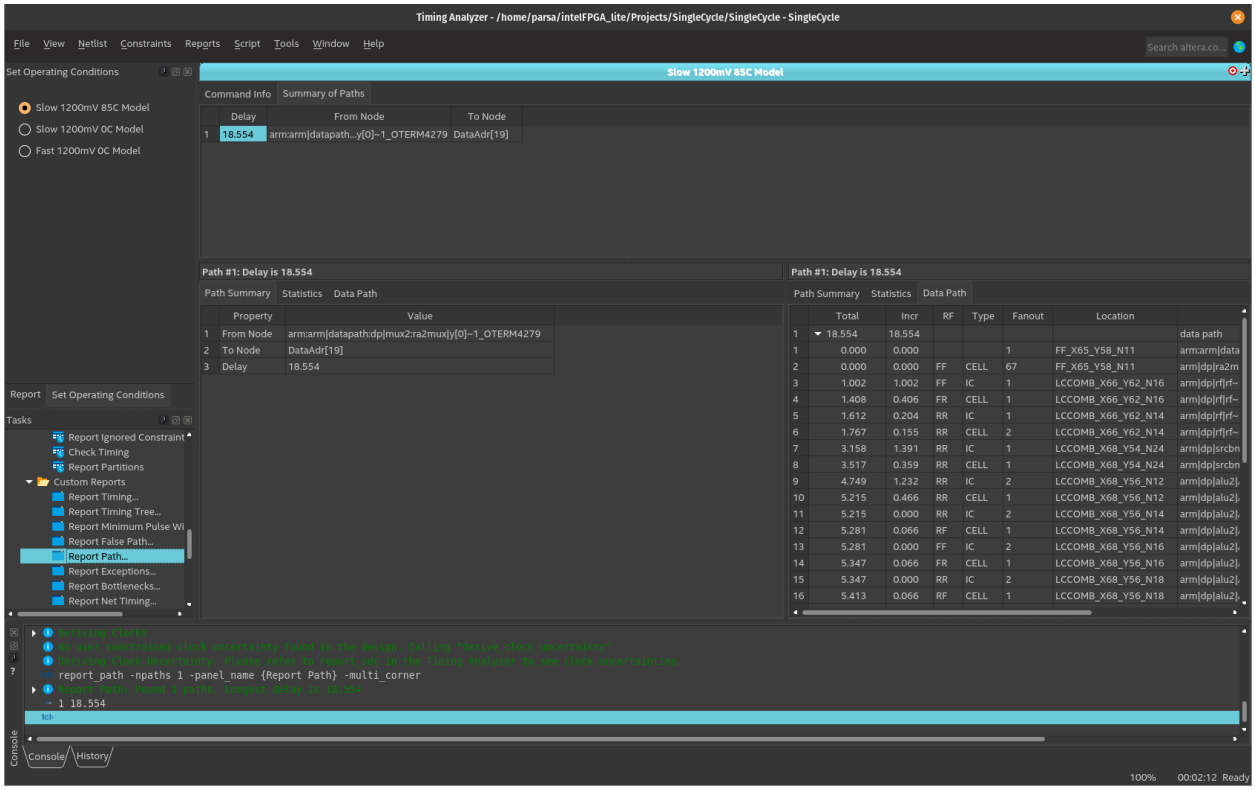
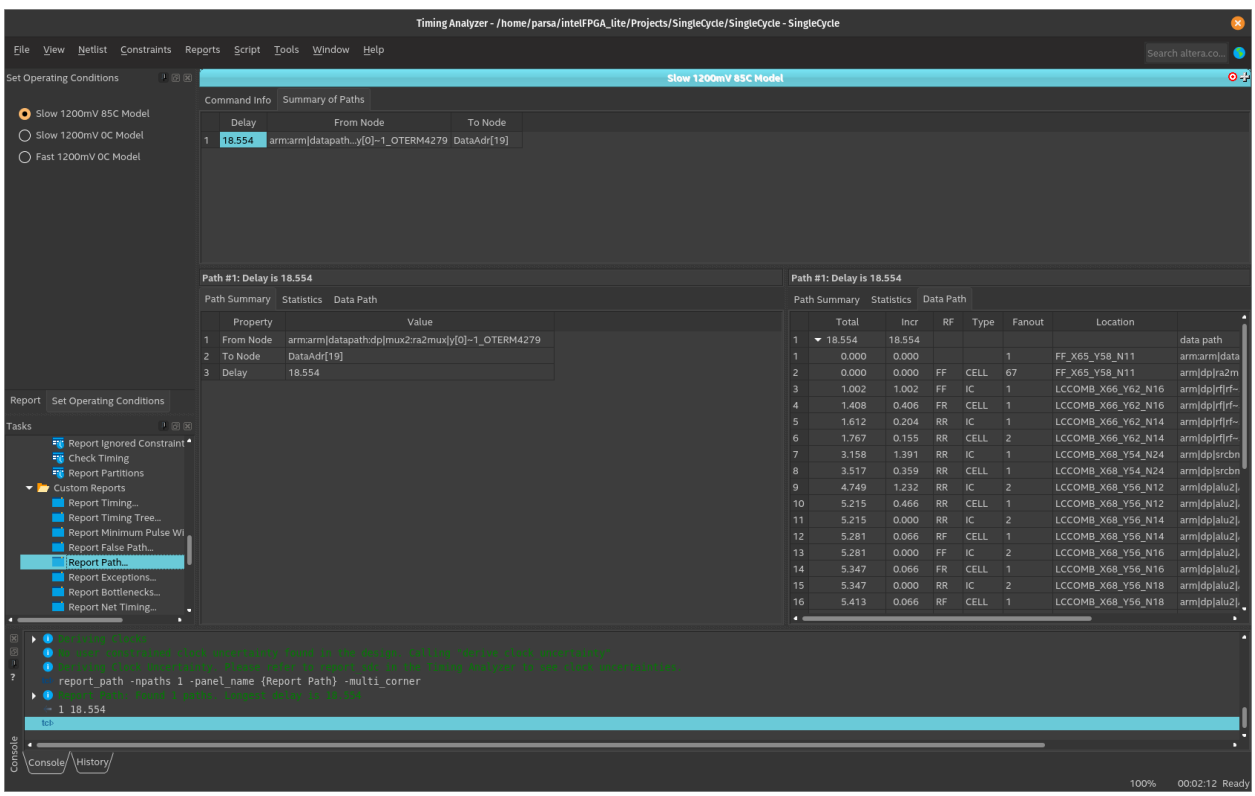


Figure 7.13 Complete single-cycle processor



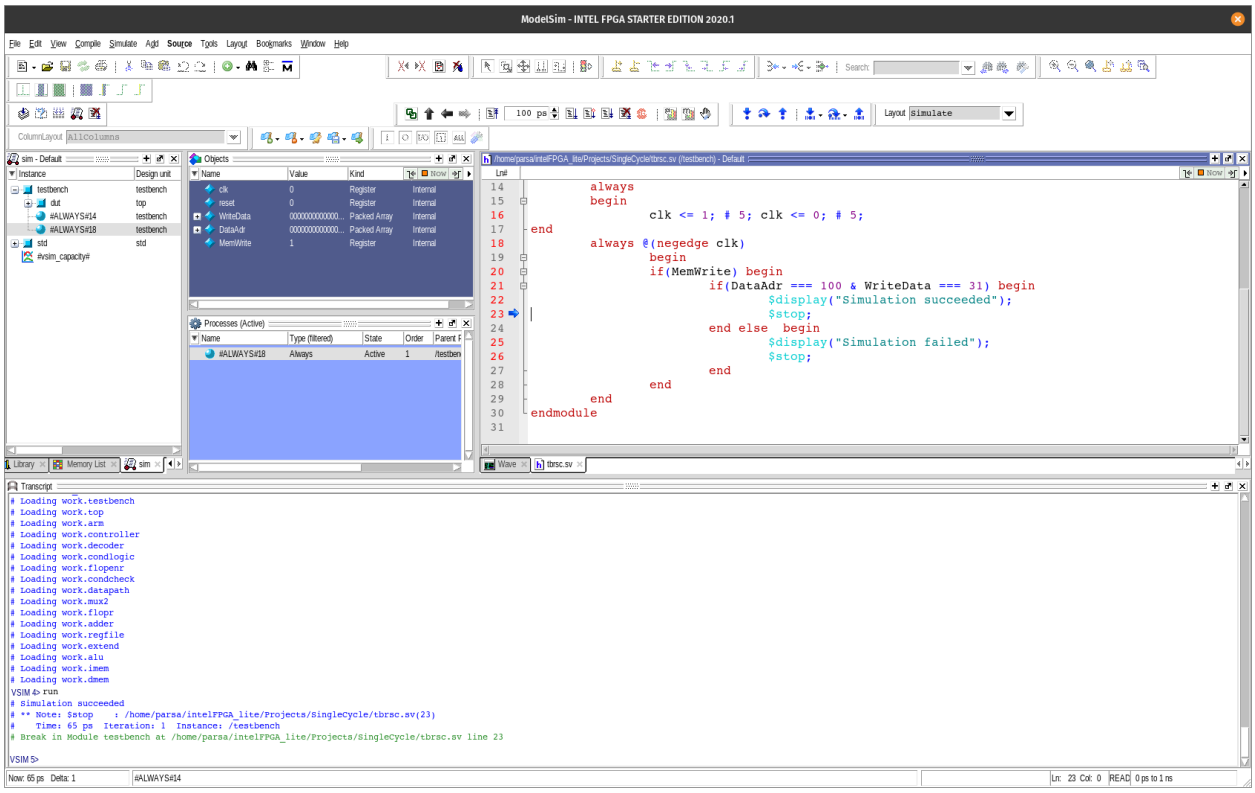




تعداد Logic Element ها از ۳۷۰۴ به ۴۲۶۰ رسیده که یعنی مساحت افزایش یافته. و تاخیر مسیر بحرانی از ۲۰.۵ به ۱۸.۵ رسیده.

۱. ج)

ماشین کد زیر را ران کرده و هنگام اجرای STR صحت عملکرد را می‌سنجیم.

```
SUB R0, R15, R15
ADD R2,R0,#90
SUB R1,R2,#30
RSC R3,R1,R2
STR R3,[R0,#100]
```

صحت عملکرد: