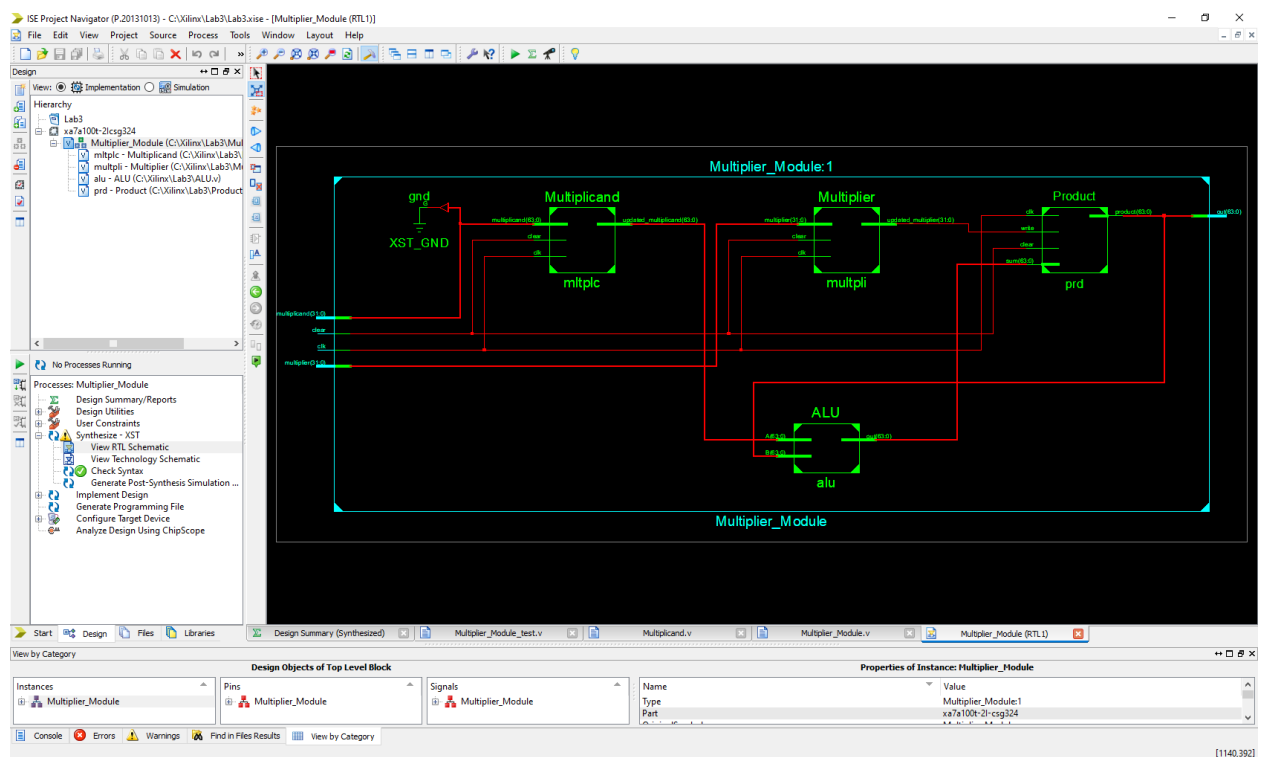
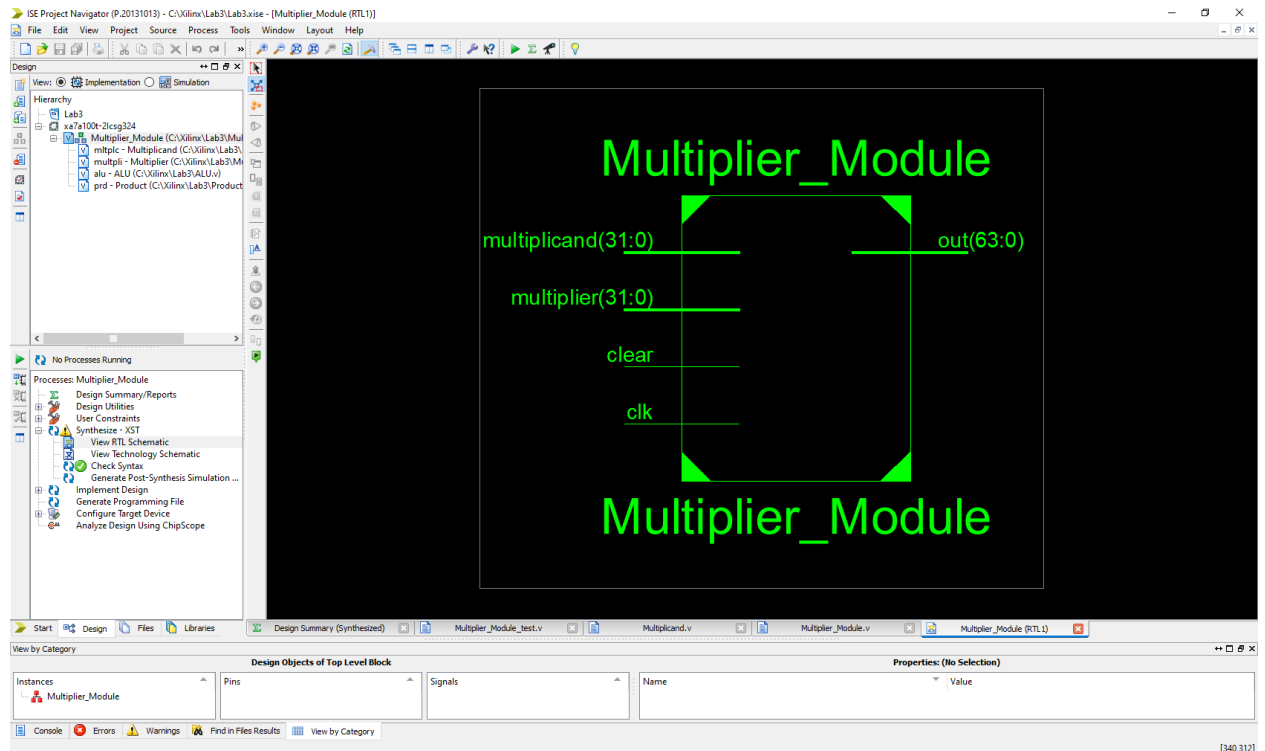
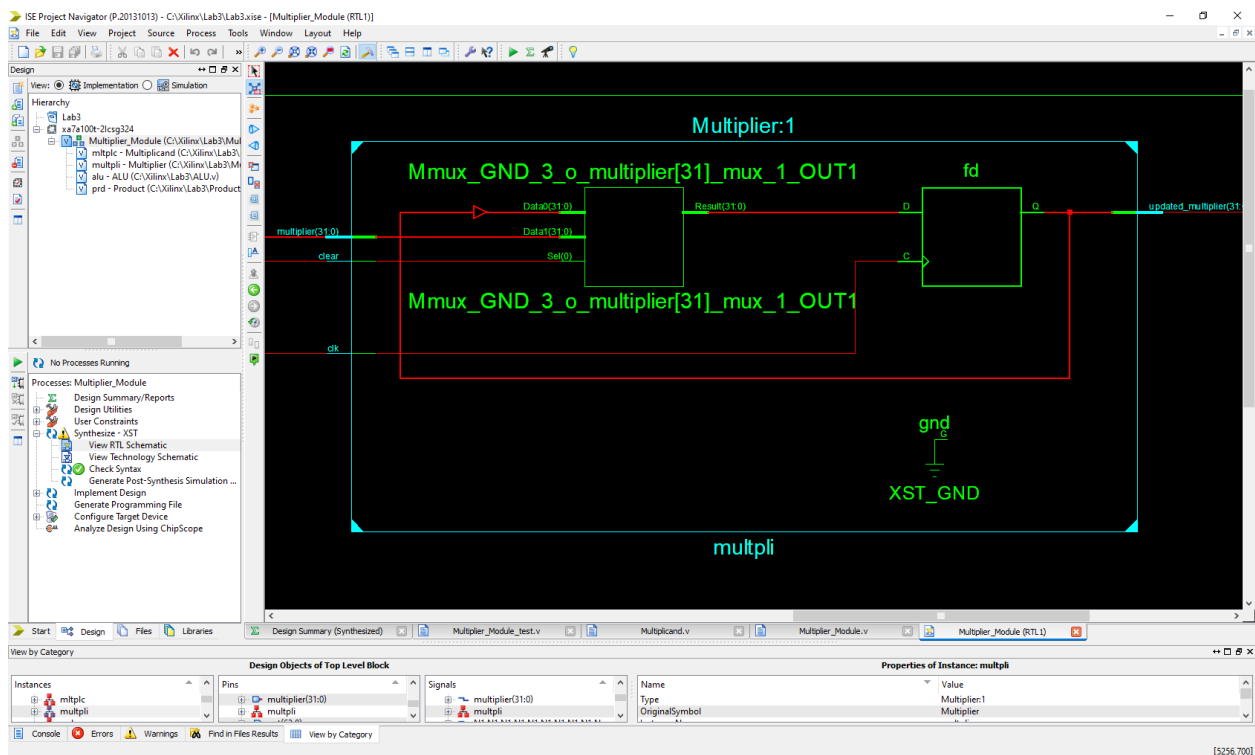
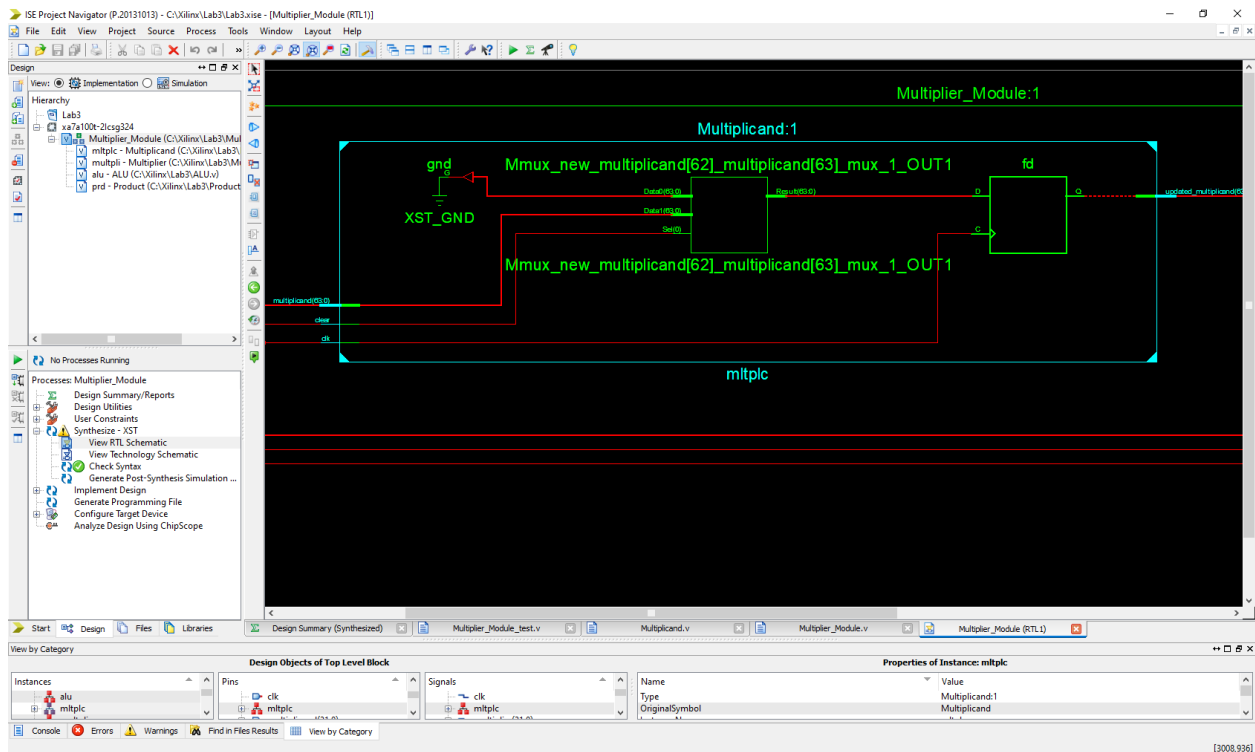
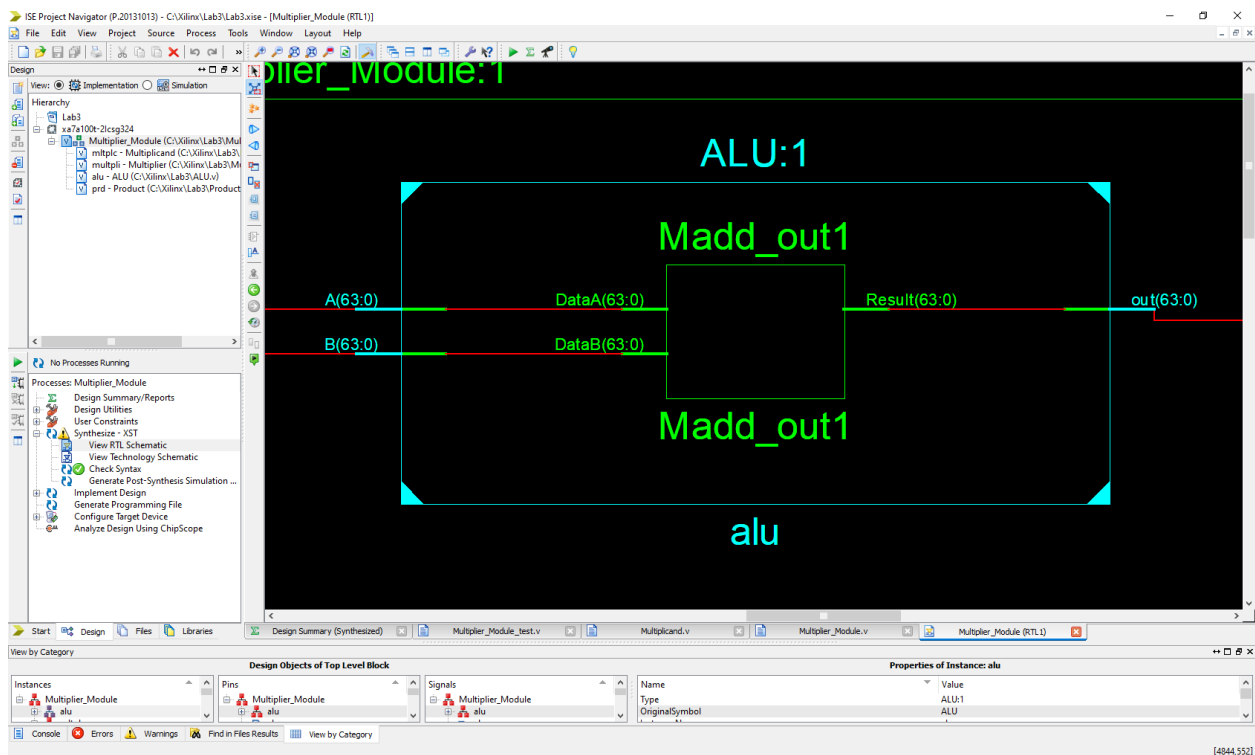
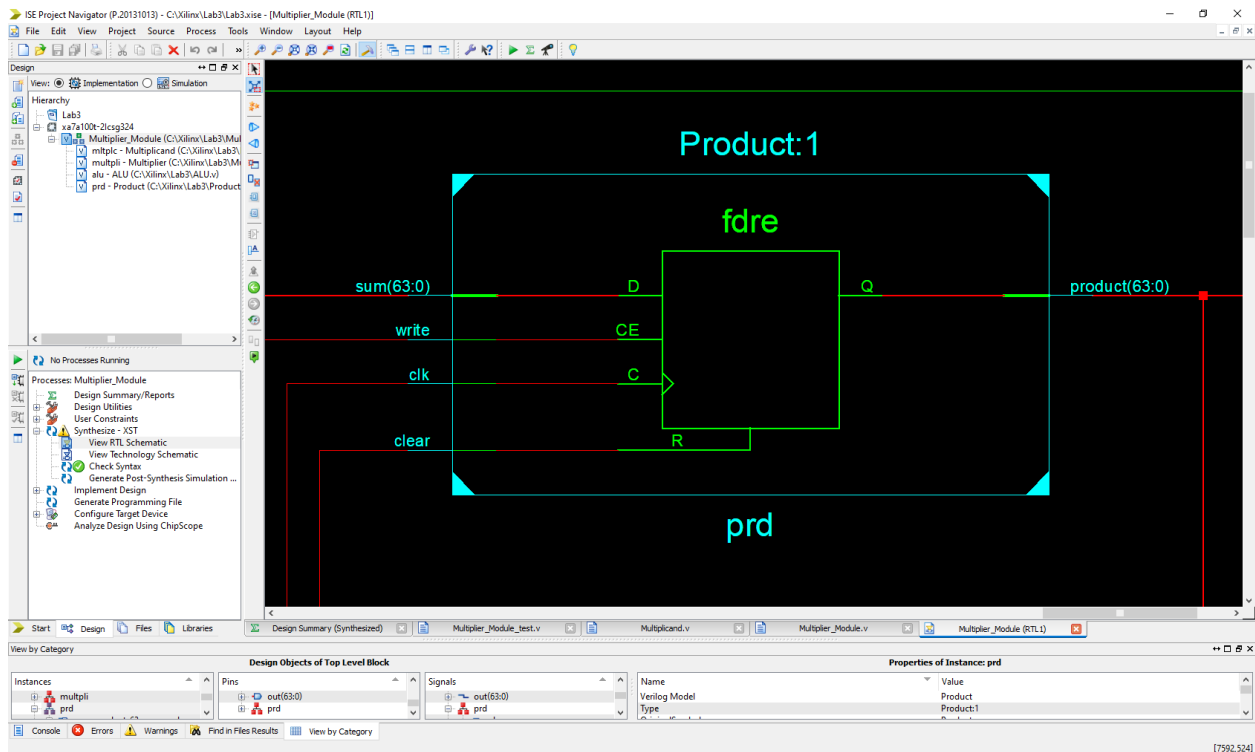


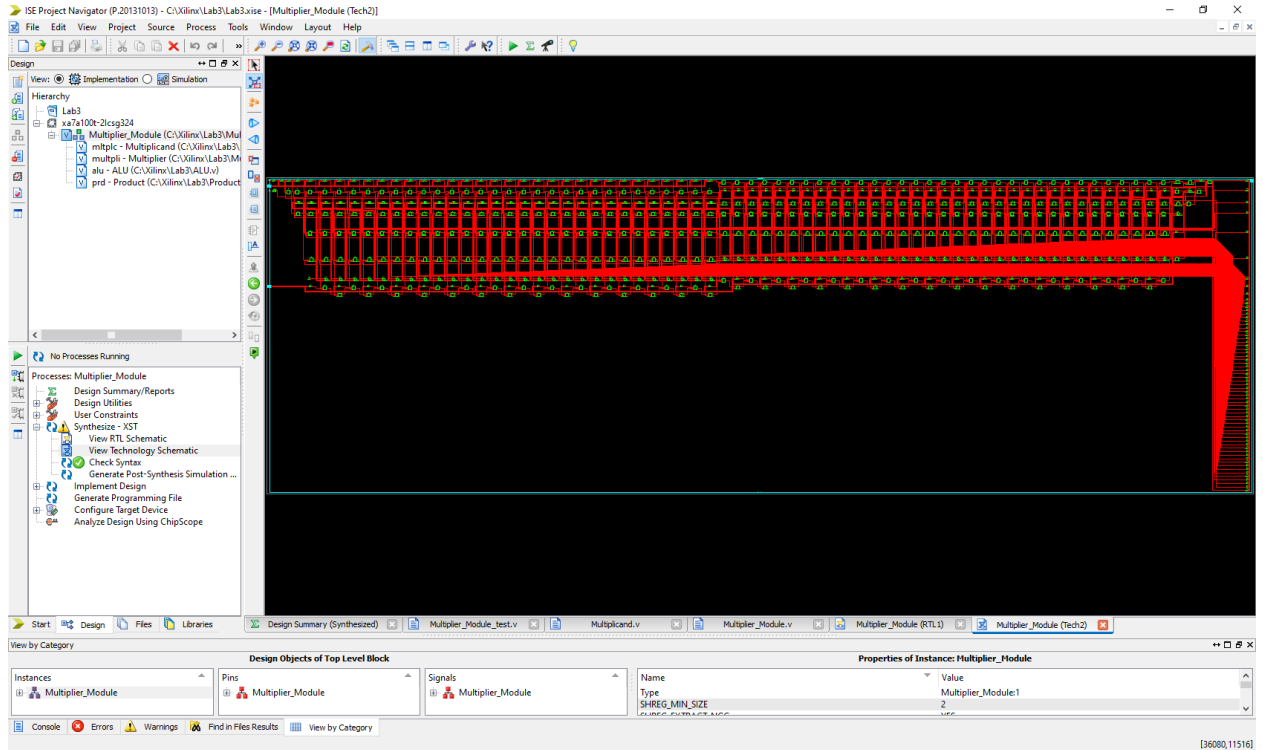
آزمایش ضرب با استفاده از شیفتر و اضافه کردن

تصویر RTL Schematic:









خروجی design summary:

ISE Project Navigator (P.20131013) - C:\Xilinx\Lab3\Lab3.xise - [Design Summary (Implemented)]

View: Implementation

Design Overview

Project File: Lab3.xise

Module Name: Multiplier_Module

Target Device: xc3s1600e-5fg320

Product Version: ISE 14.7

Design Goal: Balanced

Design Strategy: Xilinx Default (unlocked)

Environment: System Settings

Parser Errors: No Errors

Implementation State: Placed and Routed

Errors: No Errors

Warnings: 1 Warning (1 new)

Routing Results: All Signals Completely Routed

Timing Constraints: All Constraints Met

Final Timing Score: 0 (Setup: 0, Hold: 0)

Pinout Data: Pinout Report

Clock Data: Clock Report

Timing Constraints: All Constraints Met

Device Utilization Summary

| Logic Utilization | Used | Available | Utilization | Note(s) |
|--|------|-----------|-------------|---------|
| Number of Slice Flip Flops | 160 | 29,504 | 1% | |
| Number of 4 input LUTs | 128 | 29,504 | 1% | |
| Number of occupied Slices | 80 | 14,752 | 1% | |
| Number of Slices containing only related logic | 80 | 80 | 100% | |
| Number of Slices containing unrelated logic | 0 | 80 | 0% | |
| Total Number of 4 input LUTs | 128 | 29,504 | 1% | |
| Number of bonded IOBs | 130 | 250 | 52% | |
| Number of BUFIOs | 1 | 24 | 4% | |
| Average Fanout of Non-Clock Nets | 2.36 | | | |

Performance Summary

| Report Name | Status | Generated | Errors | Warnings | Infos |
|-------------------------------|---------|---------------|--------|-------------------|-----------------|
| Synthesis Report | Current | 2021 17:09:18 | 0 | 1 Warning (1 new) | 0 |
| Translation Report | Current | 2021 17:09:29 | 0 | 0 | 0 |
| Map Report | Current | 2021 17:09:37 | 0 | 0 | 2 Infos (1 new) |
| Place and Route Report | Current | 2021 17:10:02 | 0 | 0 | 2 Infos (0 new) |
| Power Report | | | | | |
| Post-PAE Static Timing Report | Current | 2021 17:10:06 | 0 | 0 | 6 Infos (2 new) |
| Bitgen Report | | | | | |

Secondary Reports

| Report Name | Status | Generated |
|-------------|--------|-----------|
| Report Name | Status | Generated |

Design Properties

Optional Design Summary Contents

Show Clock Report

Show Failing Constraints

Show Warnings

Show Errors

Design Summary (Implemented)

Multiplier_Module.v

Console | Find in Files Results | Errors | Warnings

خروجی delay ها:

Delay: 6.222ns (Levels of Logic = 65)
Source: mltplc/new_multiplicand_0 (FF)
Destination: prd/new_product_63 (FF)
Source Clock: clk rising
Destination Clock: clk rising

Data Path: mltplc/new_multiplicand_0 to prd/new_product_63

| Cell:in->out | fanout | Gate Delay | Net Delay | Logical Name (Net Name) |
|---------------------------|--------|------------|-----------|-----------------------------|
| FD:C->Q | 2 | 0.514 | 0.532 | |
| mltplc/new_multiplicand_0 | | | | (mltplc/new_multiplicand_0) |
| LUT2:I0->O | 1 | 0.612 | 0.000 | alu/Madd_out_lut<0> |
| (alu/Madd_out_lut<0>) | | | | |
| MUXCY:S->O | 1 | 0.404 | 0.000 | alu/Madd_out_cy<0> |
| (alu/Madd_out_cy<0>) | | | | |
| MUXCY:CI->O | 1 | 0.051 | 0.000 | alu/Madd_out_cy<1> |
| (alu/Madd_out_cy<1>) | | | | |
| MUXCY:CI->O | 1 | 0.051 | 0.000 | alu/Madd_out_cy<2> |
| (alu/Madd_out_cy<2>) | | | | |
| MUXCY:CI->O | 1 | 0.051 | 0.000 | alu/Madd_out_cy<3> |
| (alu/Madd_out_cy<3>) | | | | |
| MUXCY:CI->O | 1 | 0.051 | 0.000 | alu/Madd_out_cy<4> |
| (alu/Madd_out_cy<4>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<5> |
| (alu/Madd_out_cy<5>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<6> |
| (alu/Madd_out_cy<6>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<7> |
| (alu/Madd_out_cy<7>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<8> |
| (alu/Madd_out_cy<8>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<9> |
| (alu/Madd_out_cy<9>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<10> |
| (alu/Madd_out_cy<10>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<11> |
| (alu/Madd_out_cy<11>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<12> |
| (alu/Madd_out_cy<12>) | | | | |
| MUXCY:CI->O | 1 | 0.052 | 0.000 | alu/Madd_out_cy<13> |
| (alu/Madd_out_cy<13>) | | | | |

| | | | | |
|-----------------------|---|-------|-------|---------------------|
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<14> |
| (alu/Madd_out_cy<14>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<15> |
| (alu/Madd_out_cy<15>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<16> |
| (alu/Madd_out_cy<16>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<17> |
| (alu/Madd_out_cy<17>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<18> |
| (alu/Madd_out_cy<18>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<19> |
| (alu/Madd_out_cy<19>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<20> |
| (alu/Madd_out_cy<20>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<21> |
| (alu/Madd_out_cy<21>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<22> |
| (alu/Madd_out_cy<22>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<23> |
| (alu/Madd_out_cy<23>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<24> |
| (alu/Madd_out_cy<24>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<25> |
| (alu/Madd_out_cy<25>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<26> |
| (alu/Madd_out_cy<26>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<27> |
| (alu/Madd_out_cy<27>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<28> |
| (alu/Madd_out_cy<28>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<29> |
| (alu/Madd_out_cy<29>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<30> |
| (alu/Madd_out_cy<30>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<31> |
| (alu/Madd_out_cy<31>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<32> |
| (alu/Madd_out_cy<32>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<33> |
| (alu/Madd_out_cy<33>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<34> |
| (alu/Madd_out_cy<34>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<35> |
| (alu/Madd_out_cy<35>) | | | | |

| | | | | |
|-----------------------|---|-------|-------|---------------------|
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<36> |
| (alu/Madd_out_cy<36>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<37> |
| (alu/Madd_out_cy<37>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<38> |
| (alu/Madd_out_cy<38>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<39> |
| (alu/Madd_out_cy<39>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<40> |
| (alu/Madd_out_cy<40>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<41> |
| (alu/Madd_out_cy<41>) | | | | |
| MUXCY:CI->0 | 1 | 0.052 | 0.000 | alu/Madd_out_cy<42> |
| (alu/Madd_out_cy<42>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<43> |
| (alu/Madd_out_cy<43>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<44> |
| (alu/Madd_out_cy<44>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<45> |
| (alu/Madd_out_cy<45>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<46> |
| (alu/Madd_out_cy<46>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<47> |
| (alu/Madd_out_cy<47>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<48> |
| (alu/Madd_out_cy<48>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<49> |
| (alu/Madd_out_cy<49>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<50> |
| (alu/Madd_out_cy<50>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<51> |
| (alu/Madd_out_cy<51>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<52> |
| (alu/Madd_out_cy<52>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<53> |
| (alu/Madd_out_cy<53>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<54> |
| (alu/Madd_out_cy<54>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<55> |
| (alu/Madd_out_cy<55>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<56> |
| (alu/Madd_out_cy<56>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<57> |
| (alu/Madd_out_cy<57>) | | | | |

| | | | | |
|-----------------------|---|---------|--------------------------------|---------------------------|
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<58> |
| (alu/Madd_out_cy<58>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<59> |
| (alu/Madd_out_cy<59>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<60> |
| (alu/Madd_out_cy<60>) | | | | |
| MUXCY:CI->0 | 1 | 0.051 | 0.000 | alu/Madd_out_cy<61> |
| (alu/Madd_out_cy<61>) | | | | |
| MUXCY:CI->0 | 0 | 0.051 | 0.000 | alu/Madd_out_cy<62> |
| (alu/Madd_out_cy<62>) | | | | |
| XORCY:CI->0 | 1 | 0.699 | 0.000 | alu/Madd_out_xor<63> |
| (sum<63>) | | | | |
| FDRE:D | | 0.268 | | prd/new_product_63 |
| ----- | | | | |
| Total | | 6.222ns | (5.690ns logic, 0.532ns route) | (91.5% logic, 8.5% route) |

تصویری از شکل موج:

