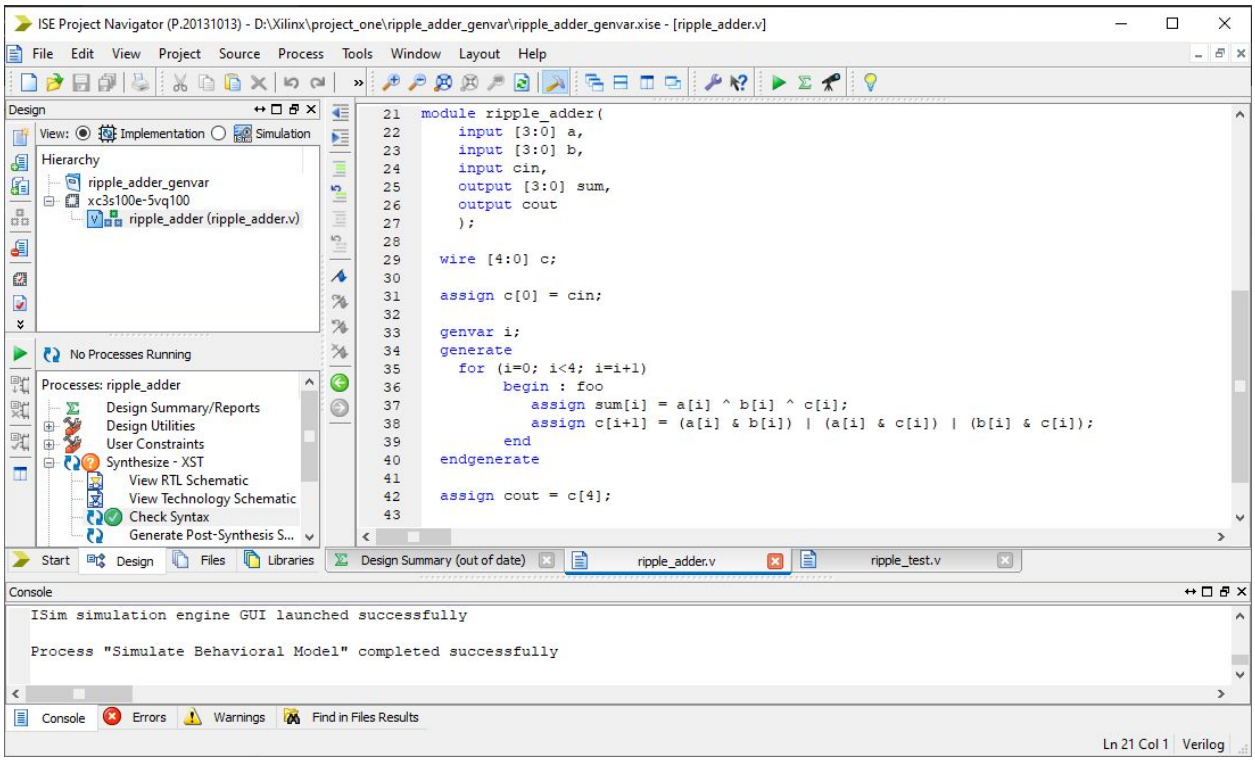
گزارش آزمایشگاه

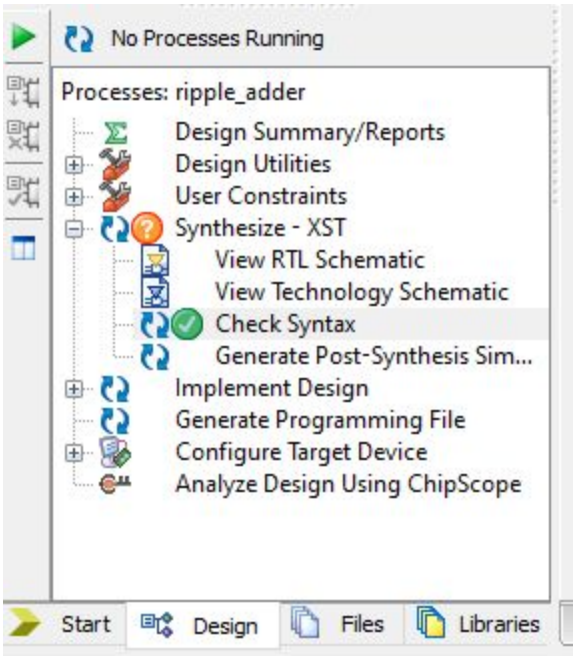
بخش ۱:

در اینجا بایستی مادامی که یک sum را خروجی می‌دهیم کری مربوط به آن را نیز حساب کنیم تا در حساب و کتاب جایگاه بعدی آن را به کار ببریم.

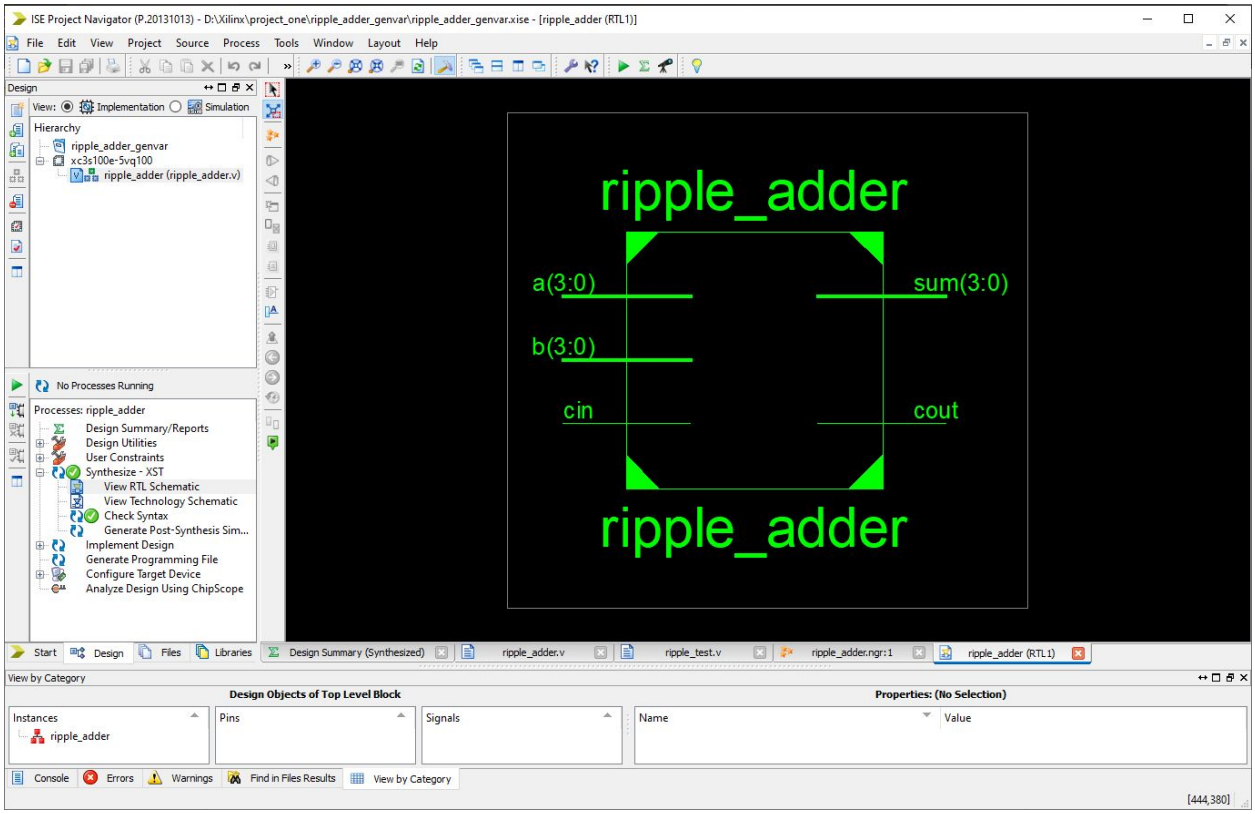
الف)

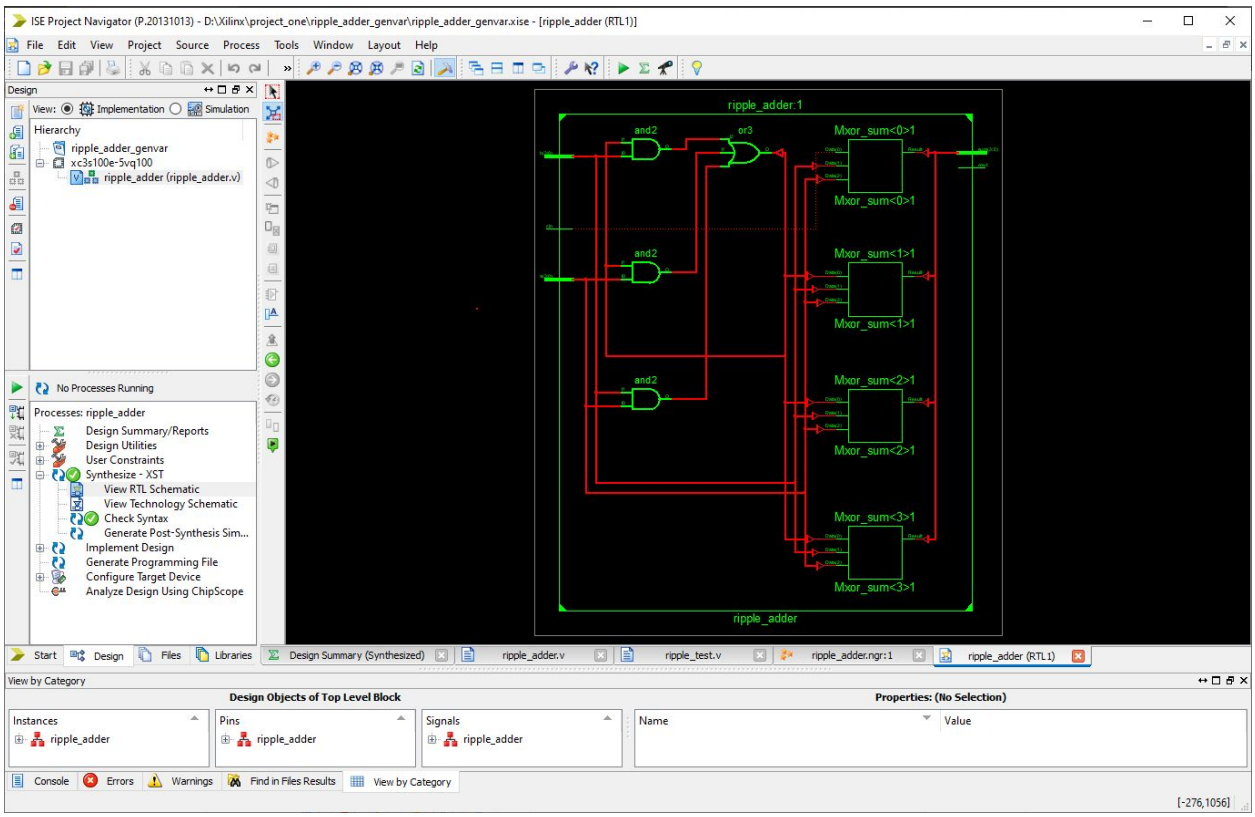


ب)

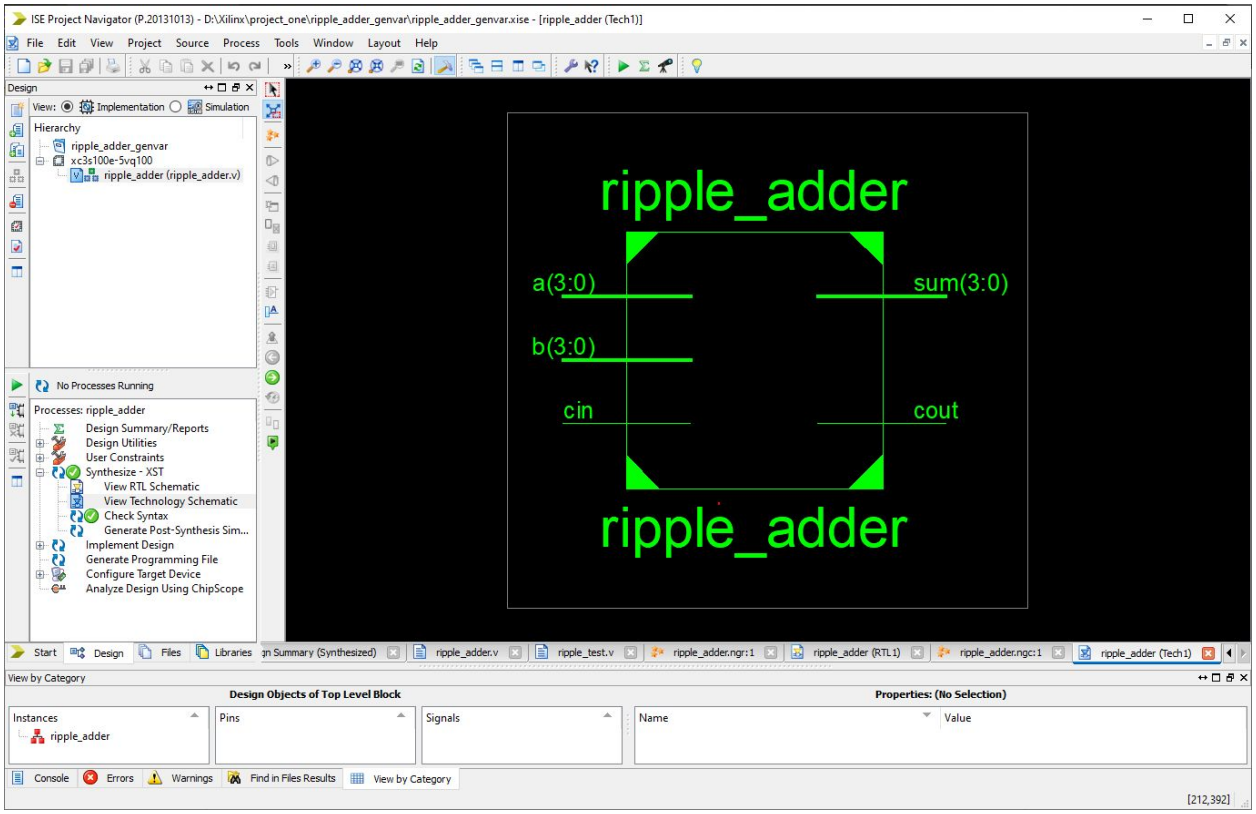


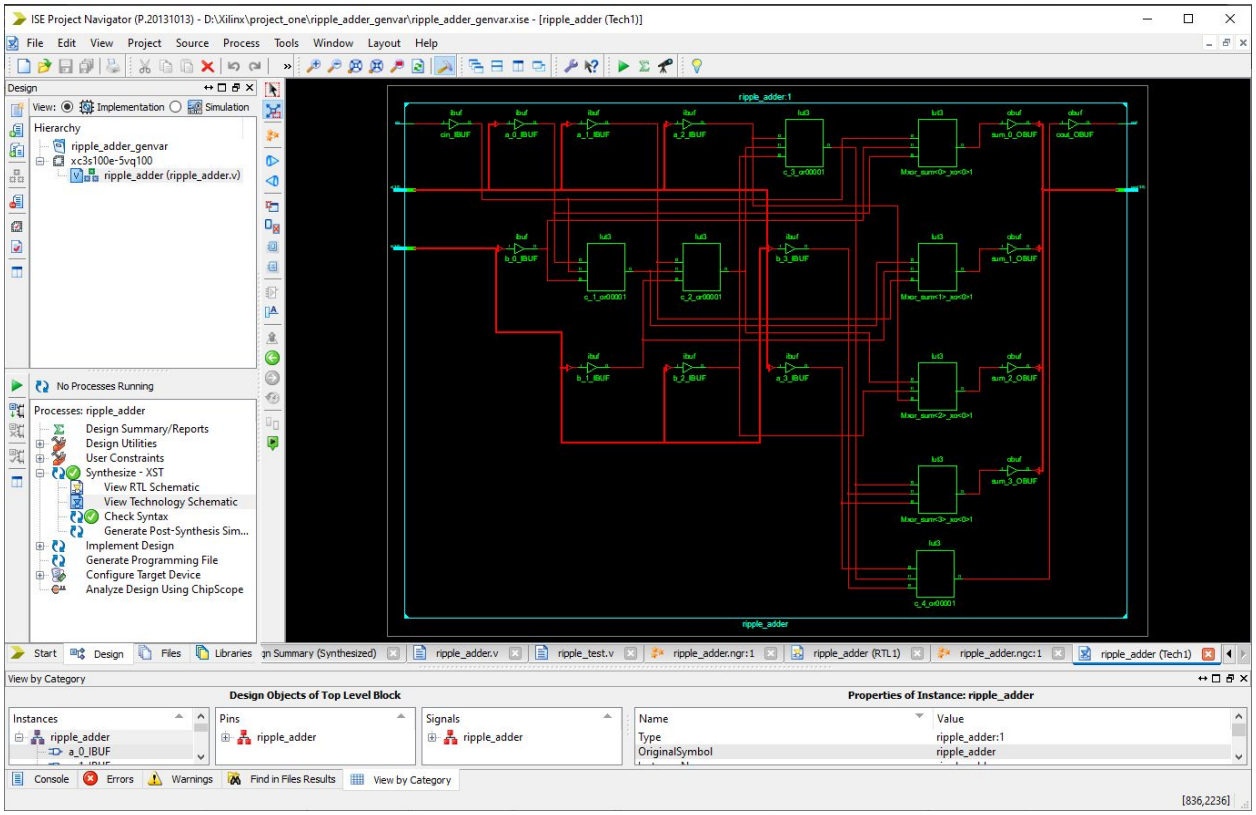
پ)RTL Schematic:



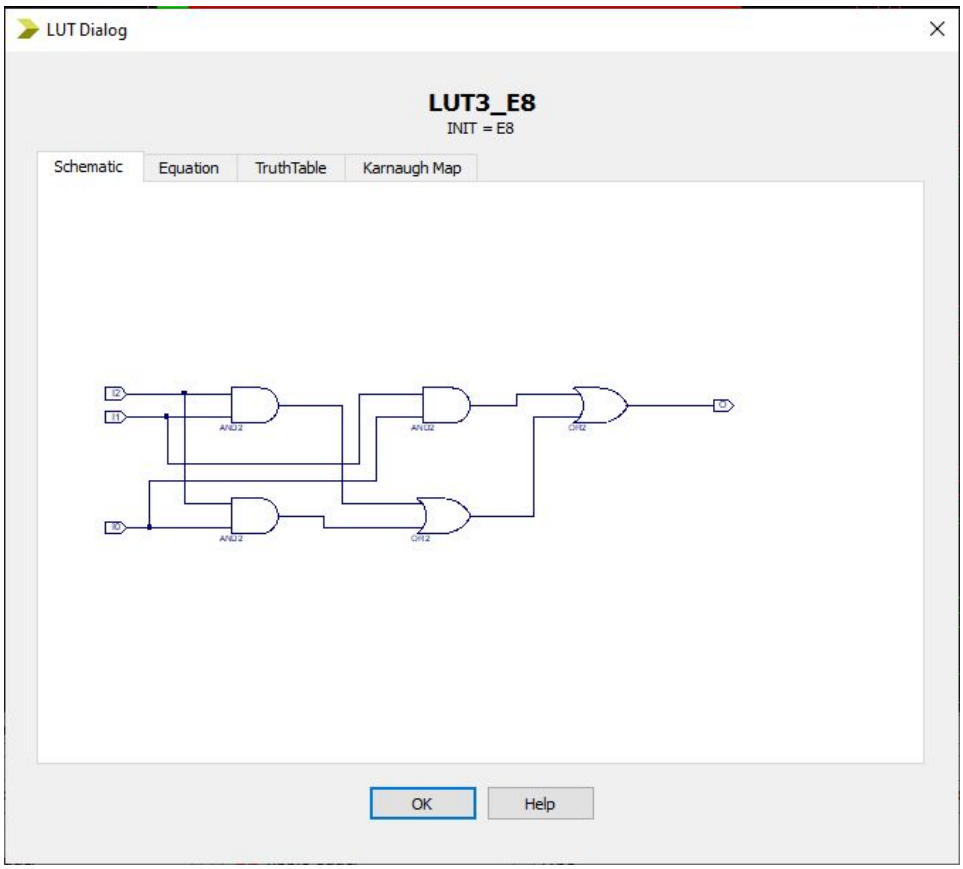


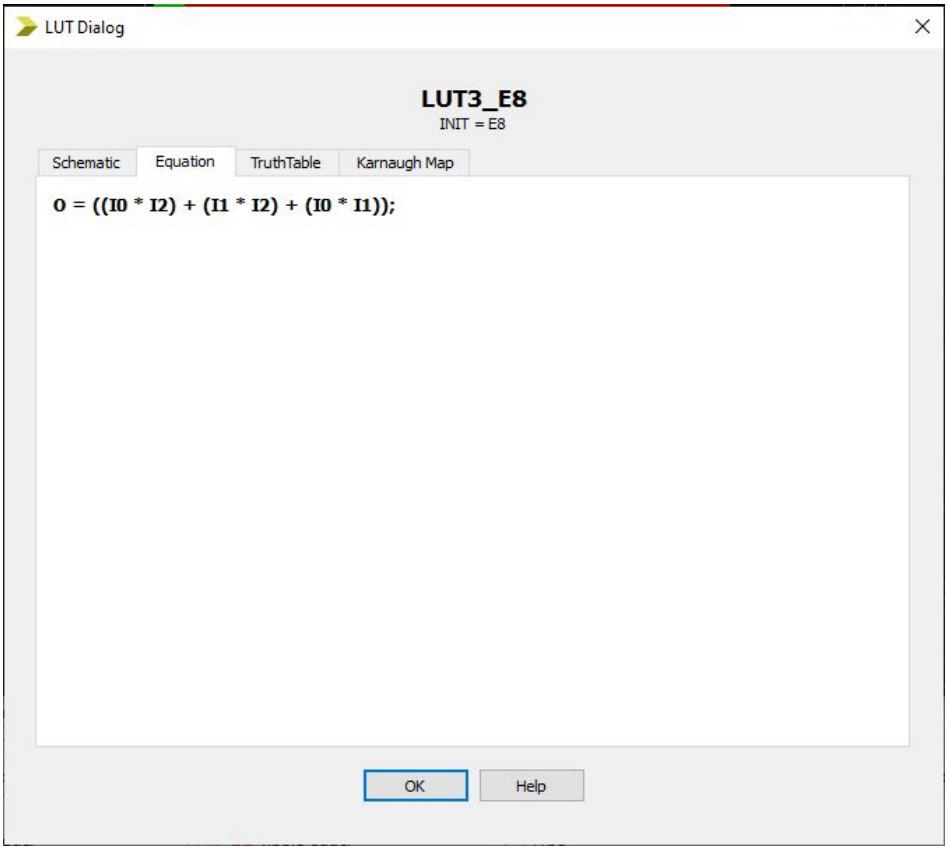
Technology Schematic:




ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\ripple_adder_genvar\ripple_adder_genvar.xise - [ripple_adder (Tech1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
ripple_adder_genvar
xc3s100e-5vq100
ripple_adder (ripple_adder.v)
No Processes Running
Processes: ripple_adder
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Sim...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
ripple_adder:1
ripple_adder
Start
Design
Files
Libraries
Summary (Synthesized)
ripple_adder.v
ripple_test.v
ripple_adder.ngr:1
ripple_adder (RTL1)
ripple_adder.ngc:1
ripple_adder (Tech1)
View by Category
Design Objects of Top Level Block
Instances
ripple_adder
a_0_IBUF
Pins
ripple_adder
Signals
ripple_adder
Properties of Instance: ripple_adder
Name
Value
Type
ripple_adder:1
OriginalSymbol
ripple_adder
Console
Errors
Warnings
Find in Files Results
View by Category
[836,2236]

ت)


LUT Dialog
LUT3_E8
INIT = E8
Schematic
Equation
TruthTable
Karnaugh Map
I2
I1
I0
O
AND2
AND2
OR2
AND2
OR2
OK
Help


LUT Dialog
LUT3_E8
INIT = E8
Schematic
Equation
TruthTable
Karnaugh Map
O = ((I0 * I2) + (I1 * I2) + (I0 * I1));
OK
Help

LUT Dialog

LUT3_E8

INIT = E8

Schematic | Equation | TruthTable | Karnaugh Map

I2	I1	I0	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

OK | Help

LUT Dialog

LUT3_E8

INIT = E8

Schematic | Equation | TruthTable | Karnaugh Map

OK | Help

ث)

Pad to Pad

Source Pad	Destination Pad	Delay
a<0>	cout	8.381
a<0>	sum<0>	5.692
a<0>	sum<1>	7.003
a<0>	sum<2>	7.996
a<0>	sum<3>	8.744
a<1>	cout	7.626
a<1>	sum<1>	6.226
a<1>	sum<2>	7.241
a<1>	sum<3>	7.989
a<2>	cout	6.245
a<2>	sum<2>	5.860
a<2>	sum<3>	6.608
a<3>	cout	5.934
a<3>	sum<3>	6.141
b<0>	cout	8.146
b<0>	sum<0>	5.765
b<0>	sum<1>	6.768
b<0>	sum<2>	7.761
b<0>	sum<3>	8.509
b<1>	cout	7.903
b<1>	sum<1>	6.469
b<1>	sum<2>	7.518
b<1>	sum<3>	8.266
b<2>	cout	6.393
b<2>	sum<2>	6.008
b<2>	sum<3>	6.756
b<3>	cout	5.725
b<3>	sum<3>	6.077
cin	cout	8.623
cin	sum<0>	6.340
cin	sum<1>	7.245
cin	sum<2>	8.238
cin	sum<3>	8.986

ج)

ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\ripple_adder_genvar\ripple_adder_genvar.xise - [ripple_test.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
ripple_adder_genvar
xc3s100e-5vq100
ripple_test (ripple_test.v)
uut - ripple_adder (ripple_adde
No Processes Running
Processes: ripple_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
// Revision 0.01 - File Created
// Additional Comments:
//
module ripple_test;
// Inputs
reg [3:0] a;
reg [3:0] b;
reg cin;
// Outputs
wire [3:0] sum;
wire cout;
// Instantiate the Unit Under Test (UUT)
ripple_adder uut (
.a(a),
.b(b),
.cin(cin),
.sum(sum),
.cout(cout)
);
initial begin
a = 4'b0011; b = 4'b1100; cin = 1'b0; #100;
a = 4'b0011; b = 4'b1100; cin = 1'b1; #100;
a = 4'b0001; b = 4'b1111; cin = 1'b1; #100;
end
endmodule
Start Design Files Libraries
Design Summary (Implemented)
ripple_adder.v
ripple_test.v
ripple_adder.ngr:1
ripple_adder (RTL1)
ripple_adder.ngc:1
View by Category
Design Objects of Top Level Block
Instances
cout_OBUF
c_1_or00001
Pins
ripple_adder
Signals
ripple_adder
Properties of Instance: c_1_or00001
Name
Value
Type
lut3
Instance Name
c_1_or00001
Console
Errors
Warnings
Find in Files Results
View by Category
Ln 25 Col 1
Verilog

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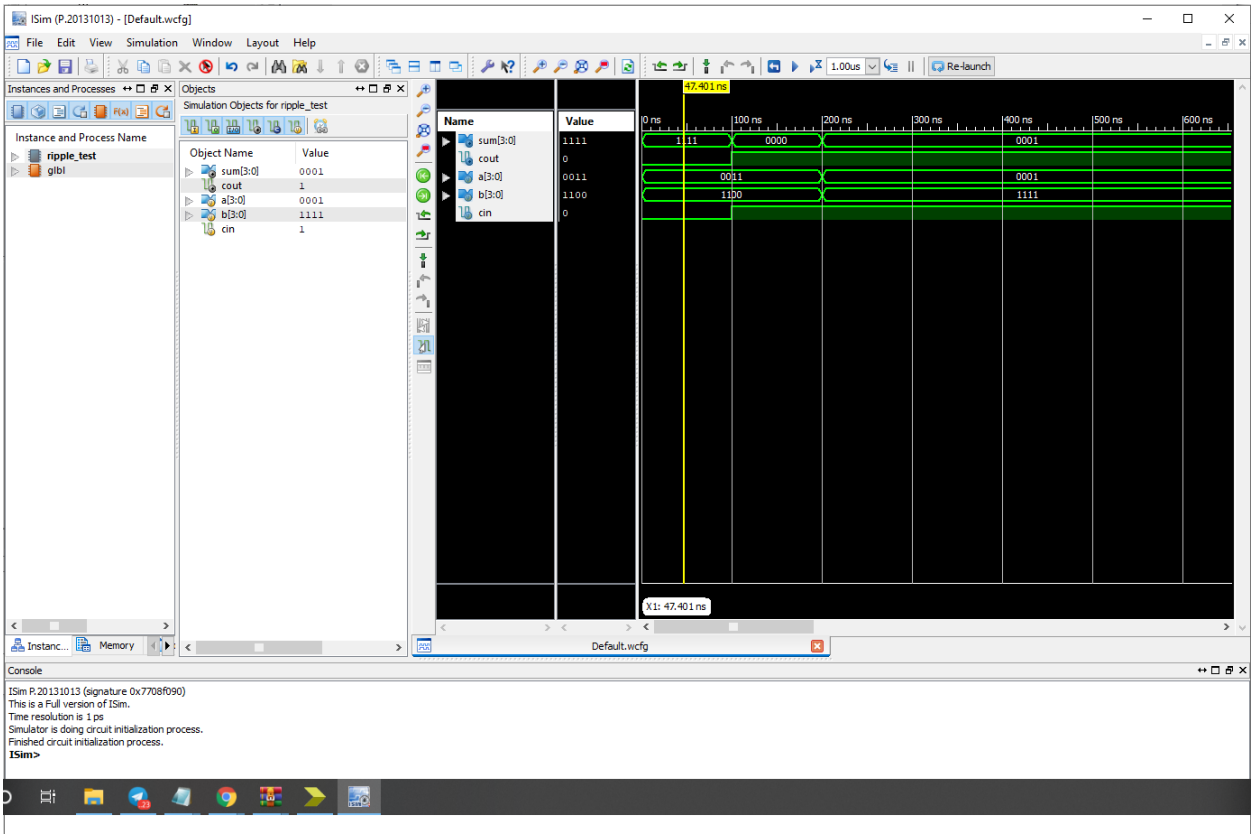
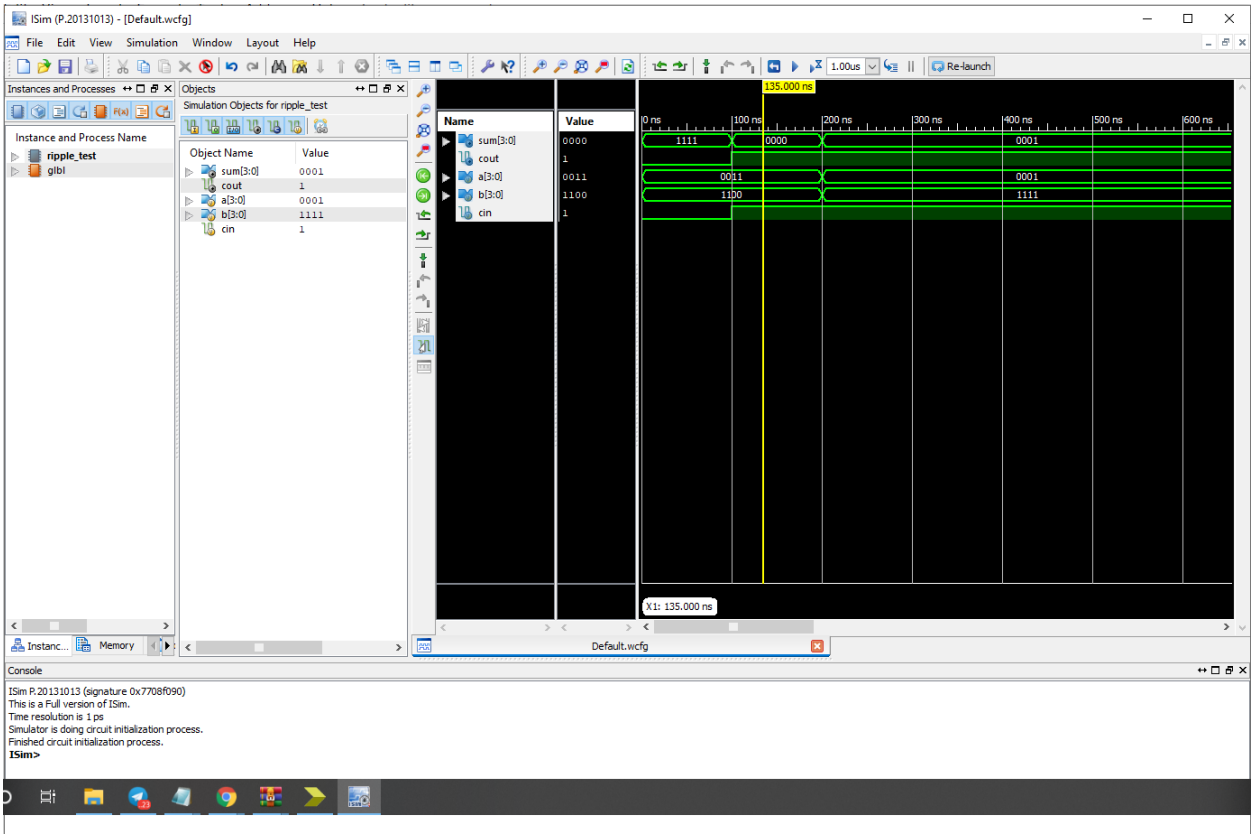
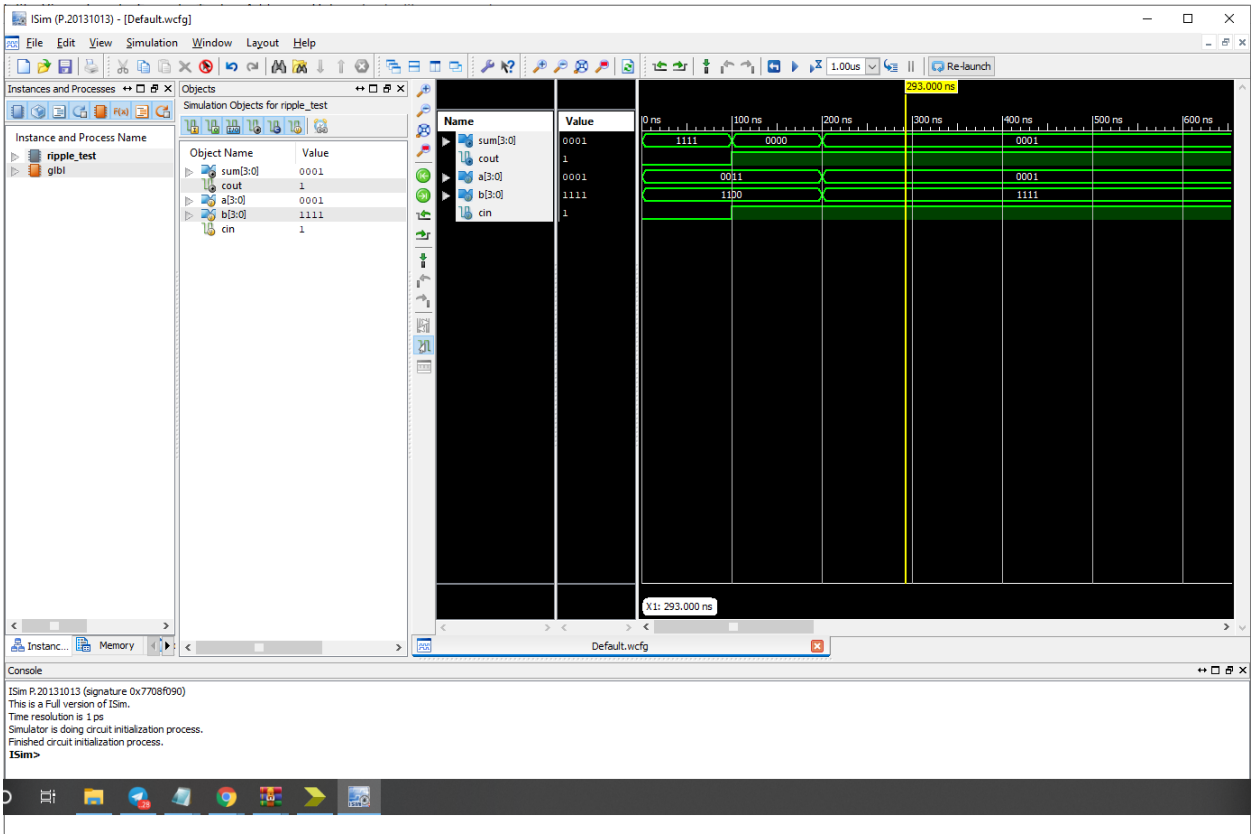
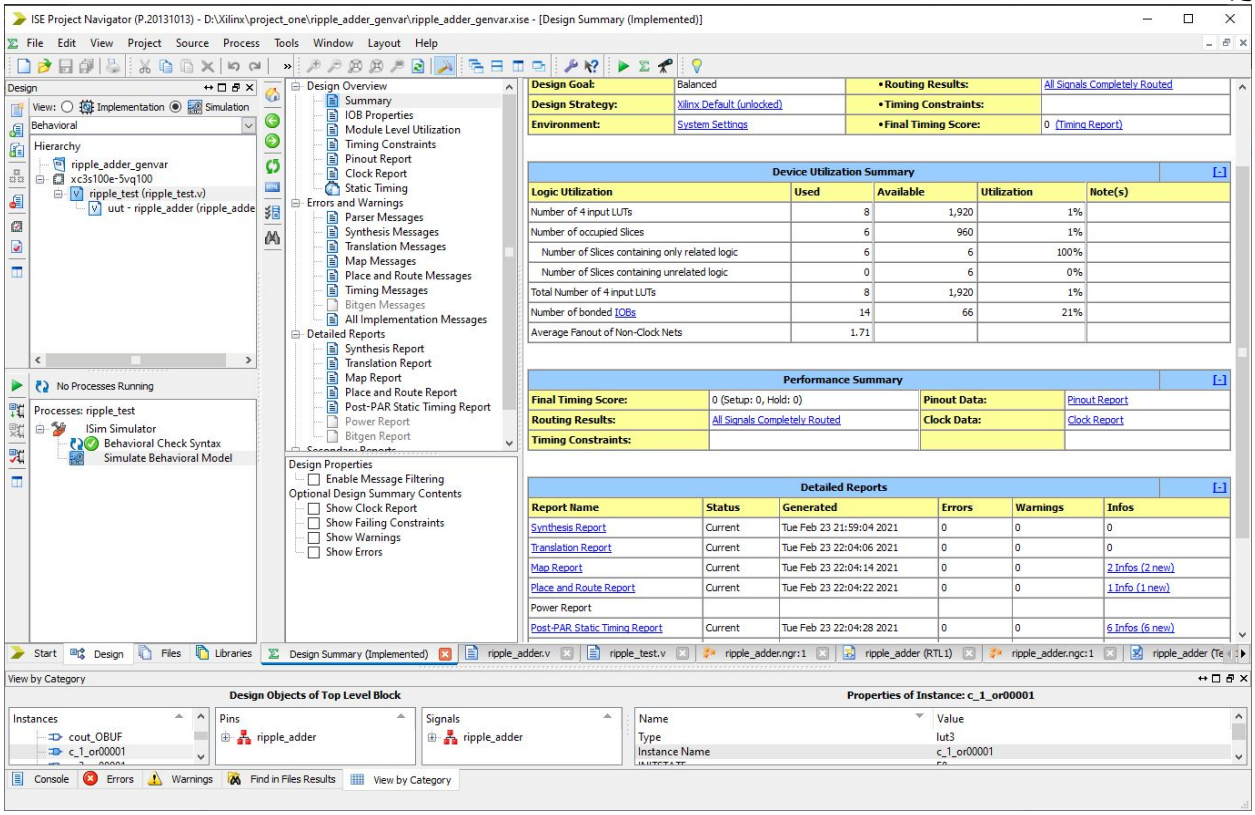

ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
ripple_test
glbl
Objects
Simulation Objects for ripple_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name Value
sum[3:0] 1111
cout 0
a[3:0] 0011
b[3:0] 1100
cin 0
47.401 ns
0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns
X1: 47.401 ns
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
ripple_test
glbl
Objects
Simulation Objects for ripple_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name Value
sum[3:0] 0000
cout 1
a[3:0] 0011
b[3:0] 1100
cin 1
135.000 ns
0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns
X1: 135.000 ns
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
ripple_test
glbl
Objects
Simulation Objects for ripple_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name
Value
293.000 ns
0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns
1111 0000 0001
0011 0001
1100 1111
X1: 293.000 ns
Instanc... Memory
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\ripple_adder_genvar\ripple_adder_genvar.xise - [Design Summary (Implemented)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
ripple_adder_genvar
xc3s100e-5vq100
ripple_test (ripple_test.v)
uut - ripple_adder (ripple_adde
No Processes Running
Processes: ripple_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Translation Report
Map Report
Place and Route Report
Post-PAR Static Timing Report
Power Report
Bitgen Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
Design Goal: Balanced
Design Strategy: Xilinx Default (unlocked)
Environment: System Settings
•Routing Results: All Signals Completely Routed
•Timing Constraints:
•Final Timing Score: 0 (Timing Report)
Device Utilization Summary
Logic Utilization | Used | Available | Utilization | Note(s)
Number of 4 input LUTs | 8 | 1,920 | 1%
Number of occupied Slices | 6 | 960 | 1%
Number of Slices containing only related logic | 6 | 6 | 100%
Number of Slices containing unrelated logic | 0 | 6 | 0%
Total Number of 4 input LUTs | 8 | 1,920 | 1%
Number of bonded IOBs | 14 | 66 | 21%
Average Fanout of Non-Clock Nets | 1.71
Performance Summary
Final Timing Score: 0 (Setup: 0, Hold: 0)
Routing Results: All Signals Completely Routed
Timing Constraints:
Pinout Data: Pinout Report
Clock Data: Clock Report
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Feb 23 21:59:04 2021 | 0 | 0 | 0
Translation Report | Current | Tue Feb 23 22:04:06 2021 | 0 | 0 | 0
Map Report | Current | Tue Feb 23 22:04:14 2021 | 0 | 0 | 2 Infos (2 new)
Place and Route Report | Current | Tue Feb 23 22:04:22 2021 | 0 | 0 | 1 Info (1 new)
Power Report
Post-PAR Static Timing Report | Current | Tue Feb 23 22:04:28 2021 | 0 | 0 | 6 Infos (6 new)
Start Design Files Libraries
Design Summary (Implemented)
ripple_adder.v
ripple_test.v
ripple_adder.ngr:1
ripple_adder (RTL1)
ripple_adder.ngc:1
View by Category
Design Objects of Top Level Block
Instances
cout_OBUF
c_1_or00001
Pins
ripple_adder
Signals
ripple_adder
Properties of Instance: c_1_or00001
Name | Value
Type | lut3
Instance Name | c_1_or00001
Console Errors Warnings Find in Files Results View by Category

بخش دوم

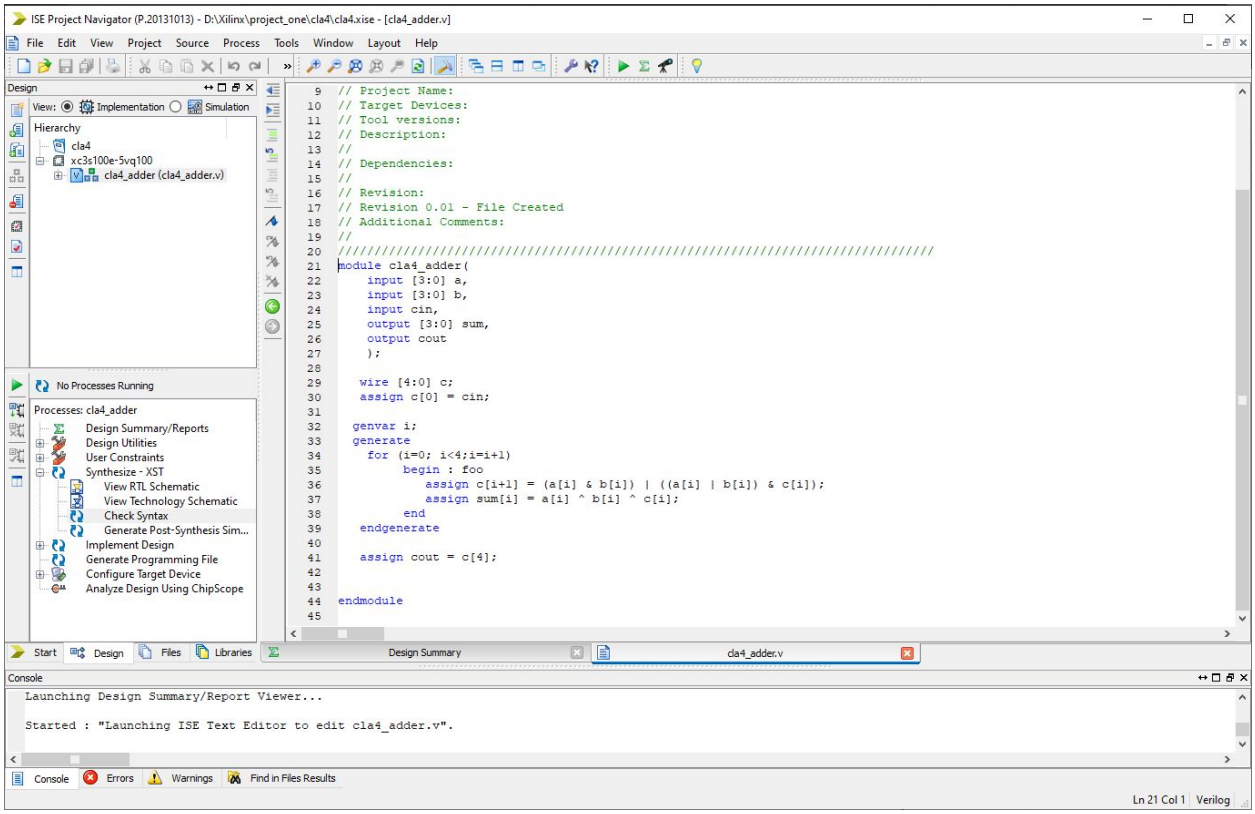
می‌دانیم:

$$C_{i+1} = G_i + P_i C_i$$
$$P_i = A_i + B_i$$
$$G_i = A_i B_i$$

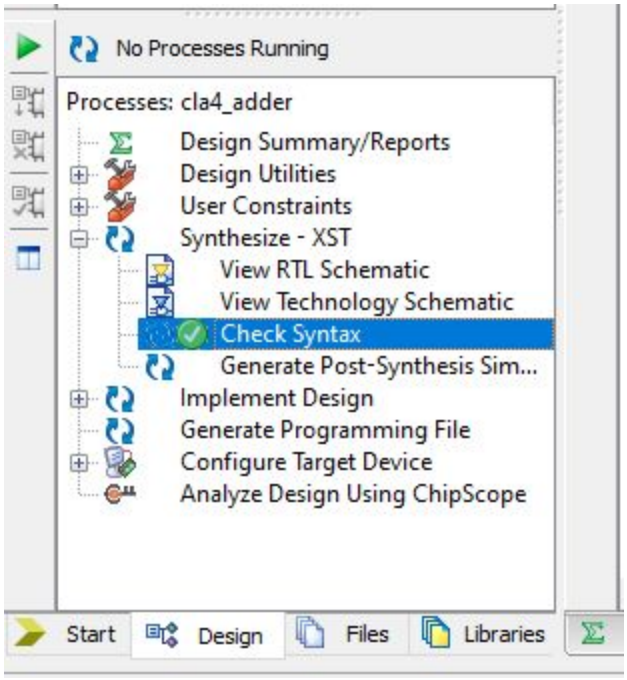
پس داریم:

$$C_{i+1} = A_i B_i + (A_i + B_i) C_i$$

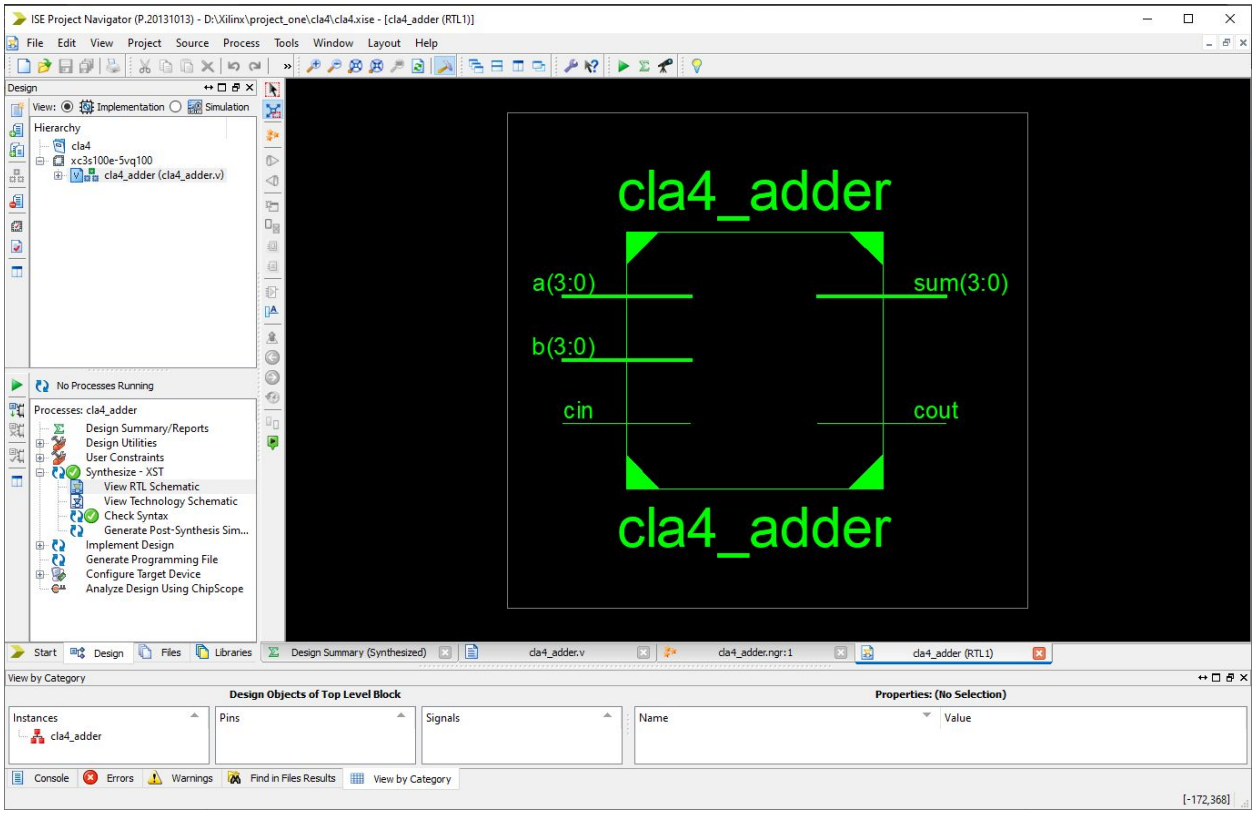
الف)

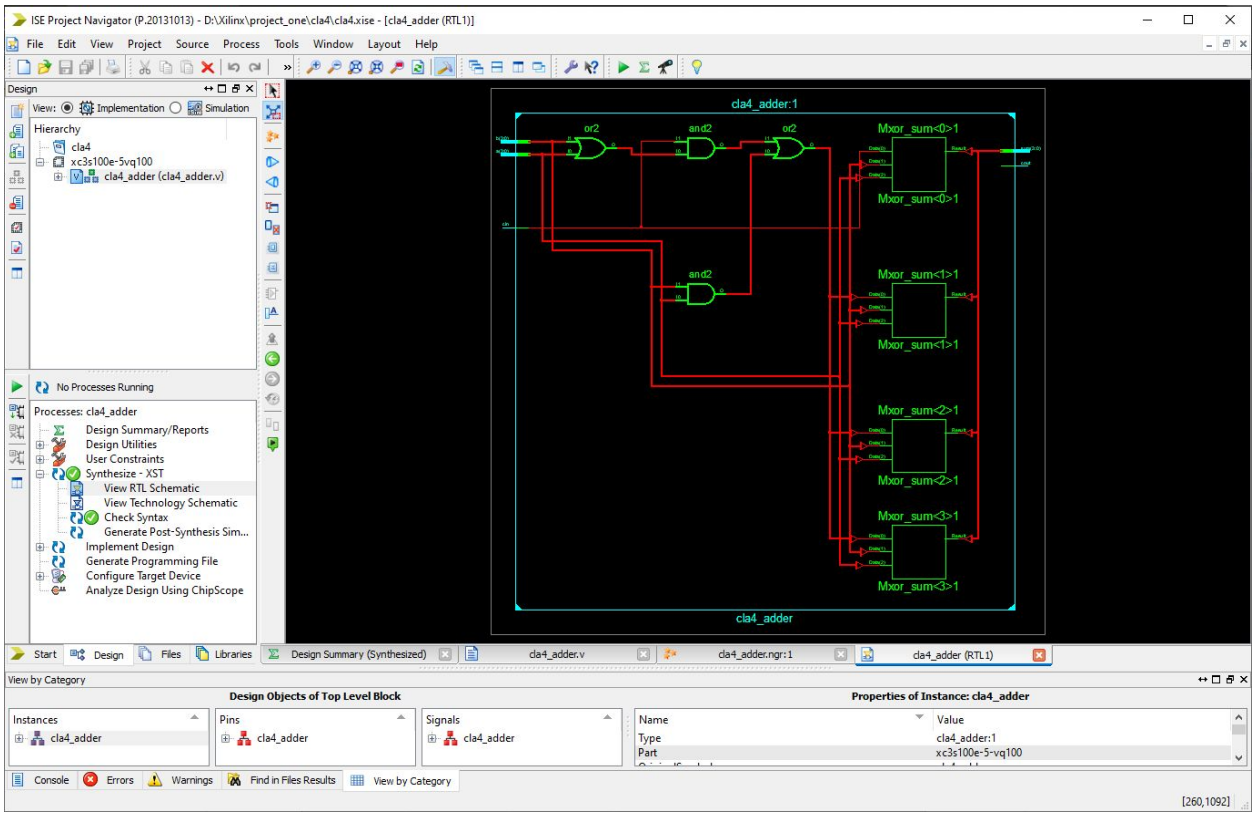


ب)

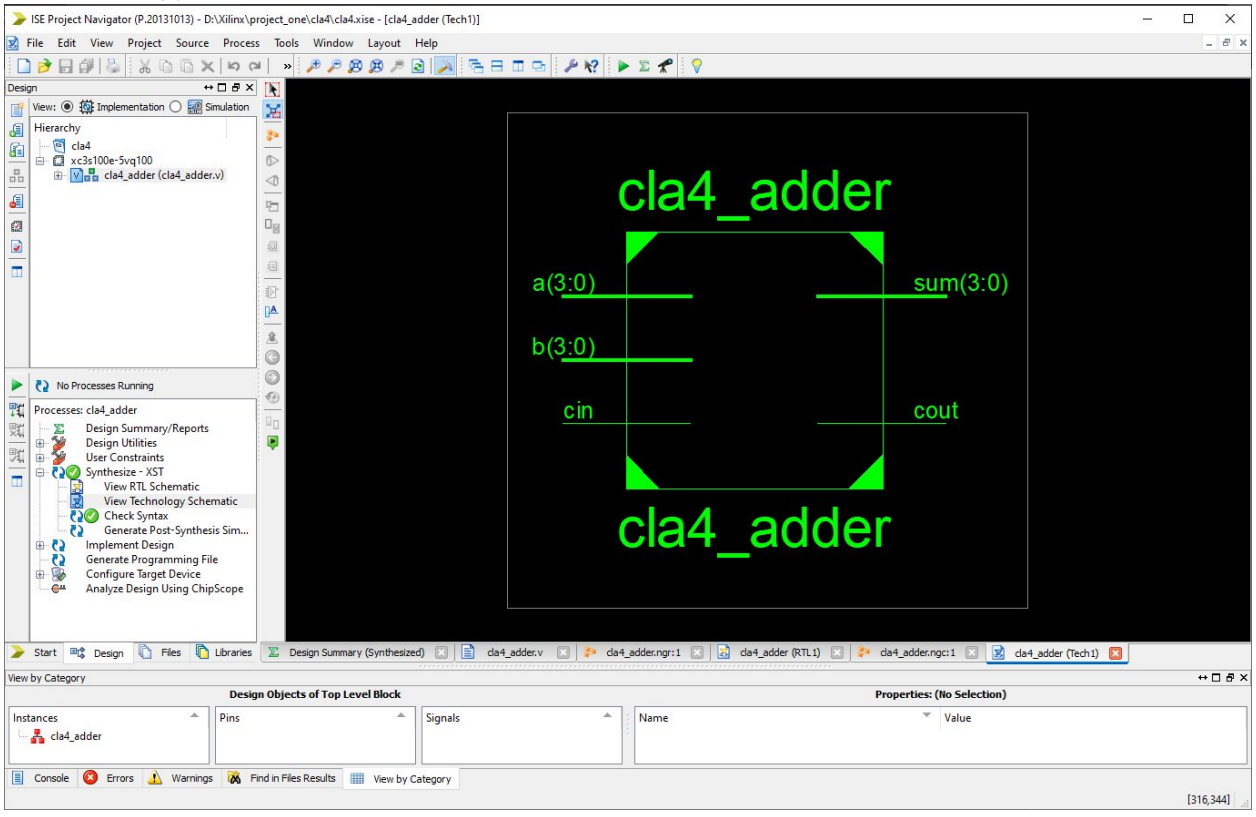


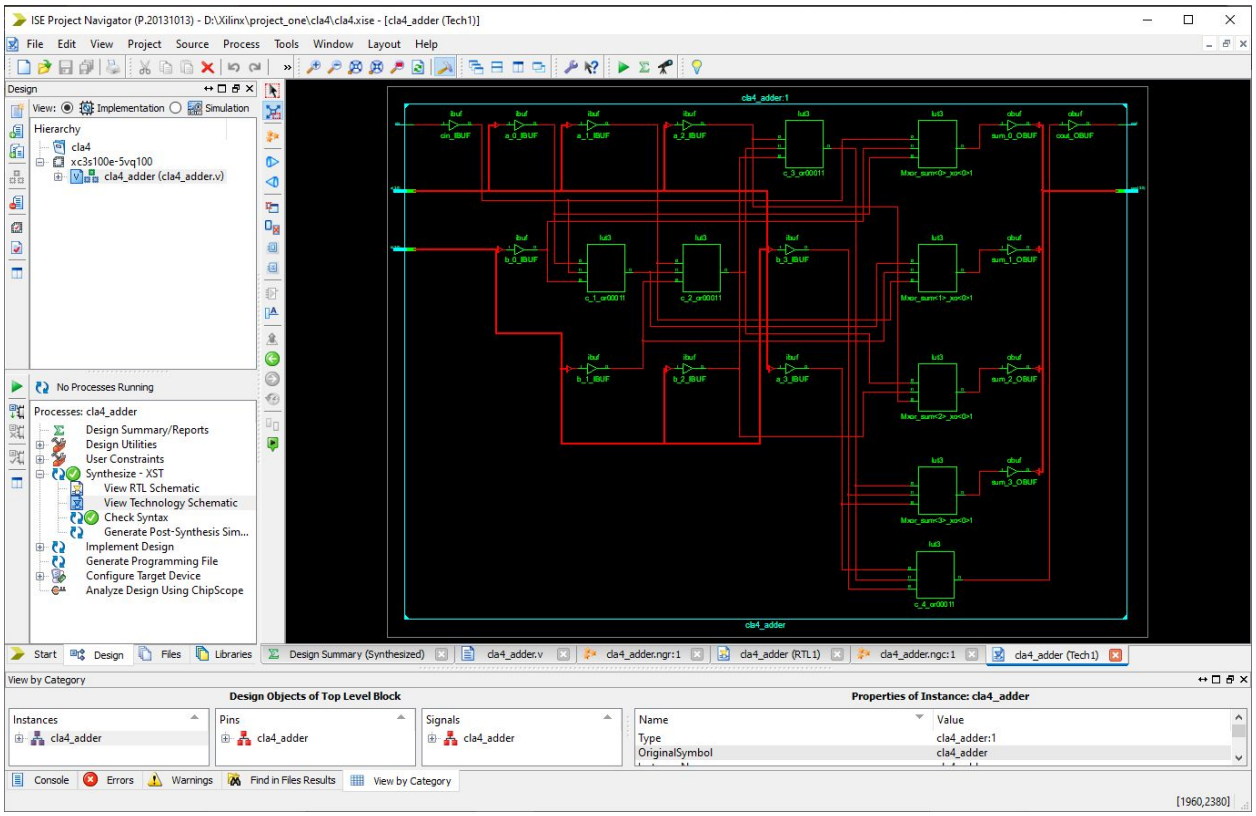
پ) RTL Schematic:



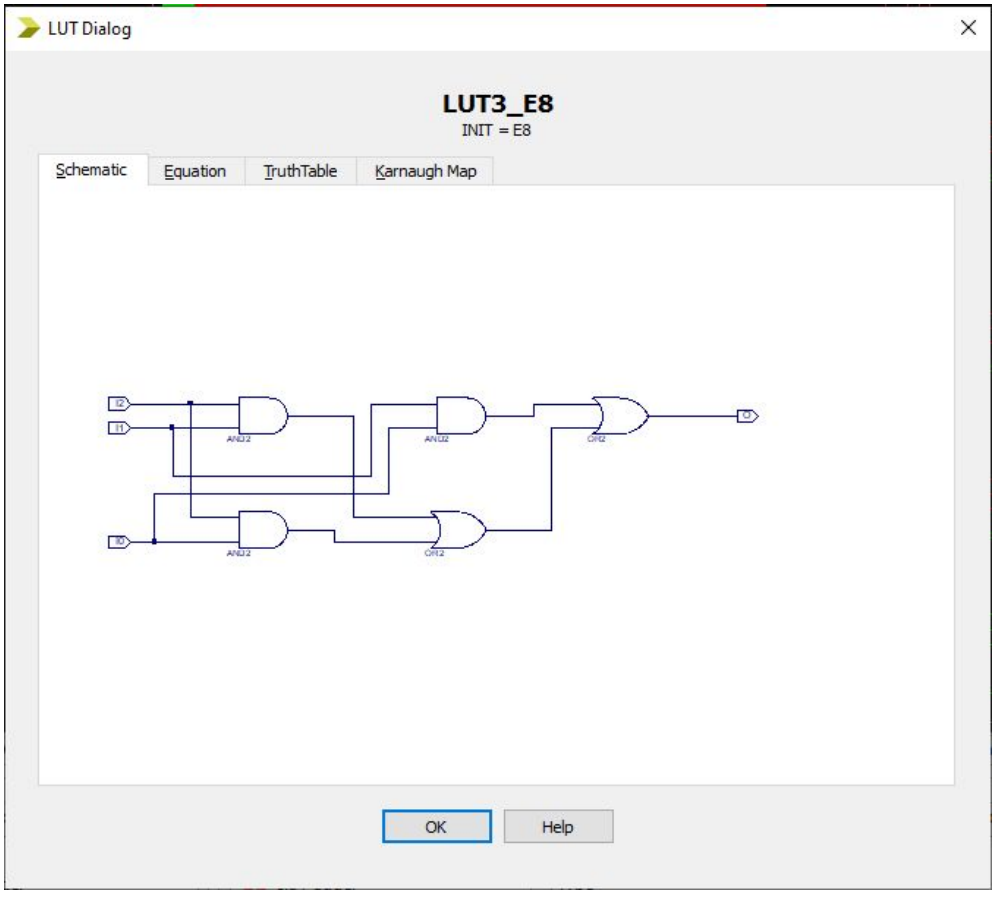


Technology Schematic:




ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\cla4\cla4.xise - [cla4_adder (Tech1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
cla4
xc3s100e-5vq100
cla4_adder (cla4_adder.v)
No Processes Running
Processes: cla4_adder
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Sim...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
cla4_adder:1
cla4_adder
Start Design Files Libraries Design Summary (Synthesized) cla4_adder.v cla4_adder.ngr:1 cla4_adder (RTL:1) cla4_adder.ngc:1 cla4_adder (Tech1)
View by Category
Design Objects of Top Level Block
Instances
cla4_adder
Pins
cla4_adder
Signals
cla4_adder
Properties of Instance: cla4_adder
Name
Value
Type
cla4_adder:1
OriginalSymbol
cla4_adder
Console Errors Warnings Find in Files Results View by Category
[1960,2380]

ت)


LUT Dialog
LUT3_E8
INIT = E8
Schematic
Equation
TruthTable
Karnaugh Map
I2
I1
I0
AND2
AND2
OR2
AND2
OR2
O
OK
Help


LUT Dialog

LUT Dialog

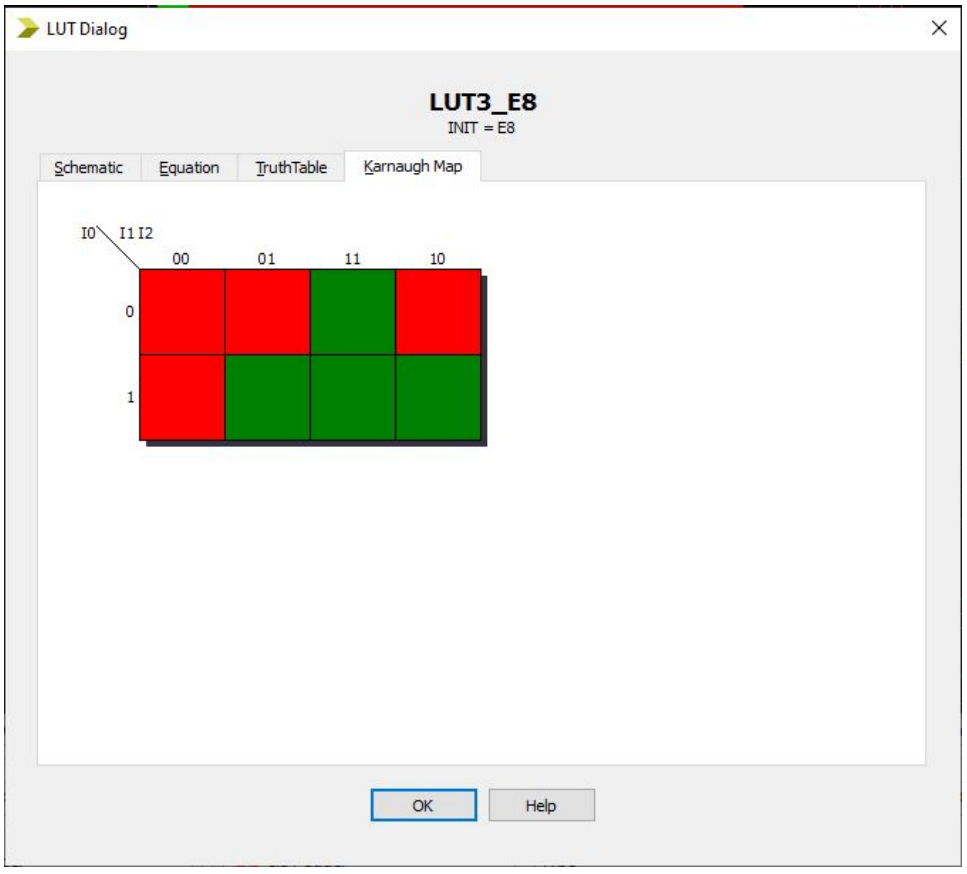
LUT3_E8

INIT = E8

Schematic | Equation | TruthTable | Karnaugh Map

I2	I1	I0	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

OK | Help



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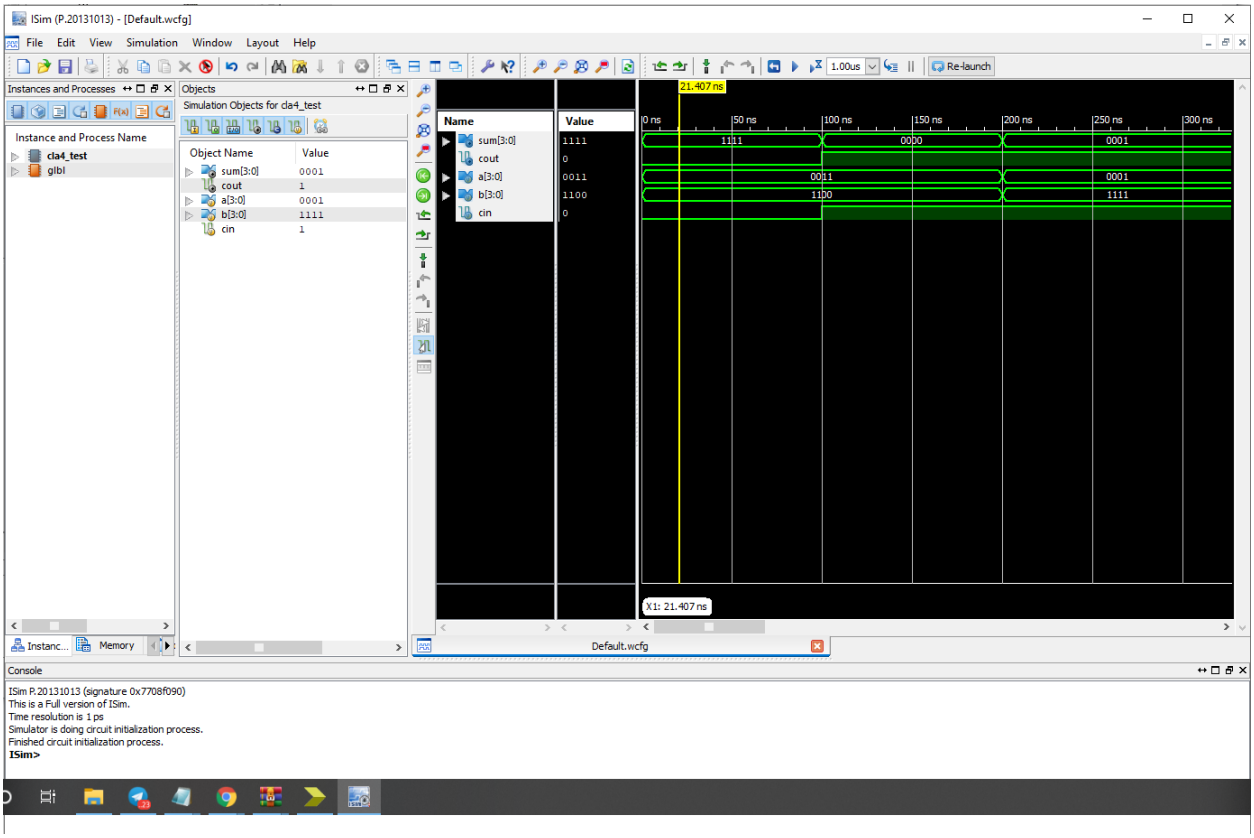
Pad to Pad

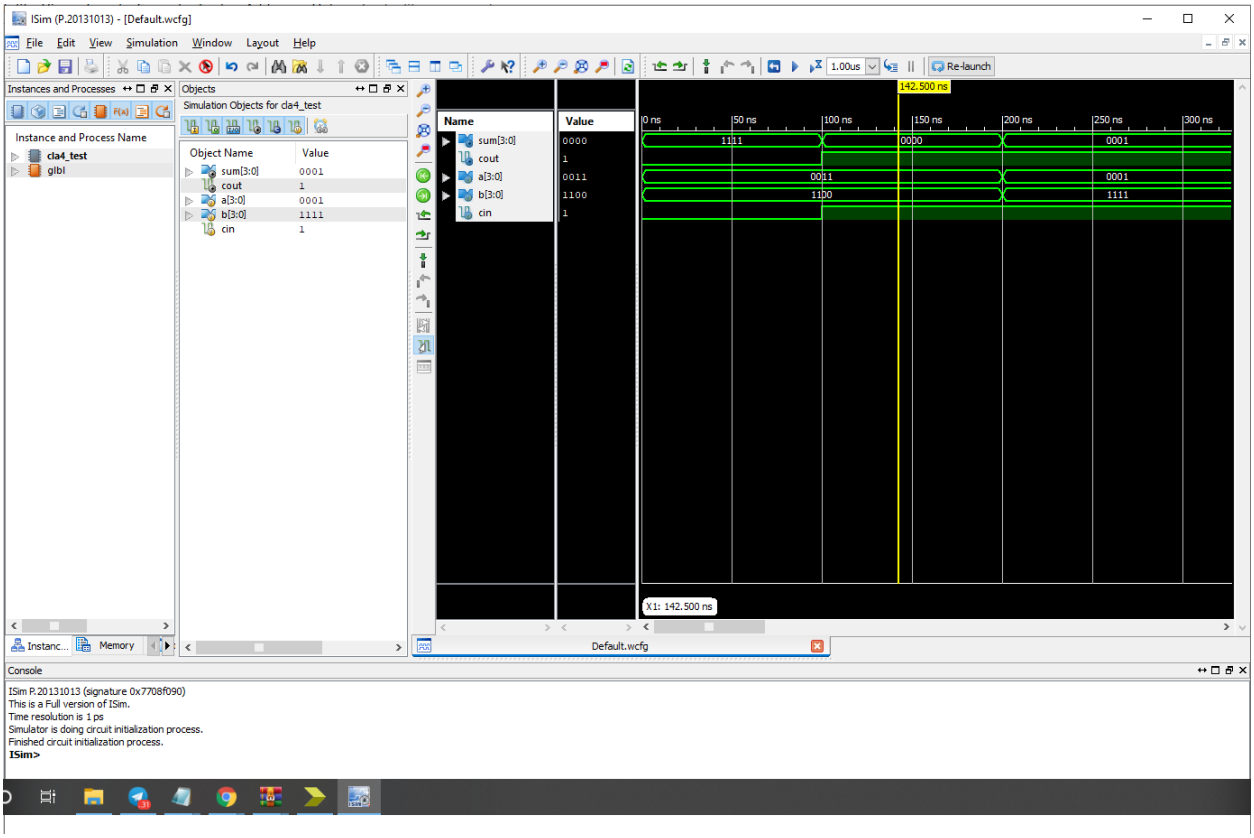
Source Pad	Destination Pad	Delay
a<0>	cout	8.381
a<0>	sum<0>	5.692
a<0>	sum<1>	7.003
a<0>	sum<2>	7.996
a<0>	sum<3>	8.744
a<1>	cout	7.626
a<1>	sum<1>	6.226
a<1>	sum<2>	7.241
a<1>	sum<3>	7.989
a<2>	cout	6.245
a<2>	sum<2>	5.860
a<2>	sum<3>	6.608
a<3>	cout	5.934
a<3>	sum<3>	6.141
b<0>	cout	8.146
b<0>	sum<0>	5.765
b<0>	sum<1>	6.768
b<0>	sum<2>	7.761
b<0>	sum<3>	8.509
b<1>	cout	7.903
b<1>	sum<1>	6.469
b<1>	sum<2>	7.518
b<1>	sum<3>	8.266
b<2>	cout	6.393
b<2>	sum<2>	6.008
b<2>	sum<3>	6.756
b<3>	cout	5.725
b<3>	sum<3>	6.077
cin	cout	8.623
cin	sum<0>	6.340
cin	sum<1>	7.245
cin	sum<2>	8.238
cin	sum<3>	8.986

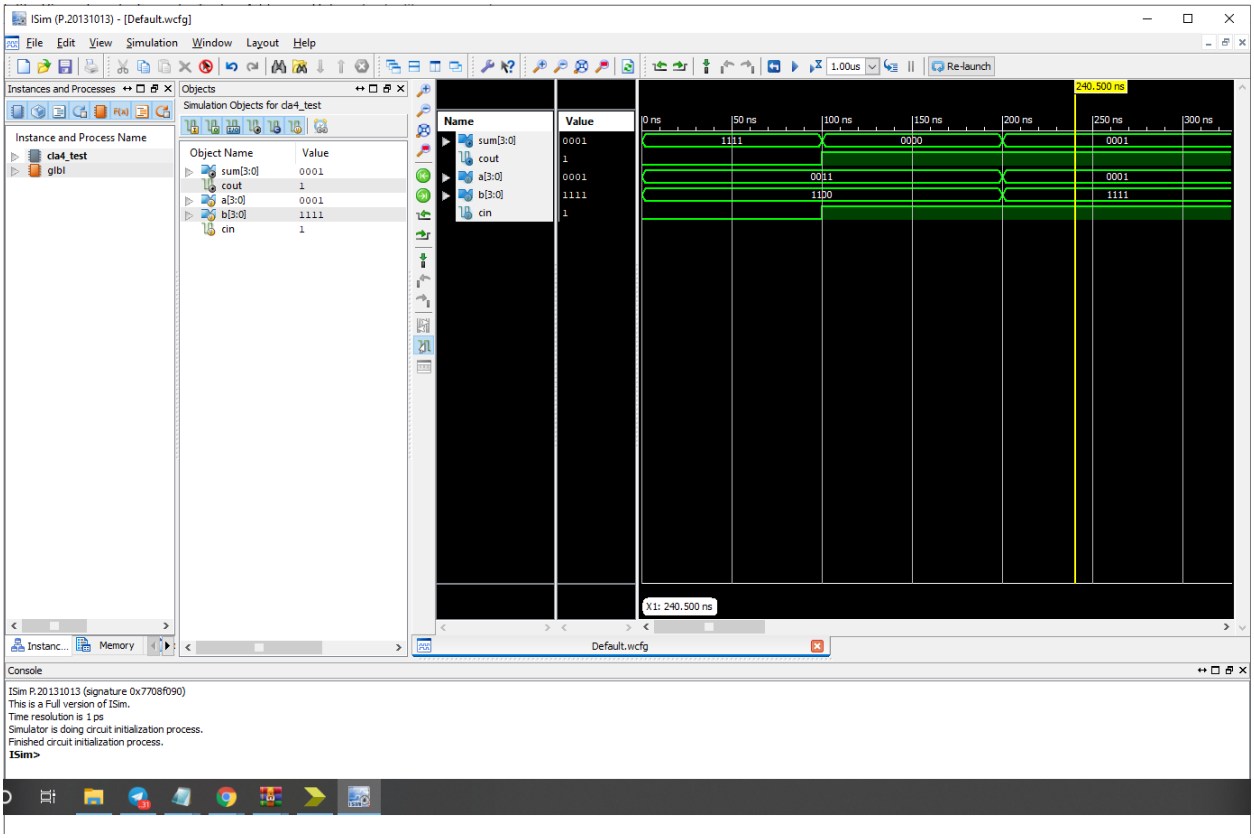
ج)

ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\cla4\cla4.xise - [cla4_test.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
cla4
xc3s100e-5vq100
cla4_test (cla4_test.v)
No Processes Running
Processes: cla4_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//
module cla4_test;
// Inputs
reg [3:0] a;
reg [3:0] b;
reg cin;
// Outputs
wire [3:0] sum;
wire cout;
// Instantiate the Unit Under Test (UUT)
cla4_adder uut (
.a(a),
.b(b),
.cin(cin),
.sum(sum),
.cout(cout)
);
initial begin
a = 4'b0011; b = 4'b1100; cin = 1'b0; #100;
a = 4'b0011; b = 4'b1100; cin = 1'b1; #100;
a = 4'b0001; b = 4'b1111; cin = 1'b1; #100;
end
endmodule
Start Design Files Libraries
Design Summary (Synthesized)
cla4_adder.v
cla4_adder.ngr:1
cla4_adder (RTL1)
cla4_adder.ngc:1
cla4_adder (Tech1)
cla4_test.v
View by Category
Design Objects of Top Level Block
Properties of Instance: c_1_or00011
Instances
cout_OBUF
c_1_or00011
Pins
cla4_adder
Signals
cla4_adder
Name
Value
Type
lut3
Instance Name
c_1_or00011
Console
Errors
Warnings
Find in Files Results
View by Category
Ln 25 Col 1
Verilog

ج)


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
cla4_test
glbl
Objects
Simulation Objects for cla4_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name Value
sum[3:0] 1111
cout 0
a[3:0] 0011
b[3:0] 1100
cin 0
21.407 ns
0 ns 50 ns 100 ns 150 ns 200 ns 250 ns 300 ns
1111 0000 0001
0011 0001
1100 1111
X1: 21.407 ns
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
cla4_test
glbl
Objects
Simulation Objects for cla4_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name Value
sum[3:0] 0000
cout 1
a[3:0] 0011
b[3:0] 1100
cin 1
142.500 ns
0 ns 50 ns 100 ns 150 ns 200 ns 250 ns 300 ns
1111 0000 0001
0011 0001
1100 1111
X1: 142.500 ns
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
cla4_test
glbl
Objects
Simulation Objects for cla4_test
Object Name Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
Name
Value
sum[3:0] 0001
cout 1
a[3:0] 0001
b[3:0] 1111
cin 1
0 ns 50 ns 100 ns 150 ns 200 ns 250 ns 300 ns
240.500 ns
1111 0000 0001
0011 0001
1100 1111
X1: 240.500 ns
Instanc... Memory
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>

ISE Project Navigator (P.20131013) - D:\Xilinx\project_one\cla4\cla4.xise - [Design Summary (Implemented)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
cla4
xc3s100e-5vq100
cla4_adder (cla4_adder.v)
cla4_test.bmm
No Processes Running
Processes: cla4_adder
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Sim...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Translation Report
Map Report
Place and Route Report
Post-PAR Static Timing Report
Power Report
Bitgen Report
Secondary Reports
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
cla4_adder Project Status (02/23/2021 - 22:26:26)
Project File: cla4.xise
Parser Errors: No Errors
Module Name: cla4_adder
Implementation State: Placed and Routed
Target Device: xc3s100e-5vq100
•Errors: No Errors
Product Version: ISE 14.7
•Warnings: No Warnings
Design Goal: Balanced
•Routing Results: All Signals Completely Routed
Design Strategy: Xilinx Default (unlocked)
•Timing Constraints:
Environment: System Settings
•Final Timing Score: 0 (Timing Report)
Device Utilization Summary
Logic Utilization | Used | Available | Utilization | Note(s)
Number of 4 input LUTs | 8 | 1,920 | 1%
Number of occupied Slices | 6 | 960 | 1%
Number of Slices containing only related logic | 6 | 6 | 100%
Number of Slices containing unrelated logic | 0 | 6 | 0%
Total Number of 4 input LUTs | 8 | 1,920 | 1%
Number of bonded IOBs | 14 | 66 | 21%
Average Fanout of Non-Clock Nets | 1.71
Performance Summary
Final Timing Score: 0 (Setup: 0, Hold: 0)
Pinout Data: Pinout Report
Routing Results: All Signals Completely Routed
Clock Data: Clock Report
Timing Constraints:
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Feb 23 22:12:32 2021 | 0 | 0 | 0
Start Design Files Libraries Design Summary (Implemented) cla4_adder.v cla4_adder.ngr:1 cla4_adder (RTL) cla4_adder.ngc:1 cla4_adder (Tech) cla4_test.v
View by Category
Design Objects of Top Level Block
Instances
cout_OBUF
c_1_or00011
Pins
cla4_adder
Signals
cla4_adder
Properties of Instance: c_1_or00011
Name | Value
Type | lut3
Instance Name | c_1_or00011
Console Errors Warnings Find in Files Results View by Category

بخش سوم:

از آن جا که در هنگام نوشتن کد Verilog به صورت Data flow کامپایلر و یا Xilinx ISE خود اقدام به تعیین و بهبود کد ما می‌کند، در این جا در هر دو نوع CLA و Ripple Adder زمان تاخیر یکسان شده این به دلیل آن است که به احتمال زیاد Xilinx ISE کد ما را به یک صورت سنتز کرده است.

این در حالی است که به لحاظ تئوری میدانیم که در Ripple Adder ، تاخیر بیشتر و گیت ها و در نتیجه منابع مورد استفاده کمتر و در CLA تاخیر کمتر و منابع مورد استفاده بیشتر است.