Design of an SPI interface

to load data from external registers to internal register

Submitted by
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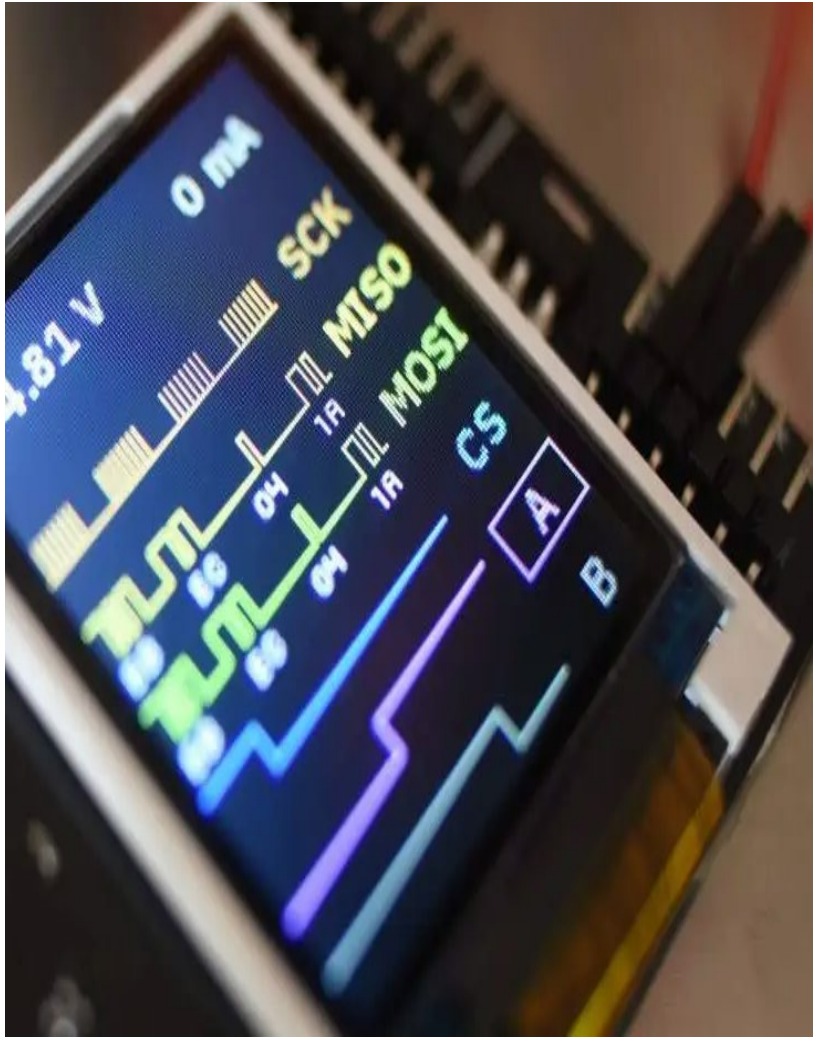
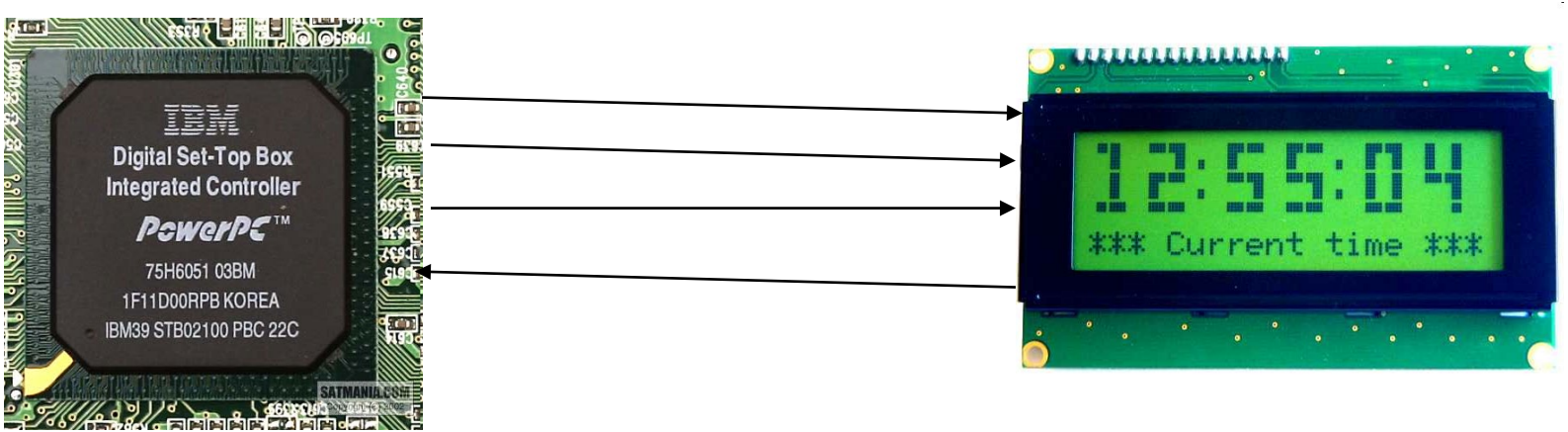


Objectives

1. Get familiar with digital design process of Serial Peripheral Interface.
2. Writing hierarchical RTL code for SPI master-slave interface.
3. Verifying RTL code with test bench.
4. Performing RTL synthesis of the RTL code.
5. Analyzing reports consists of area, time and power.
6. Performing Place and Route (PnR) of synthesized code.
7. Analyzing best PPA (Power Performance Area) on the design.
8. Performing Design Rule Check on the design.

What is SPI?

- Serial bus protocol
- Fast, easy to use, and simple
- Very widely used
- Not “standardized”



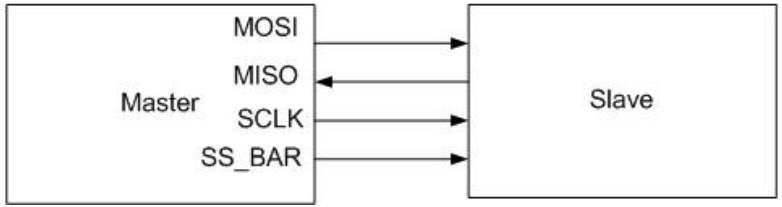
SPI Basics

- A 4-wire communications bus
- Typically communicate across short distances
    - Single Master
    - Multiple Slaves
- Synchronized
    - Communications are “clocked”

SPI Capabilities

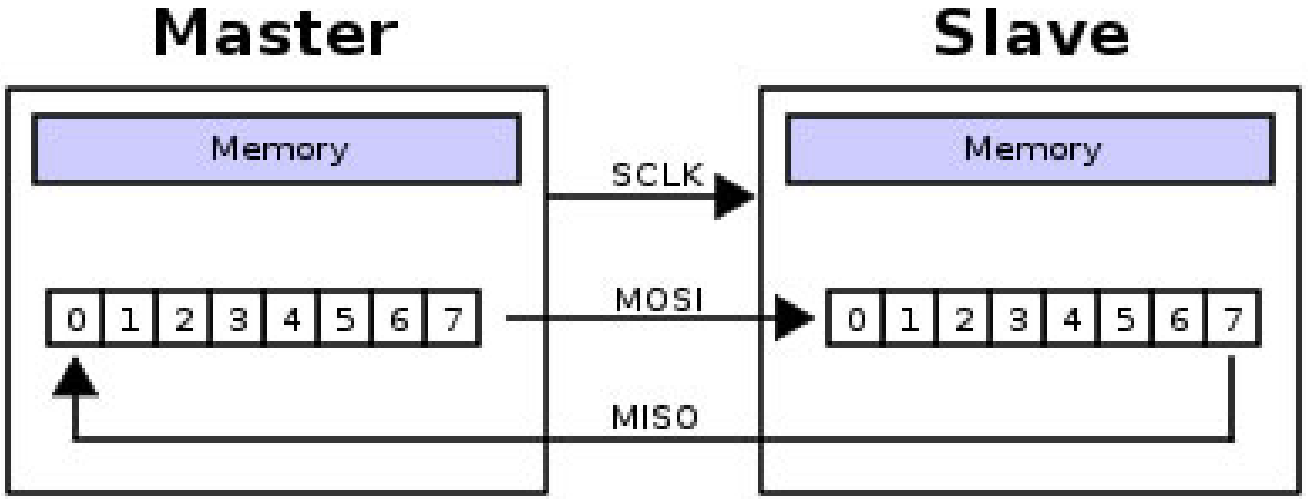
- Always full-duplex
  - Communicates in both directions simultaneously
  - Transmitted (or received) data may not be meaningful
- Multiple Mbps transmission speeds
  - 0-50 MHz clock speeds not uncommon
- Transfer data in 4 to 16 bit characters
- Supports multiple slaves

SPI bus wiring



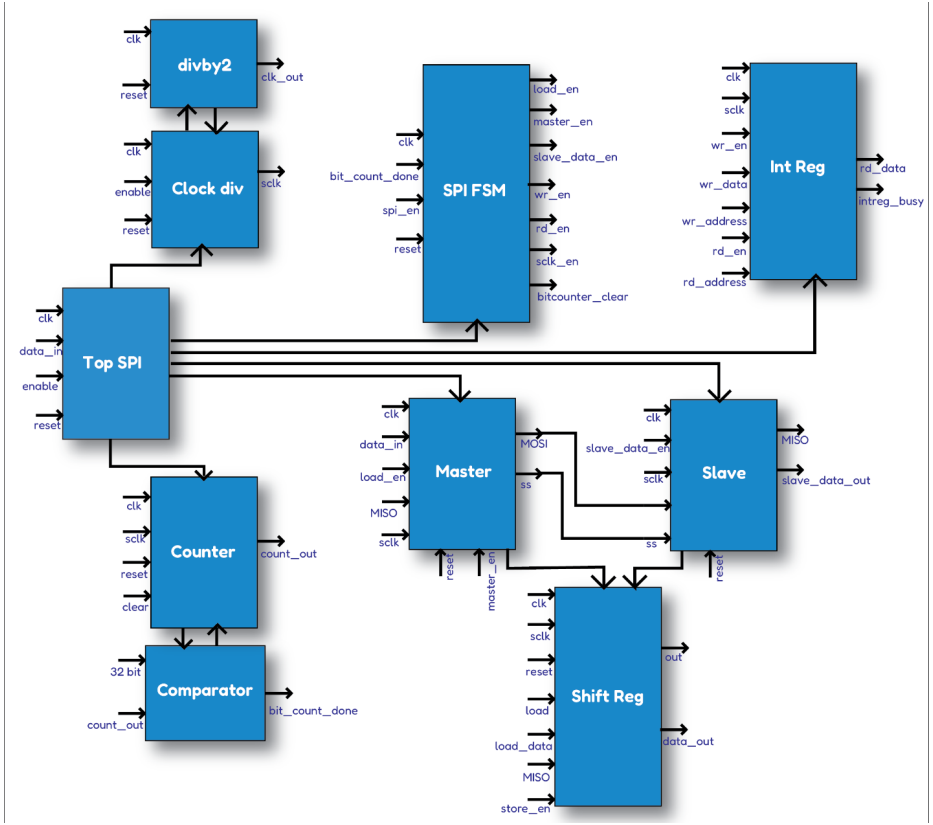
- Bus wires
  - Master-Out, Slave-In (MOSI)
  - Master-In, Slave-Out (MISO)
  - System Clock (SCLK)
  - Slave Select/Chip Select
- Master asserts slave/chip select line
- Master generates clock signal
- Shift registers shift data in and out

SPI uses a “shift register” model of communications

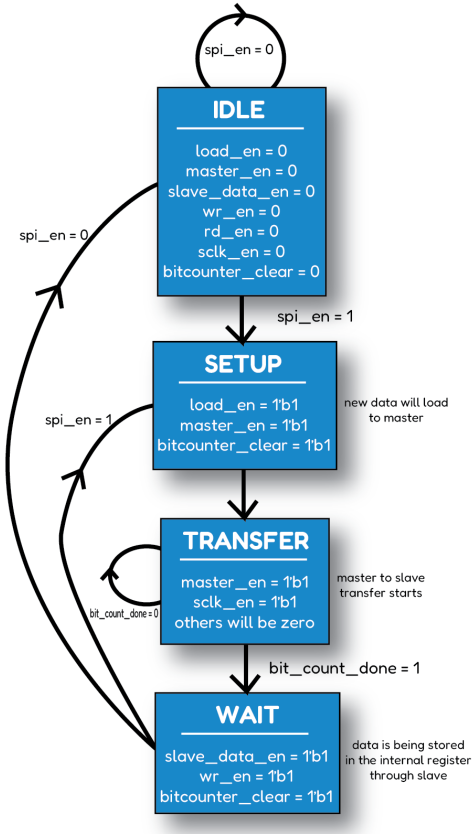


Master shifts out data to Slave, and shifts in data from Slave

Block Diagram of the overall RTL Code



Block Diagram of Master FSM



Verification Procedure : Compilation

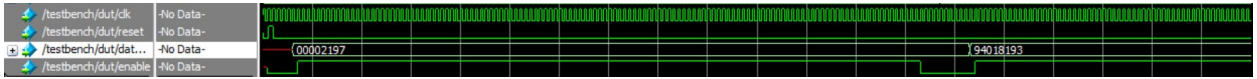
```
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog clockdiv.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: clockdiv.v
        module digital_lib.clockdiv
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog ncvlog comparator.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
ncvlog: *E,COFILE: cannot open source file 'ncvlog'.
file: comparator.v
        module digital_lib.comparator
                errors: 0, warnings: 0
        Total errors/warnings found outside modules and primitives:
                errors: 1, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog comparator.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: comparator.v
        module digital_lib.comparator
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog counter.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: counter.v
        module digital_lib.counter
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog divby2.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: divby2.v
        module digital_lib.divby2
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog intreg.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: intreg.v
        module digital_lib.intreg
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog master.v
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog master.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: master.v
        module digital_lib.master
                errors: 0, warnings: 0
```

```
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog shiftreg.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: shiftreg.v
        module digital_lib.shiftreg
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog slave.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: slave.v
        module digital_lib.slave
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog spifsm.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: spifsm.v
        module digital_lib.spifsm
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog topspi.v -message
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: topspi.v
        module digital_lib.topspi
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncvlog testbench.v -MESS
ncvlog(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
file: testbench.v
        module digital_lib.testbench
                errors: 0, warnings: 0
[vlsi10@CadenceServer3 ~/Peace]$ ncelab testbench
ncelab(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
        $readmemh("TestData.txt", testdata);
```

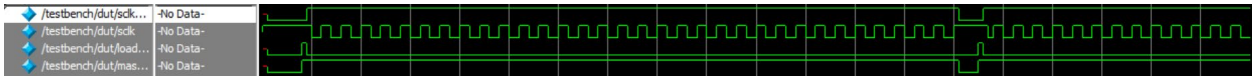
Verification Procedure : Elaboration

```
[vlsi10@CadenceServer3 ~/Peace]$ ncelab testbench
ncelab(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
        $readmemh("TestData.txt", testdata);
                                  |
ncelab: *W,MEMODR (./testbench.v,25|34): $readmem default memory order incompatible with IEEE1364.
[vlsi10@CadenceServer3 ~/Peace]$ ncsim testbench
ncsim(64): 15.10-s015: (c) Copyright 1995-2016 Cadence Design Systems, Inc.
ncsim> run
Simulation complete via $finish(1) at time 11060 NS + 0
./testbench.v:58        $finish;
ncsim> exit
```

Verification Procedure : Simulation Waveform



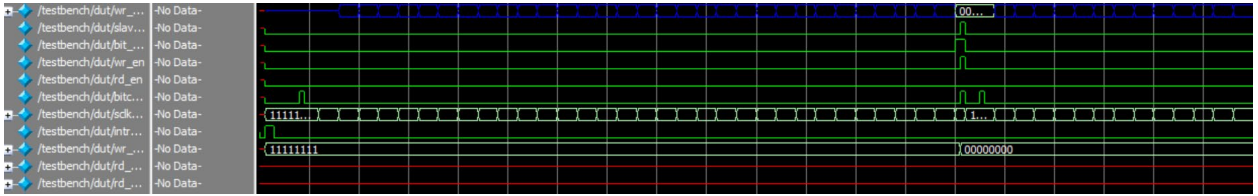
(Clock, Reset, data_in and enable signals)



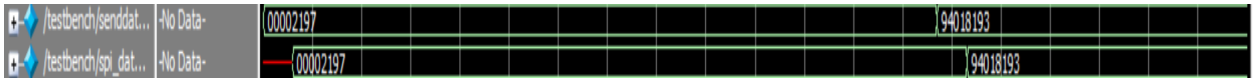
(Sclk_en, sclk, load_en and mater_en signals)

(miso, mosi and ss signals)

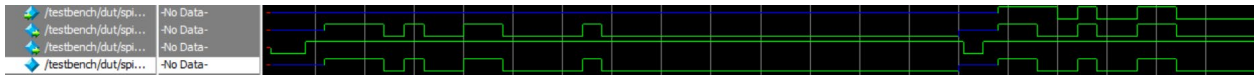
Verification Procedure : Simulation Waveform



(write_data, slave_data_en, bit_count_done, wr_en, rd_en, bitcounter_clear, sclk_en, intregbusy, wr_data, rd_data signals)

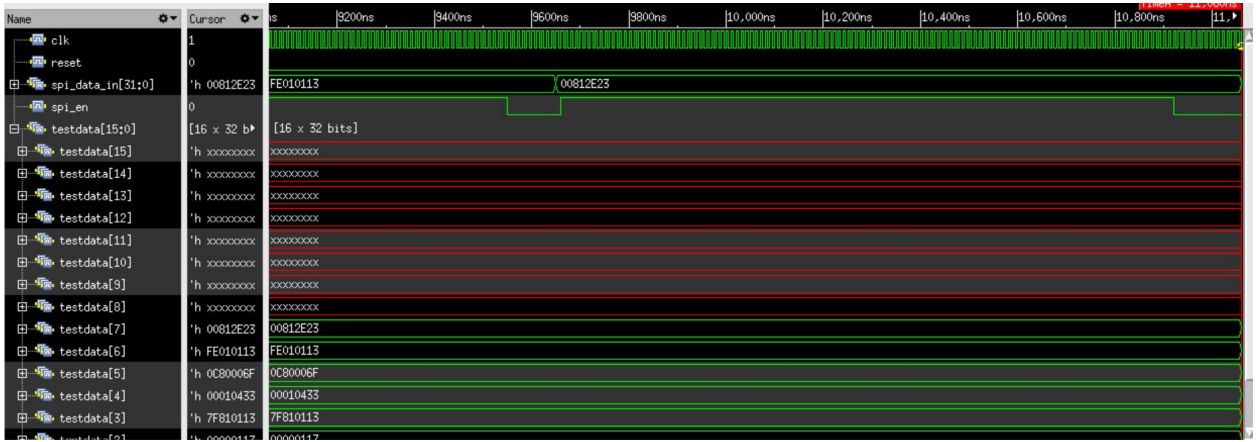


(send data and transmitted data to slave signals)



(master out signal transmitted to mosi signal)

Verification Procedure : Simulation Waveform



(Simulation Waveform on Cadence nclaunch)

RTL Synthesis - SDC Code:

```
# setting up time units
set_units -time 1ns -capacitance pF
# setting the clock period 10ns, as period = 1/freq,
here, freq = 100MHz
set clock_period 10;
set top_module "topspi_syn"
set clock_port {clk};
set reset_port {reset;
# setting the input ports in a list to a variable
set input_ports {data_in,enable} ;
# setting the output ports in a list to a variable
set output_ports {bit_count_done,sclk_en} ;
# define the clocks
create_clock -period ${clock_period} -waveform {0
6} -name func_clk
[get_ports ${clock_port}]
# setting up constraints for the reset signal
set_multicycle_path -setup 3 -from [get_ports
${reset_port}]
set_multicycle_path -hold 2 -from [get_ports
${reset_port}]

# Define input delays
set_input_delay 0.4 -clock [get_clocks {func_clk}]
${input_ports}
# Define output delays
set_output_delay 0.6 -clock [get_clocks {func_clk}]
${output_ports}
```

RTL Synthesis - TCL Code:

Optimized Design Parameter Definition with "medium" level synthesis:

```
set DESIGN topspi_syn
set SYN_EFF medium
set MAP_EFF medium
set OPT_EFF medium
```

Minium Supply Voltage Define:

```
slow_vdd1v0_basicCells_hvt.lib \
slow_vdd1v0_basicCells.lib \
slow_vdd1v0_basicCells_lvt.lib"
```

Load Design:

```
### Load Design
###source verilog_files.tcl
read_hdl "\
${DESIGN}.v"
elaborate $DESIGN
puts "Runtime & Memory after 'read_hdl'"
time_info Elaboration
check_design -unresolved
```

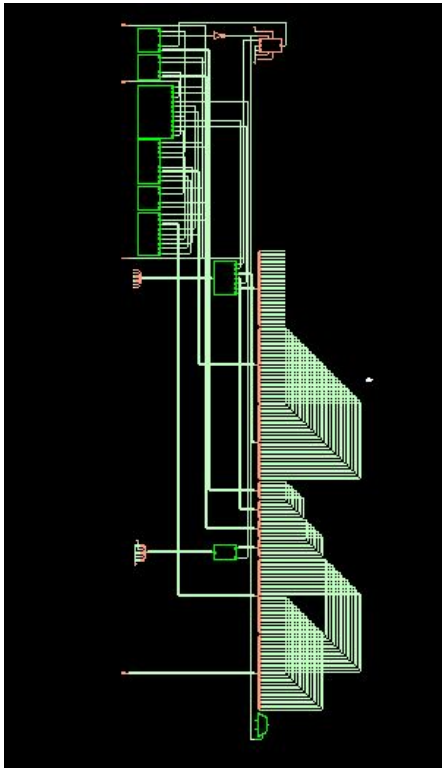
Constraints Setup:

```
read_sdc topspi_syn.sdc
report timing -encounter >> reports/${DESIGN}_pretim.rpt
 ### Synthesizing to generic
report datapath > reports/${DESIGN}_datapath_generic.rpt
generate_reports -outdir reports -tag generic
write_db -to_file ${DESIGN}_generic.db
```

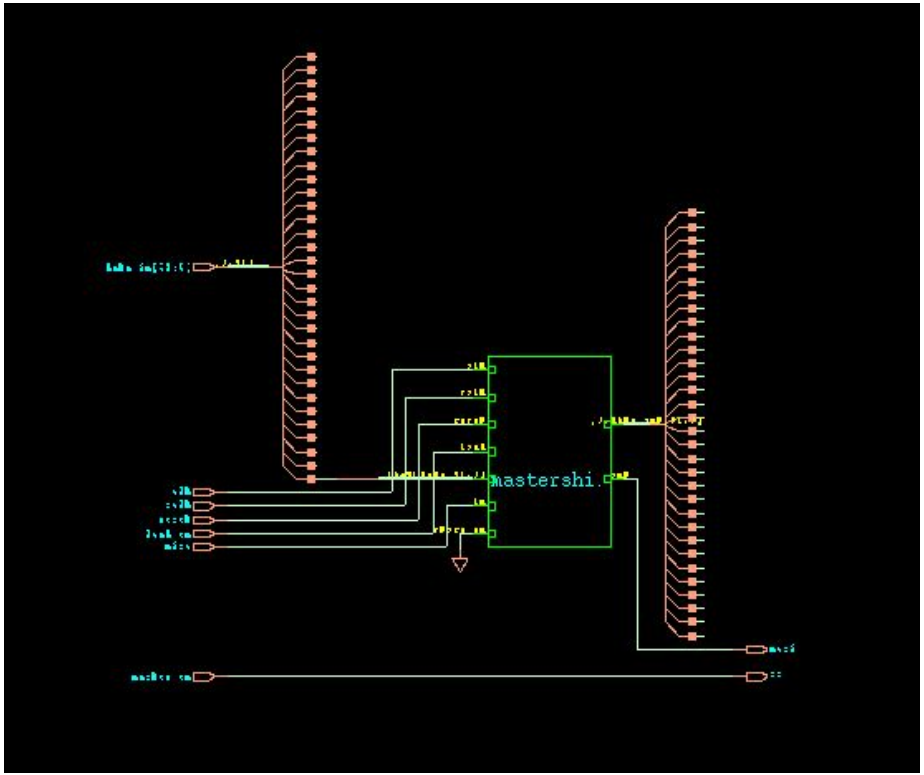
Report Timing:

```
report timing -encounter >> reports/${DESIGN}_generic.rpt
##This synthesizes your code
synthesize -to_mapped
## This writes all your files
write -mapped > topspi_synthesize.v
```

RTL Synthesis - Synthesized Circuits

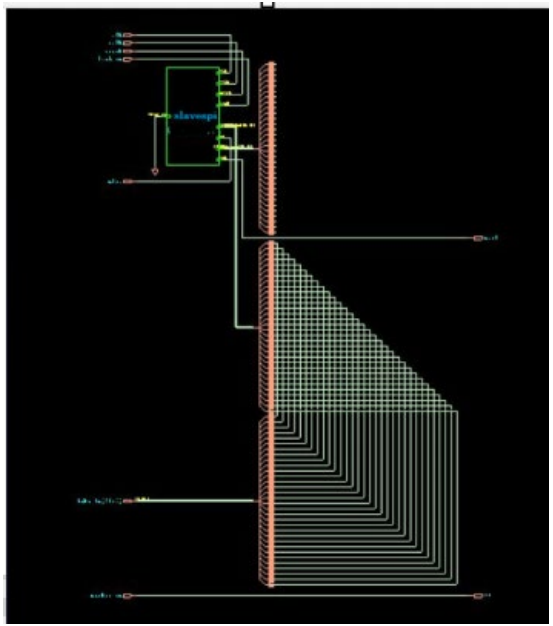


Overall Design

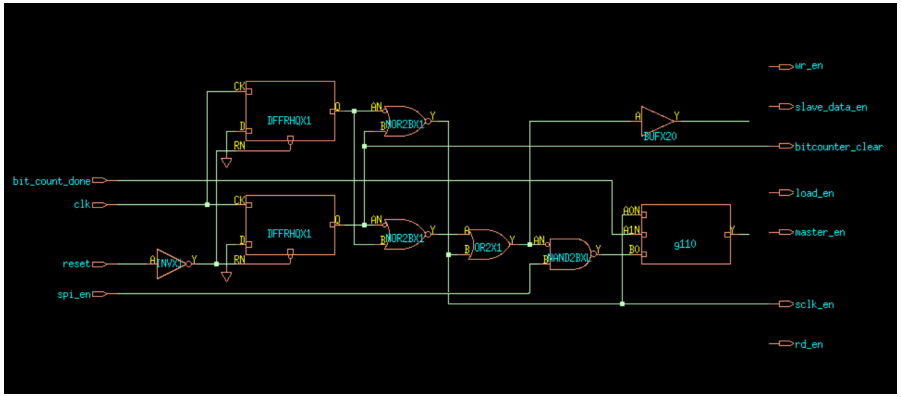


Master

RTL Synthesis - Synthesized Circuits

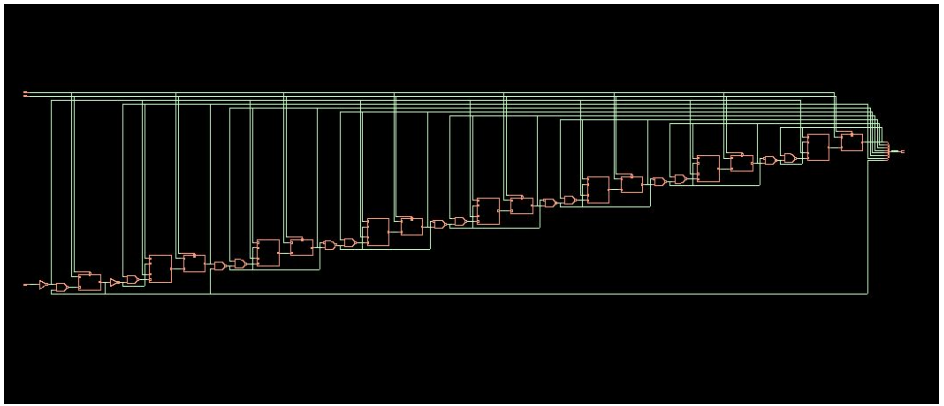


Slave

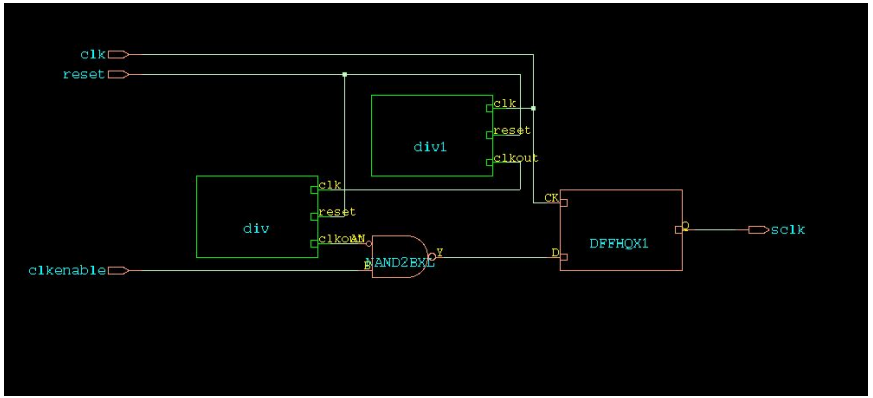


Spi fsm

RTL Synthesis - Synthesized Circuits

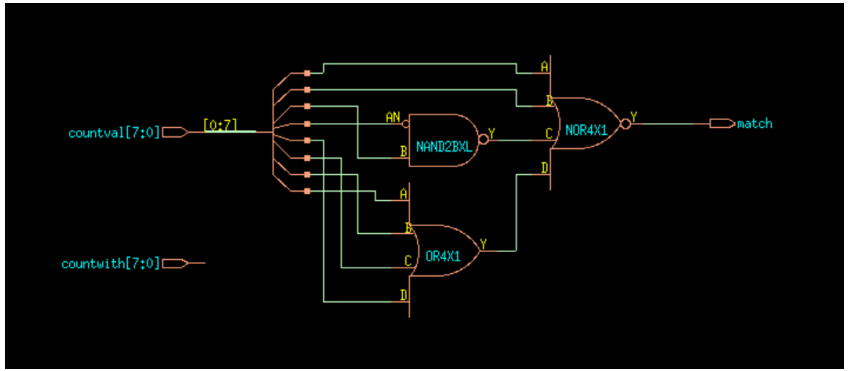


Counter

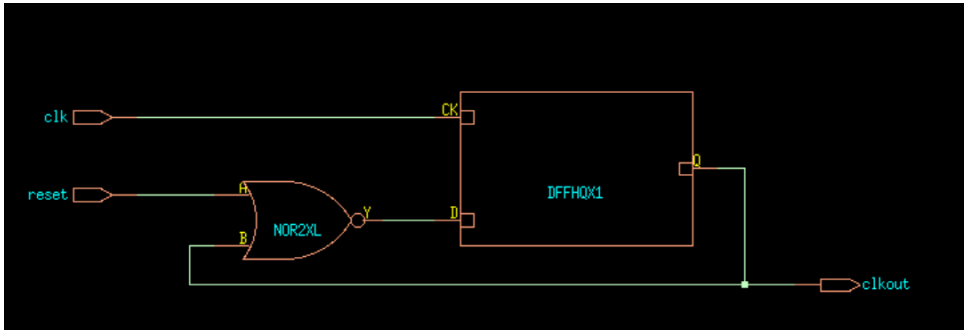


Clock Divider Circuit

RTL Synthesis - Synthesized Circuits



Comparator Block



Internal Register

RTL Synthesis : Report Analysis

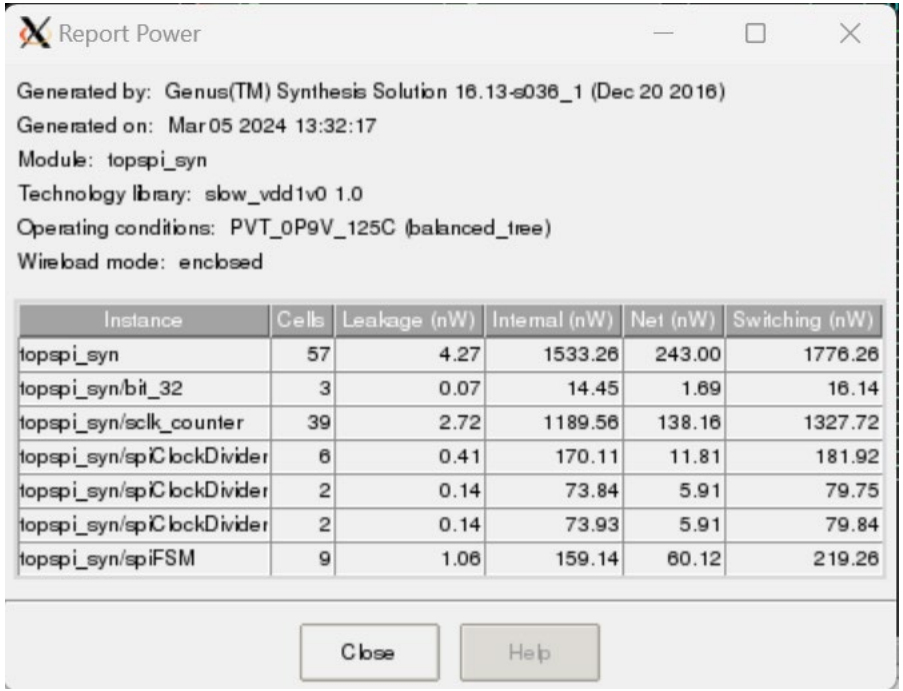
Summary Report

Generated by: Genus(TM) Synthesis Solution 16.13-s036_1 (Dec 20 2016)
Generated on: Mar 05 2024 13:43:21
Module: topspi_syn
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode: enclosed

Gate	Instances	Area	Library
BUFX20	1	8.21	slow_vdd1v0
DFFHQX1	6	32.83	slow_vdd1v0
DFFQXL	5	27.36	slow_vdd1v0
DFFRHQX1	2	12.31	slow_vdd1v0
DFFSHQX1	8	51.98	slow_vdd1v0
INVX1	3	2.05	slow_vdd1v0
NAND2BX1	1	1.37	slow_vdd1v0
NAND2BXL	8	10.94	slow_vdd1v0
NAND2XL	1	1.03	slow_vdd1v0
NOR2BX1	2	2.74	slow_vdd1v0
NOR2XL	2	2.05	slow_vdd1v0
NOR4X1	1	1.71	slow_vdd1v0
OAI2BB1X1	1	1.71	slow_vdd1v0
OR2X1	8	10.94	slow_vdd1v0
OR4X1	1	2.05	slow_vdd1v0
XNOR2X1	6	14.36	slow_vdd1v0
XOR2X1	1	2.74	slow_vdd1v0
TOTAL	57	186.38	

RTL Synthesis : Report Analysis

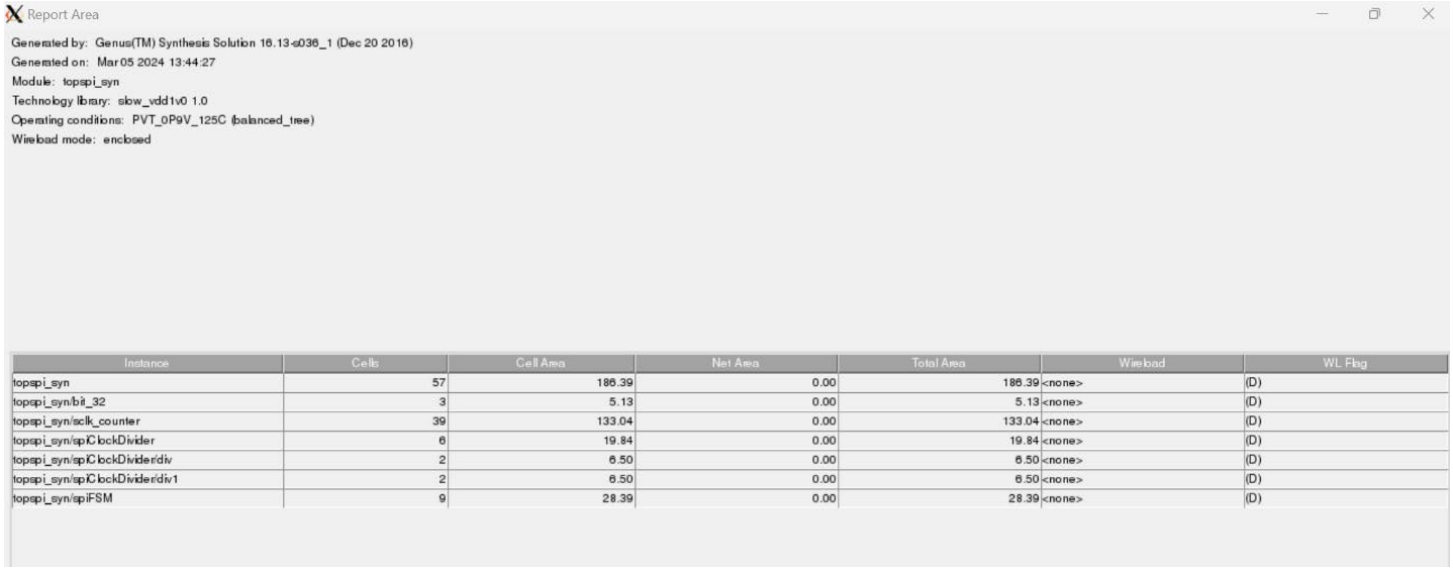
Detailed Power Report



Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
topspi_syn	57	4.27	1533.26	243.00	1776.26
topspi_syn/bit_32	3	0.07	14.45	1.69	16.14
topspi_syn/sclk_counter	39	2.72	1189.56	138.16	1327.72
topspi_syn/spiClockDivider	6	0.41	170.11	11.81	181.92
topspi_syn/spiClockDivider	2	0.14	73.84	5.91	79.75
topspi_syn/spiClockDivider	2	0.14	73.93	5.91	79.84
topspi_syn/spiFSM	9	1.06	159.14	60.12	219.26

RTL Synthesis : Report Analysis

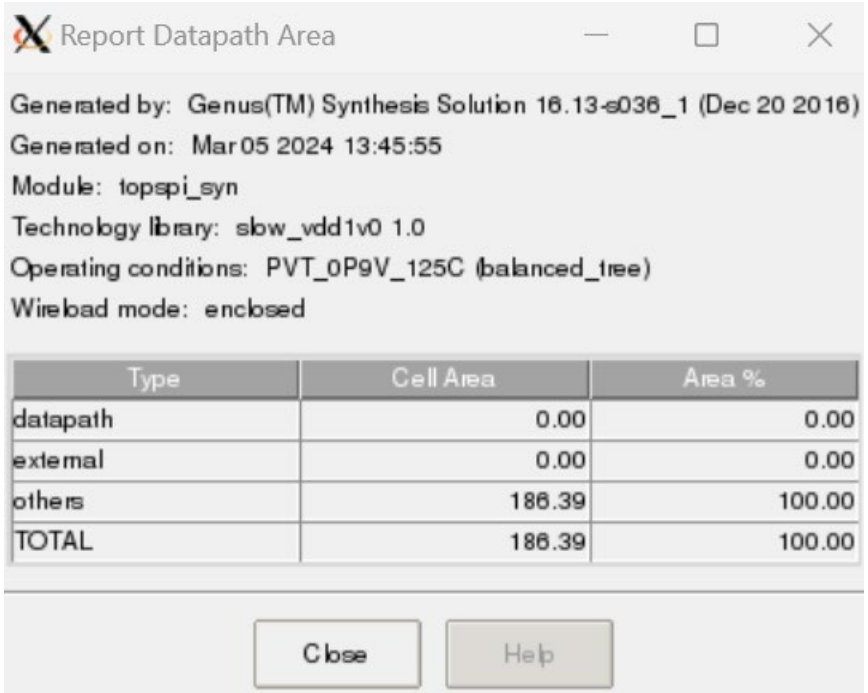
Report -Area



Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
topspi_syn	57	186.39	0.00	186.39	<none>	(D)
topspi_syn/bit_32	3	5.13	0.00	5.13	<none>	(D)
topspi_syn/sclk_counter	39	133.04	0.00	133.04	<none>	(D)
topspi_syn/spiClockDivider	6	19.84	0.00	19.84	<none>	(D)
topspi_syn/spiClockDivider/div	2	6.50	0.00	6.50	<none>	(D)
topspi_syn/spiClockDivider/div1	2	6.50	0.00	6.50	<none>	(D)
topspi_syn/spiFSM	9	28.39	0.00	28.39	<none>	(D)

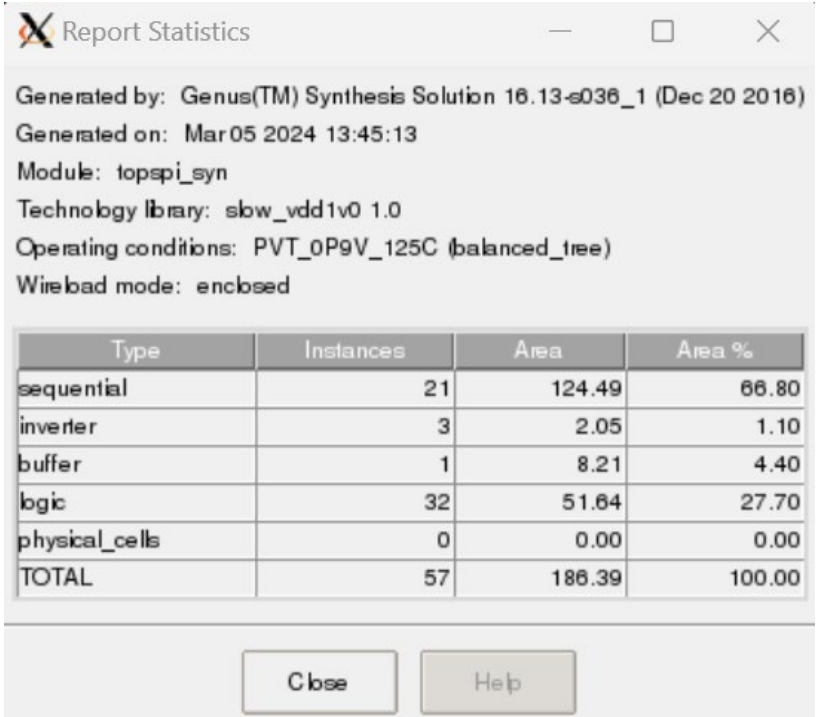
RTL Synthesis : Report Analysis

Report -Datapath



RTL Synthesis : Report Analysis

Report -Statistics



Type	Instances	Area	Area %
sequential	21	124.49	66.80
inverter	3	2.05	1.10
buffer	1	8.21	4.40
logic	32	51.64	27.70
physical_cells	0	0.00	0.00
TOTAL	57	186.39	100.00

RTL Synthesis : Report Analysis

Timing Report

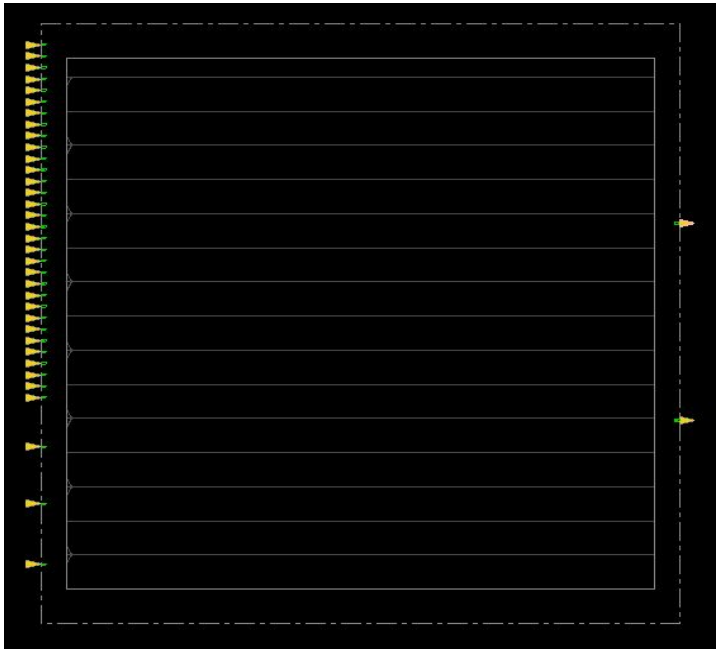
Timing Report - (id: 1)

Options | Endpoint: sclk_counter/countout_reg[7]/D | Close

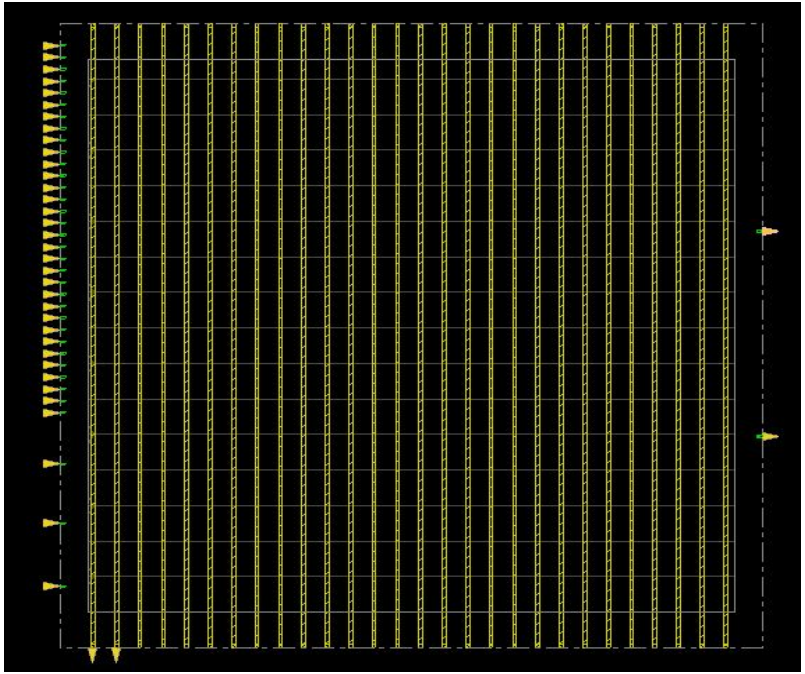
Airlines	Endpoint	Slack (ps)	Rise Slew (ps)	Fall Slew (ps)
cpath_1_1	sclk_counter/countout_reg[7]/D	uncon	24.50	26.00

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
countout_reg[1]6/CK				0.00		0.00	R
countout_reg[1]6/Q	DFFHQX1	4	1.00	21.20	173.30	173.30	R
g177/A					0.00	173.30	
g177/Y	NAND2XL	2	0.60	96.80	85.50	258.80	F
g158/AN					0.00	258.80	
g158/Y	NAND2BXL	2	0.60	97.60	135.50	394.30	F
g155/AN					0.00	394.30	
g155/Y	NAND2BXL	2	0.60	97.60	135.80	530.10	F
g152/AN					0.00	530.10	
g152/Y	NAND2BXL	2	0.60	97.60	135.80	665.90	F
g149/AN					0.00	665.90	
g149/Y	NAND2BXL	2	0.60	97.60	135.80	801.70	F
g146/AN					0.00	801.70	
g146/Y	NAND2BXL	1	0.40	78.00	124.70	926.40	F
g142/B					0.00	926.40	
g142/Y	XNOR2X1	1	0.30	24.50	180.40	1106.80	R
countout_reg[7]/D	DFFSHQX1				0.00	1106.80	
countout_reg[7]/CK	setup			0.00	119.00	1225.80	R

Physical Design:

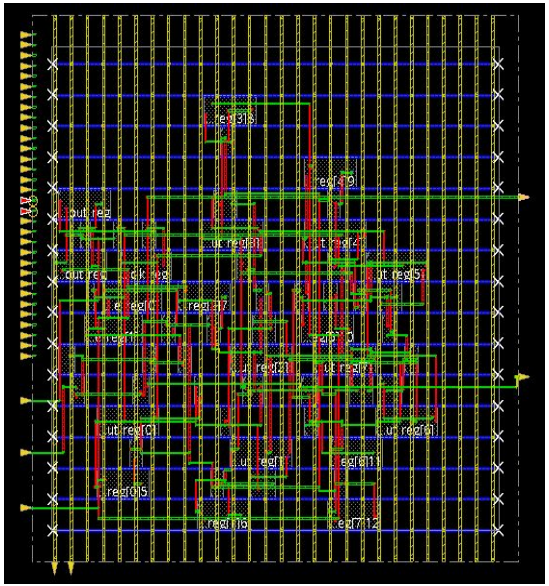


Floorplan



Power Mesh

Physical Design:



vlsi10@CadenceServer3:~/Peace

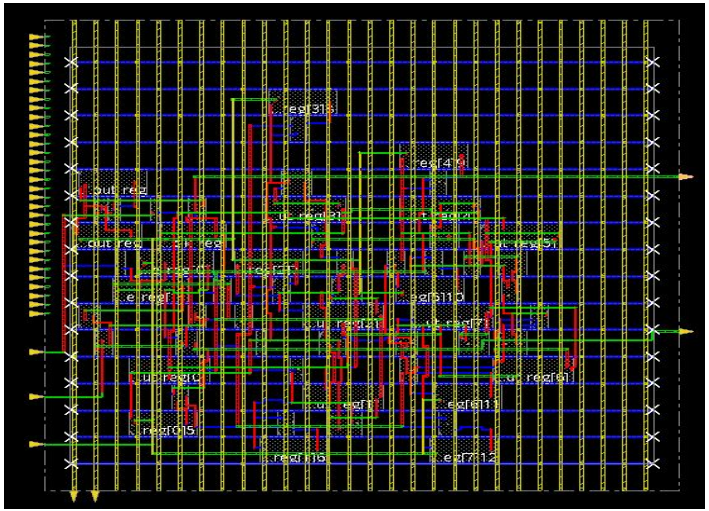
File Edit View Search Terminal Help

```
Total Memory Usage: 1063.851562 Mbytes
innovus 16> innovus 16> report_timing
#------------------------------------------------------------------
#  Generated by:       Cadence Innovus 16.10-p004_1
#  OS:                 Linux x86_64(Host ID CadenceServer3.localdomain)
#  Generated on:       Wed Mar  6 15:50:26 2024
#  Design:             topspi_syn
#  Command:            report_timing
#------------------------------------------------------------------
Path 1: MET Setup Check with Pin spiClockDivider/sclk_reg/CK
Endpoint:   spiClockDivider/sclk_reg/D (v) checked with  leading edge of 'func_
clk'
Beginpoint: spiFSM/pstate_reg[0]/Q     (v) triggered by  leading edge of 'func_
clk'
Path Groups: {func_clk}
Analysis View: func@BC_rcbest0.hold
Other End Arrival Time          -0.000
- Setup                          0.016
+ Phase Shift                    2.500
= Required Time                  2.484
- Arrival Time                   0.165
= Slack Time                     2.320
     Clock Rise Edge                      0.000
     + Clock Network Latency (Prop)      -0.000
     = Beginpoint Arrival Time           -0.000
     +-------------------------------------------------------------------------+
     |          Instance          |     Arc     |   Cell   | Delay | Arrival | Required |
     |                            |             |          |       |  Time   |   Time   |
     |----------------------------+-------------+----------+-------+---------+----------|
     | spiFSM/pstate_reg[0]       | CK ^        |          |       |  -0.000 |    2.320 |
     | spiFSM/pstate_reg[0]       | CK ^ -> Q v | DFFRHQX1 | 0.073 |   0.073 |    2.393 |
     | spiFSM/g115                | B v -> Y ^  | NOR2BX1  | 0.054 |   0.127 |    2.447 |
     | spiClockDivider/g4         | B ^ -> Y v  | NAND2BXL | 0.038 |   0.165 |    2.484 |
     | spiClockDivider/sclk_reg   | D v         | DFFHQX1  | 0.000 |   0.165 |    2.484 |
     +-------------------------------------------------------------------------+

innovus 17>
```

Placement

Clock Tree Synthesis

Physical Design:



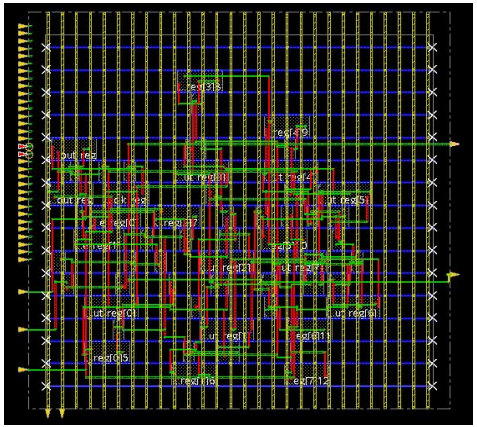
Nano -route

```
------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

Setup views included:
 func@BC_rcbest0.hold

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  2.327  |  2.327  |  2.458  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   10    |   10    |    1    |
+--------------------+---------+---------+---------+

+--------------------+----------------------------------+----------------+
|                    |              Real                |       Total    |
|        DRVs        +------------------+---------------+----------------+
|                    |  Nr nets(terms)  |  Worst Vio    |  Nr nets(terms)|
+--------------------+------------------+---------------+----------------+
|   max_cap          |      0 (0)       |     0.000     |      0 (0)     |
|   max_tran         |      0 (0)       |     0.000     |      0 (0)     |
|   max_fanout       |      0 (0)       |       0       |      0 (0)     |
|   max_length       |      0 (0)       |       0       |      0 (0)     |
+--------------------+------------------+---------------+----------------+

Density: 7.255%
Total number of glitch violations: 0
------------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 2.93 sec
Total Real time: 3.0 sec
Total Memory Usage: 1205.292969 Mbytes
Reset AAE Options
```

```
------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

Hold  views included:
 func@BC_rcbest0.hold

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.012  |  0.057  |  0.012  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   10    |   10    |    1    |
+--------------------+---------+---------+---------+

Density: 7.255%
------------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 0.51 sec
Total Real time: 0.0 sec
Total Memory Usage: 1181.832031 Mbytes
Reset AAE Options
```

Post Route

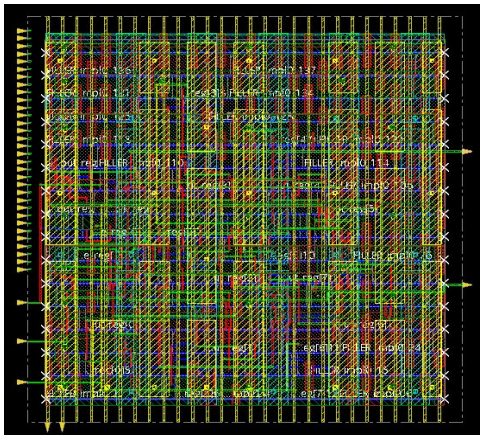
Physical Design:



Filler Cell

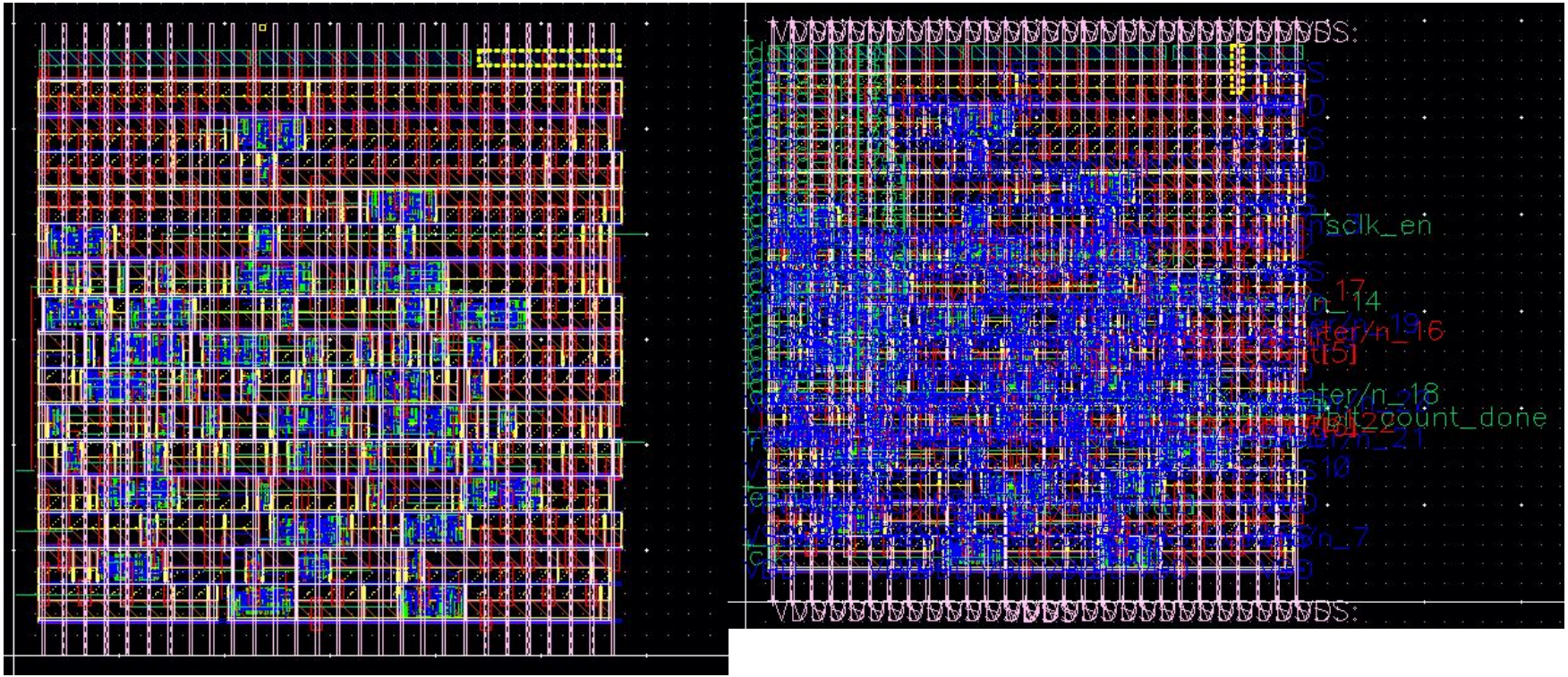
```
innovus 26> innovus 26>  *** Starting Verify Geometry (MEM: 1503.4) ***

**WARN: (IMPVFG-257):    verifyGeometry command is replaced by verify_drc command. It still works in this release but
will be removed in future release. Please update your script to use the new command.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 1920
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells           :  0 Viols.
  VERIFY GEOMETRY ..... SameNet         :  0 Viols.
  VERIFY GEOMETRY ..... Wiring          :  0 Viols.
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.
```

SI Optimization



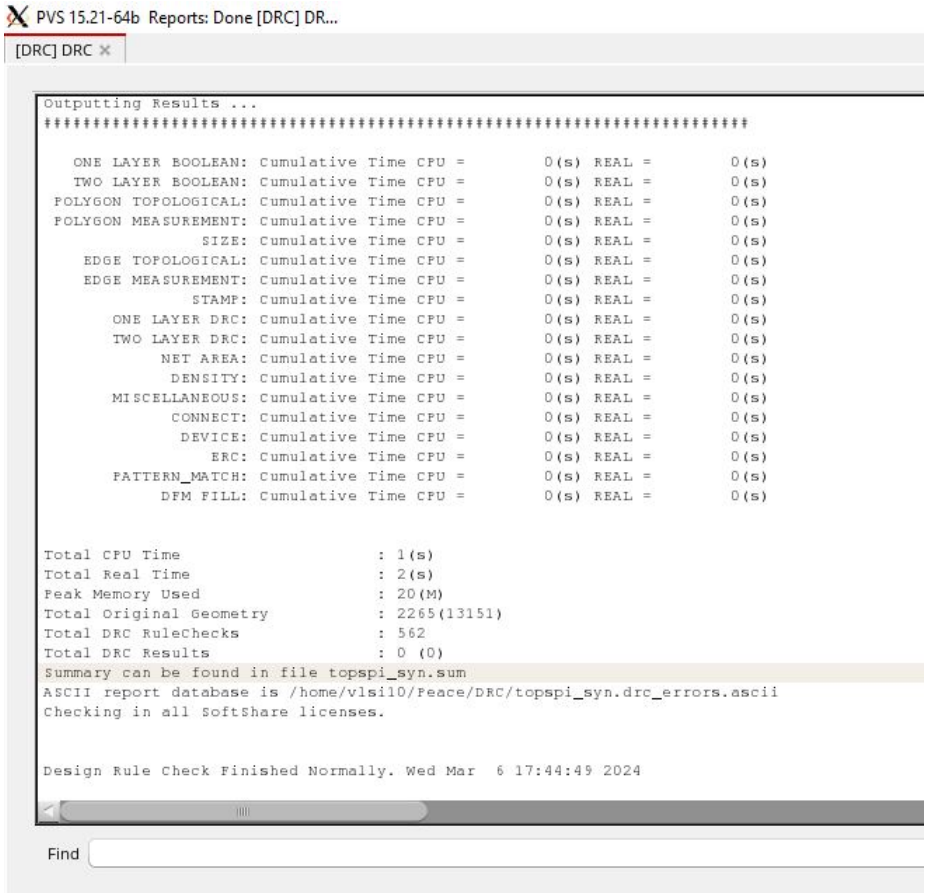
Metal-Filler Cell

Physical Design:



Layout of the designed structure

DRC check


PVS 15.21-64b Reports: Done [DRC] DR...
[DRC] DRC
Outputting Results ...
##
ONE LAYER BOOLEAN: Cumulative Time CPU = 0(s) REAL = 0(s)
TWO LAYER BOOLEAN: Cumulative Time CPU = 0(s) REAL = 0(s)
POLYGON TOPOLOGICAL: Cumulative Time CPU = 0(s) REAL = 0(s)
POLYGON MEASUREMENT: Cumulative Time CPU = 0(s) REAL = 0(s)
SIZE: Cumulative Time CPU = 0(s) REAL = 0(s)
EDGE TOPOLOGICAL: Cumulative Time CPU = 0(s) REAL = 0(s)
EDGE MEASUREMENT: Cumulative Time CPU = 0(s) REAL = 0(s)
STAMP: Cumulative Time CPU = 0(s) REAL = 0(s)
ONE LAYER DRC: Cumulative Time CPU = 0(s) REAL = 0(s)
TWO LAYER DRC: Cumulative Time CPU = 0(s) REAL = 0(s)
NET AREA: Cumulative Time CPU = 0(s) REAL = 0(s)
DENSITY: Cumulative Time CPU = 0(s) REAL = 0(s)
MISCELLANEOUS: Cumulative Time CPU = 0(s) REAL = 0(s)
CONNECT: Cumulative Time CPU = 0(s) REAL = 0(s)
DEVICE: Cumulative Time CPU = 0(s) REAL = 0(s)
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 2(s)
Peak Memory Used : 20(M)
Total Original Geometry : 2265(13151)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file topspi_syn.sum
ASCII report database is /home/vlsi10/Peace/DRC/topspi_syn.drc_errors.ascii
Checking in all SoftShare licenses.
Design Rule Check Finished Normally. Wed Mar 6 17:44:49 2024
Find

RTL Synthesis: Fanout

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 16.13-s036_1
  Generated on:           Mar 04 2024  06:42:02 pm
  Module:                 spi
  Technology library:     slow_vddiv0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

path   1:

     Pin                      Type          Fanout Load Slew Delay Arrival   Location
                                                  (fF) (ps)  (ps)   (ps)       (x,   y)
-------------------------------------------------------------------------------------
(clock clk)           launch                                        0 R
clk0
  dff_inst0
    Q_reg/clk                                                       0 R
    Q_reg/q   (i) (u)  unmapped_d_flop       2  0.0    0  +305     305 F
    g3/data_in_0                                              +0     305
    g3/z          (u)  unmapped_not          1  1.2    0   +22     328 R
    Q_reg/clk          setup                            0  +119     447 R
-------------------------------------------------------------------------------------
(clock clk)           capture                                   10000 R
-------------------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :    9553ps
Start-point  : clk0/dff_inst0/Q_reg/clk
End-point    : clk0/dff_inst0/Q_reg/d

(u) : Net has unmapped pin(s).
(i) : Net is ideal.
```

```
spifsm/load_en
s0/load_en
  g159/in_0                                                    +0     339
  g159/z              (u)  unmapped_nor2        36  7.2    0  +125     464 R
  inc_ADD_UNS_OP_1/CI
    g2/in_1                                                    +0     464
    g2/z              (u)  unmapped_and2         2  2.4    0   +68     532 R
    g7/in_1                                                    +0     532
    g7/z              (u)  unmapped_and2         2  2.4    0   +68     600 R
    g9/in_1                                                    +0     600
    g9/z              (u)  unmapped_and2         2  2.4    0   +68     668 R
    g11/in_1                                                   +0     668
    g11/z             (u)  unmapped_and2         2  2.4    0   +68     736 R
    g13/in_1                                                   +0     736
    g13/z             (u)  unmapped_and2         1  1.2    0   +58     794 R
    g14/in_1                                                   +0     794
    g14/z             (u)  unmapped_xor2         2  2.4    0  +142     935 F
  inc_ADD_UNS_OP_1/Z[5]
  g184/in_0                                                    +0     935
  g184/z              (u)  unmapped_not          1  1.2    0   +22     958 R
  g188/in_0                                                    +0     958
  g188/z              (u)  unmapped_nand4        1  1.2    0  +149    1106 F
  g191/in_2                                                    +0    1106
  g191/z              (u)  unmapped_nor3         8 16.8    0  +179    1286 R
  done_reg/srd            unmapped_d_flop                      +0    1286
  done_reg/clk            setup                            0  +278    1564 R
-------------------------------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : fsm0/load_en_reg/clk
End-point    : s0/done_reg/srd
```

```
s0/load_en
  g159/in_0                                                    +0     339
  g159/z              (u)  unmapped_nor2        36  7.2    0  +125     464 R
  inc_ADD_UNS_OP_1/CI
    g2/in_1                                                    +0     464
    g2/z              (u)  unmapped_and2         2  2.4    0   +68     532 R
    g7/in_1                                                    +0     532
    g7/z              (u)  unmapped_and2         2  2.4    0   +68     600 R
    g9/in_1                                                    +0     600
    g9/z              (u)  unmapped_and2         2  2.4    0   +68     668 R
    g11/in_1                                                   +0     668
    g11/z             (u)  unmapped_and2         2  2.4    0   +68     736 R
    g13/in_1                                                   +0     736
    g13/z             (u)  unmapped_and2         1  1.2    0   +58     794 R
    g14/in_1                                                   +0     794
    g14/z             (u)  unmapped_xor2         2  2.4    0  +142     935 F
  inc_ADD_UNS_OP_1/Z[5]
  g184/in_0                                                    +0     935
  g184/z              (u)  unmapped_not          1  1.2    0   +22     958 R
  g188/in_0                                                    +0     958
  g188/z              (u)  unmapped_nand4        1  1.2    0  +149    1106 F
  g191/in_2                                                    +0    1106
  g191/z              (u)  unmapped_nor3         8 16.8    0  +179    1286 R
  done_reg/srd            unmapped_d_flop                      +0    1286
  done_reg/clk            setup                            0  +278    1563 R
-------------------------------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : fsm0/load_en_reg/clk
End-point    : s0/done_reg/srd

(u) : Net has unmapped pin(s).
```

```
  sclk_en_reg/clk                                              0              0 R
  sclk_en_reg/q       (u)  unmapped_d_flop       4  4.8    0  +333     333 R
spifsm/sclk_en
s0/sclk_en
  g182/in_0                                                    +0     333
  g182/z              (u)  unmapped_not          2  2.4    0   +33     366 F
  g187/in_1                                                    +0     366
  g187/z              (u)  unmapped_nor2        40  8.4    0  +134     499 R
  mux_data_224_19_g16/sel0                                     +0     499
  mux_data_224_19_g16/z     unmapped_bmux3       2  2.4    0  +142     641 R
  mux_data_236_19_g17/data1                                    +0     641
  mux_data_236_19_g17/z     unmapped_bmux3       2  2.4    0  +142     783 R
  mux_dout_245_10_g17/data1                                    +0     783
  mux_dout_245_10_g17/z     unmapped_bmux3       1  1.2    0  +131     914 R
  dout_reg[15]/d            unmapped_d_flop                    +0     914
  dout_reg[15]/clk          setup                            0  +119    1033 R
-------------------------------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : fsm0/sclk_en_reg/clk
End-point    : s0/dout_reg[15]/d

(u) : Net has unmapped pin(s).

path  29:

          Pin                      Type          Fanout Load Slew Delay Arrival   Location
                                                       (fF) (ps)  (ps)   (ps)       (x,   y)
-------------------------------------------------------------------------------------------
fsm0
  sclk_en_reg/clk                                              0              0 R
  sclk_en_reg/q       (u)  unmapped_d_flop       4  4.8    0  +333     333 R
```

Future Plan

- Perform LVS on this design
- Implement the circuit into FPGA

THANK YOU