BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (January2023)

AICD Laboratory

Final Project Report

Section: G1, Project Group: 02

Designing a 1:8 Analog De-multiplexer

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Signature of Instructor: _____

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"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

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Table of Contents

1 Abstract

In this collaborative project, a team of four individuals undertook the design and implementation of a 1:8 Analog De-multiplexer using MOSFETs within the Cadence environment. The objective of this endeavour was to develop a high-performance analog circuit capable of accurately and efficiently demultiplexing an input signal into eight distinct output channels. To achieve this, the team employed the MOSFETs, leveraging their exceptional characteristics to construct transmission gates for signal routing and manipulation

2 Introduction

A 1:8 analog demux, also known as a 1-to-8 analog demultiplexer, is an electronic component or circuit that is used to take a single input signal and route it to one of eight output channels. The term "demux" is short for "demultiplexer," and it essentially performs the opposite function of a multiplexer (mux). While a multiplexer combines multiple input signals into one output, a demultiplexer takes one input signal and distributes it to multiple outputs.

The primary function of a 1:8 analog demux is to select one of its eight output channels and pass the input signal to that selected channel. The selection of the output channel is typically controlled by a binary input. In the case of a 1:8 demux, we would need three control lines (binary inputs) to select one of the eight outputs. Depending on the binary input, the demux will route the input signal to the corresponding output channel.

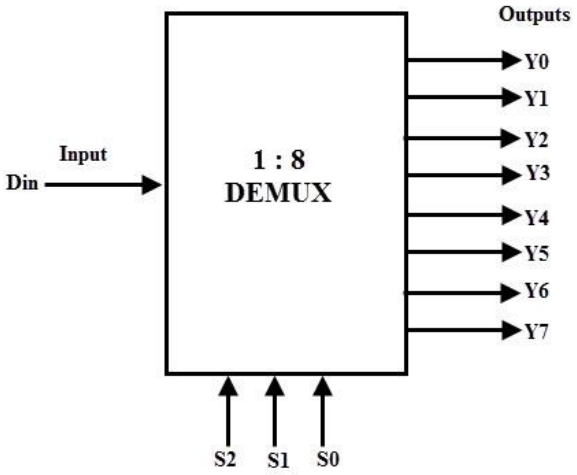

Fig 1: 1:8 de-multiplexer symbol

Analog demultiplexers are commonly used in various applications, including data acquisition systems, telecommunications, and signal routing. For example, in a data acquisition system, a 1:8 analog demux can be used to select one of eight different sensors or signal sources for processing by an analog-to-digital converter (ADC). This allows us to sample or measure

multiple analog signals using a single ADC, which can help reduce the complexity and cost of the system.

In summary, a 1:8 analog demux is a component or circuit that takes a single input signal and routes it to one of eight output channels based on control inputs. Its primary purpose is to distribute an input signal to multiple destinations, making it a valuable tool in various electronic and communication systems.

3 Design

3.1 Design Method (PO(a))

1. Designing Transmission Gate
2. Checking characteristics of the transmission gate
3. Building smaller De-multiplexer
4. Building 1:8 De-multiplexer
5. Plotting/checking outputs
6. Checking different characteristics
7. Investigating trade-offs for the given specifications
8. Selecting optimized parameters.

3.2 Circuit Diagram

Transmission Gate Model:

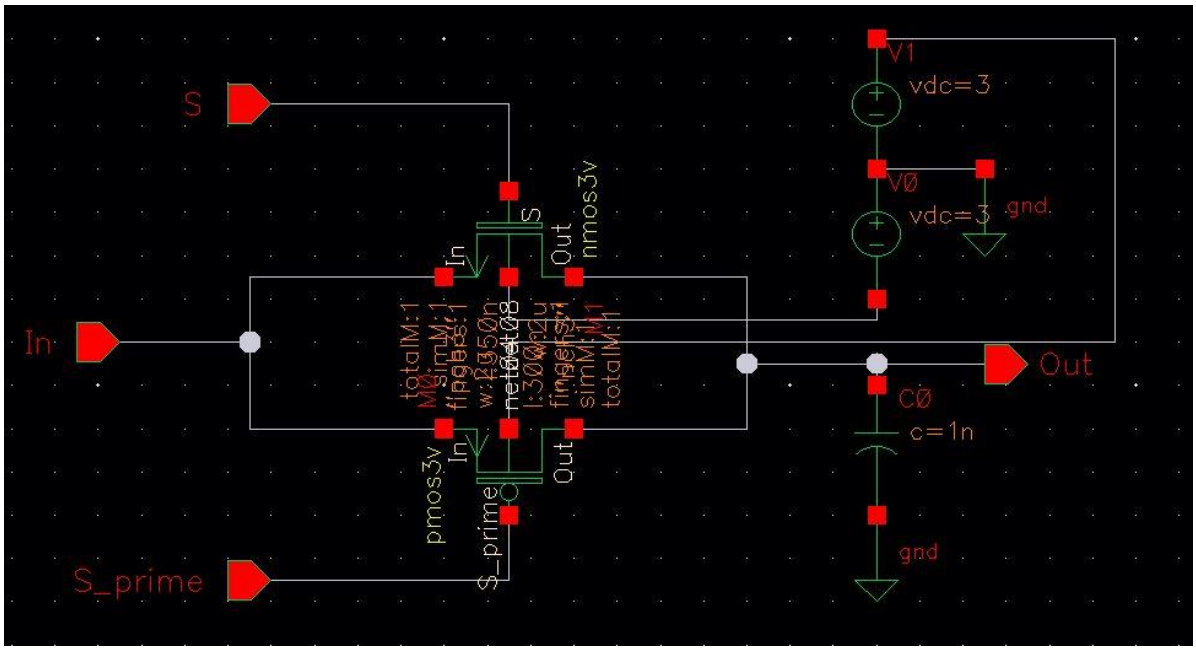

Fig 2: Circuit diagram for one transmission gate

Transmission Gate Symbol:

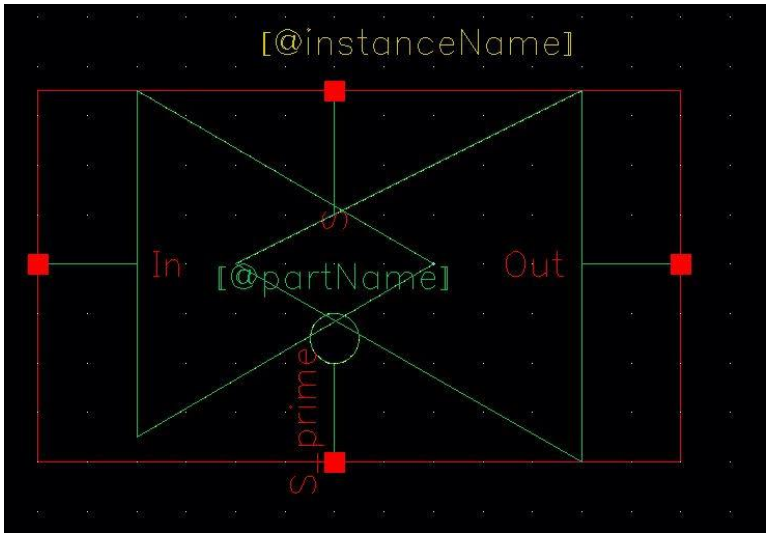

Fig 3: Drawn symbol for transmission gate

CMOS inverter:

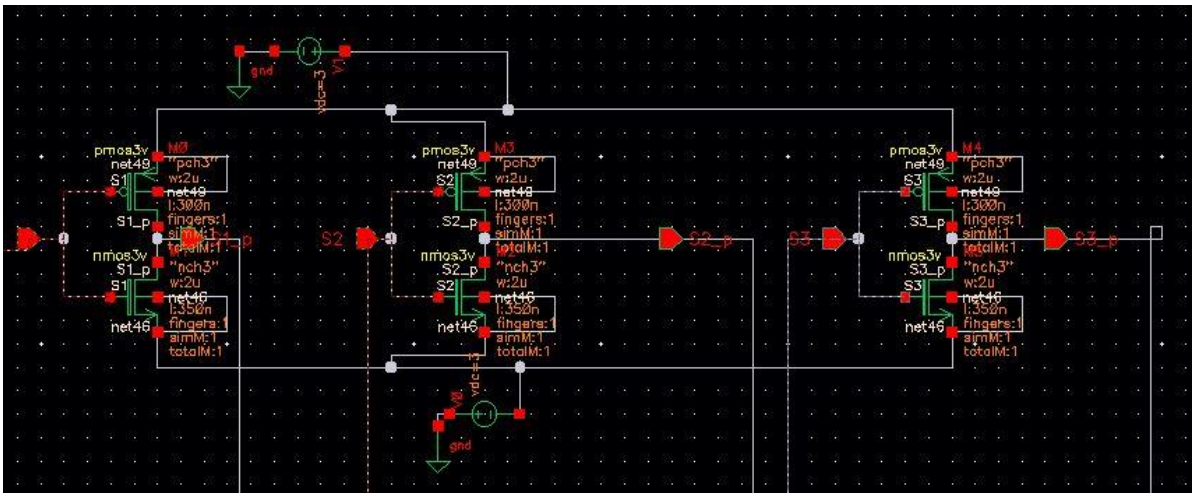

Fig 4: Circuit diagram of three CMOS inverter

Final Circuit:

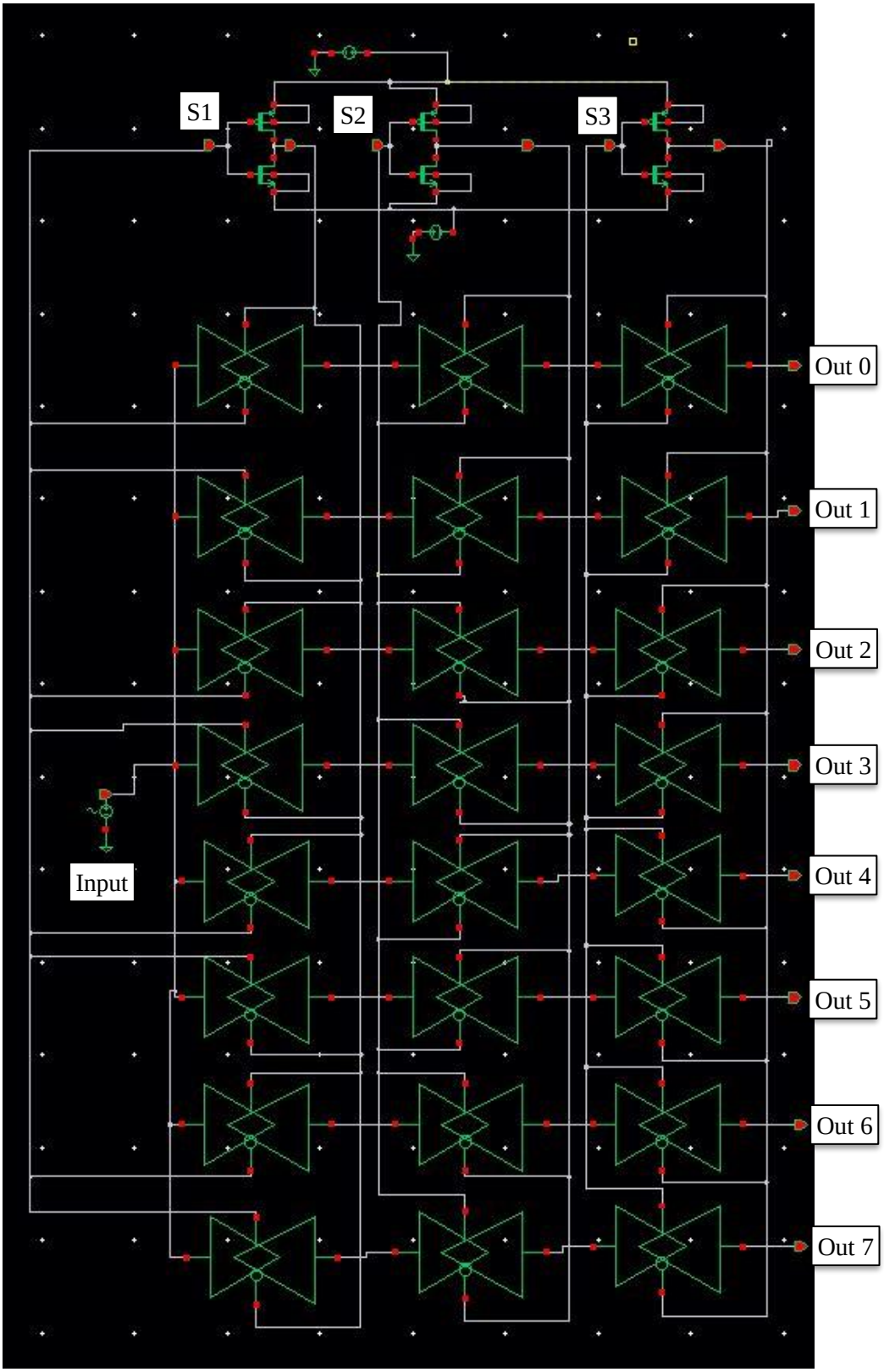

Fig 5: Circuit diagram of 1:8 demultiplexer using transmission gates

4 Design Analysis and Evaluation

4.1 Results and Analysis

4.1.1 Main Output:

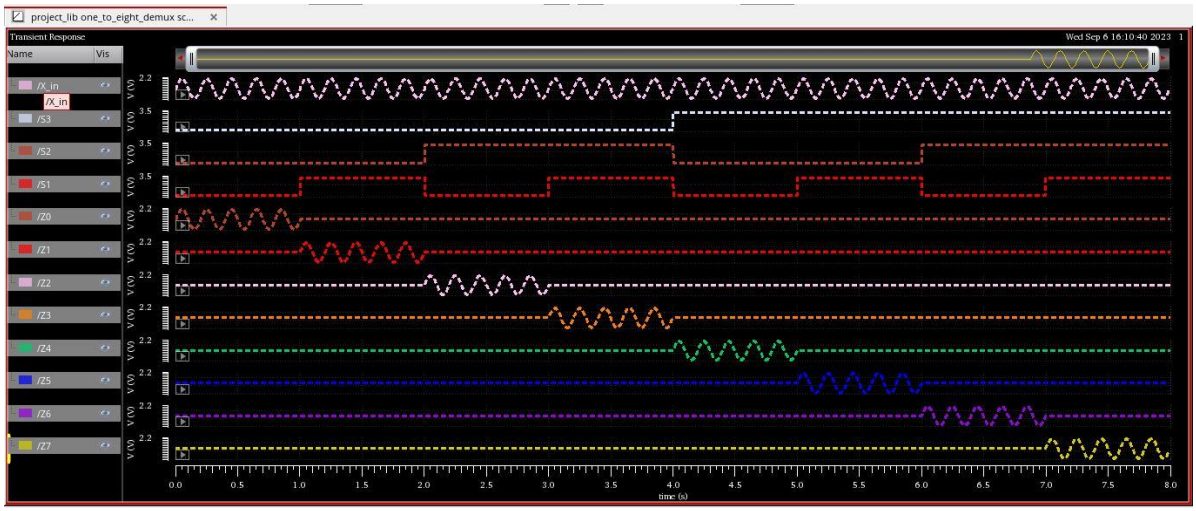

Fig 6: Output plot

In the output plot, we can see that input(X_in) is directed to different outputs (Z0 to Z7) depending on the sequence of three select pins: S1, S2, S3.

4.1.2 Specifications: Bandwidth (3dB)

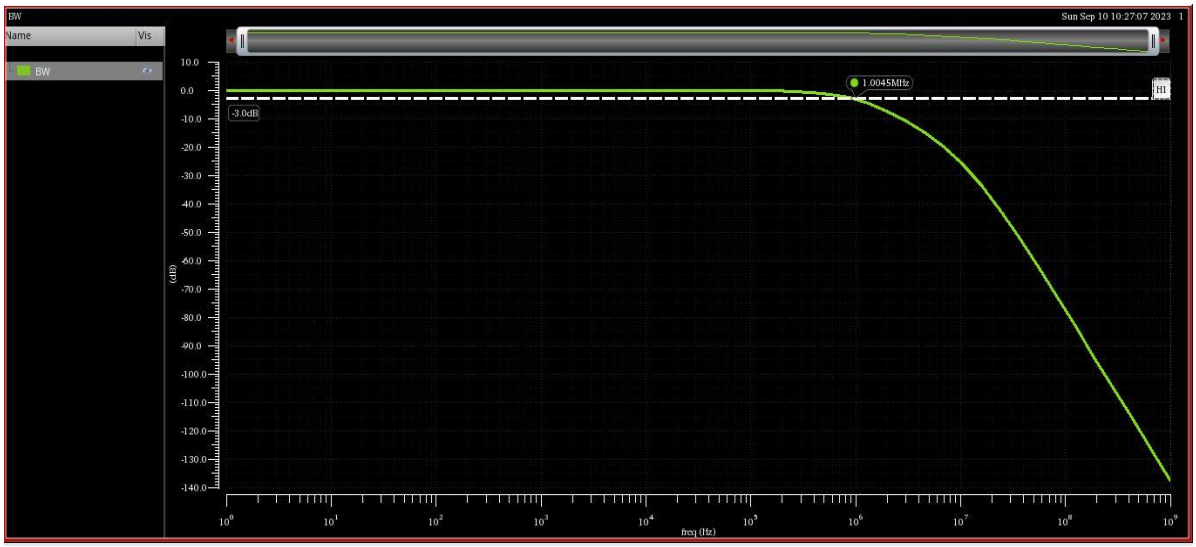

Fig 7: 3 dB bandwidth plot for the analog demux circuit

From this plot, we can notice that the 3 dB bandwidth for the circuit is 1.0045 MHz which is nearly equal to our target bandwidth **1 MHz.** To achieve this, we had to change the width of the MOSFET accordingly.

4.1.3 Specifications: Switching On Time

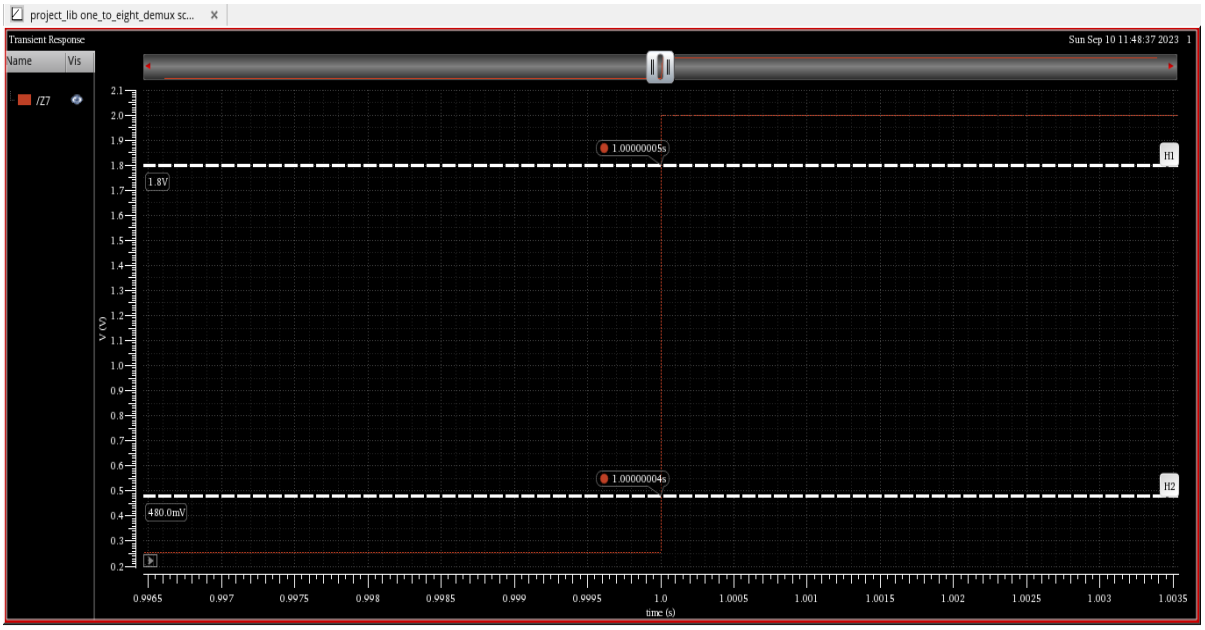

Fig 8: Plot for determining switching on time

To determine switching on time (t_{on}), we connected 1 kΩ load resistance and 10 pF load capacitance with the output pins. Then we switched on a specific pin after a specific time (1 sec) and observed how much time it takes to turn on.

From the plot,

t_{on} = 1.00000005-1.00000004

= 1×10^{-8} s

= 10 ns

4.1.4 Specifications: Power Dissipation

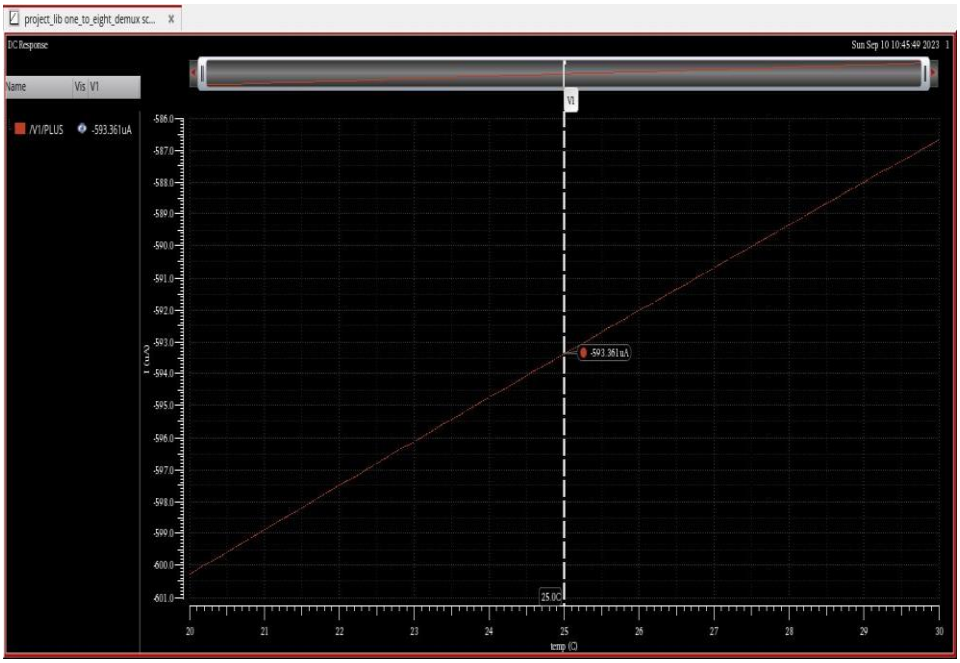

Fig 9: Plot for determining power dissipation

To determine the total power dissipation of the circuit, we calculated the current flowing from the V_{dd} source on the top at room temperature (25^o C). Then multiplied it with the voltage of V_{dd} (3V) to determine the power dissipation.

Here,

Supply Voltage (V_{dd}) = 3V

Current (from plot) = 0.593mA

So, power dissipation, $P = 3 \times 0.593 \times 10^{-3}$

= 1.78 mW

There is a limitation of the process we have used here to calculate the power dissipation. As we haven't considered the power drawn from other minor power sources like the sources used inside the transmission gate symbol for body biasing and sources used for the select pins, the total power dissipation of the circuit will slightly higher than our calculation.

4.1.5 Specifications: On Resistance

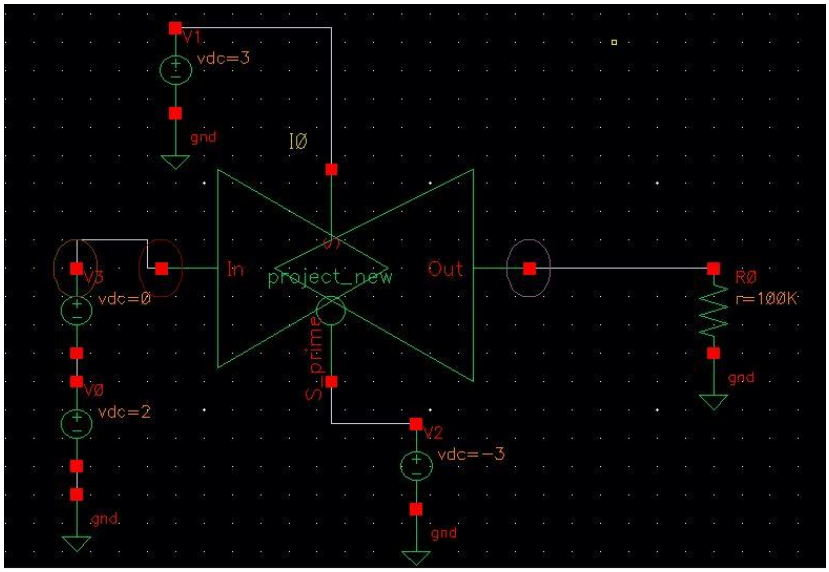

Fig 10: Circuit for on resistance calculation

To calculate the on resistance of the demux, we built a separate circuit consisting of only one transmission gate and calculated the difference between the input and output voltage. And also calculated the current flowing through the transmission gate.

```
DC Operating Point:
    I(I0:1) = 19.9993 uA
    I(I0:2) = -19.9993 uA
    V(net01) = 2 V
    V(net1) = -3 V
    V(net2) = 3 V
    V(net04) = 1.99993 V
    V(net4) = 2 V
    I(V0:p) = -19.9993 uA
    I(V1:p) = 0 A
    I(V2:p) = 0 A
    I(V3:p) = -19.9993 uA
    V(I0.net04) = 3 V
    V(I0.net08) = -3 V
    I(I0.V0:p) = -16.2707 pA
    I(I0.V1:p) = -3.11599 pA
```

Fig 11: DC operating point outputs for resistance calculation

Here,

Voltage at the input terminal, V_{in} = 2 V
Voltage at the output terminal, V_{out} = 1.99993 V
Current through transmission gate, I =19.9993 µA

On resistance for one transmission gate,

$$R_{on} = (V_{out}-V_{in})/I$$
$$= (2-1.9993)/19.9993\ \mu$$
$$= 3.5\ \Omega$$

As one path to the output consists of three transmission gates in our demux circuit,
Total on resistance = 3 x R_{on} = 3.5 x 3 Ω
= 10.5 Ω

4.1.6 Specifications: Charge Injection over the full signal swing range

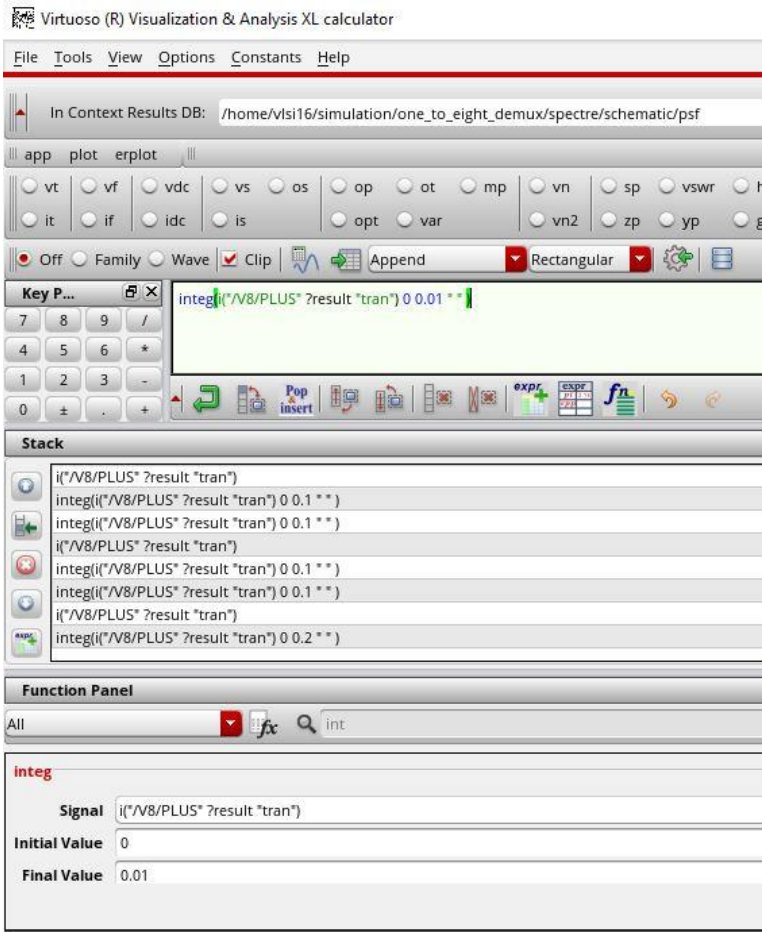

Fig 12: Calculator setup for calculating charge injection over a full signal swing range

We know,

$$Q = \int_0^T I(t)\, dt$$

For calculating the charge injection over a full signal swing range, we integrated the current through the input pin over a full time period of the input signal of 100 Hz.

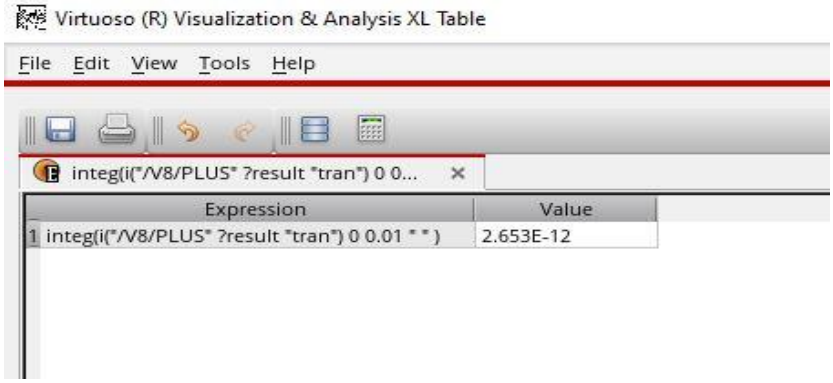

Fig 13: Integration output for charge injection

From the output table, we found charge injection over the full swing range = **2.653 pC**

4.1.7 Specifications: Input Capacitance

We know,

$$C = \frac{1}{V_C}\int_0^T I_C(t)dt$$

From previous calculation,

value of integration of input current (for one cycle) = 2.653 pC

Input voltage(rms) = $2/\sqrt{2}$
So, Input Capacitance, C_{in} = 1.812 pF

5 Design Analysis and Evaluation

5.1 Novelty

Incorporating MOSFETs into our analog demux project involved several innovative techniques and optimizations to enhance performance. One key optimization was custom sizing of the MOSFETs in our transmission gates. By carefully selecting the dimensions of the MOSFETs, we were able to achieve better speed and reduced leakage current, improving the overall efficiency of our circuit.

To improve energy efficiency, we implemented low-power modes in our design. This allowed us to dynamically adjust the biasing of the MOSFETs based on the operational requirements, effectively reducing power consumption during idle or less active periods. This energy-efficient approach sets our circuit apart from conventional designs.

Robustness and reliability were paramount in our project. We took measures to mitigate the impact of process variations by using techniques such as redundancy and feedback mechanisms. These design choices ensured that our circuit could maintain consistent performance even in the face of manufacturing process fluctuations.

5.2 Design Considerations (PO(c))

5.2.1 Considerations to public health and safety

Considerations for public health and safety in the design and implementation of our Analog De-multiplexer include adhering to electrical safety standards, preventing fire and overheating, minimizing environmental impact, ensuring user-friendly operation, implementing rigorous testing, and maintaining comprehensive documentation to meet industry standards and regulations.

5.2.2 Considerations to environment

Energy Efficiency: This Analog De-multiplexer is designed to be highly energy-efficient, thus leads to reduced energy consumption when it is operational. This directly translates to lower greenhouse gas emissions if powered by conventional energy sources.

Future Sustainability: Demonstrating your commitment to ongoing sustainability efforts in our project report signals a dedication to minimizing environmental impact and continually improving the project's eco-friendliness.

5.3 Investigations (PO(d))

5.3.1 Results and Analysis

Specification	Required value	Obtained value
Supply Voltage	+/- 3 V	+/- 3 V
Logic High Level	1.4 V	1.4 V
Logic Low Level	0 V	0 V
Input Capacitance (max)	50 pF	1.812 pF
Charge injection over the full signal swing range (max)	5 pC	2.653 pC
Switching On time (t_{ON}) (at R_L = 1 kΩ, C_L = 10 pF) (max)	100 ns	10 ns
Analog Signal Range	-2 to 2 V	-2 to 2 V
Power Dissipation (max)	10 mW	1.78 mW
On-Resistance	10 Ω	10.5 Ω
Bandwidth, 3 dB	1 MHz	1.0045 MHz

5.3.2 Interpretation and Conclusions on Data

From the above table, it can be seen that most of the required specifications have been met in this project. Though some approximations involve in some of the calculation methods, these results serve as a reassuring affirmation of the soundness and effectiveness of our project.

6 Reflection on Individual and Team work (PO(i))

In the pursuit of successfully completing this project within the Analog Integrated Circuits Laboratory, our team of four members collectively and diligently dedicated equal efforts to its accomplishment.

7 Communication to External Stakeholders (PO(j))

7.1 Executive Summary

Throughout this report, we have demonstrated the advantages of using transmission gates in demultiplexer designs, such as improved speed, reduced power consumption, and versatility in various digital applications. However, it is essential to consider the trade-offs associated with this design, such as increased complexity and potential signal integrity issues due to the use of transmission gates.

In conclusion, the 1-to-8 demux with transmission gate design has been thoroughly examined in this report. We have discussed the fundamental principles behind demultiplexers and transmission gates, highlighting their importance in digital circuitry. The design and operation of the 1-to-8 demultiplexer using transmission gates have been explained in detail, including plots and timing diagrams.

8 Future Work (PO(l))

In the future, there are several promising avenues for further development in the 1:8 analog demux project. These include exploring advanced MOSFET technologies to boost performance and reduce power consumption, implementing advanced signal processing techniques for improved signal fidelity, integrating digital control interfaces for enhanced user-friendliness, optimizing power efficiency in low-power modes, enhancing robustness to handle variations, investigating miniaturization and integration for space-constrained applications, conducting comprehensive real-world testing and validation, and considering security measures for applications where data integrity is paramount. These endeavors would continue to advance the capabilities and versatility of the analog demux circuit.

9 References

https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=1a802c57a55cf58157c19ae90d8556642f8c118f