به نام خدا

تمرین کامپیوتری سری 4

سیستم های دیجیتال 2

فردین عباسی 810199456

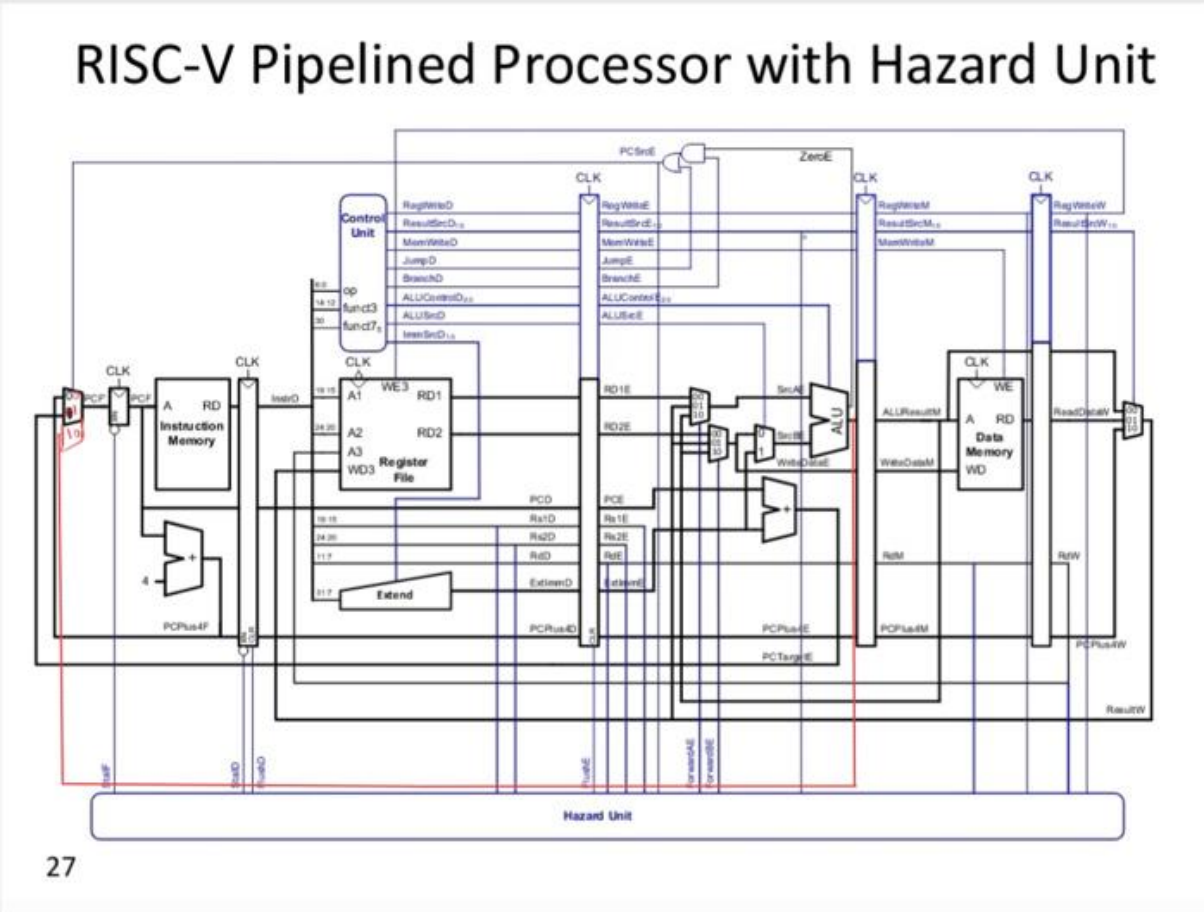
سهیل عبداللهی 810199459

دانشکده مهندسی برق و کامپیوتر

دانشگاه تهران

بهار 1402

Data Path



Controller

Imm Src		
000	{20Imm[31],Imm[31:20]}	**I Type**
001	{20Imm[31],Imm[31:25],Imm[11,7]}	**S Type**
010	{19Imm[31],Imm[31],Imm[7],Imm[30:25],Imm[11:8],1'b0}	**B Type**
011	{Imm[31:12],12'b0}	**U Type**
100	{Imm[20],Imm[10:1],Imm[11],Imm[19:12]}	**J Type**

ALU Controller	
000	**A+B**
001	**A-B**
010	**A & B**
011	**A | B**
100	**A slt B**
101	**A XOR B**

ALU OP	Function 7	Function 3	ALU Controller
00	0000000	000	000 (A+B)
	0100000	000	001 (A-B)
	0000000	111	010 (AND)
	0000000	110	011 (OR)
	0000000	010	100 (SLT)
01		000	000 (ADDi)
		110	011 (Ori)
		100	101 (XORi)
		010	100 (SLTi)
10		010	000 (LW)
		000	001 (Beq)
		001	001 (Bne)
		100	100 (Blt)
		101	100 (Bge)
11			000 (Jal & Jalr)

Jump	WD3 Src	Reg Write	Imm Src	ALU Src	Mem Write	Result Src	ALU OP	Branch	
0	1	1	_	0	0	00	00	0	R Type
0	0	1	000	1	0	00	01	0	I Type
1	1	1	000	1	0	00	11	0	Jalr
0	0	1	000	1	0	01	10	0	LW
0	0	0	001	1	1	_	10	0	SW
0	0	0	010	0	0	_	10	1	B Type
0	0	1	011	_	0	11	_	0	LUi
1	1	1	100	_	0	_	_	0	Jal

Hazard Unit:

Summary of Hazard Logic

Data hazard logic (shown for SrcA of ALU):

if ((*Rs1E* == *RdM*) AND *RegWriteM*) AND (Rs1E != 0) // Case 1
ForwardAE = 10
else if ((*Rs1E* == *RdW*) AND *RegWriteW*) AND (Rs1E != 0) // Case 2
ForwardAE = 01
else ***ForwardAE*** = 00 // Case 3

Load word stall logic:

lwStall = ((*Rs1D* == *RdE*) OR (*Rs2D* == *RdE*)) AND $ResultSrcE_0$
StallF = ***StallD*** = *lwStall*

Control hazard flush:

FlushD = *PCSrcE*
FlushE = *lwStall* OR *PCSrcE*

Test Code:

```
addi X7,X0,16;
addi X8,X0,30;
sub X9,X8,X7;
and X10,X8,X7;
or X11,X8,X7;
slt X12,X8,X7;
xori X13,X7,13;
ori X14,X7,13;
slti X15,X7,13;
sw X8,400(x7);
lui X17,60;
jalr X16,X7,10;
```