

**Fall 2024**

**Selected Topics in Computer Design-CSE416s**

**Final Project**

**Adaptive Traffic Light Controller-Part B**

**Team #4**

Members:

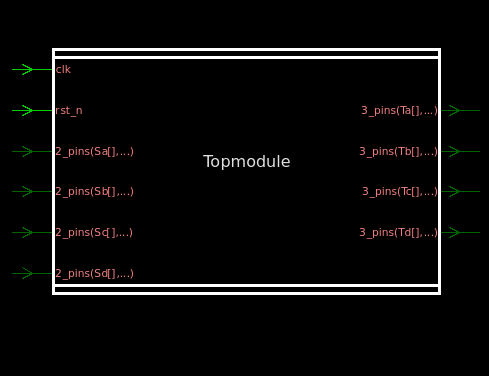
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| Youssef Hany Elreweny | 2101449 | CSE |
| Ahmed Ashraf Ali | 2100255 | CSE |
| Youssef Ossama Sayed | 2101240 | CSE |

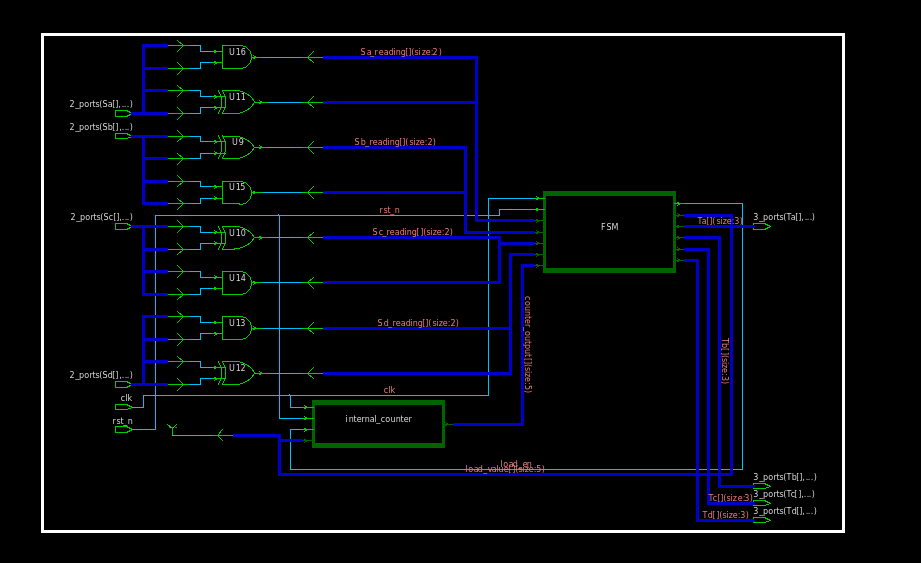
After completing RTL verification and ensuring that our design meets the project requirements, the next step involves synthesizing the RTL code into a technology-mapped Gate Level (GL) netlist. The objective is to ensure there are no timing violations and to perform formal verification to confirm that the functionality remains correct after synthesis.

### **Steps:**

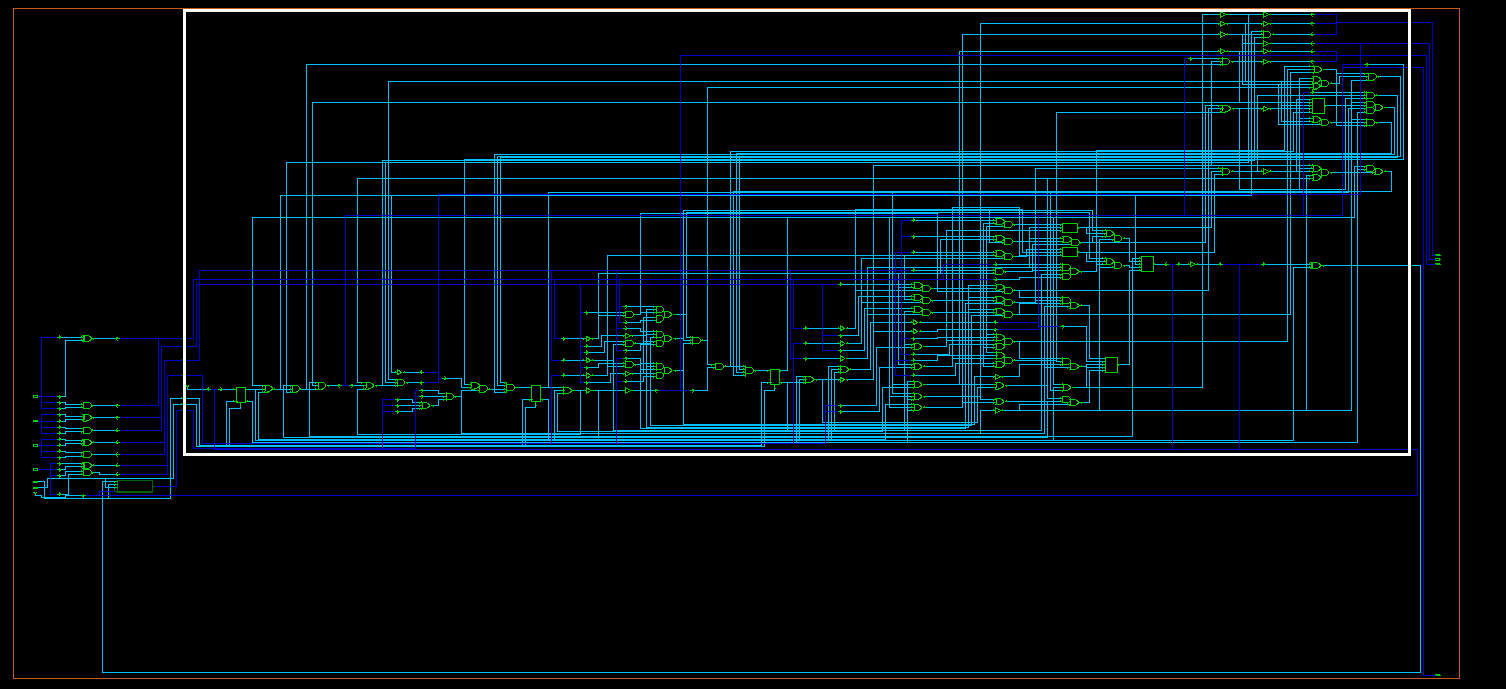
1. **Synthesis Script Implementation:**  
   We created a synthesis script (syn\_script.tcl) to define the RTL code and standard cells of the given Library for the synthesis tool, Design Compiler.
2. **Constraints Script Implementation:**  
   A constraints script (cons.tcl) was developed to specify system clock properties, including clock period, uncertainty, and rising/falling edge times. The script also sets input and output path delays, driving cells, output load, and wire loads to enable the tool to perform Static Timing Analysis (STA) using these constraints.
3. **Netlist Generation and Validation:**  
   After running the synthesis and constraints scripts, a GL netlist was generated. We ensured that the synthesis process was error-free and verified that no unintended components, such as latches, were present.
4. **Constraints Review:**  
   We reviewed the constraints reports to confirm that all constraints were met and verified that there were no timing violations.
5. **Formal Verification:**  
   Finally, a formal verification script (syn\_fm\_script.tcl) was implemented to compare the GL netlist with the original RTL code. Using the Formality tool, we confirmed that the system's functionality remained unchanged. The formal verification process was concluded by extracting and reviewing the verification reports.

* **Schematic :**

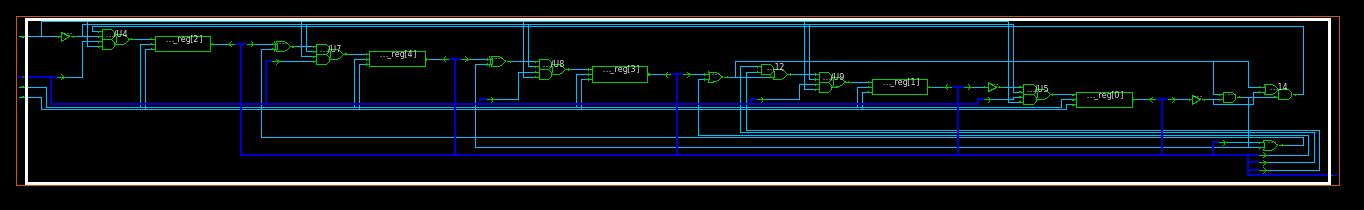
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**TopModule**

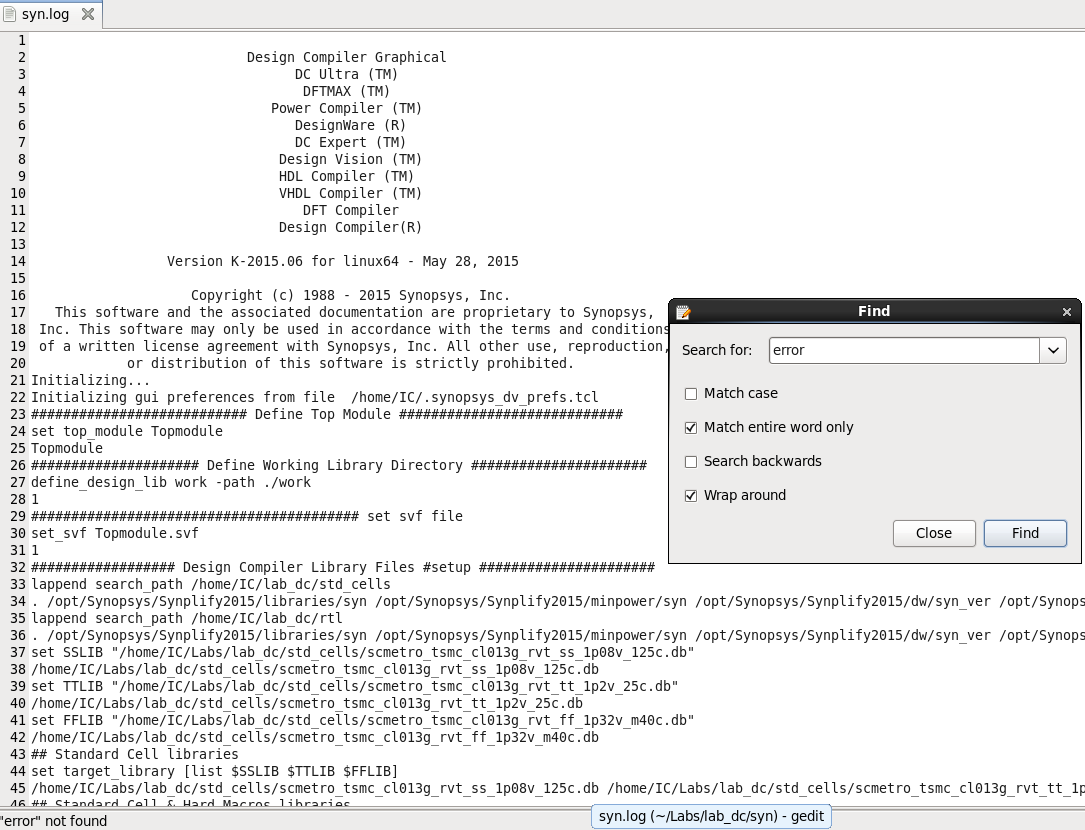
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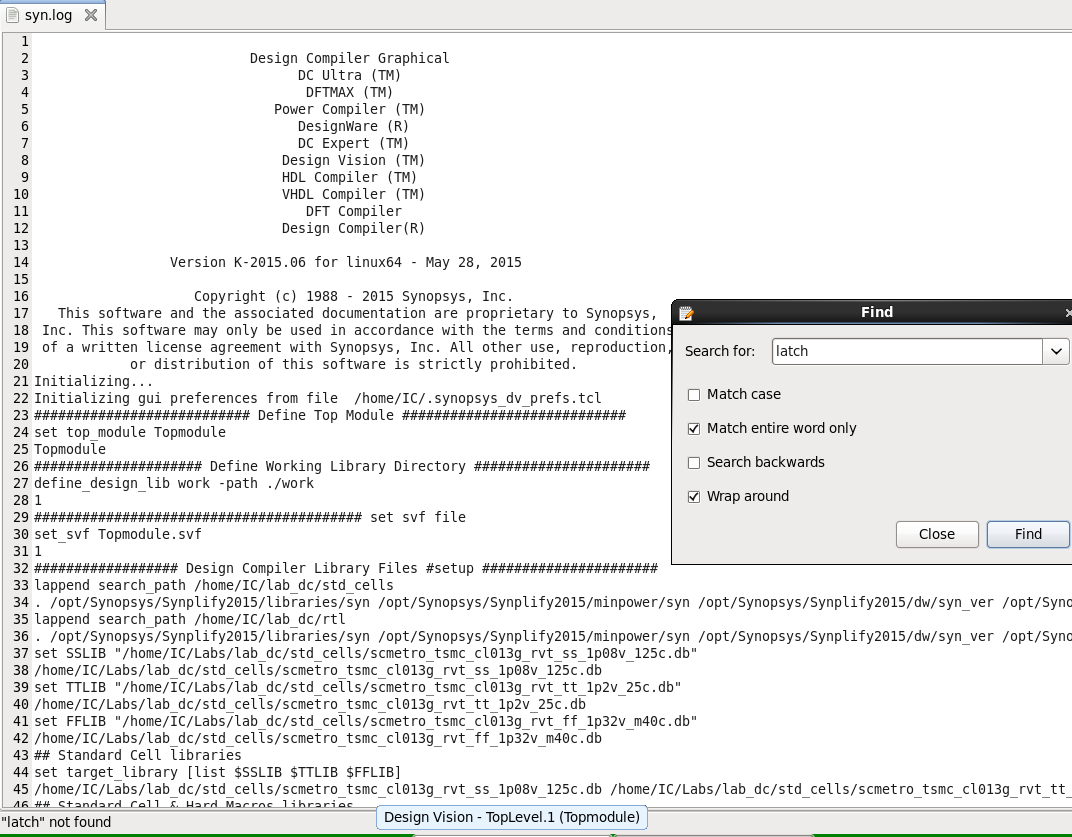
**FSM**

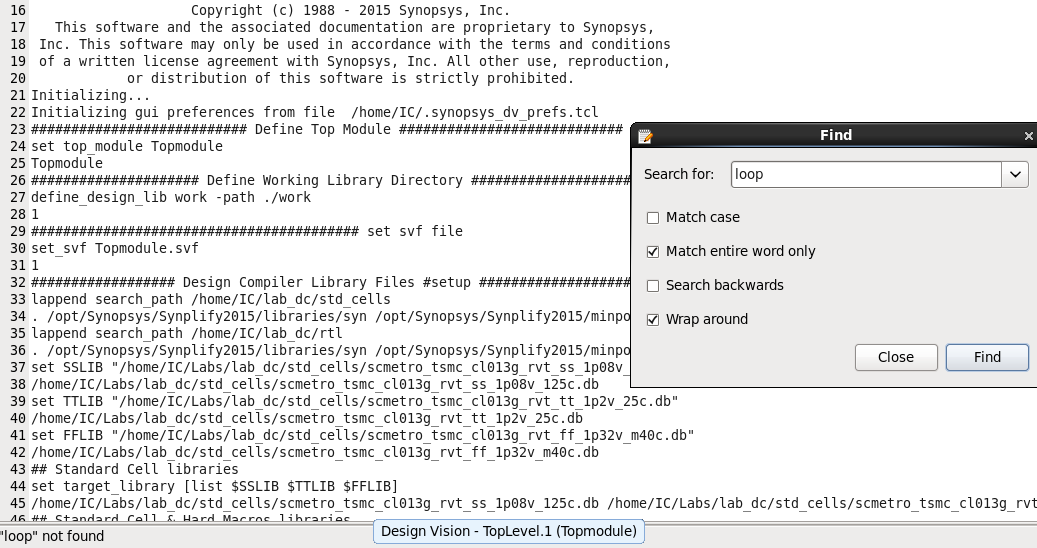


**Counter**

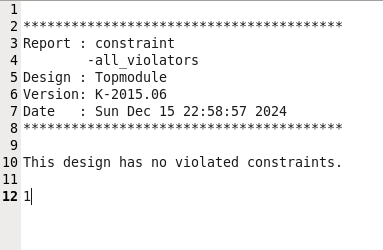
* **no error found in log:**

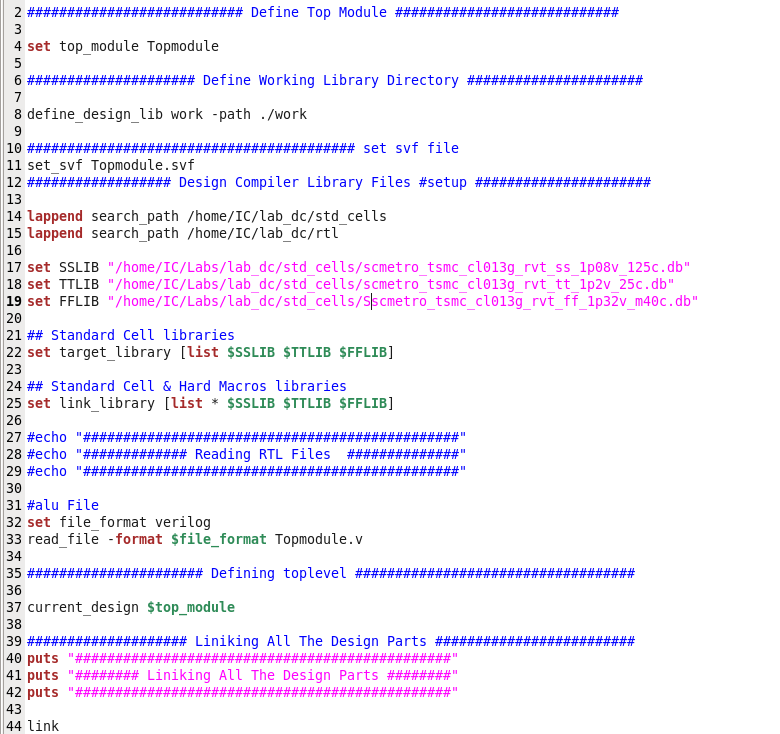
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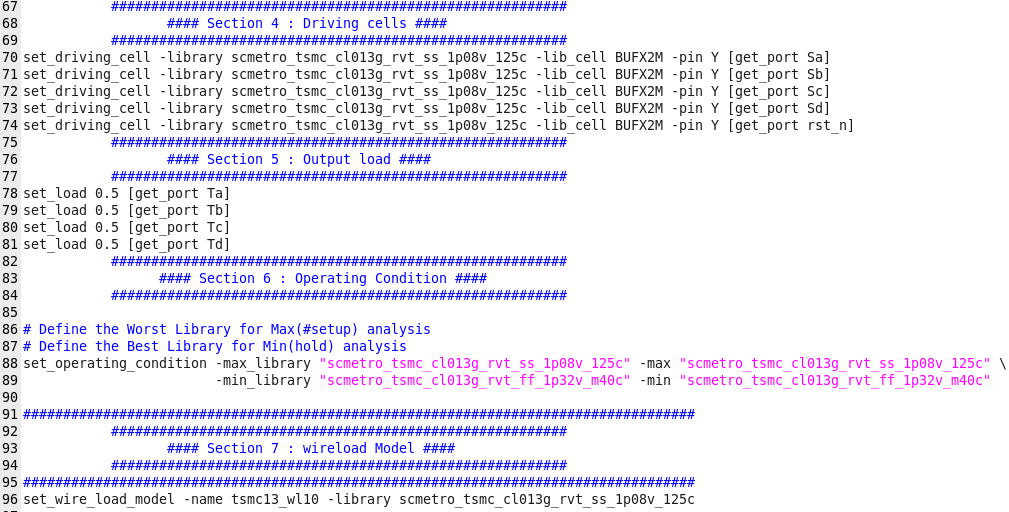
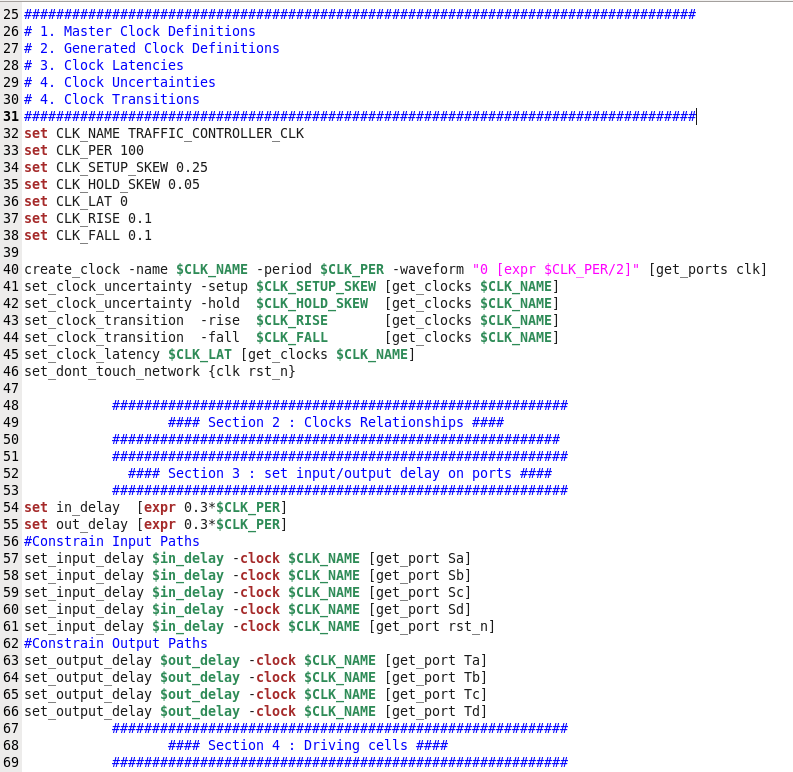
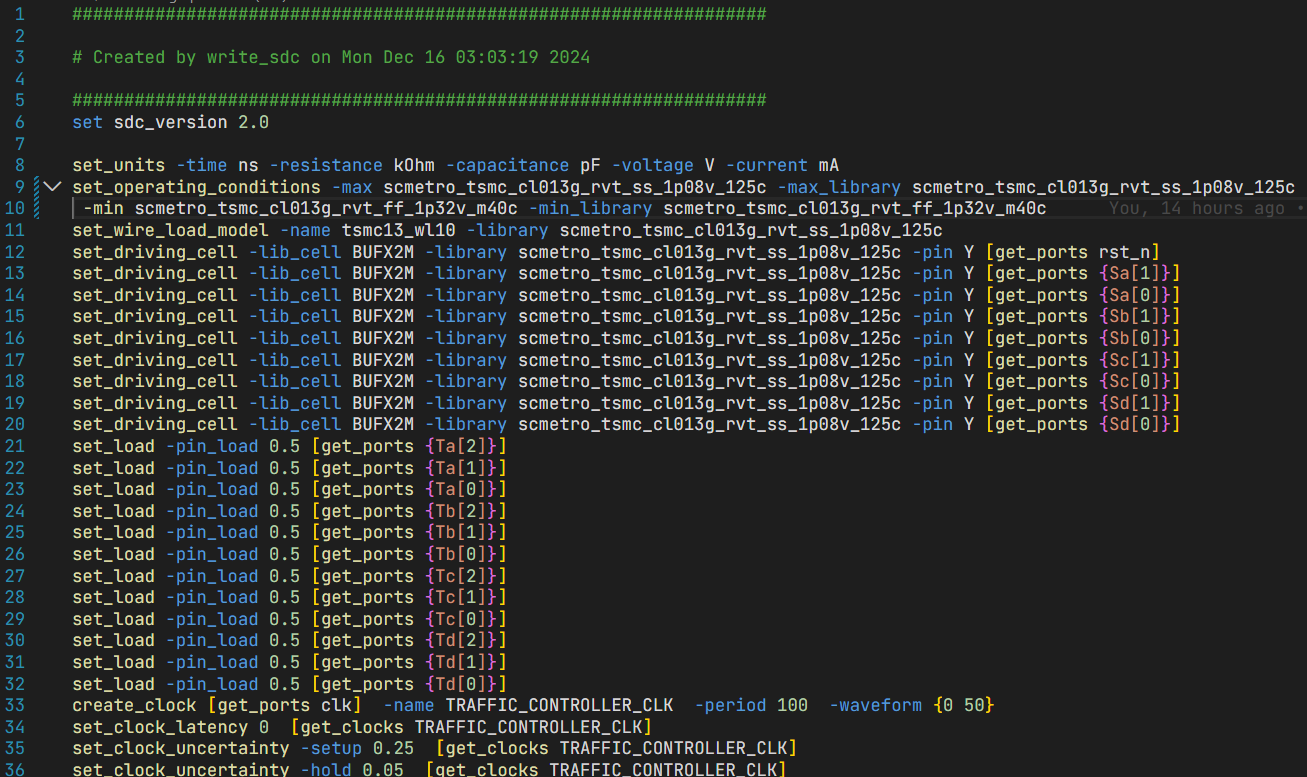
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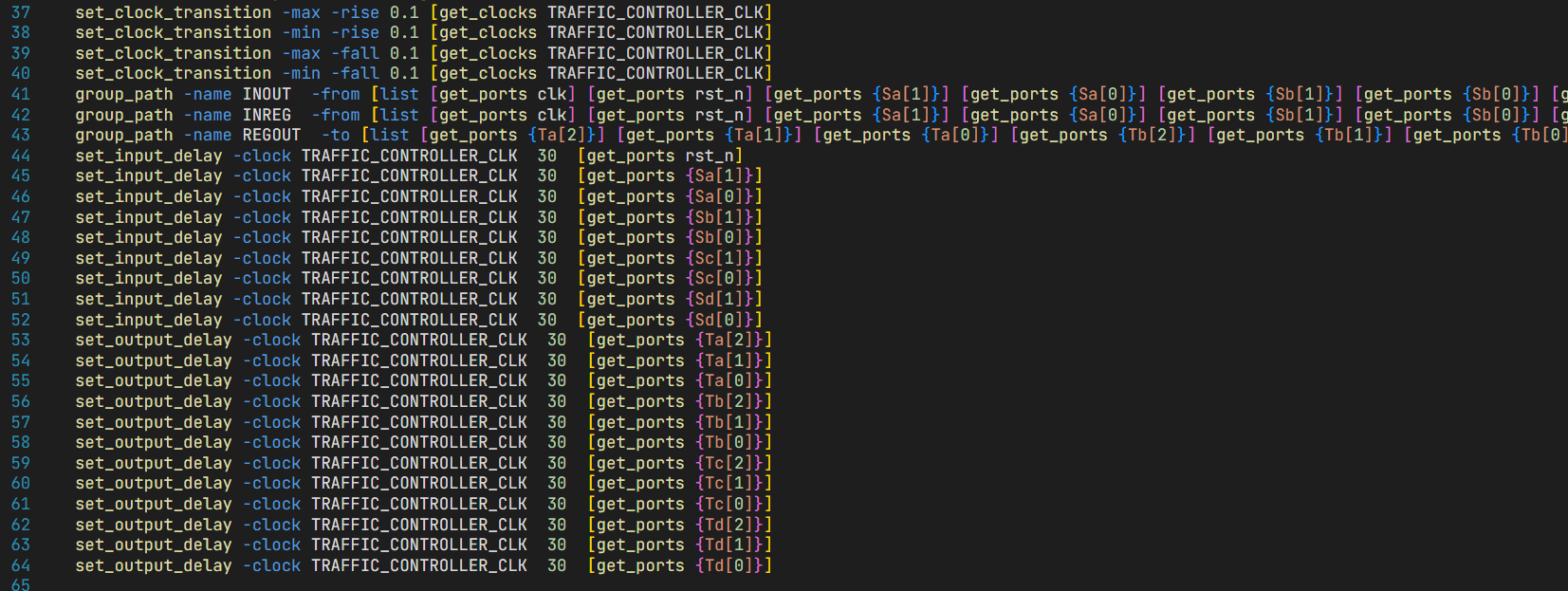
* **constraint Report:**

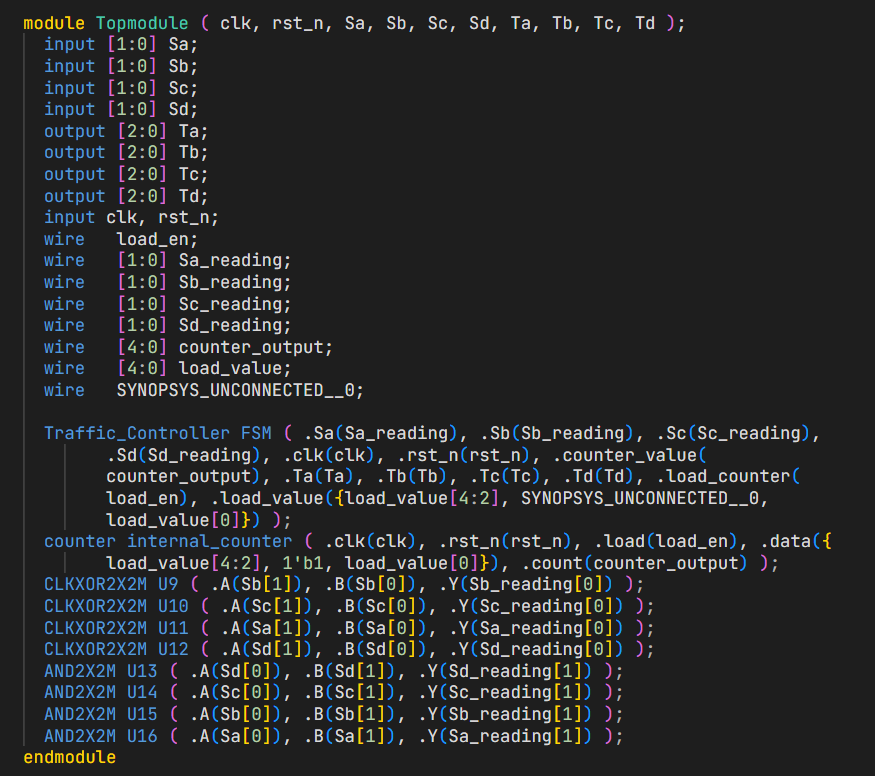
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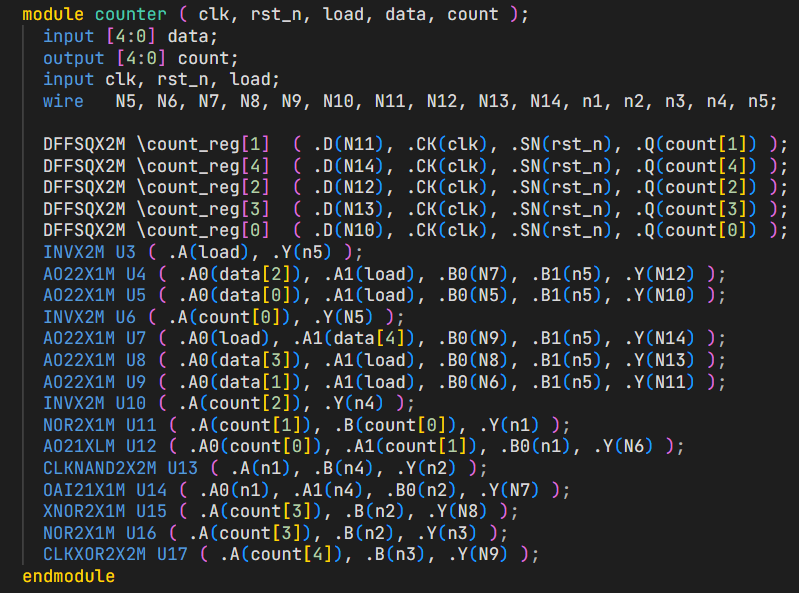
* **scripts files:**
* **syn\_script.tcl:**



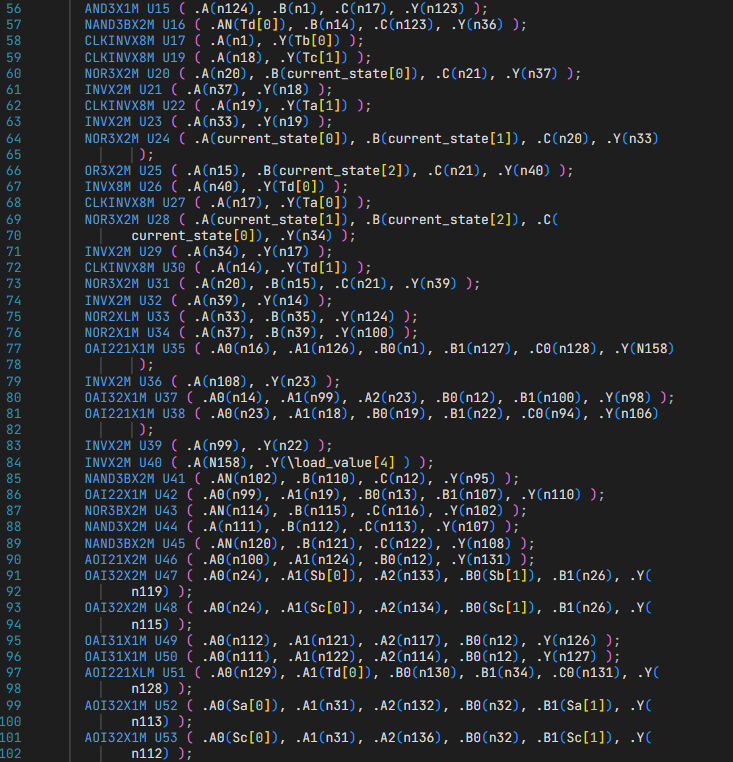
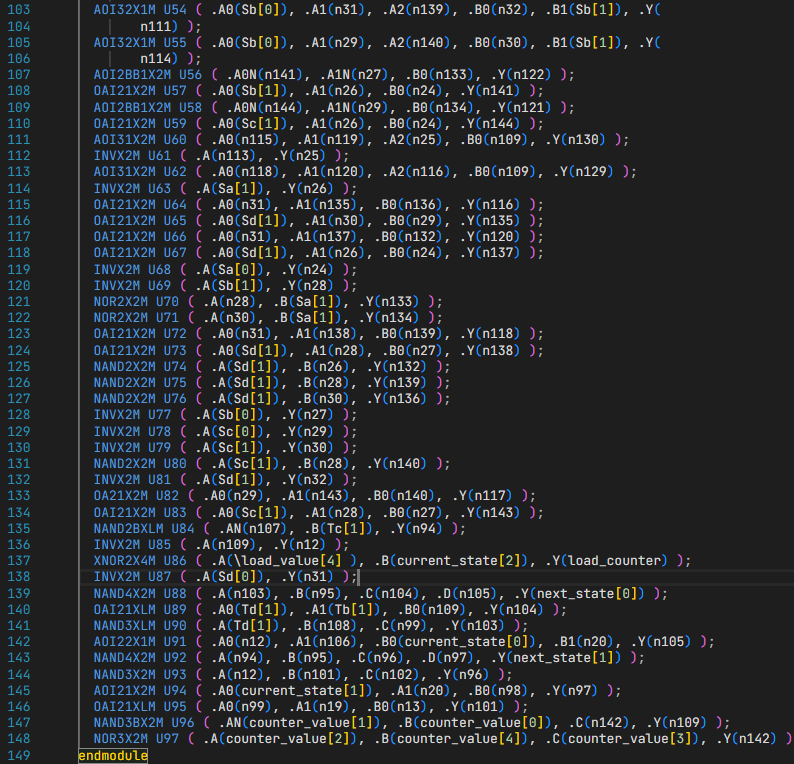
* **cons.tcl:**
* **Topmodule.sdc:**

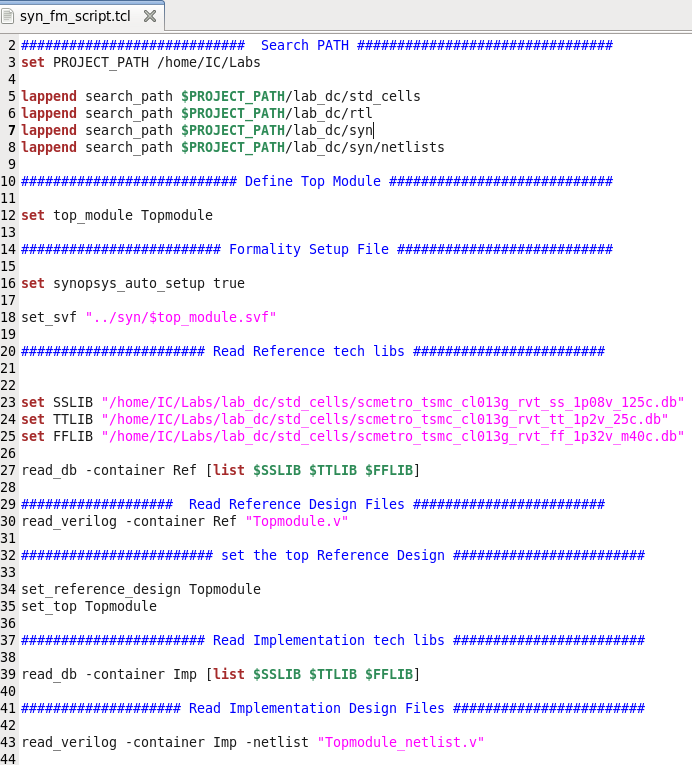
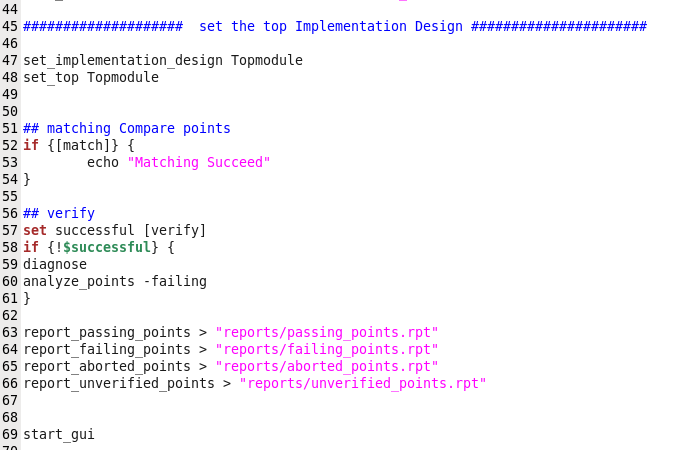


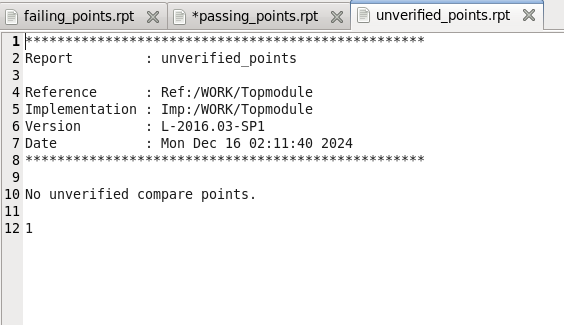
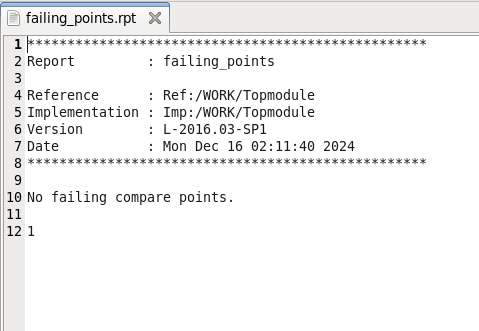
* **Netlist:**

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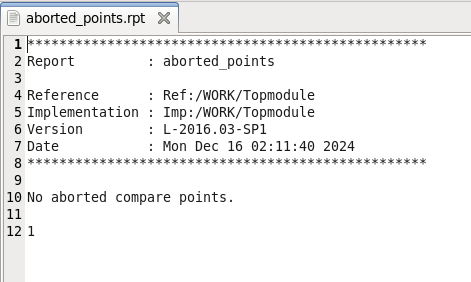
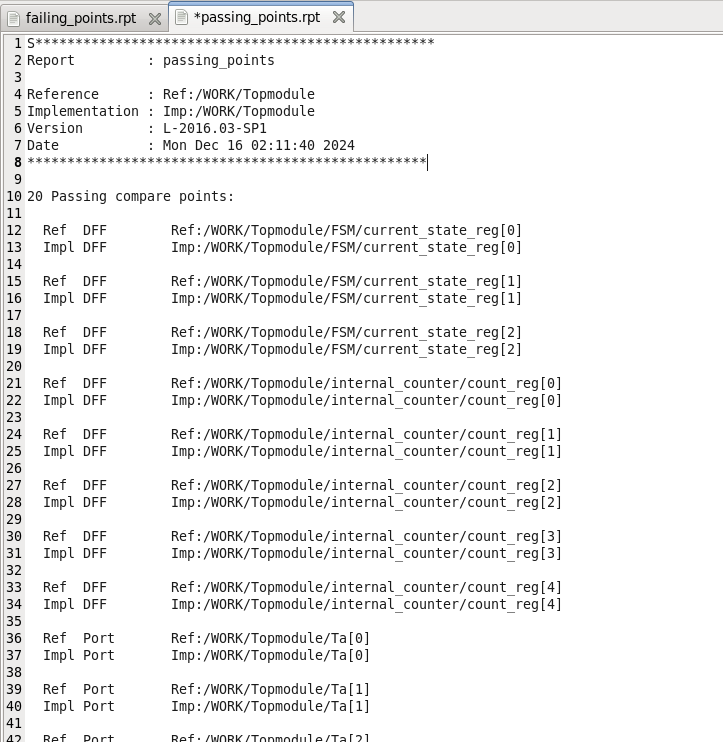
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* **Formal Verification:**
* **Script:**
* **Reports:**

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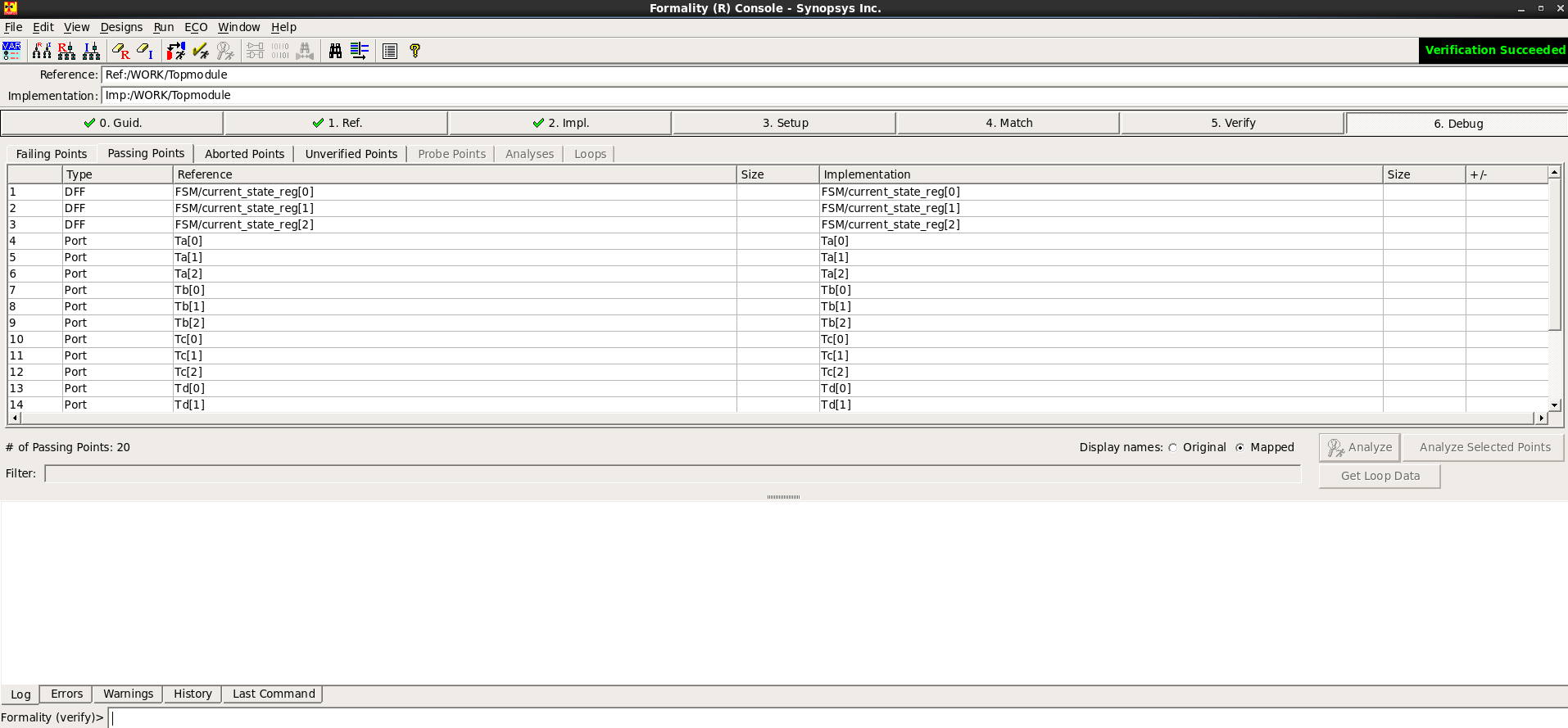
**Unverified points**

**Failing points**

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**Abroted points**

**Passing points**

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