# Session 2 Exercise

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* Indicates required question

Which of the following constraints ensures that a value is within a given range? * 1 point

- inside
- size()
- range_constraint
- scope

What does the typedef keyword allow you to do in SystemVerilog? * 1 point

- Define constant values
- Create new modules
- Declare enumerated types
- Define constant valueDefine new types that can be used as type aliases

What is the purpose of the enum keyword in SystemVerilog? * 1 point

- To define a fixed-size array
- To create meaningful names instead of numerical values, specially on waveforms
- To declare a dynamic array
- To define a new type of class
- convert from numbers to string

When using foreach looping, which of the about the loop variable? * 1 point

- you must firstly declare a loop counter
- it is created automatically

Answer The following Question: * 1 point

```
Given the following code sample :
bit[7:0] my_mem [3] = '{default:5'hA4};
logic [3:0] mem_logic [5] ='{0 , 1 , 2 , 3 , 4 };
logic [3:0] my_logic= 4'h6;
evaluate in order:
1)  my_mem[3] = my_logic ;
2)  my_mem[2] =mem_logic[5];
3)  my_logic = mem_logic[5];
```

- i) ignore ii) X iii) 0
- i) X ii) ignore iii) 0
- i) ignore ii) 0 iii) X
- i) 4'h6 ii) 4 iii) 5

**What is the default weight for a value in a dist distribution if no weight is specified?** * 1 point

- 0
- 1
- 10
- The compiler generates an error.

**What happens if a class constructor is not defined in SystemVerilog?** * 1 point

- The compiler generates an error.
- A default constructor is automatically provided.
- The class cannot be instantiated.
- The class becomes abstract.

**while using foreach (looping) , it start with LSB** * 1 point

- True
- False

What does the toupper() string method do in SystemVerilog? *

1 point

- Converts all lowercase characters to uppercase
- Converts all uppercase characters to lowercase
- Reverses the string
- Removes whitespace

2-states are .. and 4-states are .. *

1 point

- 0, 1 .. 0, 1, X, Z
- X, Z .. B, H, X, Z
- Other:

Which type of array is generally used to represent registers in hardware design? *

1 point

- Unpacked arrays
- Packed arrays
- Both types
- Neither type

Which SystemVerilog datatype is used to store and manipulate text data? * 1 point

- bit
- int
- string
- logic

Which of the following statements best describes constraints in SystemVerilog? * 1 point

- Constraints define the maximum and minimum values for random variables.
- Constraints are used to control the execution time of random tests.
- Constraints enforce specific relationships or rules between random variables.
- Constraints are used to seed the random number generator.

Which method is used to perform object-level randomization in SystemVerilog? * 1 point

- rand()
- randomize()
- generate()
- randc()

Class constructor must be defined when we write down a new class. * 1 point

- True
- False

What is a primary advantage of randomized testing over directed testing in terms of coverage? * 1 point

- Randomized testing can help us reach 100% coverage faster.
- Directed testing guarantees 100% coverage of all scenarios.
- Randomized testing is slower to implement than directed testing
- Directed testing allows for more variations in test cases.

Which format specifier is used to print arrays? * 1 point

- %t
- %a
- %p

Array reduction methods results in a data of the same data type of the array. * 1 point

- True
- False

Which method returns the length of a SystemVerilog string? * 1 point

- len()
- size()
- length()
- strlen()

Which operator is used to provide weighted distribution in constraint blocks? * 1 point

- rand
- inside
- randc
- dist

**What happens if a constraint cannot be satisfied during randomization?** * 1 point

- The randomize() method returns 0.
- The randomize() method returns 1.
- The compiler generates an error.
- The variable is set to its default value.

When declaring a dynamic array, the dynamic dimension must be .. * 1 point

- packed
- unpacked

Constraint blocks are used for * 1 point

- declaring more than one task in a block
- Handling the randomization process for a class properties (variables)
- Special Behavioural block in systemverilog for adding stimulus in the testbench

What happens when you call delete() on a dynamic array in SystemVerilog? * 1 point

- Remove all elements and deallocate memory
- It converts the array to a queue
- It sets all elements to zero
- It resizes the array to 1 element

.....to hit this default with ( legal way only ) , we can * 1 point

```
// Do the operation
always @* begin
   case (Opcode)
      Add:            Alu_out = A + B;
      Sub:            Alu_out = A - B;
      Not_A:          Alu_out = ~A;
      ReductionOR_B:  Alu_out = |B;
     default:  Alu_out = 5'b0;
   endcase
end // always @ *
```

- Remove this default to increase the statement and branch coverage.
- Assign opcode to 2'bXX
- We can't hit this default, we can exclude it .

Can a package contain multiple classes, functions, and variables? * 1 point

- ○ No, a package can only contain one class.
- ○ Yes, a package can contain multiple classes, functions, and variables.
- ○ A package can only contain variables and functions, not classes.
- ○ Only functions can be included in a package.

Which operations are supported for multidimensional arrays in SystemVerilog? * 1 point

- ☐ Copy
- ☐ Add
- ☐ Multiply
- ☐ Compare

**What is a class in SystemVerilog?** * 1 point

- ○ A data type that represents a collection of variables and methods.
- ○ A hardware block used in synthesis.
- ○ A pre-defined SystemVerilog task.
- ○ A type of procedural block.

Which of the following is a class handle? * 1 point

- ○ class_inputs my_inputs;
- ○ class_inputs my_inputs = new();
- ○ class_inputs my_inputs = 1;

An element which is out of dimension bounds in a fixed size array is returned as * 1 point

- ○ X
- ○ Zero
- ○ X if 4-state and zero if 2-state
- ○ random value

Class can have any of the following * 1 point

- ☐ Variables
- ☐ Tasks
- ☐ Functions
- ☐ module instantiation

**Which of the following is true about class properties in SystemVerilog?** * 1 point

- ◯ Properties can only be of type int.
- ◯ Properties can be variables, constants, or user-defined data types.
- ◯ Properties must always be declared as static.
- ◯ Properties cannot be accessed outside the class.

**Accessing an element in an array of multidimension, you access firstly the.....dimension from left side then the.....dimension from the left side also** * 1 point

- ◯ packed, unpacked
- ◯ unpacked,packed
- ◯ you choose the method at the start of your code

**What happens if you do not specify any constraints during randomization?** * 1 point

- ◯ The random values will be generated within default limits.
- ◯ The random values will be generated without any restrictions or checks.
- ◯ The random values will always be zero.
- ◯ The random values will be deterministic.

Can a package in SystemVerilog be used across multiple files? * 1 point

- No, packages are limited to the file they are defined in.
- Yes, packages can be used across multiple files once imported.
- A package can be used only in the same module.
- Packages can be used only in the file where they are instantiated.

What happens if there are conflicting constraints in SystemVerilog randomization? * 1 point

- The simulator will use default values
- The values will be randomly generated without constraints
- The constraint solver will return an error
- The constraints will be ignored

How can constraints affect the quality of a random test? * 1 point

- Constraints reduce the quality by making tests less diverse.
- Constraints improve the quality by ensuring tests meet specific criteria.
- Constraints have no impact on the quality of a random test.
- Constraints only affect the speed of random test generation.

What is the primary purpose of using constraints during randomization in SystemVerilog? * 1 point

- To control the randomness of the generated data
- To ensure that generated values are always unique
- To increase the randomness of generated values
- To define the seed for the random number generator

If you have three cupboards in your house, each one has three shelves and each shelve is divided into four areas,
If you wanted to map the past example to a systemverilog array, the dimension concerning the number of cupboards is....., the dimension of the divided area of the shelve is.... * 1 point

- packed,unpacked
- unpacked,packed

What does the following declaration represent in SystemVerilog: bit [3:0] arr[5:0];? * 1 point

- 6 unpacked elements, each element is composed of 4 packed bits
- 6 packed elements, each element is composed of 4 unpacked bits
- A 2D array with dimensions 3x5
- A 1D array with 5 elements each of 4 bits

How can we easily fix the issues with reduction methods when using array.sum and the array is declared of datatype bit * 1 point

- ◯ use foreach
- ◯ use type conversion
- ◯ use typedef
- ◯ use dynamic array

at posedge clk : rst = 1 and D=4'b1111 , then Y= ..... and Vaild = ..... in the following code . * 1 point

```
always @(posedge clk) begin
  if (rst)
     Y <= 2'b0;
  else
    casex (D)
      4'b1000: Y <= 0;
      4'bX100: Y <= 1;
      4'bXX10: Y <= 2;
      4'bXXX1: Y <= 3;
    endcase
    valid <= (~|D)? 1'b0: 1'b1;
end
endmodule
```

- ◯ Y = 2'b0 , Valid = 0
- ◯ Y = 2'b01 , Valid = 0
- ◯ Y = 2'b0 , Valid = 1
- ◯ None above

If you have a class named class_inputs, which of the following creates an object of it? * 1 point

- class_inputs my_inputs;
- class_inputs my_inputs = new();
- class_inputs my_inputs = 1;

What is the main difference between packed and unpacked arrays in SystemVerilog? * 1 point

- Packed arrays can only contain integers, while unpacked arrays can contain any data type.
- Unpacked arrays are always fixed-size, while packed arrays are always dynamic.
- Packed arrays can be dynamically resized, while unpacked arrays cannot.
- Packed arrays are contiguous in memory while unpacked arrays are not necessarily contiguous.

Which of the following is an example of an unpacked array declaration? * 1 point

- logic data[3:0];
- bit [3:0] data;
- int data[5];
- byte data = new[10];

What is unique in using randc modifier compated to rand modifier? * 1 point

- randc provides better random distribution.
- randc is faster than rand.
- randc and rand have the same effect on randomization
- randc generates values in a cyclic manner, ensuring all possible values are used before repeating.

What is the primary purpose of a package in SystemVerilog? * 1 point

- To provide a way to share common typedefs, parameters, etc.
- To instantiate modules
- To manage simulation timing
- To connect different modules together

Which keyword is used to specify constraints in SystemVerilog? * 1 point

- limits
- randvar
- constrain
- constraint

What is a common use case for a packed array in SystemVerilog? * 1 point

- Storing data in a compact form, such as memory word
- Managing dynamically sized lists or queues.
- Representing multidimensional data with varying sizes.
- Holding data that requires variable bit-widths.

How do you import a package into a SystemVerilog module? * 1 point

- import package_name::*;
- use package_name::*;
- include package_name;
- require package_name::*;

How would you declare an array with unpacked dimension of 8 with packed 16-bit wide signal? * 1 point

- bit [15:0] signal[7:0];
- bit [7:0] signal[15:0];
- bit signal[15:0];
- bit [15:0] signal;

Name * 1 point

Choose

**What is the purpose of the new() method in a SystemVerilog class?** * 1 point

- ◯ To delete an object.
- ◯ To initialize an object and allocate memory.
- ◯ To define a static variable.
- ◯ To declare a class.

**What is usually the purpose for a class constructor?** * 1 point

- ◯ Defining new variables
- ◯ Initializing the class variables

**Can we create an object without passing arguments if the class constructor arguments do not have initial values?** * 1 point

- ◯ True
- ◯ False

**In systemverilog you can initialize arrays without getting errors** * 1 point

- ◯ True
- ◯ False

Which of the following is acceptable constraint in SystemVerilog * 1 point

- constraint c_1{lo < med; med < hi;}
- constraint c_2{lo < med < hi;}

Which method is used to resize a dynamic array in SystemVerilog? * 1 point

- resize()
- set_size()
- new()
- delete()

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