# Session 1 Exercise

Total points 52/54

Name *

Dropdown

Fares Khalaf Salman Sultan

✓ Catching a bug in a block costs more than it does in a system * 1/1

- ○ True
- ◉ False ✓

✓ Number of spins for a design is * 1/1

- ○ The number of edits on a design from the customer
- ◉ The number of times the chip went through the tape-out process ✓
- ○ None of the above

✓ The most efficient way for a project is * 1/1

- ( ) Start with the design then verification
- ( ) Start with design and verification at the same time
- (•) Start with planning for verification firstly then going through design and verification in parallel ✓

✓ The tasks in System Verilog are always synthesisable * 1/1

- ( ) True
- (•) False ✓

✓ A non-driven output of type bit gives X on the simulation * 1/1

- ( ) True
- (•) False ✓

✓ The logic data type is a 4-state type and unsigned by default * 1/1

- (•) True ✓
- ( ) False

✓ The code coverage tests how many times you accessed each statement in the design through your test bench *1/1

- (●) True ✓
- ( ) False

✓ The code coverage tests if your design is functioning right * 1/1

- ( ) True
- (●) False ✓

✓ A do file is * 1/1

- (●) Automating script for the tool ✓
- ( ) Replacement for the testbench
- ( ) Encrypted database

✓ We ignore the code coverage details of the ... in the code coverage report *1/1

- ( ) Design
- (●) Testbench ✓

✓ The default return data type in function is * 1/1

- ○ Int
- ○ Reg
- ◉ Logic ✓

✗ typing " vcover report *****.ucdb -details -annotate -all -output ******.txt " *0/1

- ○ Before simulation
- ◉ After running simulation ✗
- ○ After ending simulation

Correct answer

- ◉ After ending simulation

✓ It is recommended to declare the signal that will be connected to the DUT output port in the testbench to be of .... data type *1/1

- ○ 2-state
- ◉ 4-state ✓
- ○ Any of them

✓ The main root cause of ASIC functional flaws * 1/1

- (●) Design Error ✓
- ( ) Changing specification
- ( ) Flaw in internal reused block cell magacell or ip

✓ Most of verification engineers spend time on * 1/1

- ( ) Test planning
- ( ) Testbench deverlopment
- (●) Debugging ✓

✓ Dynamic verification doesn't use testbench * 1/1

- ( ) True
- (●) False ✓

✓ Code coverage measures the correctness of the design, not how thoroughly your tests exercised the design. *1/1

- ( ) True
- (●) False ✓

✓ In Branch coverage details, if/else coverage is reported * 1/1

- (●) True ✓
- ( ) False

✓ What is the acceptable percntage of coverage for critical applications *1/1

- ( ) 80 - 100 %
- ( ) 60 - 100 %
- (●) 100 % ✓
- ( ) none above

✓ Number of Bins for toggle coverage are.....(where n is number of bits in the DUT) *1/1

- (●) 2n ✓
- ( ) n
- ( ) n^2

✓ What is the primary reason for the increasing need for digital verification in IC design? *1/1

- (●) IC complexity is increasing ✓
- ( ) Transistor sizes are getting larger
- ( ) Verification is easier than design
- ( ) Manufacturing costs are decreasing

✓ Which language is predominantly used in modern IC verification? * 1/1

- ( ) Verilog
- ( ) VHDL
- (●) SystemVerilog ✓
- ( ) Assembly

✓ What is the primary goal of verification? * 1/1

- ( ) Improve power efficiency
- ( ) Reduce the number of transistors
- (●) Detect design bugs before tape-out ✓
- ( ) Increase clock frequency

✓ Which of the following is a 2-state data type in SystemVerilog? * 1/1

- reg
- logic
- bit ✓
- wire

✓ What are the possible values of a 2-state bit in SystemVerilog? * 1/1

- 0, 1, X, Z
- 0, 1 ✓
- X, Z
- 0, 1, Z

✓ What is the advantage of 2-state data types over 4-state data types * 1/1

- It supports more states
- It uses less memory ✓
- It allows X and Z values
- It is required for combinational logic

✓ Which of the following SystemVerilog types is an upgrade to reg in Verilog? *1/1

- ○ bit
- ◉ logic ✓
- ○ wire
- ○ int

✓ What is the key difference between a function and a task in SystemVerilog? *1/1

- ○ A function can have delays, but a task cannot
- ◉ A task can have delays, but a function cannot ✓
- ○ A function can call a task, but a task cannot call a function
- ○ Functions return multiple values, while tasks return a single value

✓ Which of the following statements about SystemVerilog tasks is true? *1/1

- ○ They cannot include delays
- ○ They cannot call functions
- ○ They can return a value
- ◉ They can call other tasks ✓

✓ Which of the following statements is true about SystemVerilog functions? *1/1

- ○ They can contain delays
- ○ They cannot return a value
- ◉ They must execute within a single time step ✓
- ○ They can contain blocking assignments only

✓ What is the default return type of a SystemVerilog function? * 1/1

- ○ int
- ○ bit
- ○ void
- ◉ logic ✓

✓ Which of the following is NOT a type of code coverage? * 1/1

- ○ Statement coverage
- ○ Branch coverage
- ○ Functional coverage
- ◉ Power coverage ✓

✗ What is the purpose of statement coverage? * 0/1

- (●) Ensure all possible paths in a design are tested ✗
- ( ) Verify that every executable statement in the code is executed at least once
- ( ) Check that each signal transition is exercised
- ( ) Reduce simulation time

Correct answer

- (●) Verify that every executable statement in the code is executed at least once

✓ Which of the following coverage types ensures all conditional branches are executed? *1/1

- ( ) Statement coverage
- (●) Branch coverage ✓
- ( ) Toggle coverage
- ( ) Path coverage

✓ Which of the following is a major driver for the increased importance of digital verification? *1/1

- ○ Increasing complexity of IC designs
- ○ Decreasing time-to-market pressures
- ○ Rising cost of design errors
- ◉ All of the above ✓

✓ Why is early verification in the design cycle important? * 1/1

- ○ To reduce the cost of fixing bugs later
- ○ To improve design quality
- ○ To meet tight deadlines
- ◉ All of the above ✓

✓ Which datatype is suitable for modeling signals with unknown or high-impedance states? *1/1

- ○ bit
- ○ int
- ◉ logic ✓
- ○ byte

✓ What is the default datatype in SystemVerilog if no explicit datatype is specified? *1/1

- bit
- logic ✓
- int
- reg

✓ How is a non-void function called in SystemVerilog? * 1/1

- As a standalone statement.
- As an expression within an assignment. ✓
- Using the fork join statement.
- Using the begin end statement.

✓ How is a task called in SystemVerilog? * 1/1

- As an expression within an assignment.
- As a standalone statement. ✓
- Using the generate statement.
- Using the package statement.

✓ What is the purpose of using subroutines in SystemVerilog? * 1/1

- ○ To improve code reusability
- ○ To simplify complex logic
- ○ To enhance code readability
- ◉ All of the above ✓

✓ Code Coverage acts like a detective in your verification process. What is it primarily trying to solve? *1/1

- ○ Whether the testbench is functionally correct
- ◉ Whether all lines of RTL have been executed during simulation ✓
- ○ Whether the design meets timing constraints
- ○ Whether all possible input values are tested

✓ If a piece of RTL code has an if-else condition, what type of coverage will ensure that both if and else blocks are exercised? *1/1

- ○ Statement Coverage
- ○ Toggle Coverage
- ◉ Branch Coverage ✓
- ○ FSM Coverage

✓ Your RTL design has a register that is expected to toggle frequently. Which coverage metric ensures that it switches between 0 and 1? *1/1

- ○ Branch Coverage
- ○ Statement Coverage
- ◉ Toggle Coverage ✓
- ○ Path Coverage

✓ Finite State Machine (FSM) coverage is used to verify state transitions. What does it help identify? *1/1

- ○ Whether all states are reachable
- ○ Whether all possible transitions between states occur
- ○ Whether certain transitions are missing in the testbench
- ◉ All of the above ✓

✓ You ran a simulation and found that 100% Statement Coverage was achieved. Does this mean the design is fully verified? *1/1

- ○ Yes, because every line of code was executed
- ◉ No, because the DUT can have missing functionality ✓
- ○ Yes, because Code Coverage ensures complete verification

✓ What happens if an uncovered code block exists in your design? * 1/1

- (●) Testbench might have missed an important scenario ✓
- ( ) It proves the RTL has a bug
- ( ) It forces a re-synthesis of the design
- ( ) It reduces power consumption

✓ Which of the following statements about Code Coverage is FALSE? * 1/1

- (●) 100% Statement Coverage means all branches were tested ✓
- ( ) Code Coverage does not measure functionality, only execution
- ( ) FSM Coverage ensures all state transitions occur
- ( ) Toggle Coverage is useful for verifying flip-flop activity

✓ If a certain case statement in Verilog is missing a default condition, which type of coverage might highlight this issue? *1/1

- ( ) FSM Coverage
- ( ) Statement Coverage
- (●) Branch Coverage ✓
- ( ) Condition Coverage

✓ In a SystemVerilog mystery lab, a function and a task are competing. What is one key rule that makes the function different? *1/1

- ( ) Functions can have timing controls, but tasks cannot
- (•) non-void functions must return a value, while tasks cannot return anything ✓
- ( ) Tasks execute instantly, but functions take multiple simulation cycles
- ( ) Functions can call tasks, but tasks cannot call functions

✓ You are designing a SystemVerilog function that calculates the sum of two numbers. Which of the following would cause a syntax error? *1/1

- ( ) Using input arguments inside the function
- (•) Including a #5; delay inside the function ✓
- ( ) Returning a value from the function

✓ Why would you choose a task over a function in SystemVerilog? * 1/1

- ( ) If you need to execute in zero simulation time
- ( ) If you need to use blocking and non-blocking assignments
- (•) If you need to include delays or wait statements ✓
- ( ) If you need to perform a simple mathematical operation

✓ What happens if a non-void function in SystemVerilog does not explicitly return a value? *1/1

- (●) The simulator will throw a syntax error ✓
- ( ) The function will return an undefined value (X)
- ( ) The function will return 0 by default
- ( ) The function will execute but with unpredictable results

✓ If u have a signed 5 bits, then .. * 1/1

- ( ) max_pos = 32 , max_neg = -32
- ( ) max_pos = 31 , max_neg = -32
- (●) max_pos = 15 , max_neg = -16 ✓