Assignment 6 - UVM

This assignment is to practice writing a UVM testbench environment for the ALSU design. Check the notes and classwork codes uploaded on Google classroom to do the assignment. The ALSU design was shared previously. Don't forget to import uvm_pkg and uvm_macros in **all** files.
Each class created will be in a separate file and in a package.

Full ALSU environment:

- Create a full environment for the ALSU design, the same environment done for the shift register.
- Copy the constraints done in the previous assignments for ALSU in the sequence item class.
- Copy the covergroups, coverpoints done in the coverage collector class.
- Add assertions file and bind it in the top module, assertions should check the functionality for the out and leds checking all cases, valid and invalid.