Sabitha Susan Joseph | **183079028**
Electrical Engineering | **M.Tech.**
Indian Institute of Technology, Bombay | **Gender: Female**
Specialization: Electronic Systems | **DOB: 11-10-1993**

Examination	University	Institute	Year	CPI / %
Post Graduation	IIT Bombay	IIT Bombay	2021	9.13
Graduation	University of Kerala	College of Engineering Trivandrum	2015	8.42
Graduation Specialization: Applied Electronics and Instrumentation				
Intermediate	CBSE	Holy Angels School, Vanchiyoor	2011	92.00%
Matriculation	CBSE	Holy Angels School, Vanchiyoor	2009	92.60%

KEY SKILLED AREAS

Digital VLSI Design, System Design, Mixed Signal VLSI Design, Analog VLSI Design

RELEVANT COURSES

- VLSI Design
- DSP-System Design & Implementation
- Systems Design
- Mixed-Signal VLSI Design
- Foundation of VLSI CAD
- CMOS Analog VLSI Design

PROFESSIONAL EXPERIENCE

- **TISMO Technology Solutions** | Designation: **Electronics Engineer** *Jun '15 - May' 17*
  - o Developed high-level electronic designs with detailed **schematic and layout design** in **Altium Designer**
  - o **Procured** the components and **coordinated fabrication** as well as **assembly** of the developed PCB designs
  - o Maintained associated technical documents and project **documentation** in accordance with the project plan
  - o **Tested** the developed designs, prepared the **test reports** and followed up on the **defect handling process**

MAJOR PROJECT AND SEMINAR

- **M.Tech Thesis** *Jun '20 - Present*
  Title: Enhancement of SAR ADC resolution using I-ΣΔ DAC for CDAC calibration
  Guide: *Prof. Maryam Shojaei Baghini, Dept. of EE, IIT Bombay*
  - o Literature review of various **hybrid architectures** of SAR ADC for resolution enhancement
  - o System-level design and simulation of the 12-bit SAR ADC using ideal blocks in Cadence
  - o Verilog implementation of SAR logic for monotonic switching scheme and Merged Capacitor switching scheme
  - o Ongoing and future work includes implementation of the **Calibration technique** for the calibration of 12-bit SAR ADC Capacitive DAC (CDAC) using an **Incremental Sigma-Delta DAC** in UMC 180-nm Technology
- **M.Tech Seminar** *Nov '19*
  Title: Overview of hybrid SAR ADC architectures for enhanced Power and Area Efficiency
  Guide: *Prof. Maryam Shojaei Baghini, Dept. of EE, IIT Bombay*
  - o Review of 10-bit SAR ADC with hybrid Cap-MOS DAC which is more efficient than binary-weighted CDAC
  - o Review of 13-bit SAR-Incremental Sigma-Delta Modulator ADC with an opamp-less time-domain integrator

KEY COURSE PROJECTS AND ASSIGNMENTS

- **Implementation of an 8-bit Dadda Multiply and Accumulate circuit** | *VLSI Design* *Nov '18*
  - o Implemented half and full adders as behaviourally described building blocks for unsigned 8-bit MAC operation
  - o Implemented the design in Verilog and simulated the design with random test vectors using **Icarus Verilog**
- **Implementation of a 32-bit Brent Kung adder** | *VLSI Design* *Oct '18*
  - o Designed adder circuit using **domino logic** to generate G and P signals for unsigned addition of 32-bit numbers
  - o Implemented the design in VHDL and simulated in GHDL with proper test vectors to find the worst-case delay
- **Design of SAT Solver** | *Foundation of VLSI CAD* *Nov '19*
  - o Implemented a Conjunctive Normal Form Satisfiability **(CNF-SAT)** problem solver algorithm in **MATLAB**
- **Design of PLL** | *Systems Design* *Mar '19*
  - o Designed and characterised **Bang-Bang phase detector** and **Hogge phase detector** in **Cadence Virtuoso**
  - o Implemented Hogge phase detector based PLL and got center alignment of clock and data in the eye diagram
  - o Analyzed the transient response for step and ramp inputs and frequency response of the PLL in **MATLAB**

- **Design and implementation of Adaptive Equalizer** | *Systems Design* *Apr '19*
  - o Implemented a **4-tap FIR filter** with the tap coefficients being set by **LMS algorithm** in **VerilogA**
  - o Verified filter operation by using 20 Gbps PRBS data received from a matched 10m lossy transmission line
  - o Implemented Continuous Time Linear Equalizer, Decision Feedback Equalizer and Feed Forward Equalizer
  - o Verified the equalizer operations by using PRBS data received from a transmission line in presence of noise

- **Design of Guitar Tuner** | *DSP-System Design & Implementation* *Nov '19*
  - o Implemented a Guitar Tuner based on **Fast Fourier Transform** algorithm on **TMS320C5535** DSP platform
  - o Implemented spectral peak location algorithms for the frequency estimation of tones based on FFT samples
  - o Achieved a frequency **resolution of ±1 Hz** with just a sampling frequency of 8000 Hz and 2048 point FFT

- **Design & layout of Operational Transconductance Amplifier** | *CMOS Analog VLSI Design* *Oct '18*
  - o Designed **fully differential input**, single-ended output **2 stage Folded Cascode** OTA in Cadence Virtuoso
  - o Implemented $\mathbf{R_z}$ **tracking** for pole-zero cancellation and layout of the design in **180-nm CMOS** Technology
  - o Followed **common centroid technique** for the layout and verified the post-layout simulations using **Calibre**

- **Design & characterisation of a 4-bit 1 GS/s Folding Flash ADC** | *Mixed-Signal VLSI Design* *Feb '19*
  - o Designed and implemented differential track and hold circuit followed by variable gain amplifier, folding network and unity gain buffer in **45-nm CMOS** Technology in Cadence Virtuoso
  - o Designed and implemented 3-bit flash ADC using **StrongARM Latch** based LSB comparator with provisions for **reference subtraction** and **kickback reduction** that settles within 1 LSB (4-bits) of DC rail in 200 ps

- **Simulation of 16-PAM Transceiver** | *Mixed-Signal VLSI Design* *Mar '19*
  - o Designed 4-bit differential **Current Steering** DAC & obtained ENOB of 3.995 bits in 45-nm CMOS Technology
  - o Analysed the effect of frequency, length & characteristics of transmission line on SNDR and SFDR of transceiver
  - o Integrated and characterized complete 16-PAM transceiver with ADC and DAC using microstrip line as channel

- **Voltage Controlled Oscillator using Switched Capacitors** | *Electronic Systems Design* *Nov '18*
  - o Implemented a stray insensitive **Switched Capacitor** based VCO that works using **single DC power supply**
  - o Generated **non-overlapping clocks** by passing 555 Timer output through a circuit with NOR & NOT Gates

ACHIEVEMENTS

- Awarded with certificate of **Excellence** in **Research Assistantship** for Electronic Circuits Lab, Spring 2019
- Secured **99.37** percentile in **Electronics and Communication GATE 2018** among **1,25,870** candidates
- Secured **AA grade** in **Foundation of VLSI CAD** course among **71** candidates
- **School Topper** in Central Board of Secondary Education XIIth Examination, 2011

TECHNICAL SKILLS

- **Tools:** Cadence Virtuoso, Altium, Ngspice, MATLAB, Code Composer Studio, Eagle, XCircuit, LaTeX
- **Languages:** Verilog, VHDL, VerilogA, C, C++ | **Hardware:** TMS320C5535 eZdsp board

POSITIONS OF RESPONSIBILITY

- **Research Assistant** | Wadhwani Electronics Laboratory, IIT Bombay *Jul '18 - Present*
  - o Mentors and evaluates undergraduates enrolled in **'Electronic Devices'** and **'Analog Circuits'** Lab courses
  - o Assists Course Instructors in setting up tutorial sessions, question papers & in the evaluation of answer sheets
- **Student Companion** | Institute Student Companion Program, IIT Bombay *Jun '19 - Mar '20*
  - o Mentored 11 freshmen M.Tech students by providing help and support in academic and non-academic fronts
  - o Helped the Department Coordinators in creating the Department Handbook for the academic year 2019-2020
- **Executive committee member** | ISTE Student Chapter, College of Engineering Trivandrum *Jul'13 - Jun'14*
  - o Organised events and competitions along with crowd management
  - o Set up technical exhibitions open to the general public
- **Student co-ordinator** | Swarm Robotics Workshop conducted, Technophilia Systems *Sept'13*
  - o Handled end to end coordination & overseeing of the 2-day workshop held at College of Engineering Trivandrum

EXTRACURRICULAR ACTIVITIES

- Multiple accolades received for art and cultural events like group song, fabric painting, mehandi designing etc.
- Passionate landscape photographer who loves to explore and capture the everyday experiences of the cityscape
- Enjoys the experiences of craftworks, origami, quilling, painting, designing and decorating personal living spaces