

UNIT 3

Peripheral Devices and Interfacing

Address space Partitioning

How the available memory addresses are allocated to memory locations and I/O Devices

(For 16-bit address bus= $2^{16}=64K$ Bytes)

There are two schemes for the allocation of addresses to memory and I/O devices

1. Memory mapped I/O scheme
2. I/O mapped I/O scheme

Address space Partitioning...Con

1. Memory mapped I/O scheme

In this scheme there is only one address space . Some addresses are assigned to memory and some addresses to I/O devices.

2. I/O mapped I/O scheme

In this scheme the addresses assigned to memory locations are also assigned to I/O devices. (M/IO)

I/O mapped I/O scheme

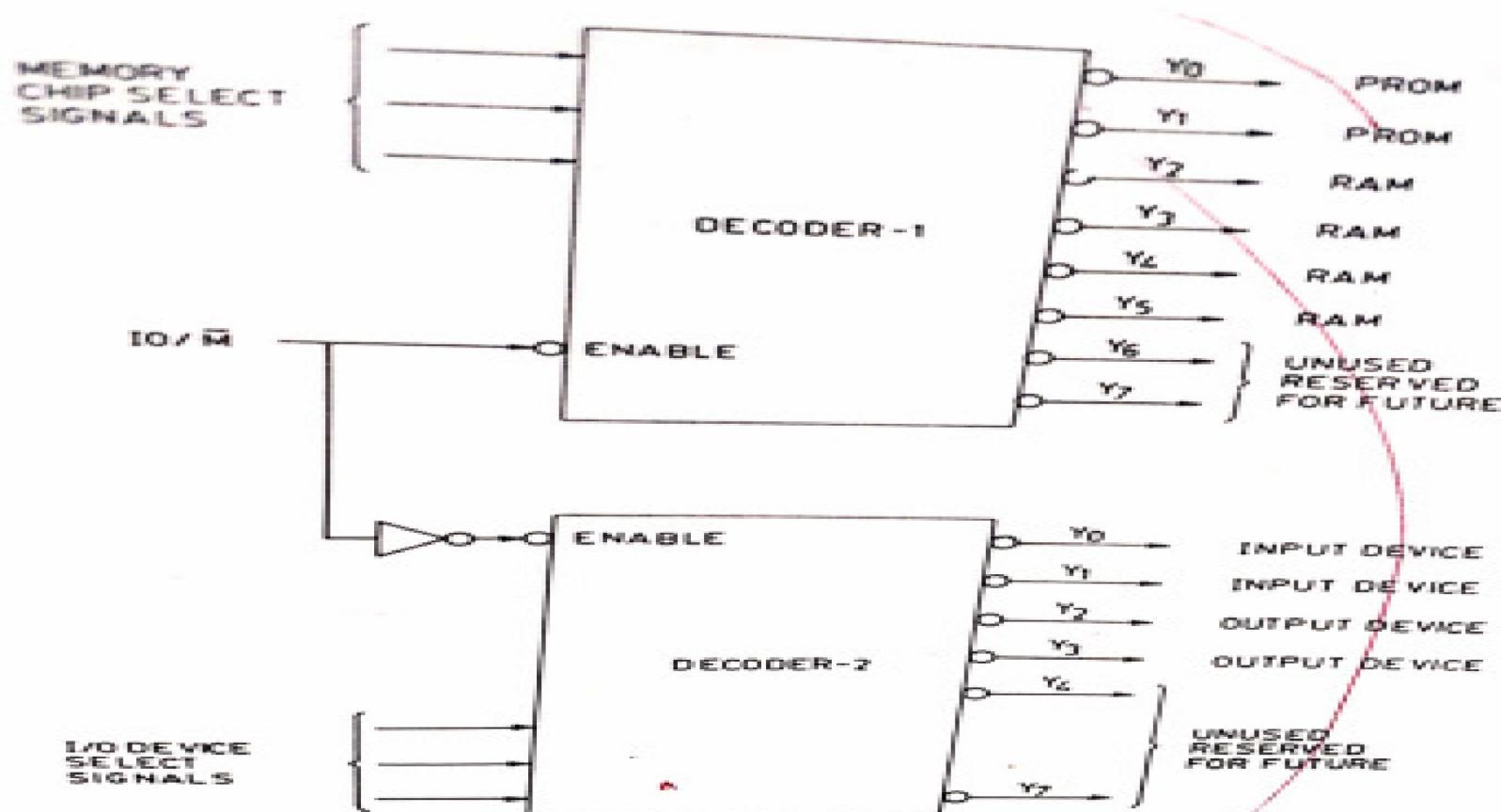


Fig. 7.2 Interfacing of Memory and I/O Devices.

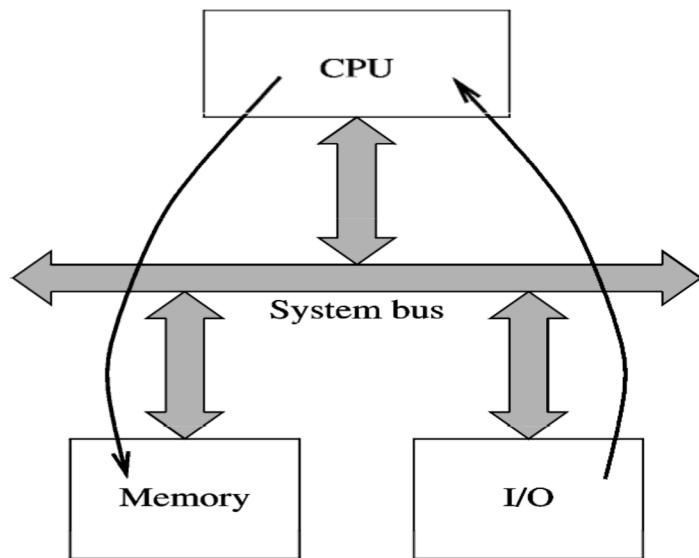
Data Transfer schemes

- In a computer system data transfer can take place between
 - a. Memory and Processor
 - b. Memory and I/O
 - c. Processors and I/O

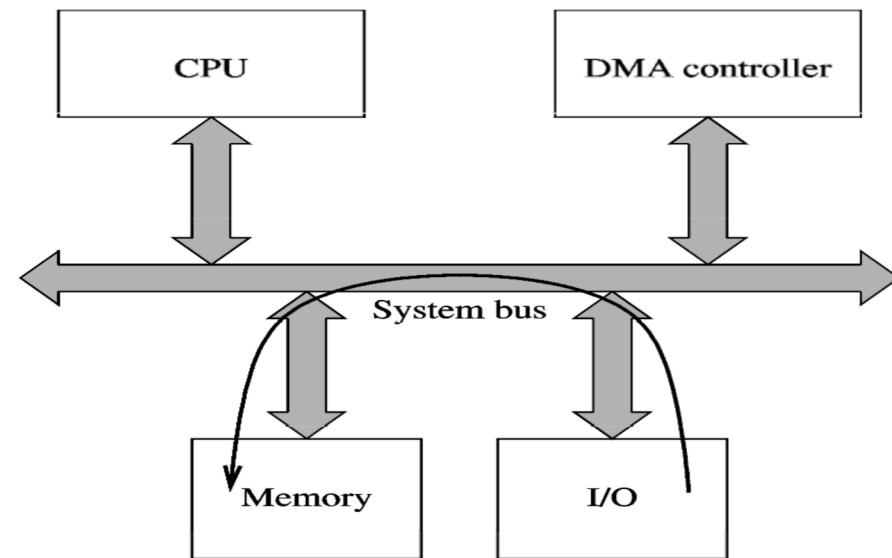
Data Transfer schemes..Con

The data transfer schemes are classified into following two broad categories

1. Programmed data transfer schemes
2. DMA (Direct memory access) data transfer scheme



(a) Programmed I/O transfer



(b) DMA transfer

Data Transfer schemes..Con

1. Programmed data transfer schemes

This scheme is controlled by CPU

This further classified into three categories

- a. Synchronous data transfer scheme
- b. Asynchronous data transfer scheme
- c. Interrupt driven data transfer scheme

Data Transfer schemes..Con

2. DMA (Direct memory access) data transfer scheme

In this scheme CPU does not participate

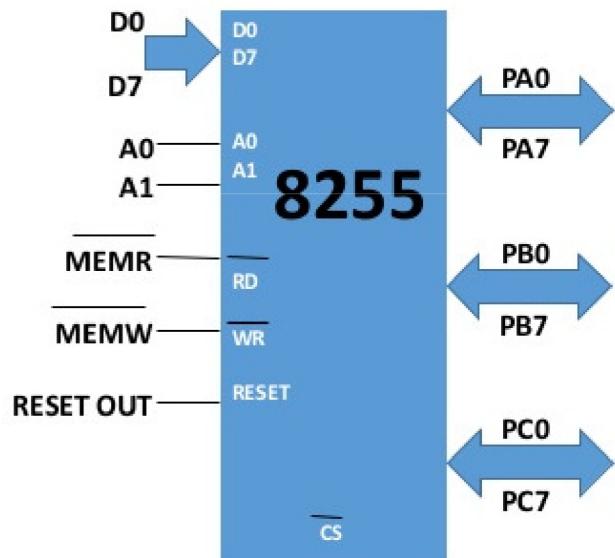
This scheme is further classified into two types

- a. Burst mode of DMA data transfer
- b. Cycle stealing techniques of DMA data transfer

Programmable Peripheral Interface (PPI)/ INTEL 8255

- Known as Multiport Device.
- Useful to interface peripheral devices with Processor.
- Intel 8255 has three 8-bit ports, namely Port A, Port B and Port C. Port C can be further divided into two 4-bit ports, known as Port C (upper) and Port C (Lower)
- Thus there are 4 ports available , two 8-bit ports and two 4-bit ports.

Pin Diagram of INTEL 8255



- 40 pins
- 8 pins for port A
- 8 pins for Port B
- 4 pins for Port C ^{lower}
- 4 pins for Port C ^{upper}
- CS-> Chip Select
- RD- For reading data or Status from 8255 by CPU
- WR- for writing data or control word in 8255
- A0 and A1-> Selection for port and CWR

A ₁	A ₀	Port selected
0	0	port A
0	1	port B
1	0	port C
1	1	control register

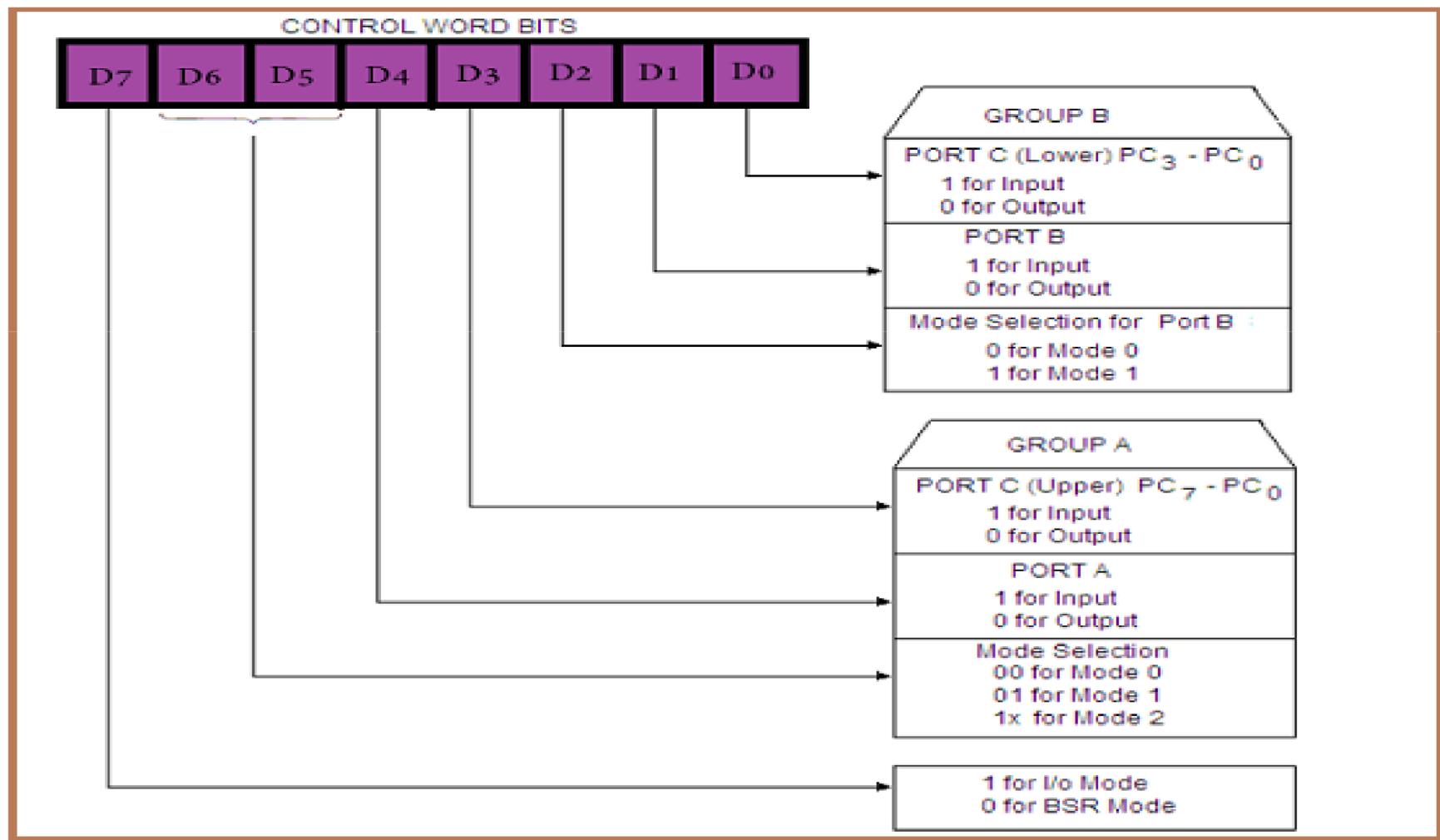
Modes of 8255

- This mode is selected when D₇ bit of the Control Word Register is 1. There are three I/O modes:
 - Mode 0 - Simple I/O
 - Mode 1 - Strobed I/O
 - Mode 2 - Strobed Bi-directional I/O

Modes of 8255..Con

- In Mode 0 any four ports (Port A, Port B, Port C_L and Port C_U) can be programmed as I/O Ports.
- In Mode 1 Port A and Port B can be programmed as I/O port. Some pins are used to control the Port A and Port B and rest of the pins can act as I/O Pins.
- In Mode 2 Port A can be Programmed as Bidirectional Port.

Control Word of 8255



Control Word of 8255..Exp

Q1. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A as an input Port
- Mode of Port A- Mode 0
- Port B as an output Port
- Mode of Port B- Mode 0
- Port C_u as an input port
- Port C_l as an output Port

Ans-

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0

=98H

Control Word of 8255..Exp

Q2. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A-output
 - Port B-output
 - Mode of Port A & B- Mode 0
 - Port C_u-input
 - Port C_l-output

Ans-

Control Word of 8255..Exp

Q3. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A-Input
 - Port B-output
 - Mode of Port A & B- Mode 1
 - Remaining pins of Port C_u (PC₆ and PC₇)-input

Ans-

Control Word of 8255..Exp

Q4. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A-output
 - Port B-output
 - Mode of Port A & B- Mode 1
 - Remaining pins of Port C_u (PC₄ and PC₅)—input

Ans-

Control Word of 8255..Exp

Q5. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A-output
- Port B-output
- Mode of Port A - Mode 1
- Mode of Port B - Mode 0
- Port C_l (PC₀ and PC₂)—output
- Remaining pins of Port C_u (PC₄ and PC₅)—output

Ans-

D7	D6	D5	D4	D3	D2	D1	D0

= H

Control Word of 8255..Exp

Q5. Design the control word when the ports of INTEL 8255 are defined as follows.

- Port A-Bidirectional
 - Port B-output
 - Mode of Port A - Mode 2
 - Mode of Port B - Mode 1

Ans-

Unit 3

Interrupts

Interrupts in 8085

- Interrupts are the signals generated by the external devices to request the microprocessor to perform a task. There are 5 interrupt signals in 8085, i.e. TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR.
- It is some kind of hindrance in the normal execution of the microprocessor.
- **Interrupt** is the method of creating a temporary halt during program execution and allows peripheral devices to access the **microprocessor**. The **microprocessor** responds to that **interrupt** with an ISR (**Interrupt** Service Routine), which is a short program to instruct the **microprocessor** on how to handle the **interrupt**.

Classification of Interrupts

- **Vector interrupt** – In this type of interrupt, the interrupt address is known to the processor. **For example:** RST7.5, RST6.5, RST5.5, TRAP.
- **Non-Vector interrupt** – In this type of interrupt, the interrupt address is not known to the processor so, the interrupt address needs to be sent externally by the device to perform interrupts. **For example:** INTR.

Classification of Interrupts

- **Maskable interrupt** – In this type of interrupt, we can disable the interrupt by writing some instructions into the program. **For example:** RST7.5, RST6.5, RST5.5.
- **Non-Maskable interrupt** – In this type of interrupt, we cannot disable the interrupt by writing some instructions into the program. **For example:** TRAP

Classification of Interrupts

- **Software interrupt** – In this type of interrupt, the programmer has to add the instructions into the program to execute the interrupt. These interrupts occurred due to some software error for example divide by zero
- **Hardware interrupt** – There are 5 interrupt pins in 8085 used as hardware interrupts, i.e. TRAP, RST7.5, RST6.5, RST5.5, INTA. These interrupts occurred due to some hardware error for example error due any I/O.

Types of Interrupts

- TRAP- It is a non-maskable interrupt, having the highest priority among all interrupts.
- RST7.5 -It is a maskable interrupt, having the second highest priority among all interrupts.
- RST 6.5-It is a maskable interrupt, having the third highest priority among all interrupts.
- RST 5.5-It is a maskable interrupt.
- INTR-It is a maskable interrupt, having the lowest priority among all interrupts. It can be disabled by resetting the microprocessor.

UNIT 3

INTEL 8257/DMA Controller

INTEL 8257/DMA Controller

- DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.
- Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory.

INTEL 8257/DMA Controller

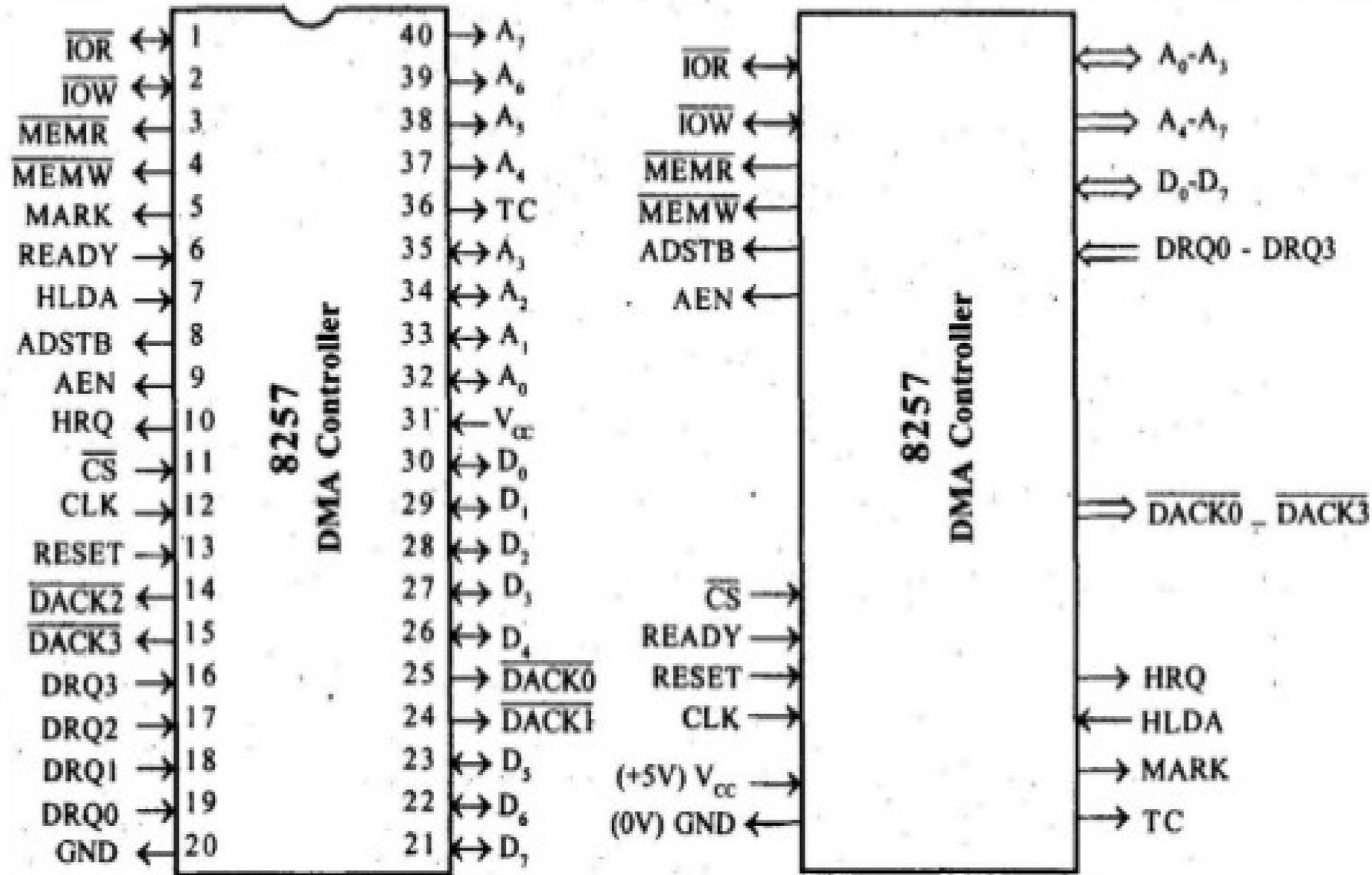
Following is the sequence of operations performed by a DMA –

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
- The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Features of 8257

- It has four channels which can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

8257 Pin Description



8257 Pin Description

- DRQ₀-DRQ₃- These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ₀ has the highest priority and DRQ₃ has the lowest priority among them.
- DACK₀ – DACK₃-These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU.
- D₀ – D₇-These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address

8257 Pin Description

- IOR- It is an active-low bidirectional input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.
- IOW-It is an active low bi-direction line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.
- CLK-It is a clock frequency signal which is required for the internal operation of 8257.
- RESET-This signal is used to RESET the DMA controller by disabling all the DMA channels.
- $A_o - A_3$ -These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

8257 Pin Description

- CS-It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.
- A₄ - A₇-These are the higher nibble of the lower byte address generated by DMA in the master mode.
- READY-which makes DMA ready .
- HRQ-This signal is used to receive the hold request signal from the output device.
- HLDA-It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU.

8257 Pin Description

- MEMR-It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.
- MEMW-It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.
- ADST-This signal is used to convert the higher byte of the memory address generated by the DMA controller into the latches.
- AEN-This signal is used to disable the address bus/data bus.
- TC-It stands for ‘Terminal Count’, which indicates the present DMA cycle to the present peripheral devices.
- MARK-The mark will be activated after each 128 cycles or integral multiples of it from the beginning.
- V_{cc} -It is the power signal which is required for the operation of the circuit.

UNIT 3

INTEL 8259/Programmable Interrupt
Controller (PIC)

INTEL 8259

- The 8259 is known as the Programmable Interrupt Controller (PIC) microprocessor.
- PIC is used when several I/O devices transfer data using interrupt.
- When the number of I/O devices are less than the number of interrupt lines in microprocessor , such controllers are not required.
- It is compatible with 8085 and 8086 microprocessor.
- By adding 8259, we can increase the interrupt handling capability.
- This chip combines the multi-interrupt input source to single interrupt output.
- This provides 8-interrupts from IR0 to IR7.
- We can mask individual bits of Interrupt Request Register.
- By cascading 8259 chips, we can increase interrupts up to 64 interrupt lines

INTEL 8259 Pin Diagram

$\overline{\text{CS}}$ →	1	28	← V _{cc}
$\overline{\text{WR}}$ →	2	27	← A ₀
$\overline{\text{RD}}$ →	3	26	← INTA
D ₇ ↔	4	25	← IR ₇
D ₆ ↔	5	24	← IR ₆
D ₅ ↔	6	23	← IR ₅
D ₄ ↔	7	22	← IR ₄
D ₃ ↔	8	21	← IR ₃
D ₂ ↔	9	20	← IR ₂
D ₁ ↔	10	19	← IR ₁
D ₀ ↔	11	18	← IR ₀
CAS ₀ ↔	12	17	→ INT
CAS ₁ ↔	13	16	↔ SP/EN
Gnd →	14	15	↔ CAS ₂

INTEL 8259 Pin Description

- CS-Chip Select
- WR- to write the control information to 8259 by Processor.
- RD-to read the information status from the 8259 by Processor.
- D0-D7- Eight bi-directional data pins.
- CAS0-CAS2- These are cascaded lines.
- SP/EN- SP*/EN* stands for “slave program/enable buffer”. It is related to cascade control.
- INT- A strong active high-output pin which interrupts the processor. Always connected to the INTR interrupt input of 8085.
- INTA- Interrupt Acknowledgement
- IR0-IR7- There are Eight interrupt request inputs.
- A0- An address input pin used along with RD* and WR* which is used to identify the various command words.

Registers of 8259

- **Interrupt Request Register-** It stores the interrupt request of inputs.

1		0		1		1		0		0		1		0
---	--	---	--	---	--	---	--	---	--	---	--	---	--	---

- **Interrupt Service Register-** Which interrupt is currently being serviced .

0		0		0		0		0		0		1		0
---	--	---	--	---	--	---	--	---	--	---	--	---	--	---

- **Interrupt Mask Register-** It contains a specific bits for each interrupt lines. It is used to mask (disable) or unmask(enable) individual interrupt request.

0		0		0		1		0		0		1		0
---	--	---	--	---	--	---	--	---	--	---	--	---	--	---

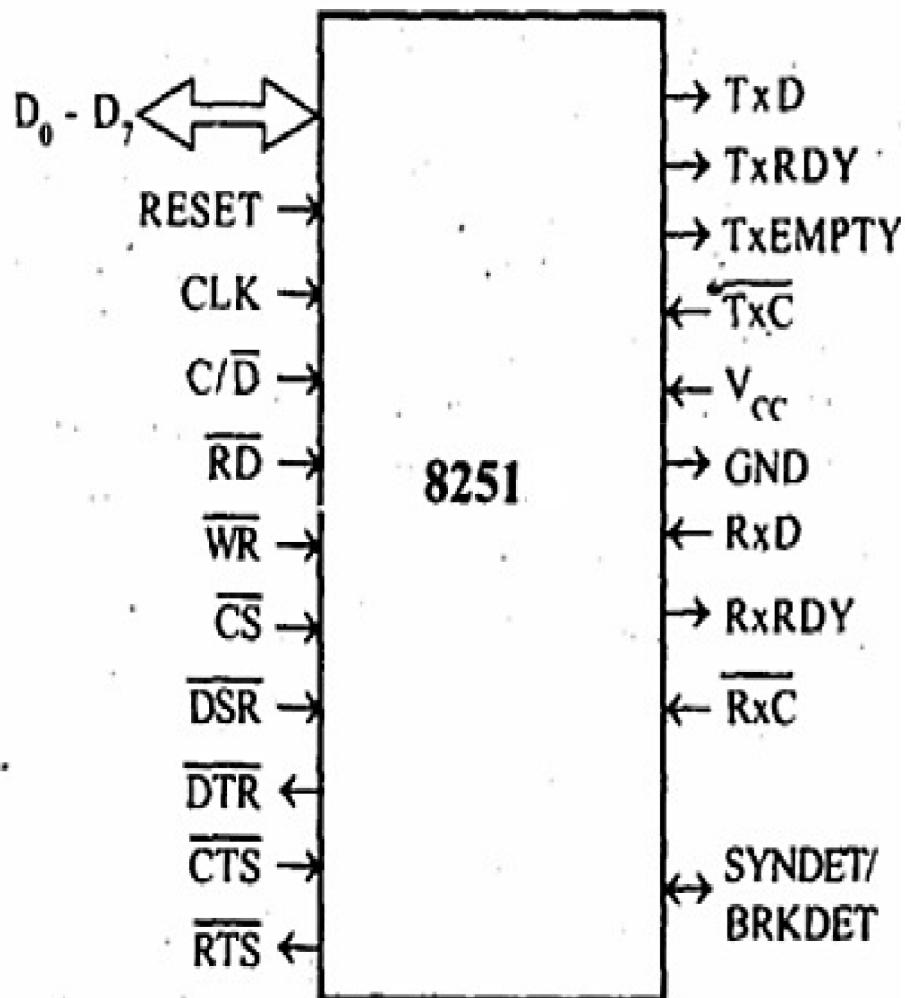
UNIT 3

INTEL 8251/Programmable
Communication Interface

INTEL 8251

- The 8251 chip is Universal Synchronous Asynchronous Receiver Transmitter (USART).
- It acts as a mediator between the microprocessor and peripheral devices.
- It converts serial data to parallel form and vice versa.
- This chip has 28 pins.
- It is compatible with 8085, 8086 Microprocessor.

The pin description of 8251



The pin description of 8251

C/D	Control register or Data buffer select
RD	Read Control
WR	Write control
DSR	Data Set Ready
DTR	Data Terminal Ready
RTS	Request to send Data
CTS	Clear to send Data (A low on this pin enables 8251 to transmit serial data)
TxC	Transmitter Clock (It governs the rate of data transmission)
TxE	Transmitter Empty (It goes high when 8251 has no char to transmit)
TxRDY	Transmitter Ready

The pin description of 8251

RxRDY	Receiver Ready
RxD	Line for receive data
TxD	Line for serial data Transmission
RxC	Receiver Clock (It governs the rate of data transmission)
CS	Chip Select
SYNDET/BRKDET	Synchronous Detect/ Detect Break
V _{cc}	V _{cc} (5V)
GND	Ground(0V)

UNIT 3

Intel 8279/ programmable keyboard
and display controller

Intel 8279

8279 programmable keyboard/display controller is designed by Intel that interfaces a keyboard with the CPU. The keyboard first scans the keyboard and identifies if any key has been pressed. It then sends their relative response of the pressed key to the CPU and vice-a-versa.

- The Keyboard can be interfaced either in the interrupt or the polled mode. In the **Interrupt mode**, the processor is requested service only if any key is pressed, otherwise the CPU will continue with its main task.
- In the **Polled mode**, the CPU periodically reads an internal flag of 8279 to check whether any key is pressed or not with key pressure.
- The keyboard consists of maximum 64 keys, which are interfaced with the CPU by using the key-codes. These key-codes are de-bounced and stored in an 8-byte FIFO RAM, which can be accessed by the CPU.

8279 – Pin Description

RL ₂	1	40	V _{CC} (+5V)
RL ₃	2	39	RL ₁
CLOCK	3	38	RL ₀
IRQ	4	37	CNTL/STB
RL ₄	5	36	SHIFT
RL ₅	6	35	SL ₃
RL ₆	7	34	SL ₂
RL ₇	8	33	SL ₁
RESET	9	32	SL ₀
RD	10	8279	OUT B ₀
WR	11	31	OUT B ₁
DB ₀	12	30	OUT B ₂
DB ₁	13	29	OUT B ₃
DB ₂	14	28	OUT A ₀
DB ₃	15	27	OUT A ₁
DB ₄	16	26	OUT A ₂
DB ₅	17	25	OUT A ₃
DB ₆	18	24	BD
DB ₇	19	23	CS
V _{SS} (OV)	20	21	A ₀

8279 – Pin Description

- Data Bus Lines, DB₀ - DB₇ - These are 8 bidirectional data bus lines used to transfer the data to/from the CPU.
- CLK- The clock input is used to generate internal timings required by the microprocessor.
- RESET-As the name suggests this pin is used to reset the microprocessor.
- CS Chip Select-When this pin is set to low, it allows read/write operations, else this pin should be set to high.
- A₀ -This pin indicates the transfer of command/status information. When it is low, it indicates the transfer of data.
- RD, WR-This Read/Write pin enables the data buffer to send/receive data over the data bus.

8279 – Pin Description

- IRQ -This interrupt output line goes high when there is data in the FIFO sensor RAM. The interrupt line goes low with each FIFO RAM read operation. However, if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.
- V_{ss} , V_{cc} -These are the ground and power supply lines of the microprocessor.
- SL_0 – SL_3 -These are the scan lines used to scan the keyboard matrix and display the digits. These lines can be programmed as encoded or decoded, using the mode control register.
- RL_0 – RL_7 -These are the Return Lines which are connected to one terminal of keys, while the other terminal of the keys is connected to the decoded scan lines. These lines are set to 0 when any key is pressed.

8279 – Pin Description

- SHIFT -The Shift input line status is stored along with every key code in FIFO in the scanned keyboard mode. Till it is pulled low with a key closure, it is pulled up internally to keep it high
- CNTL/STB - CONTROL/STROBED I/P Mode-In the keyboard mode, this line is used as a control input and stored in FIFO on a key closure. The line is a strobe line that enters the data into FIFO RAM, in the strobed input mode. It has an internal pull up. The line is pulled down with a key closure.
- BD-It stands for blank display. It is used to blank the display during digit switching.
- OUTA₀ – OUTA₃ and OUTB₀ – OUTB₃ -These are the output ports for two 16x4 or one 16x8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and the keyboard.