

Intel 8253 - Programmable Interval Timer

Unit 4

Intel 8253

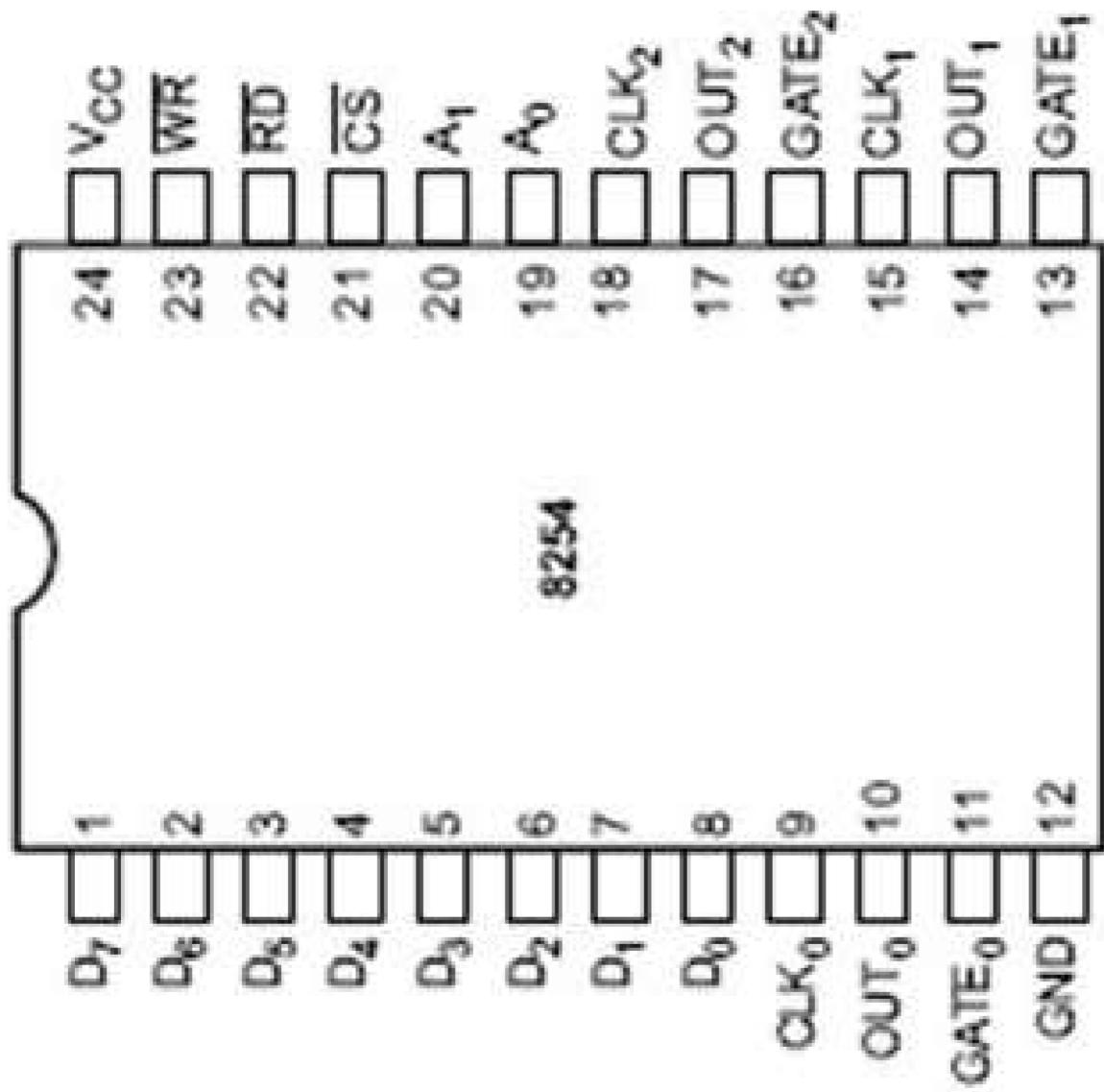
The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for "OUT" output.

To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Features of 8253

- It has three independent 16-bit down counters.
- These three counters can be programmed for either binary or BCD count.
- It is compatible with almost all microprocessors.

8253 Pin Description



8253 Pin Description

- D0-D7-> Bidirectional Data Bus
- RD->To read data by CPU from 8253
- WR-> To write data by CPU in 8253
- CS-> Chip Select
- Counters->It is having three Counters. Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register.

8253 Pin Description

A_1	A_0	Result
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

8253 modes

8253 can be operated in 6 different modes.

- Mode 0 – Interrupt on Terminal Count
- Mode 1 – Programmable One Shot
- Mode 2 – Rate Generator
- Mode 3 – Square Wave Generator
- Mode 4 – Software Triggered Mode
- Mode 5 – Hardware Triggered Mode

Control word of 8253

	7	6	5	4	3	2	1	0
SC_1	SC_0	RW_1	RW_2	M_2	M_1	M_0		$BCD /$ Binary

Control word of 8253

SC1	SC0	SELECTION
0	0	C0
0	1	C1
1	0	C2

RW1	RW0	SELECTION
0	0	Counter Latch Command
0	1	Read/Write lower byte
1	0	Read/Write higher byte
1	1	Read/Write lower byte followed by higher byte

Control word of 8253

M2 M1 M0 OPERATING MODE

0 0 0 MODE 0

0 0 1 MODE 1

X (0/1) 1 0 MODE 2

X (0/1) 1 1 MODE 3

1 0 0 MODE 4

1 0 1 MODE 5

The LSB of Control Word is used to select whether the counter is Binary or BCD. If the bit is 0 it works as binary counter and if its value is 1 it works as BCD counter.

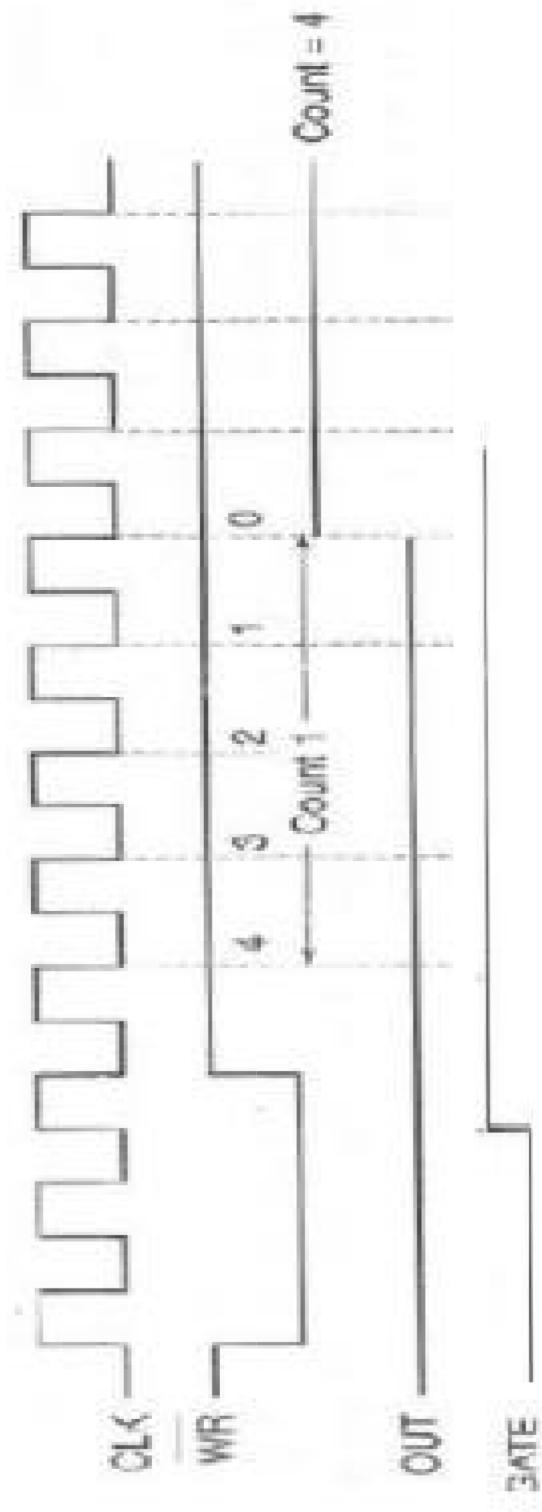
The addresses for control word register and the counters of 8253 for Vinytics Microprocessor kit are as follows

Counter 0-> 10
Counter 1-> 11
Counter 2-> 12
Control word register-> 13

Mode 0 – Interrupt on Terminal Count

- It is used to generate time delay by an interrupt to the microprocessor after a certain interval.
- One of the counter of 8253 is initialized and loaded with suitable count for desired time delay.
- When the counting is over the counter interrupts CPU.
- On Interruption the microprocessor performs the required task.
- The mode is set by loading the control word register.
- Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.

Mode 0 – Interrupt on Terminal Count Timing Diagram



Mode 0 – Interrupt on Terminal Count

- Exp- Use 8253 in Mode 0 to perform a particular task after certain delay. Take count for delay= FF50h. Use counter 1 fr Binary Counting. Design Control Word.

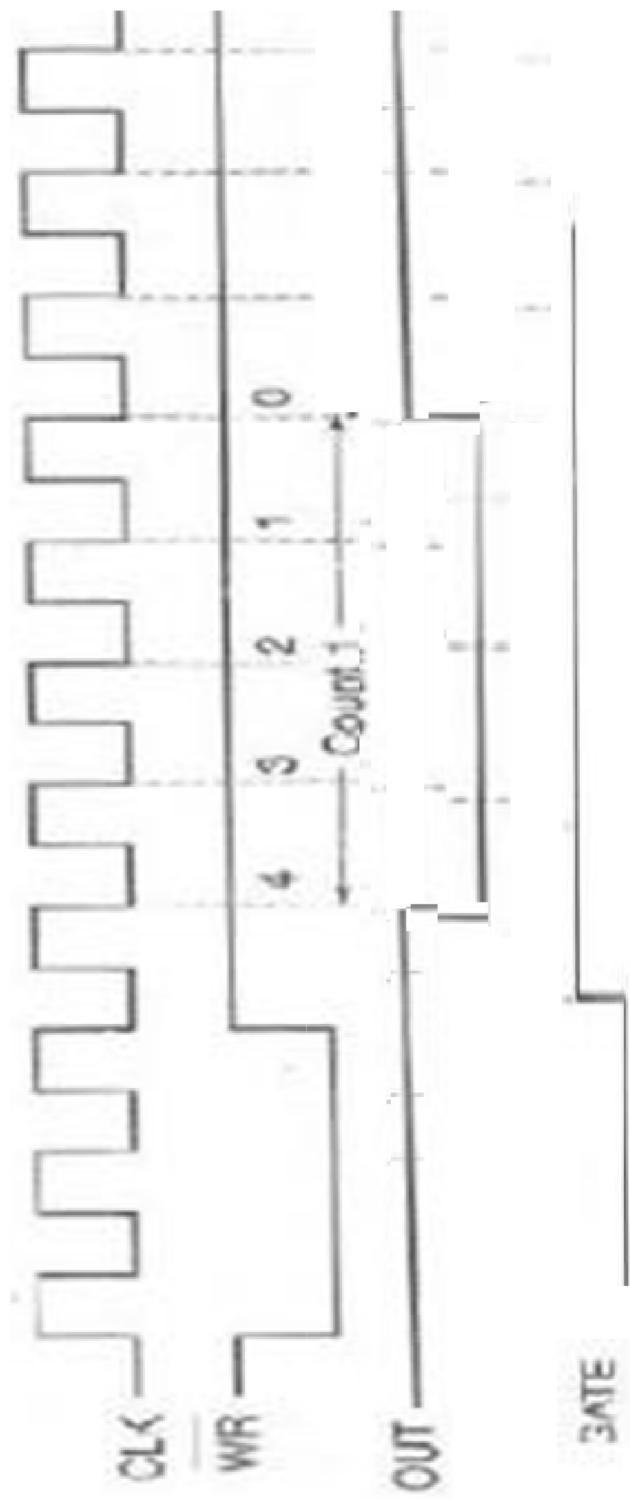
7	6	5	4	3	2	1	0
SC1	SC0	RW1	RW2	M2	M1	M0	BCD / Binary

D7	D6	D5	D4	D3	D2	D1	D0

Mode 1 – Programmable One Shot

- can be used as a mono Programmable one shot.
- The gate input is used as a trigger input in this mode.
- The output remains high until the count is loaded and a trigger is applied.
- The mode is set by loading the control word register .
- After mode is set the counter is loaded by a count value of N.
- Initially the output is high after the mode is set.
- After Triggering the gate counter decrements count.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- If the Gate is triggered in between counting, again the count value is reloaded.

Mode 1 – Programmable One Shot Timing Diagram



Mode 1 – Programmable One Shot

- Exp- Use 8253 in Mode 1 . Let N= 08. Use counter 2 for BCD Counting. Design Control Word.

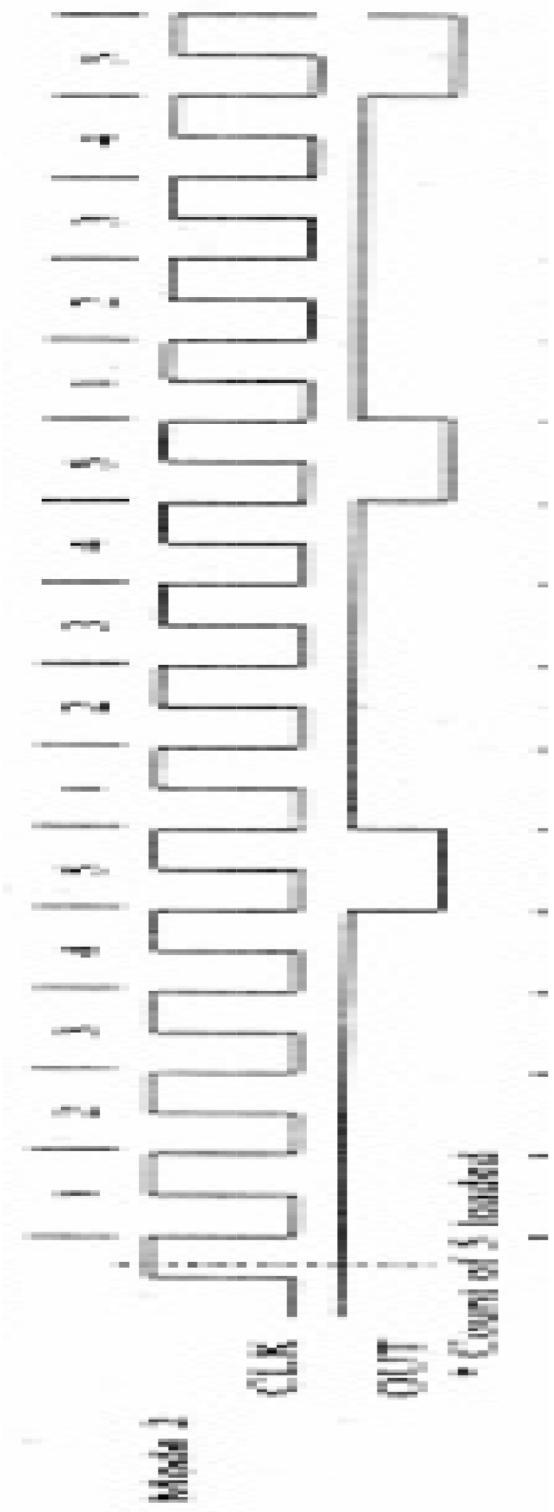
7	6	5	4	3	2	1	0
SC_1	SC_0	RW_1	RW_2	M_2	M_1	M_0	$BCD /$ Binary

D7	D6	D5	D4	D3	D2	D1	D0

Mode 2 – Rate Generator

- In Mode 2 the counter act as a simple divide by N counter.
- When this mode is set the counter becomes initially high.
- After mode set operation the counter is loaded by a count value N.
- For mode 2 operation Gate is kept high.
- In this mode the output remains high for N-1 clock pulse and then goes low for one clock pulse.
- Counter is loaded automatically when previous count ends.

Mode 2 – Rate Generator Timing Diagram



Mode 2 – Rate Generator

- Exp- Use 8253 in Mode 2 . Let N= 32. Use counter 1 for BCD Counting. Design Control Word.

7	6	5	4	3	2	1	0
SC1	SC0	RW1	RW2	M2	M1	M0	BCD / Binary

D7	D6	D5	D4	D3	D2	D1	D0

Mode 3 – Square Wave Generator

- In Mode 3 the counter act as a square wave generator.
- After mode set operation the counter is loaded by a count value N.
- For Mode 3 operation Gate is kept high.
- For even number of N output remains high for $N/2$ clock pulse and remains low for $N/2$ clock pulse.
- For Odd number of N output remains high for $N+1/2$ clock pulse and low for $N-1/2$.

Mode 3 – Square Wave Generator Timing Diagram

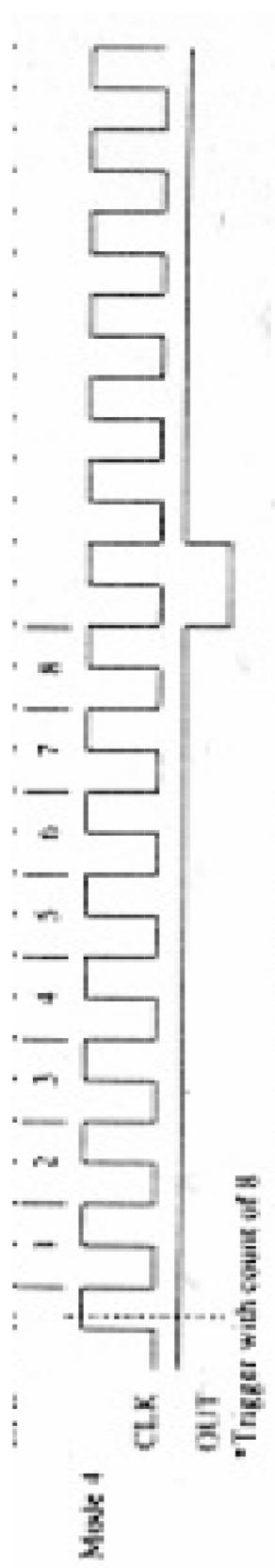


Mode 4 – Software Triggered Mode

- In this mode the output of the counter becomes initially high after the mode is set.
- Gate is kept high for this mode of operation.
- The counter begins counting immediately after the count is loaded into the count register.
- When the counter became 0 the output goes low for one clock period and then it returns to high.
- This mode of operation is referred to as a software triggered mode because the generation of the strobe signals is triggered by loading the count value into the count register.

Mode 4 – Software Triggered Mode

Timing Diagram



Mode 5 – Hardware Triggered Mode

- In this mode of operation Gate input act as a trigger.
 - After the ode is set output becomes initially high.
 - The count value is loaded into the counter.
- Following a low to high transition of the Gate Input the counter starts decrementing the count.
- When the counter became 0 the output goes low for one clock period and then it returns to high.

Mode 5 – Hardware Triggered Mode

Timing Diagram

