RV COLLEGE OF ENGINEERING®

(Autonomous Institution affiliated to VTU, Belagavi)

Department of Electronics and Instrumentation Engineering

ADDC LOGISIM SIMULATION LAB

III SEMESTER

(2020-2021)

BACHELOR OF ENGINEERING

In

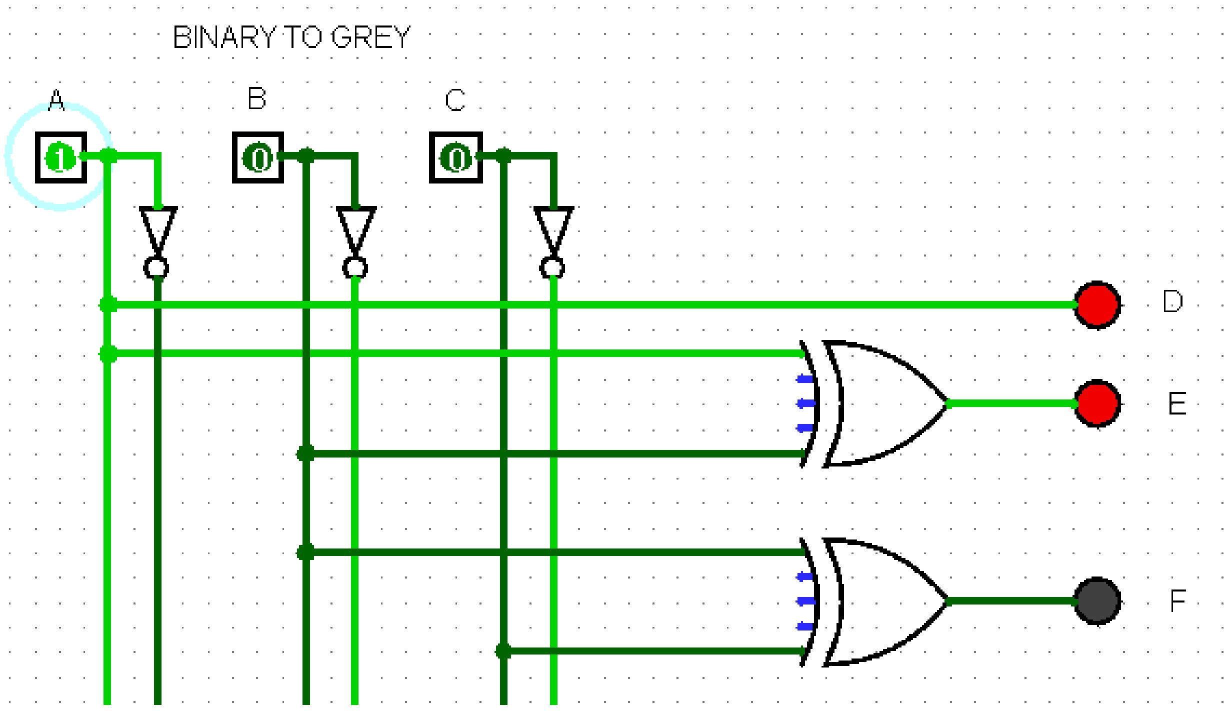
Electronics and Instrumentation Engineering

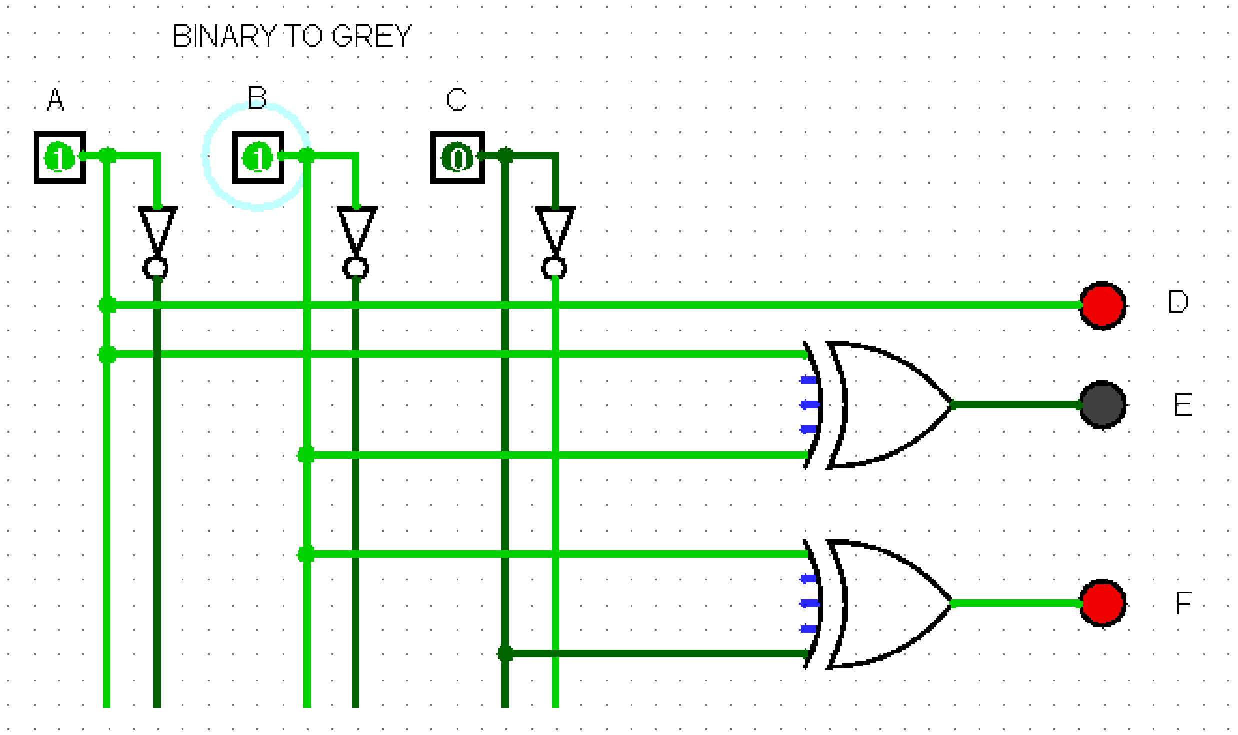
Submitted by

FARHAN AKHTER
1RV19EI017

Aim: To Design Code converters a) Binary to gray b) BCD to Excess 3

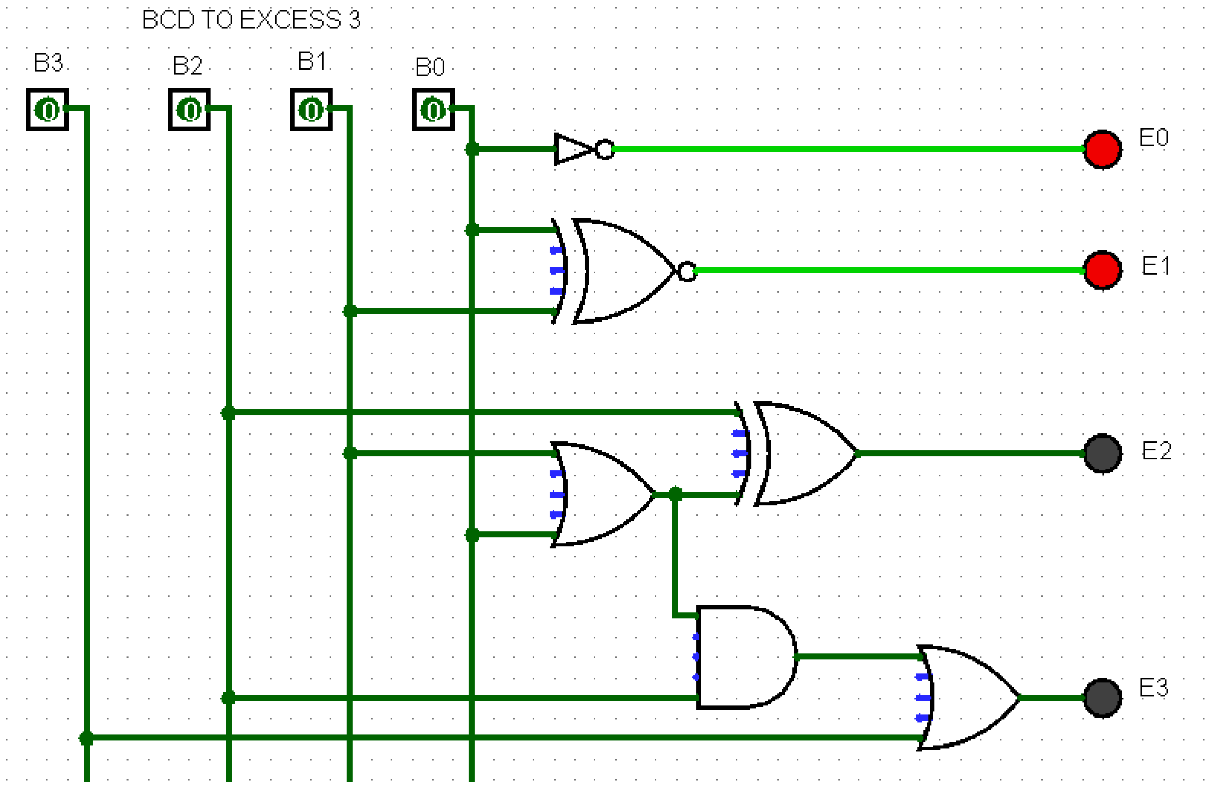
1.

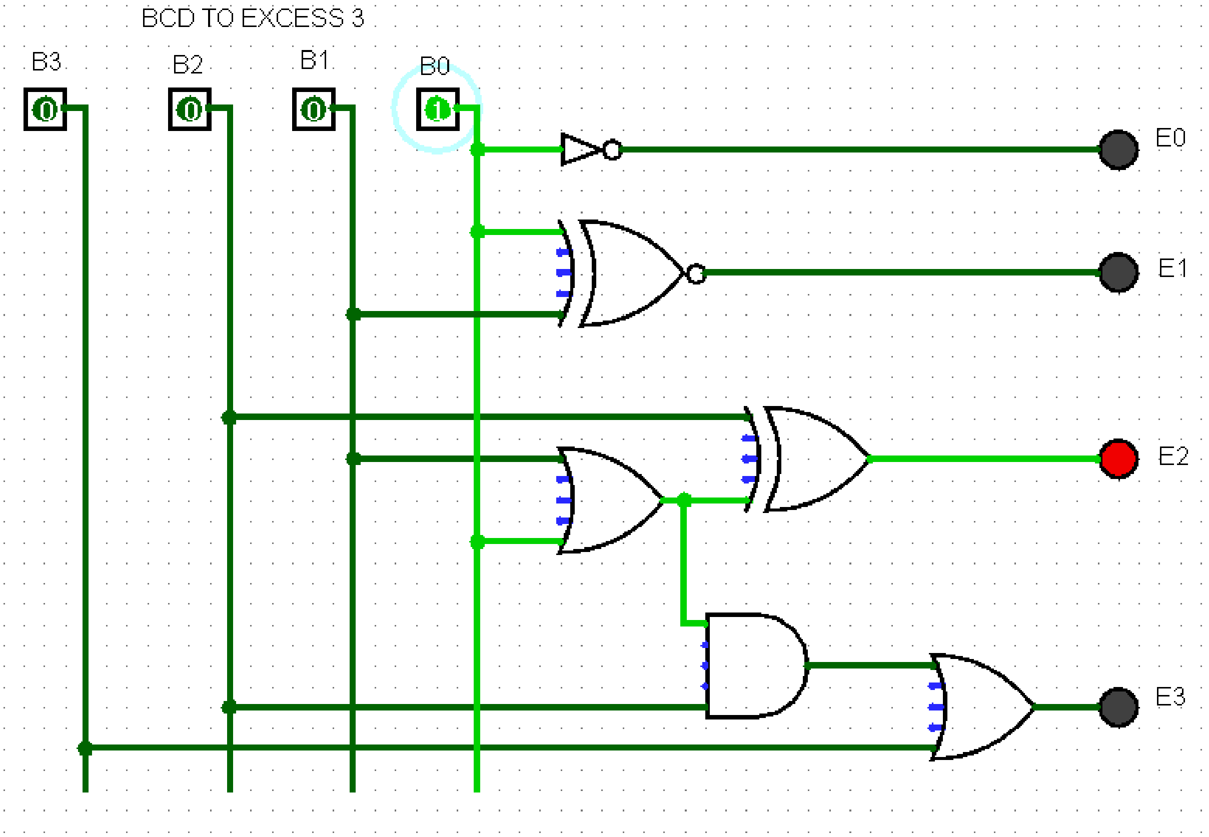




Aim: To Design Code converters a) Binary to gray b) BCD to Excess 3

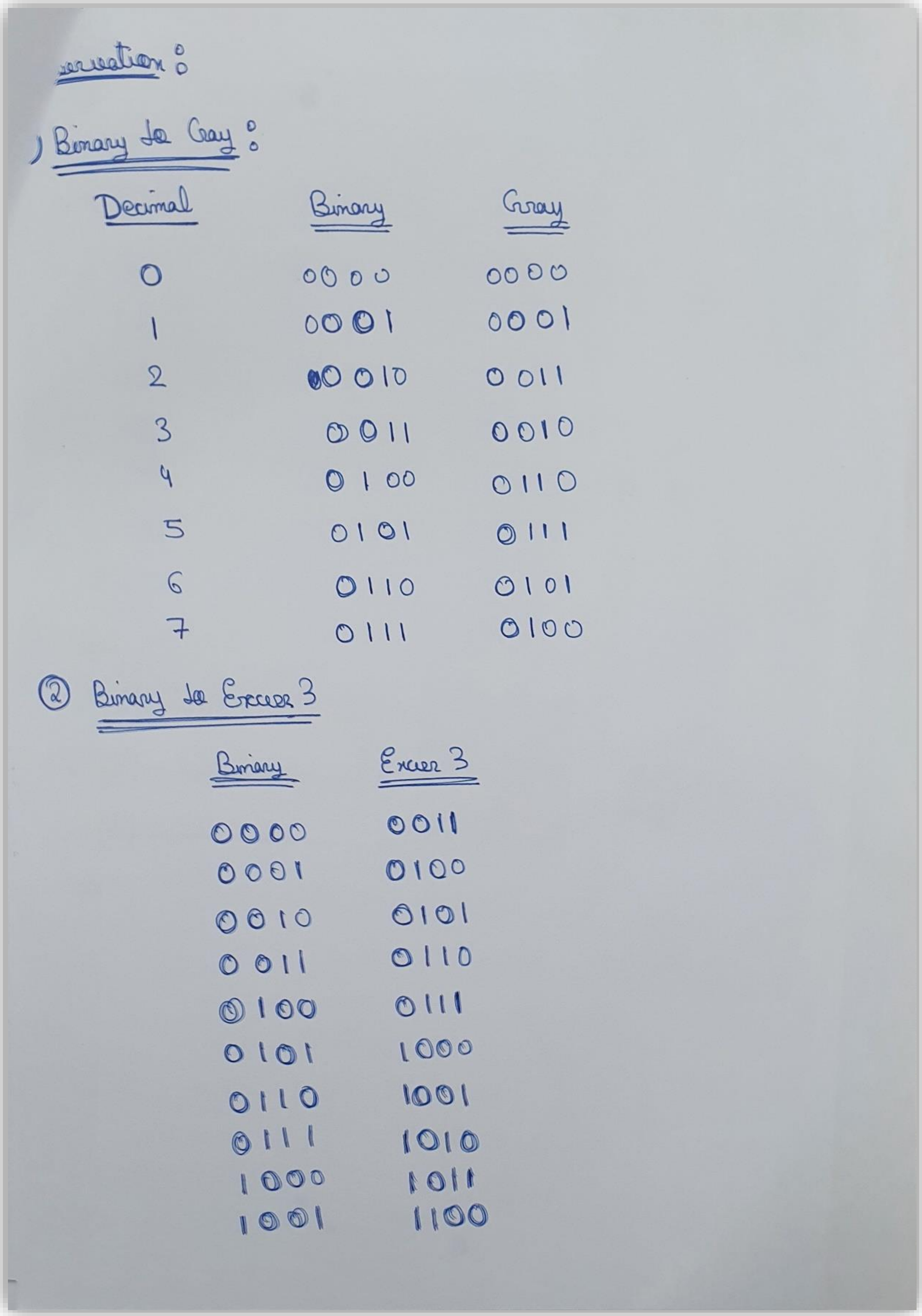
2.





Aim: To Design Code converters a) Binary to gray b) BCD to Excess 3

<u>Observation:</u>



servation :

) Binary to Gray :

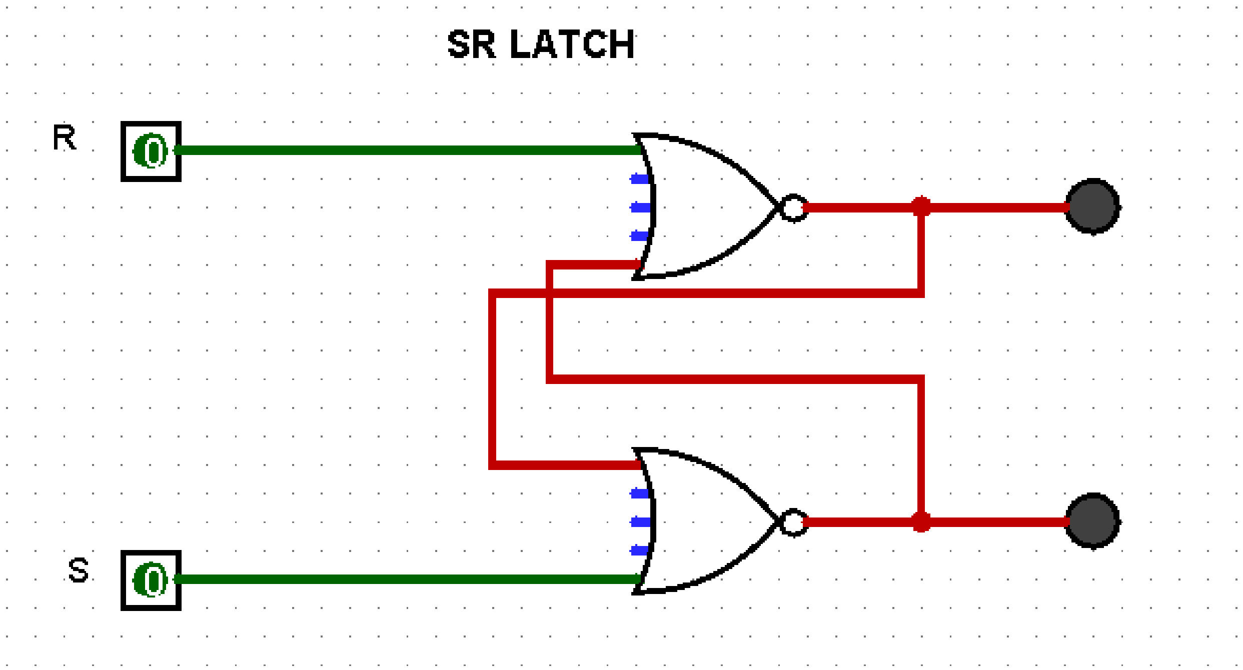
Decimal	Binary	Gray
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100

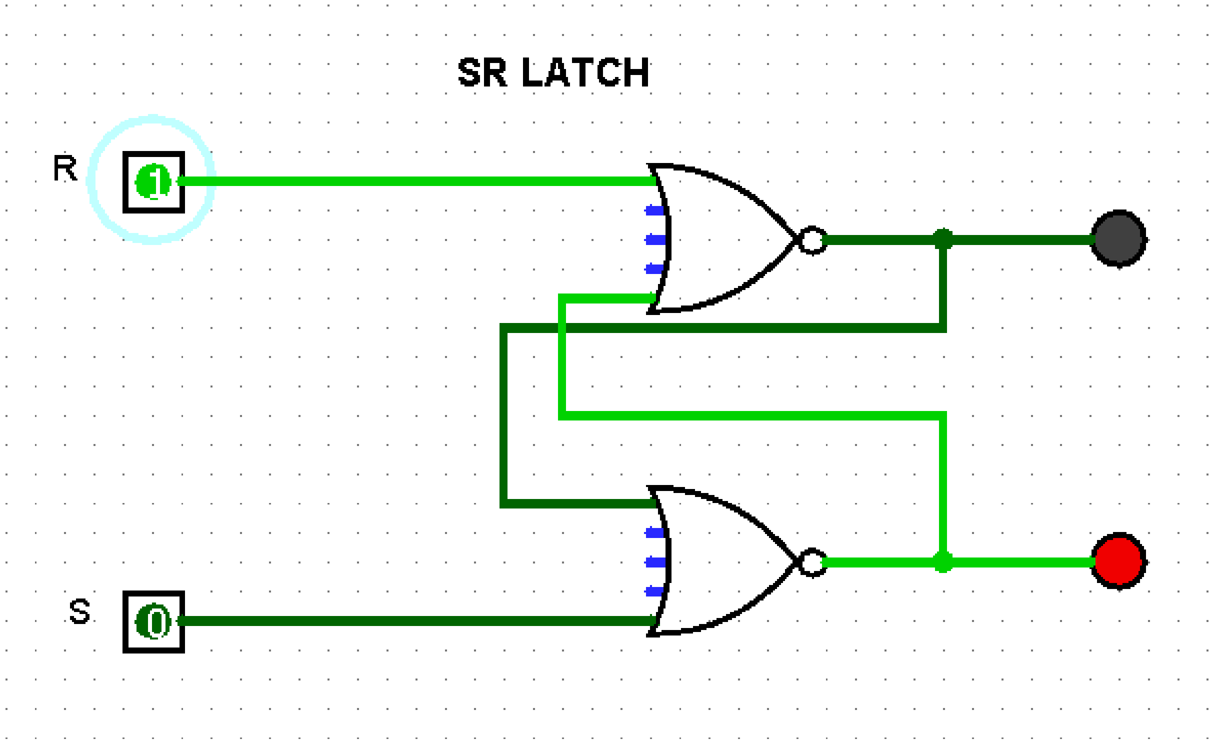
② Binary to Excess 3

Binary	Excess 3
0000	0011
0001	0100
0010	0101
0011	0110
0100	0111
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100

Aim: To construct various latches and flip flops and simulate them

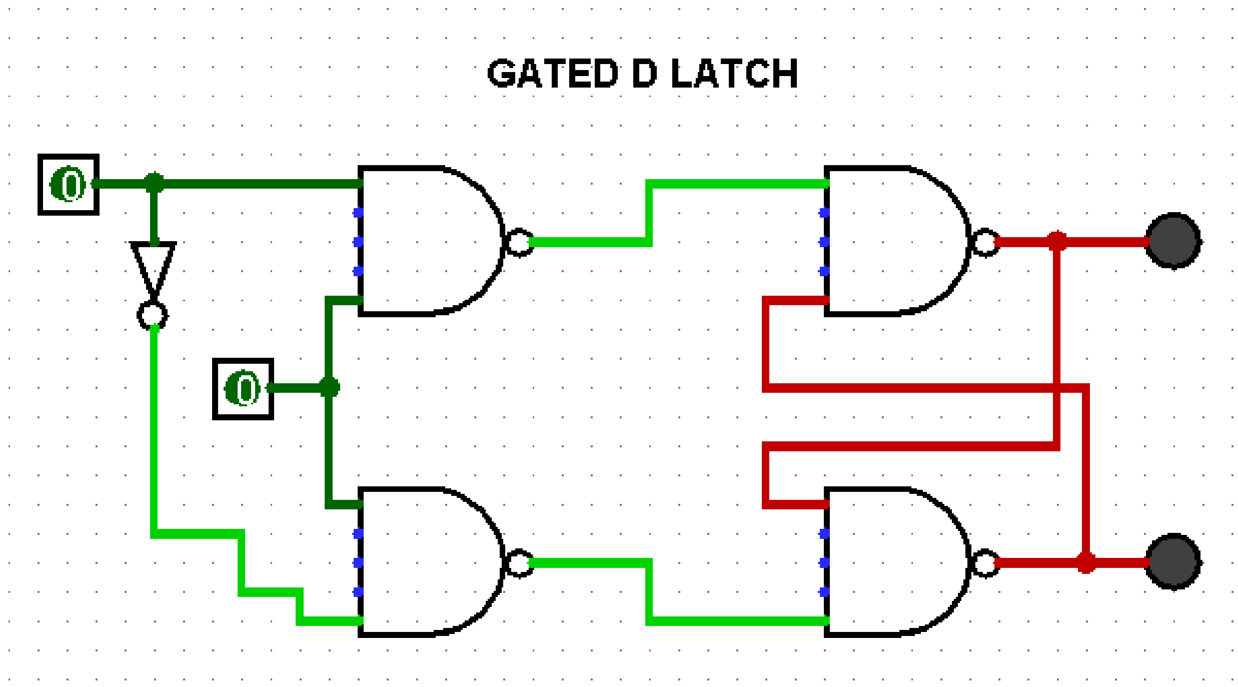
1.

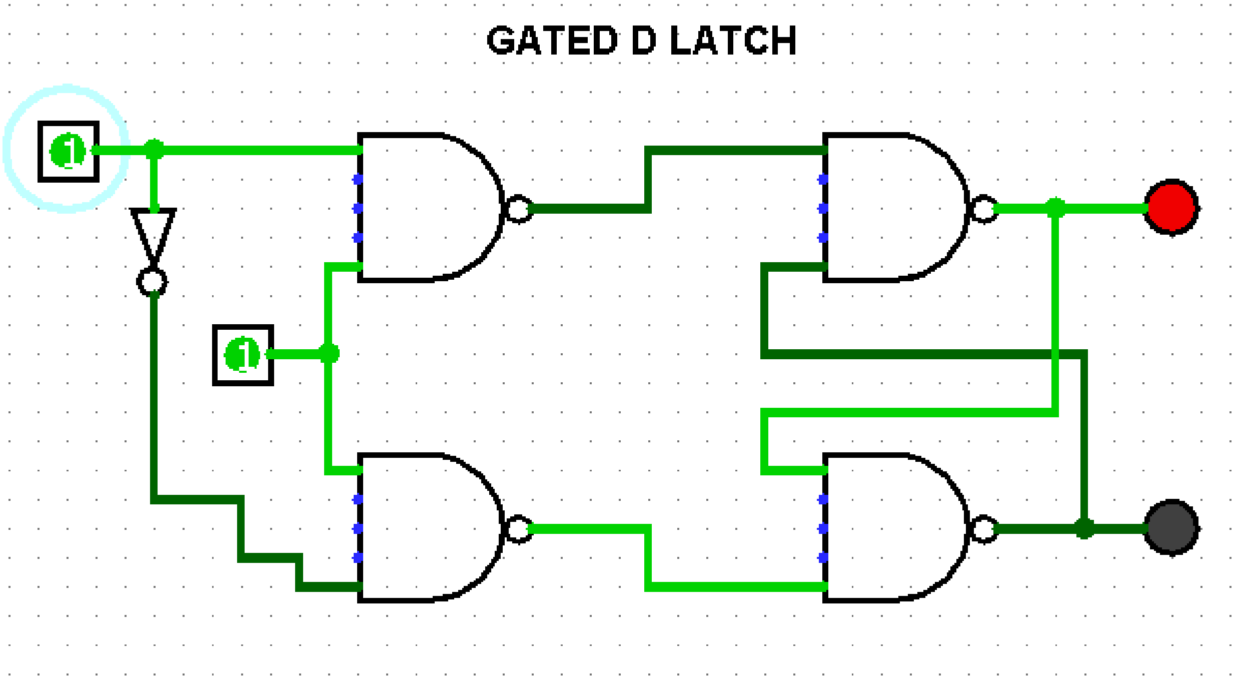




Aim: To construct various latches and flip flops and simulate them

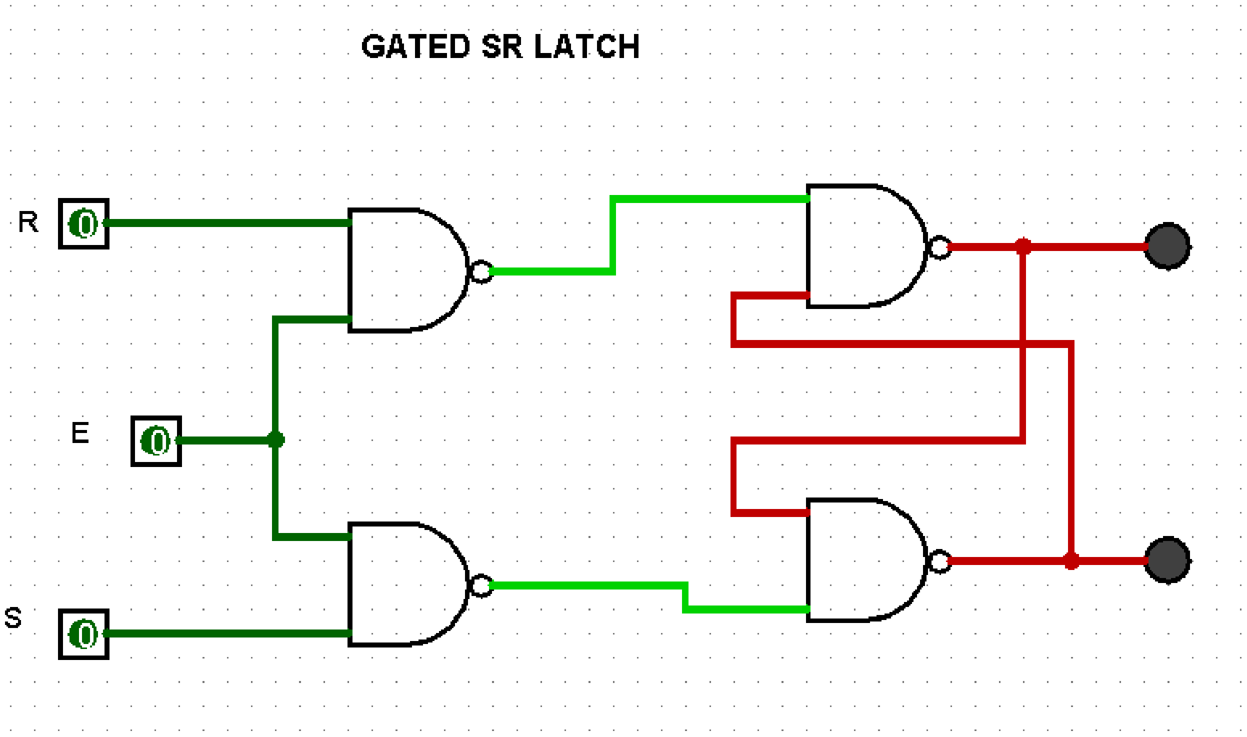
2.

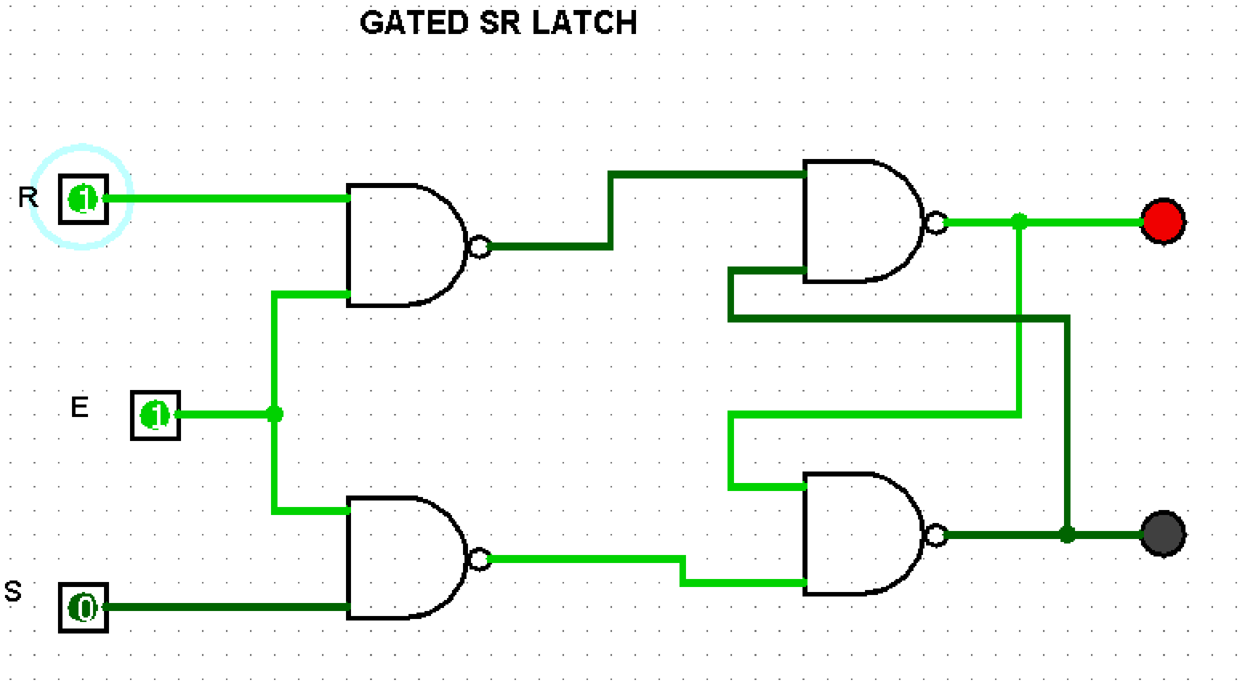




Aim: To construct various latches and flip flops and simulate them

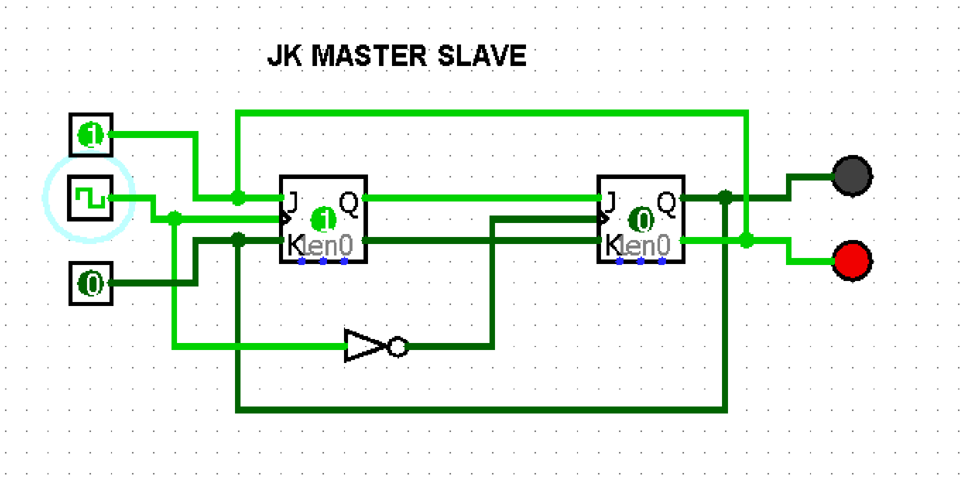
3.

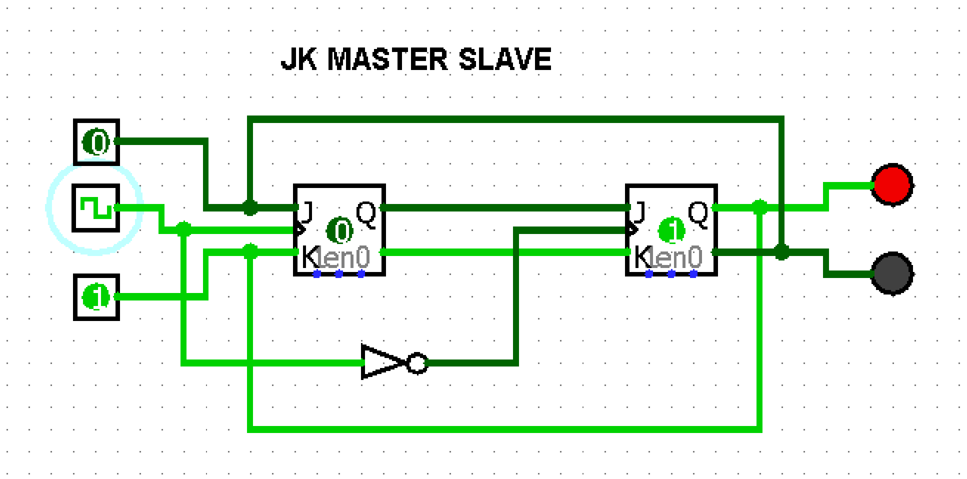


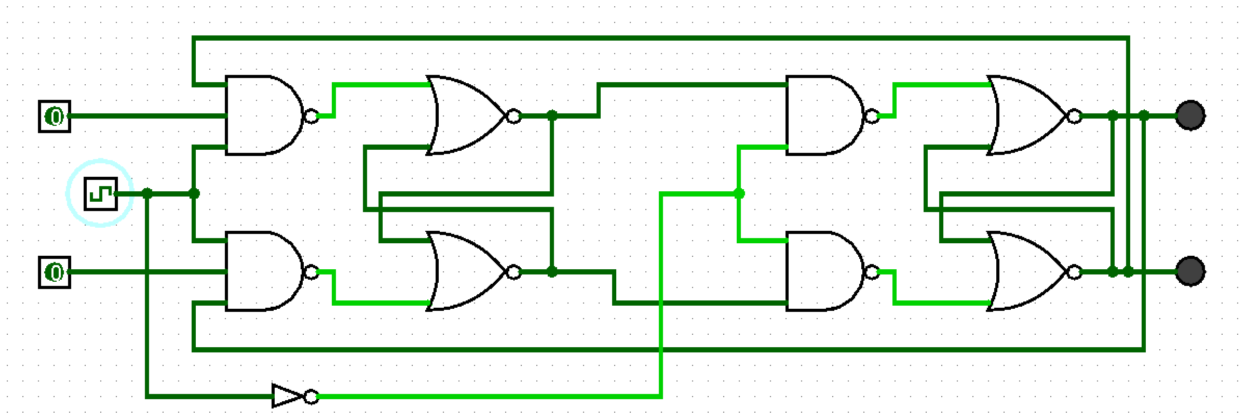


Aim: To construct various latches and flip flops and simulate them

4.

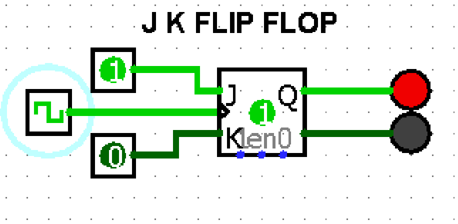


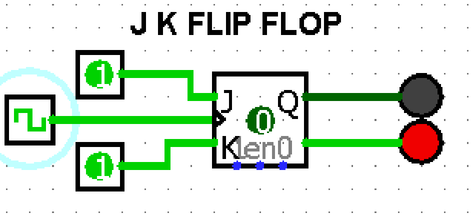




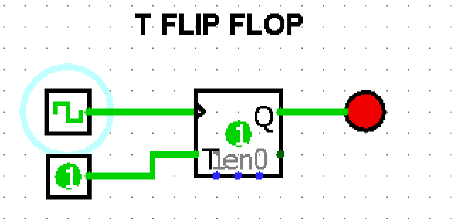
Aim: To construct various latches and flip flops and simulate them

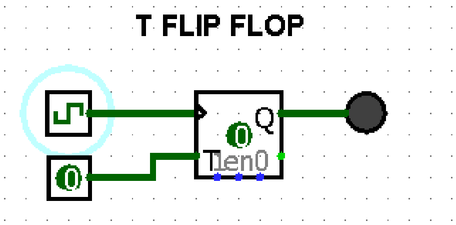
5.



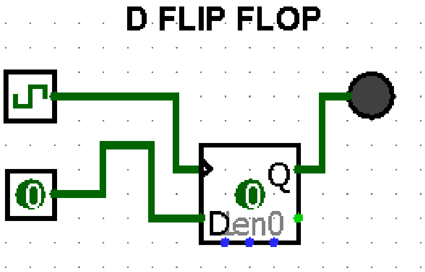


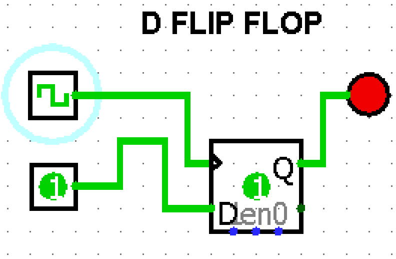
6.





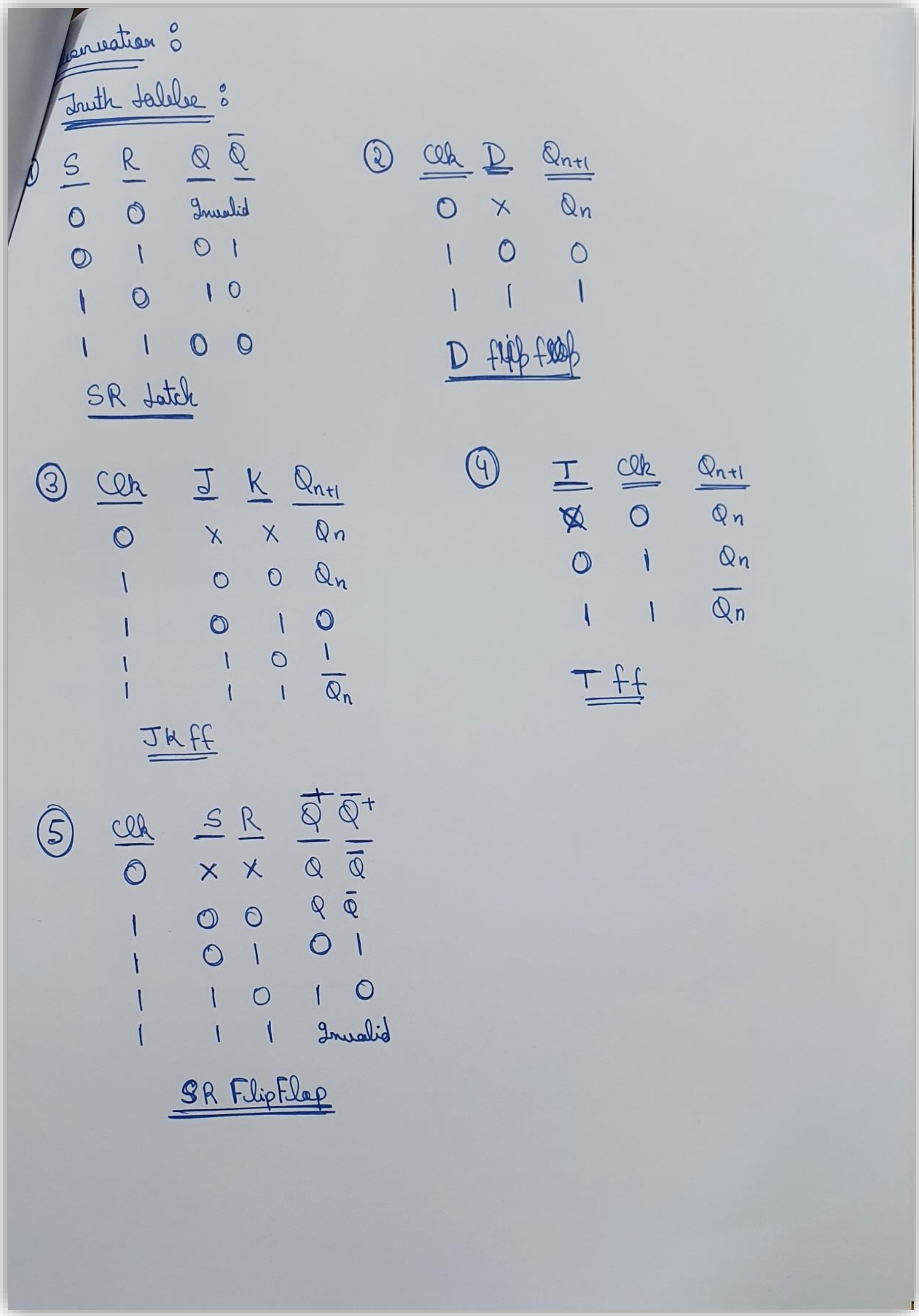
7.





Aim: To construct various latches and flip flops and simulate them

Observation:



ervation :

Truth tables :

1)

S	R	Q	$\overline{Q}$
0	0	Invalid	
0	1	0	1
1	0	1	0
1	1	0	0

SR Latch

2)

Clk	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

D flip flop

3)

Clk	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$

JK ff

4)

T	Clk	Q_{n+1}
X	0	Q_n
0	1	Q_n
1	1	$\overline{Q_n}$

T ff

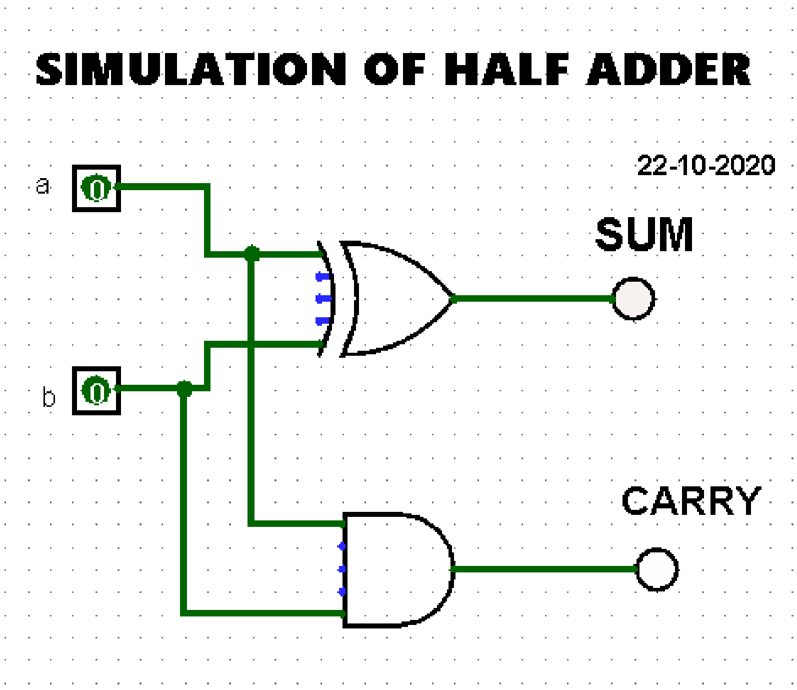
5)

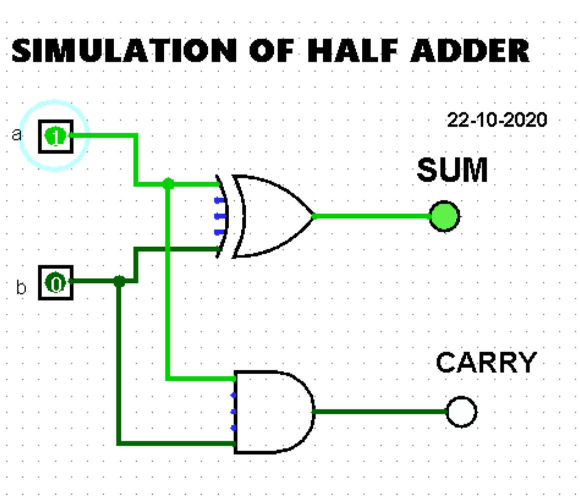
Clk	S	R	Q^+	$\overline{Q}^+$
0	X	X	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

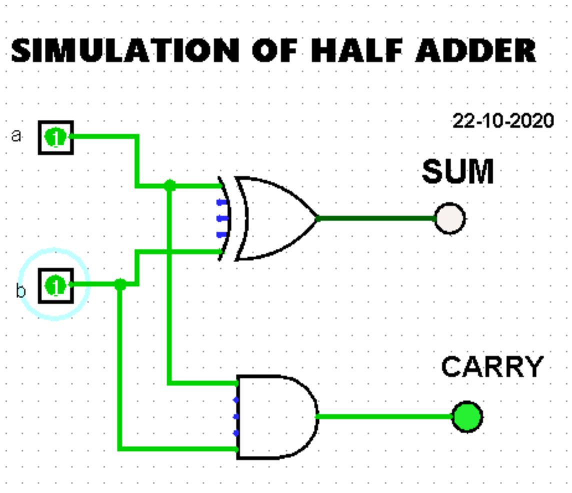
SR FlipFlop

Aim: To construct and simulate FA/FS &HA/HS

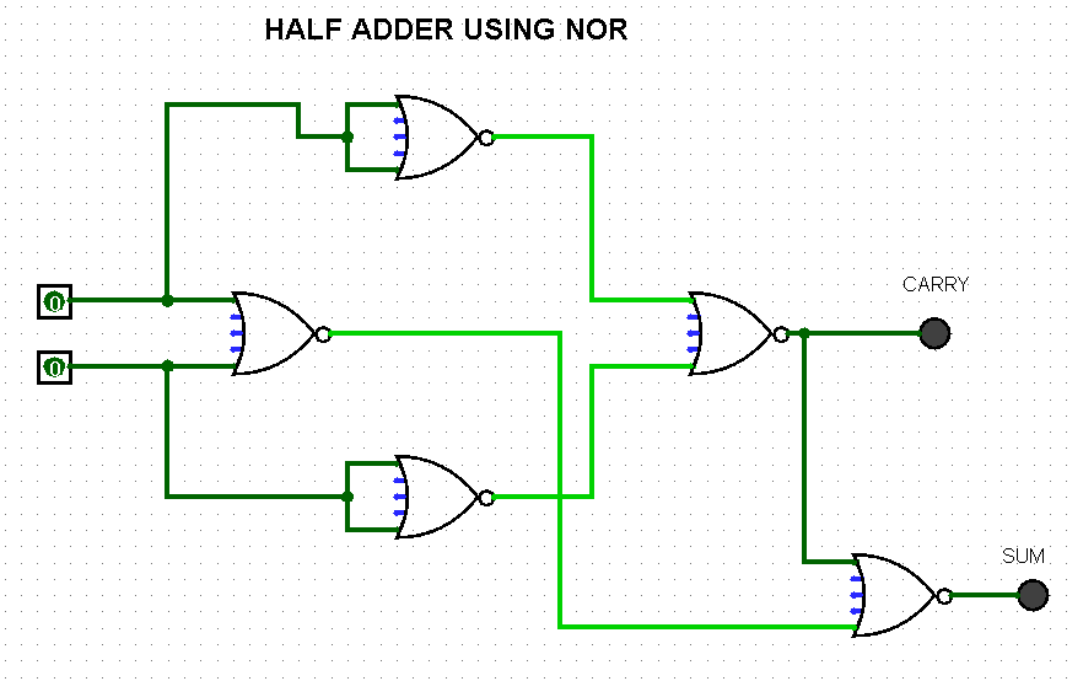
1)

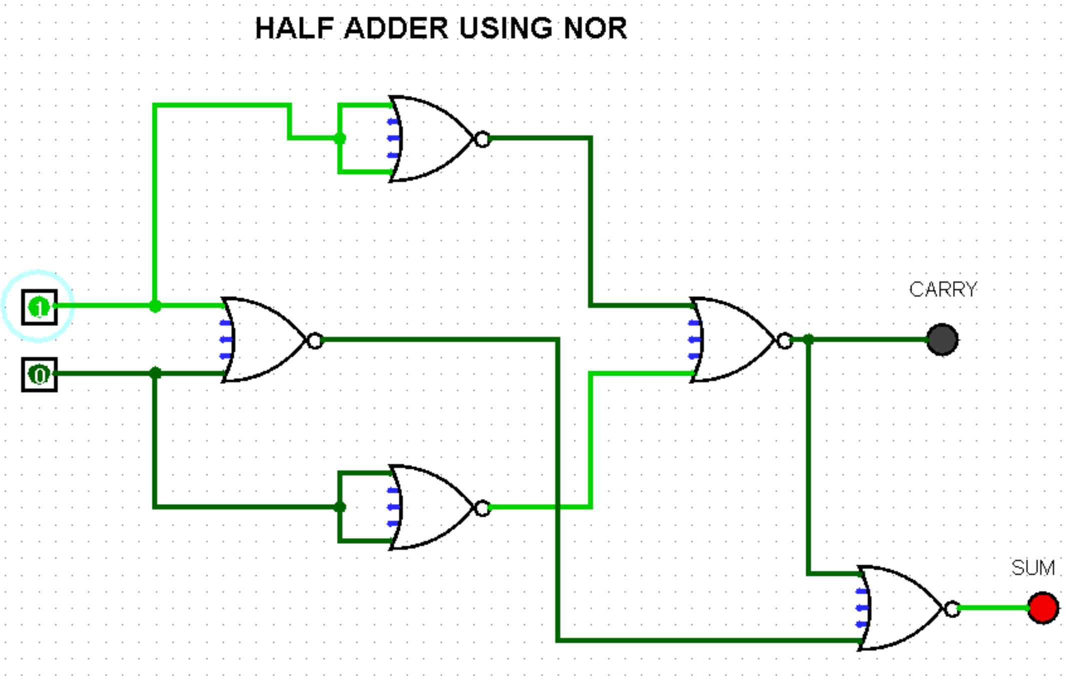




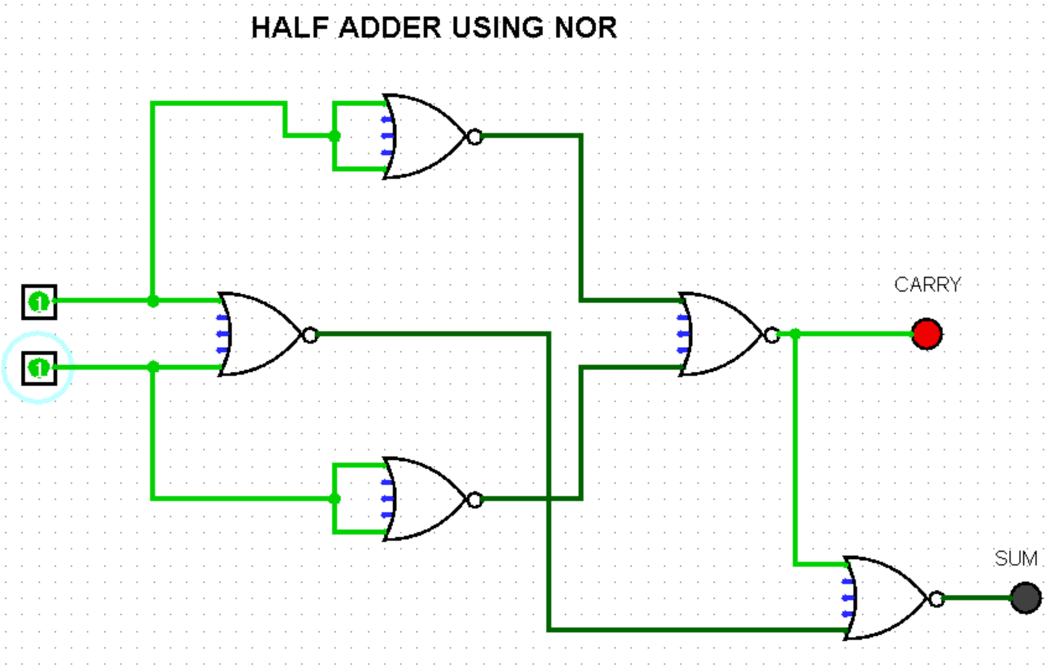


Aim: To construct and simulate FA/FS &HA/HS

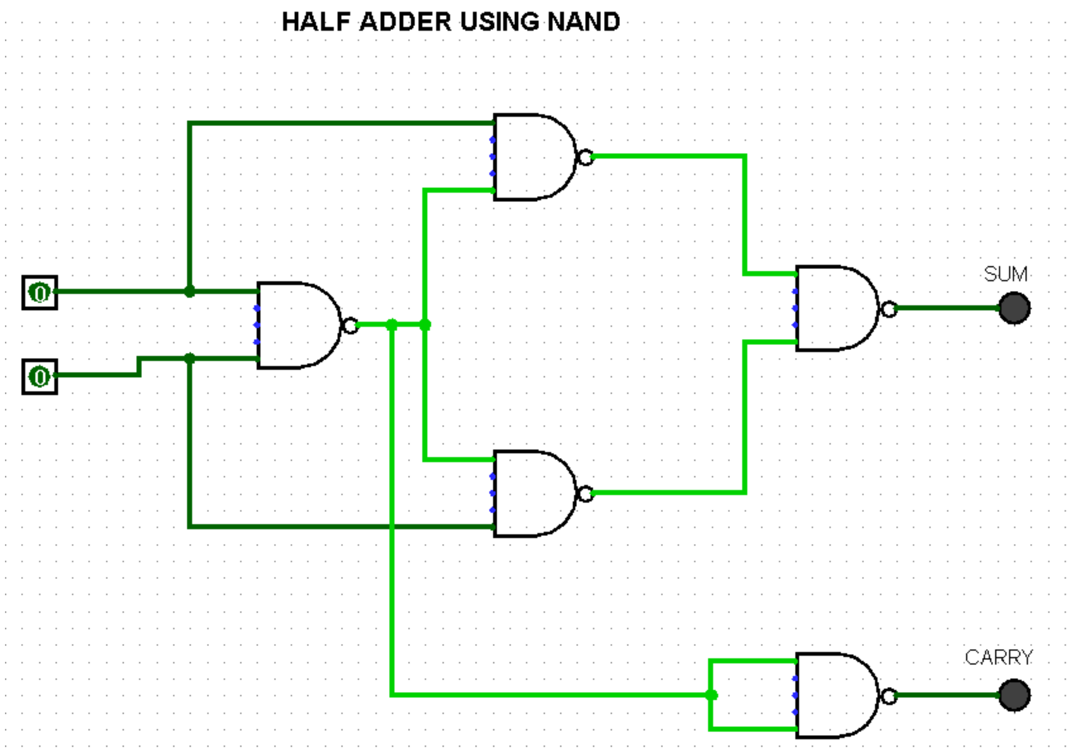


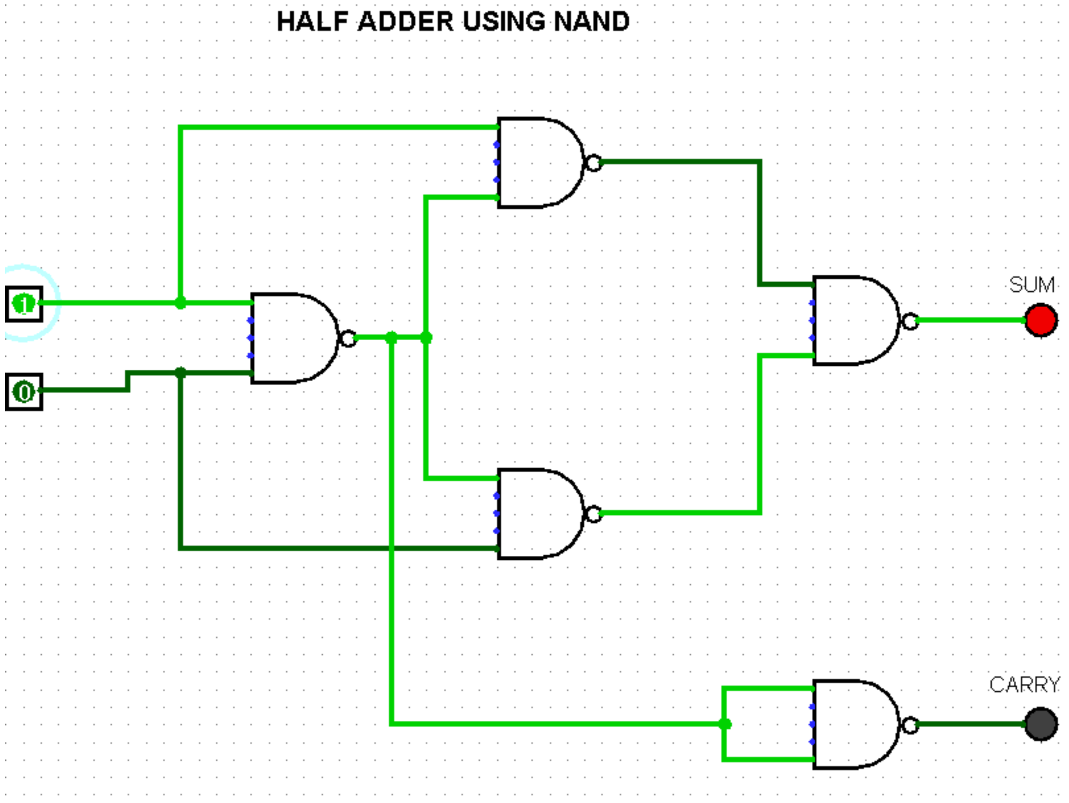


Aim: To construct and simulate FA/FS &HA/HS

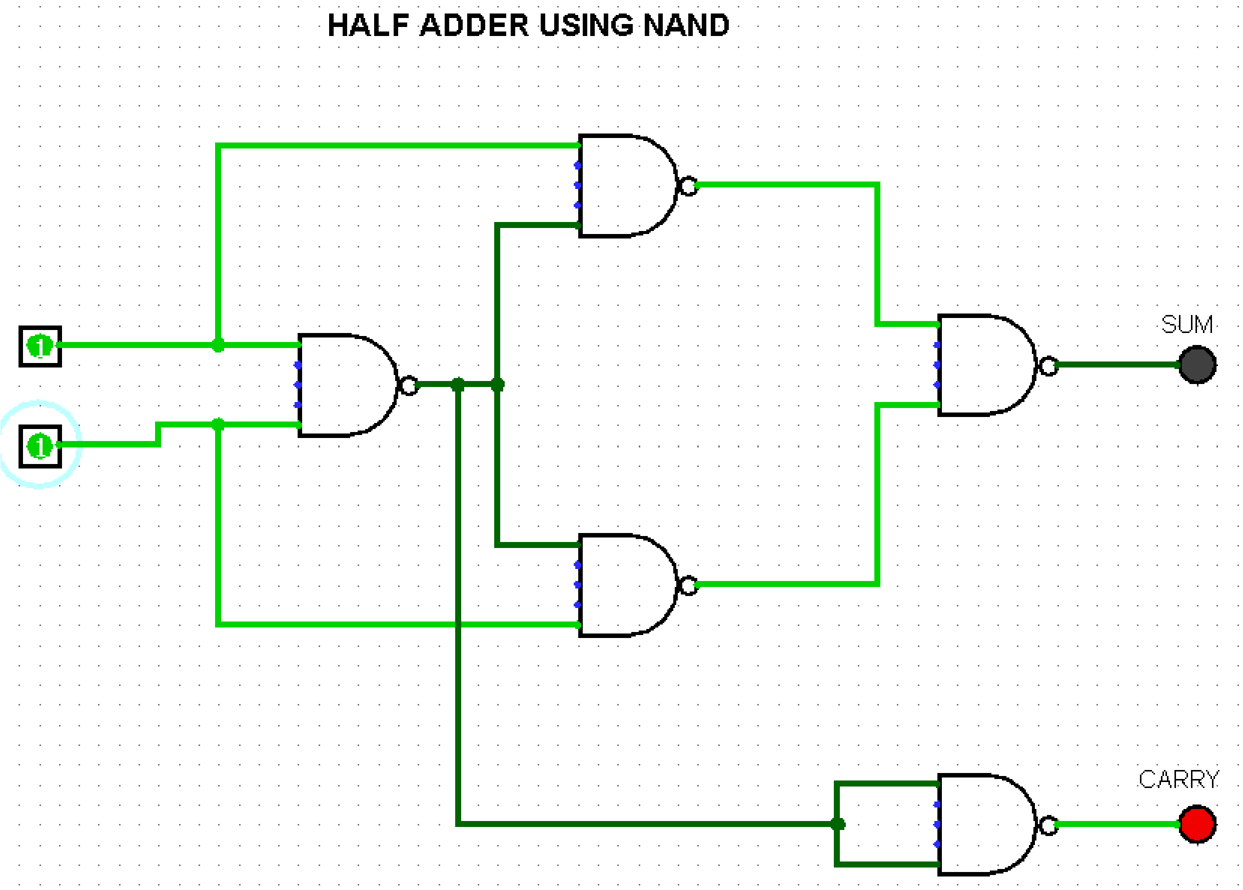


Aim: To construct and simulate FA/FS &HA/HS



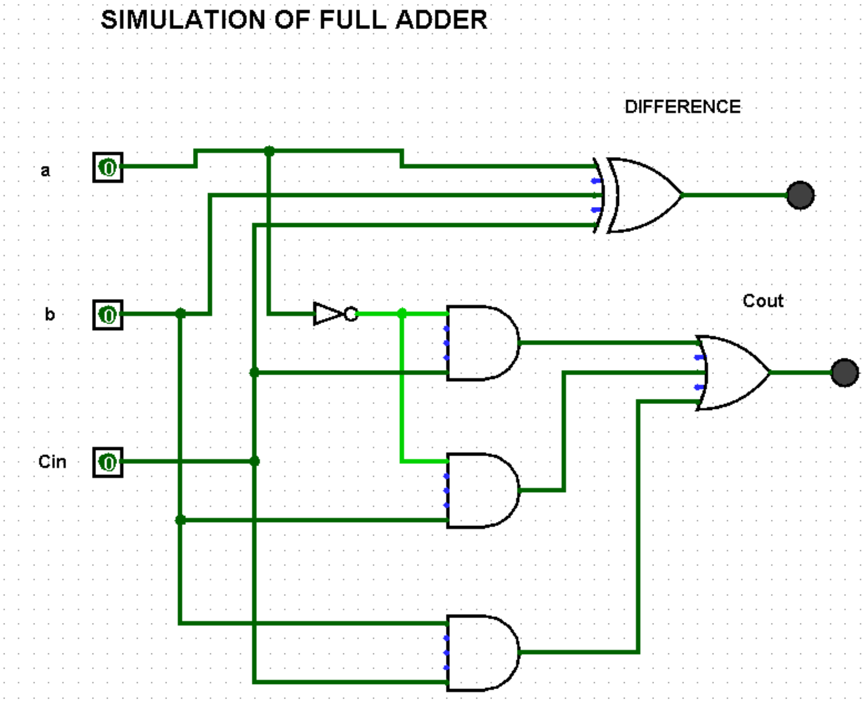


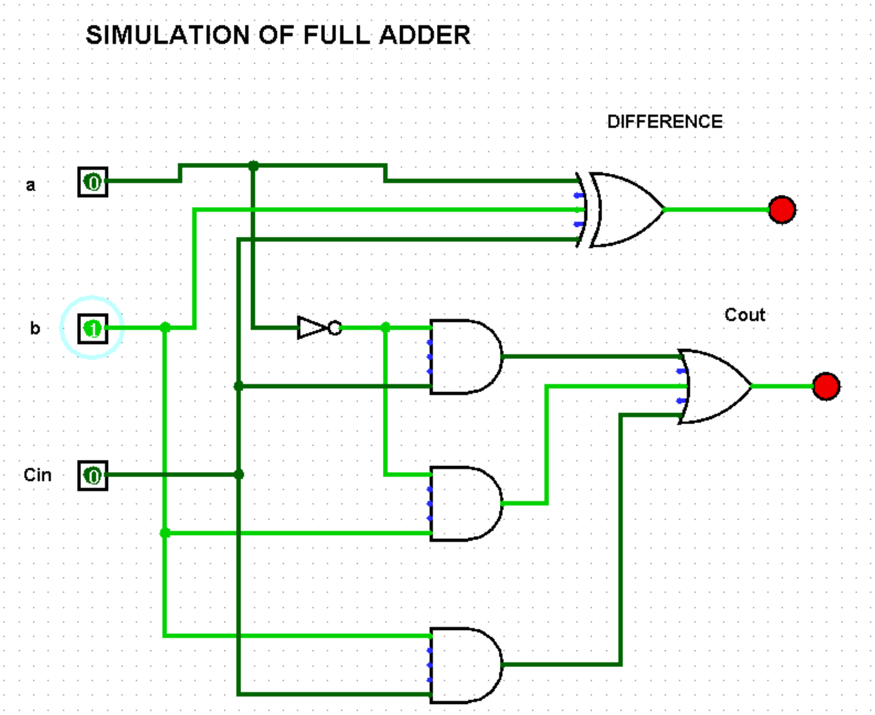
Aim: To construct and simulate FA/FS &HA/HS



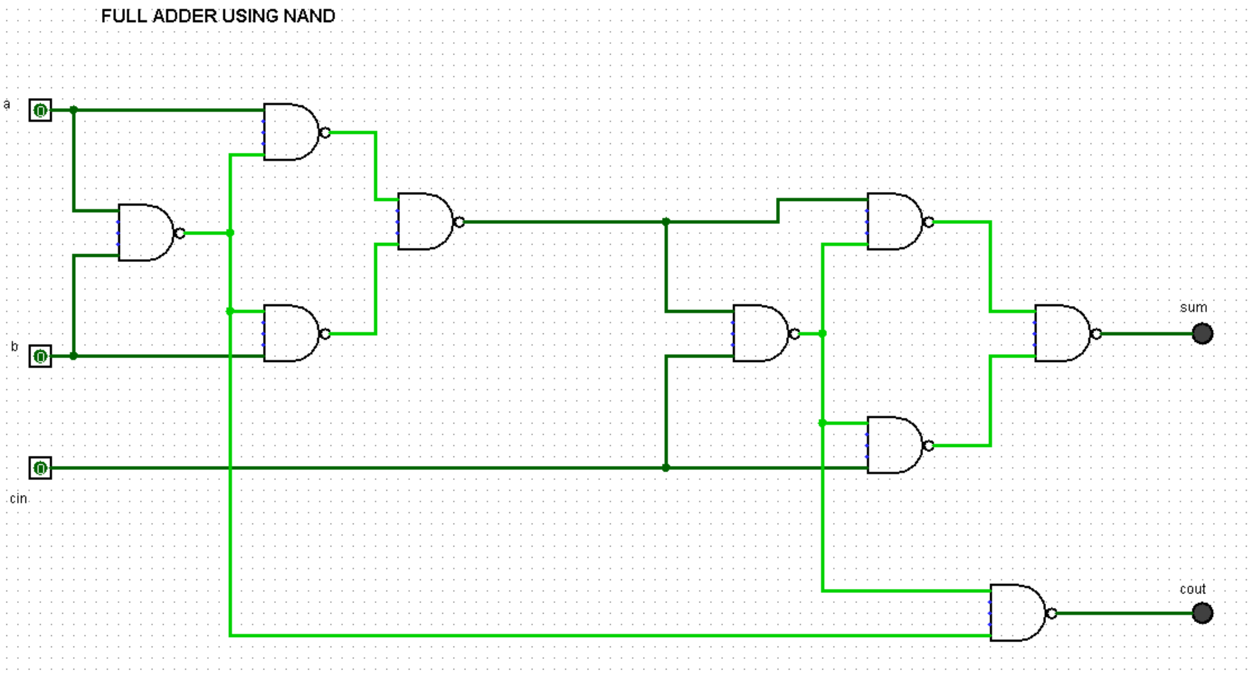
Aim: To construct and simulate FA/FS &HA/HS

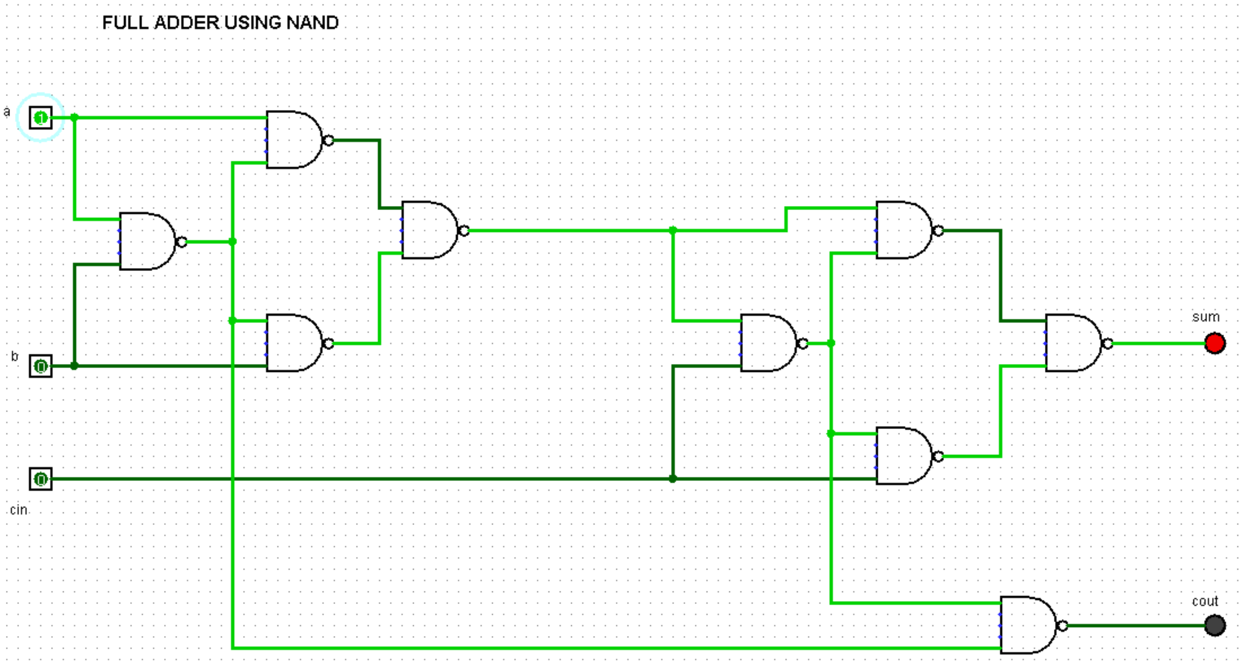
2)



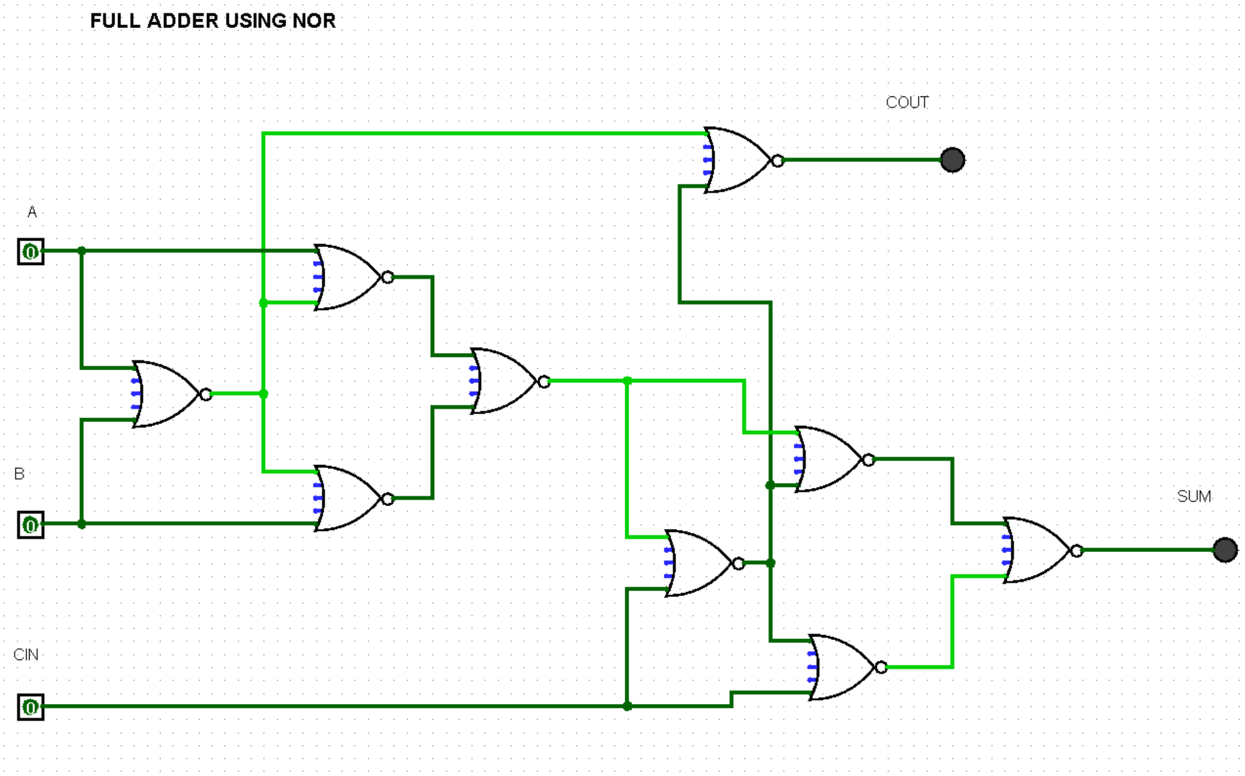


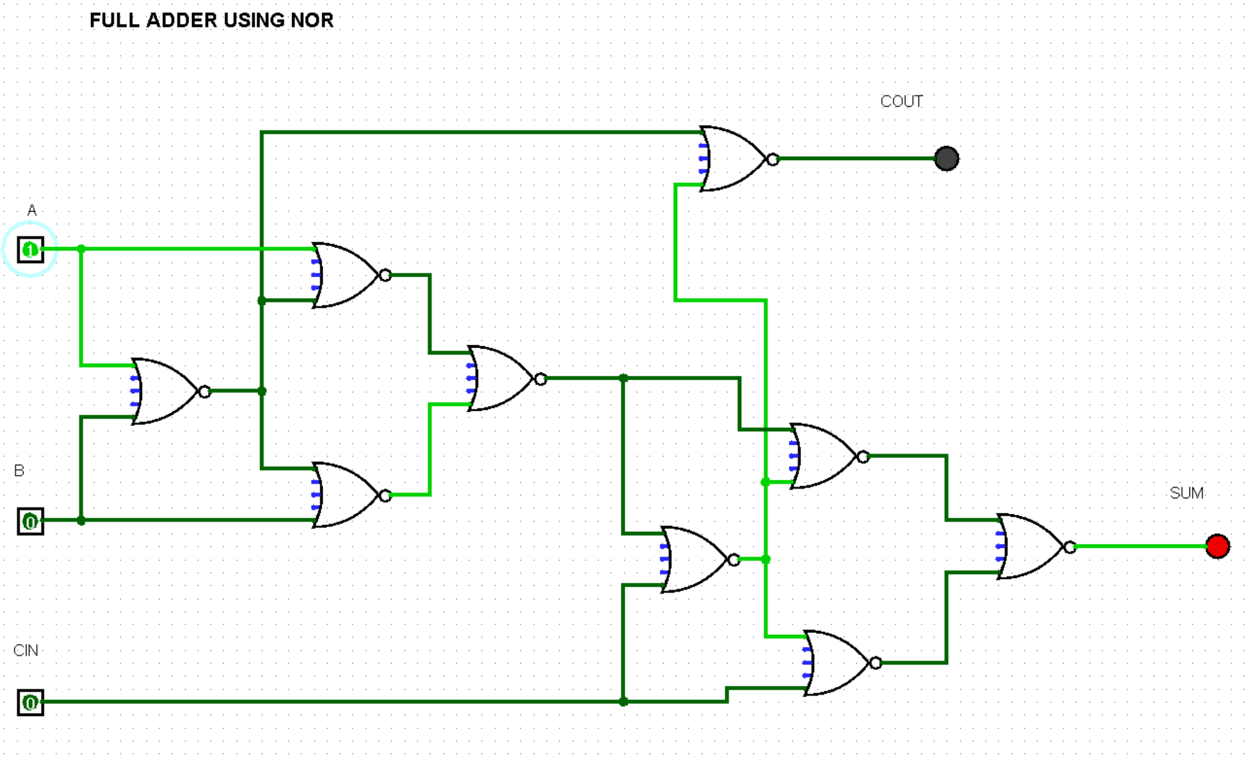
Aim: To construct and simulate FA/FS &HA/HS





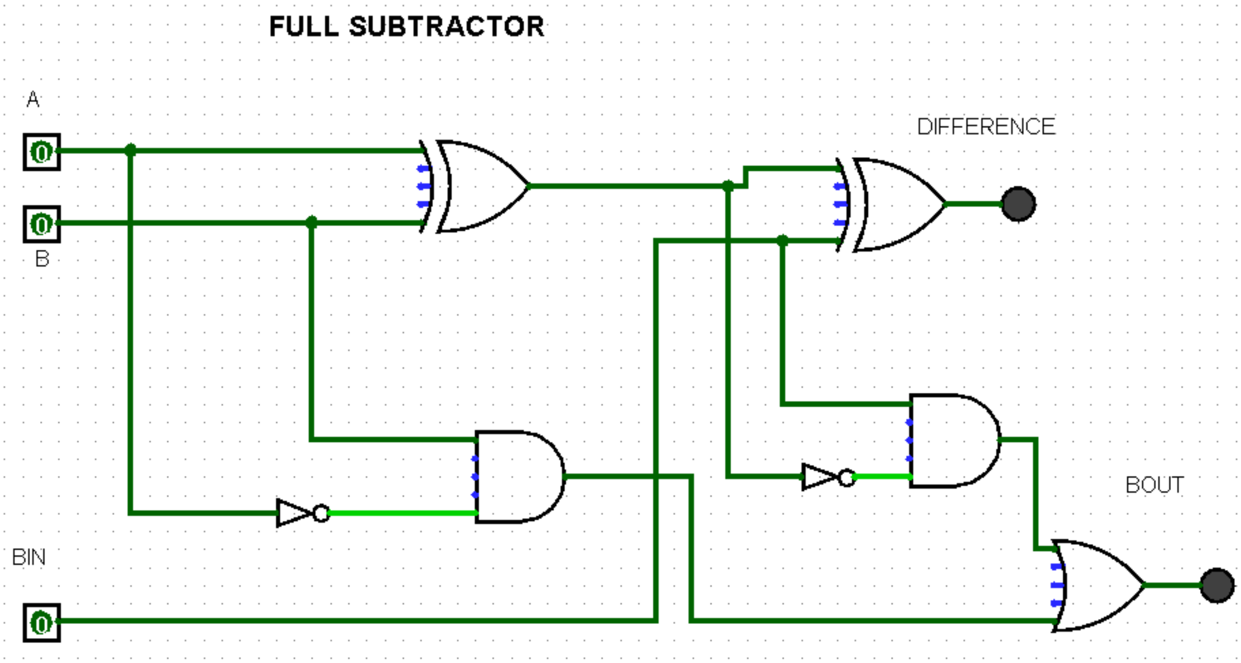
Aim: To construct and simulate FA/FS &HA/HS

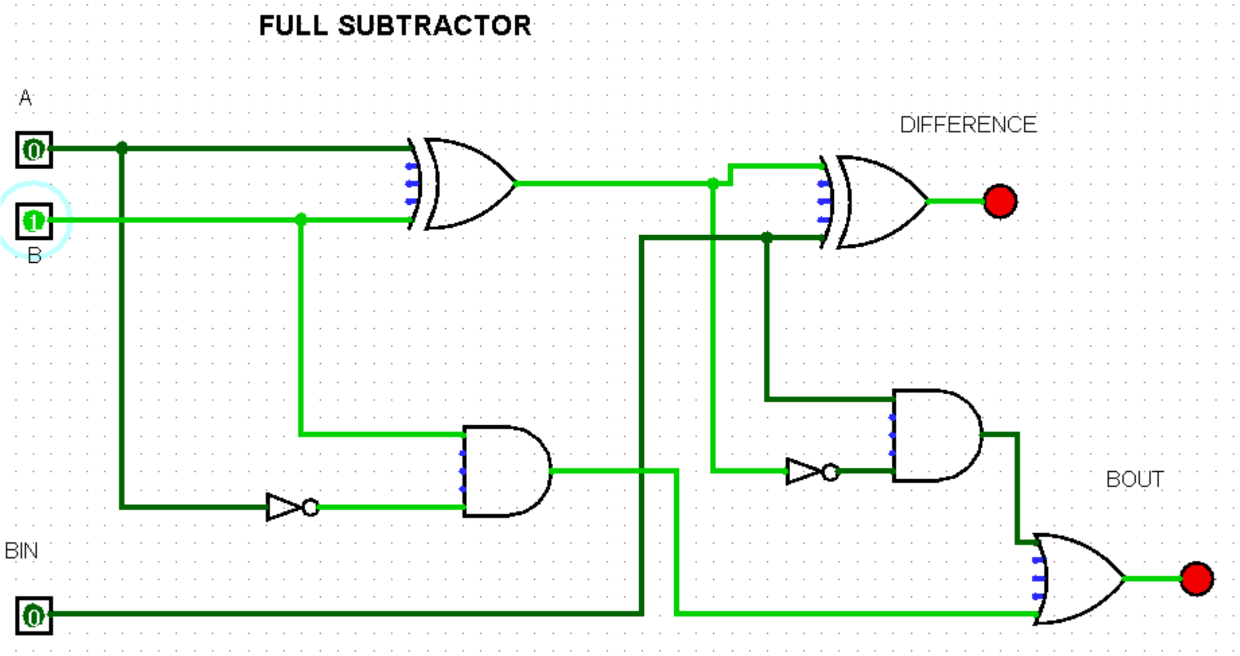




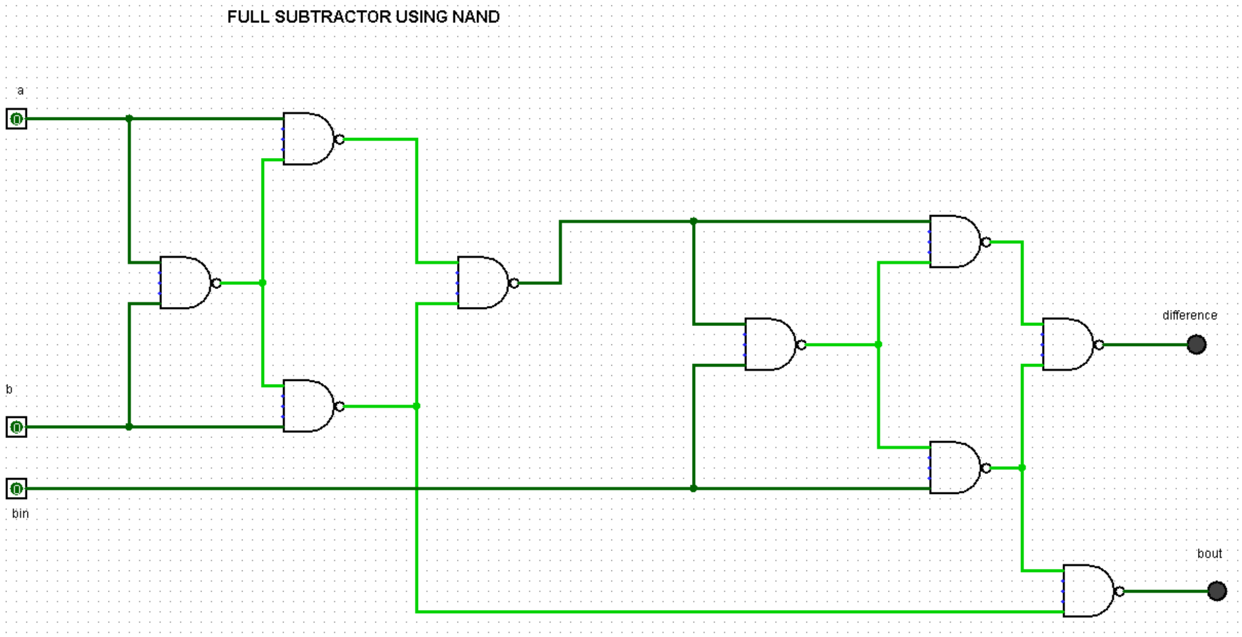
Aim: To construct and simulate FA/FS &HA/HS

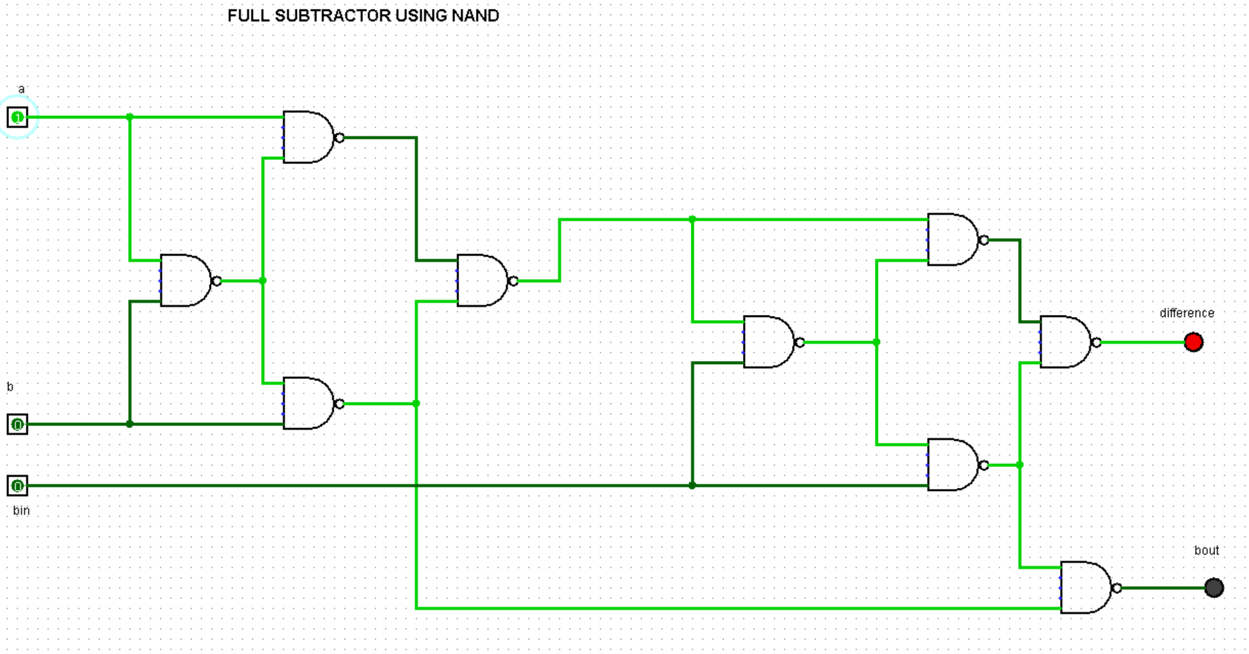
3)



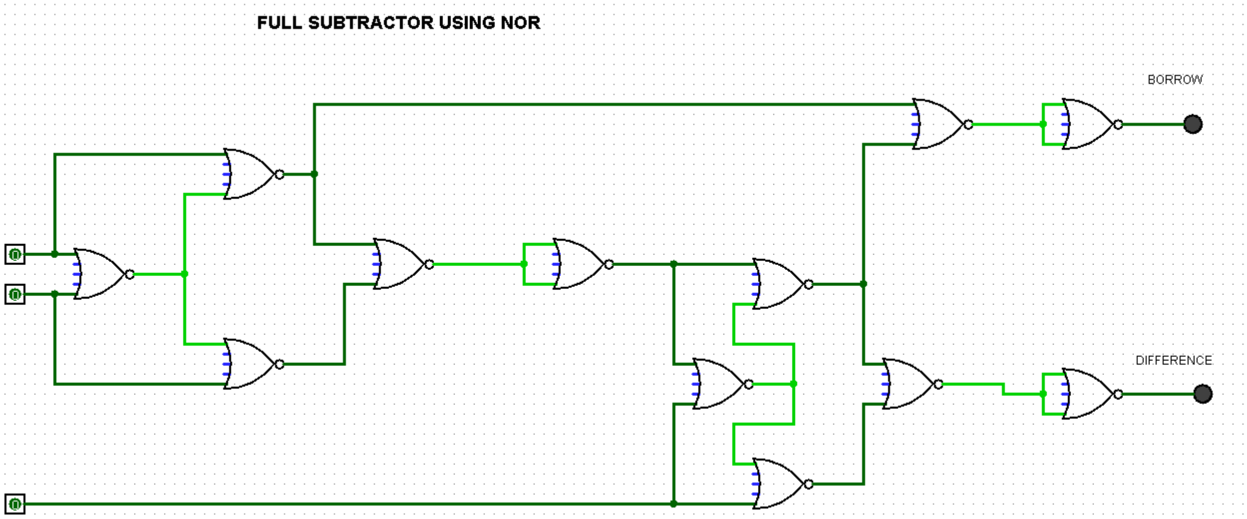


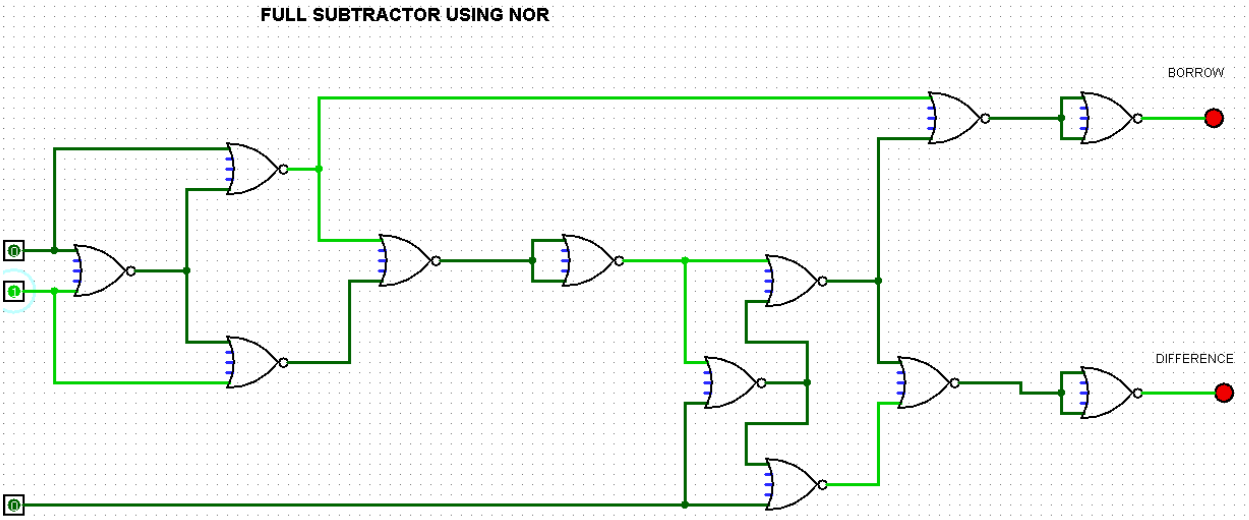
Aim: To construct and simulate FA/FS &HA/HS





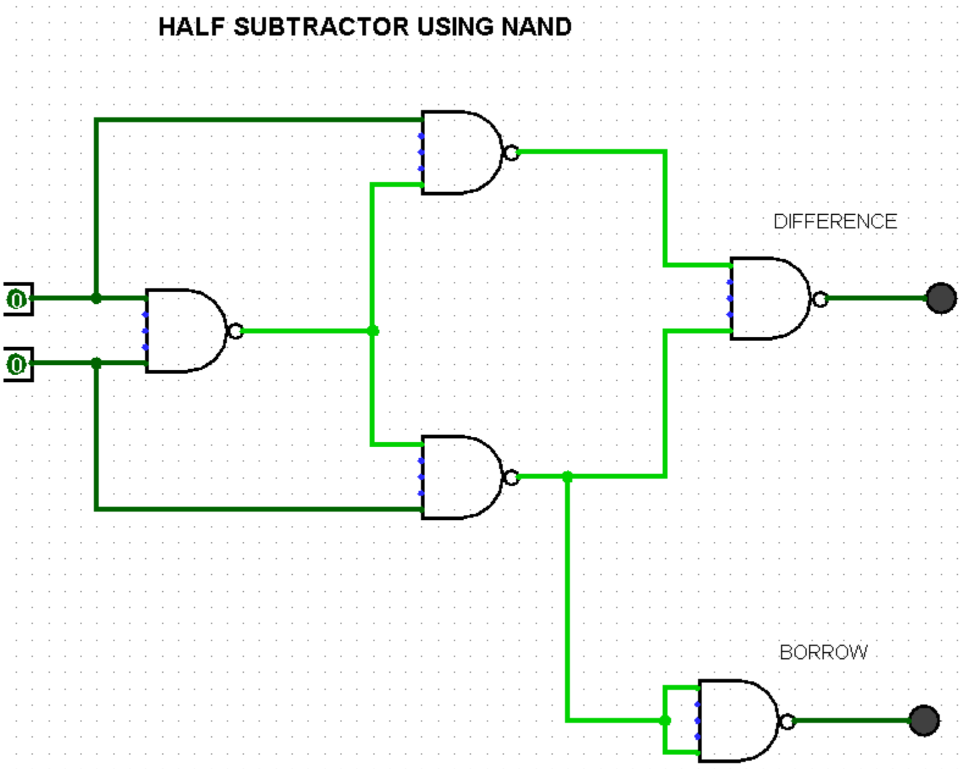
Aim: To construct and simulate FA/FS &HA/HS

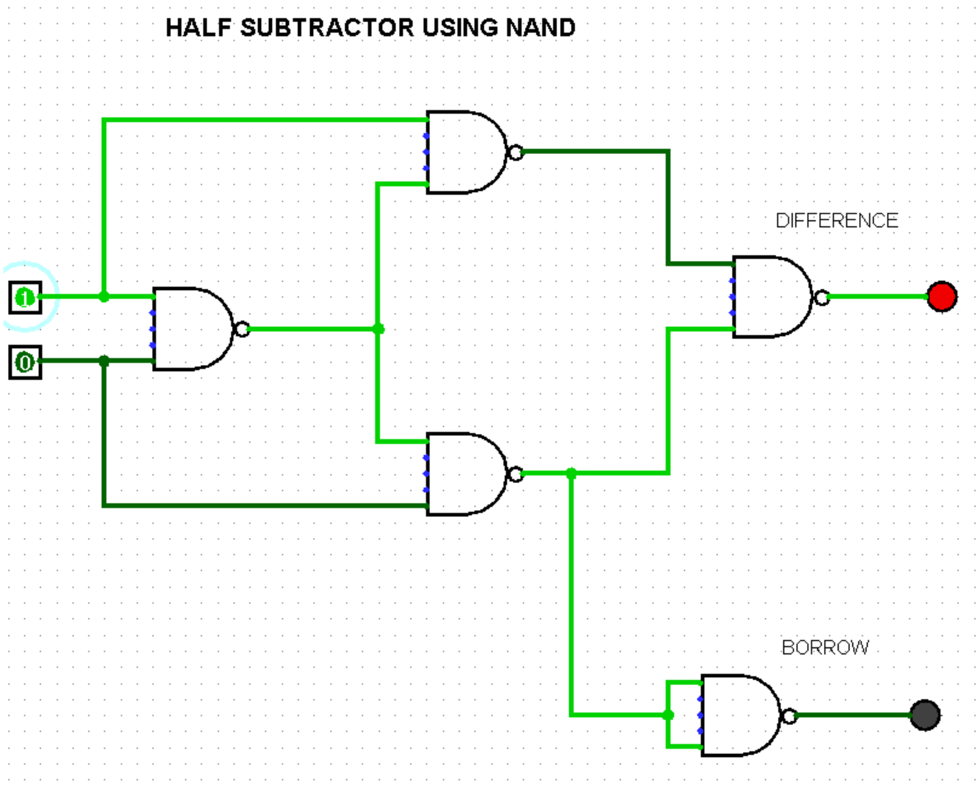




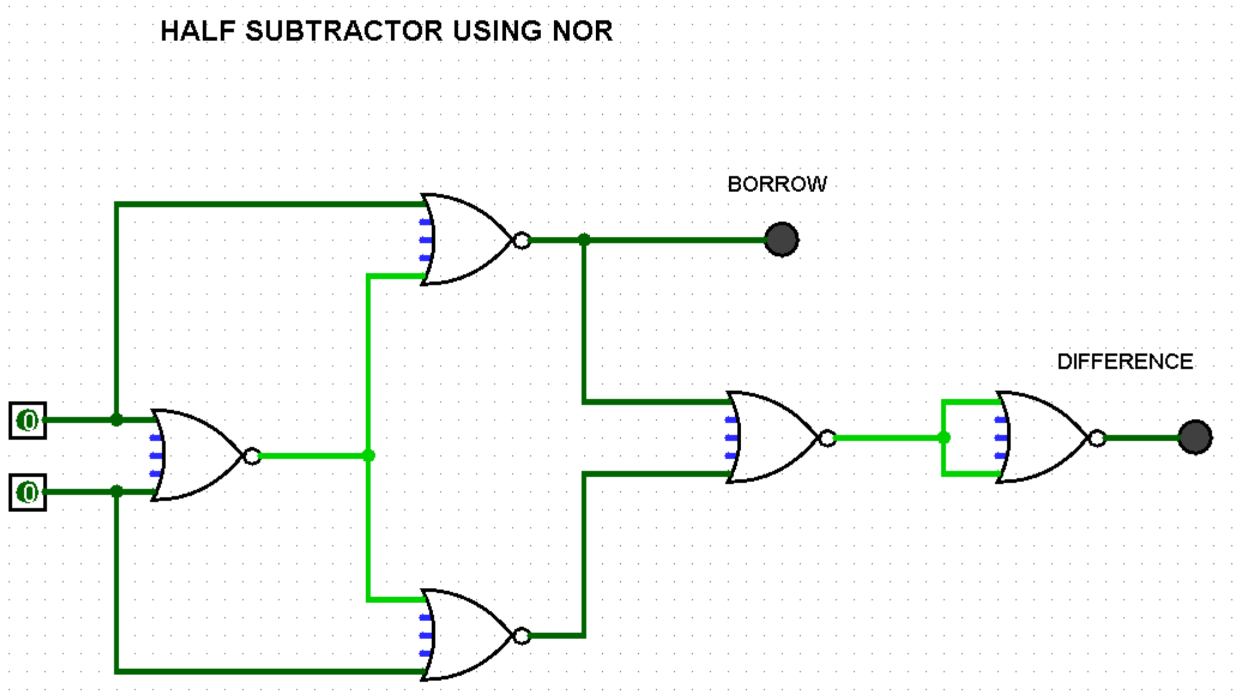
Aim: To construct and simulate FA/FS &HA/HS

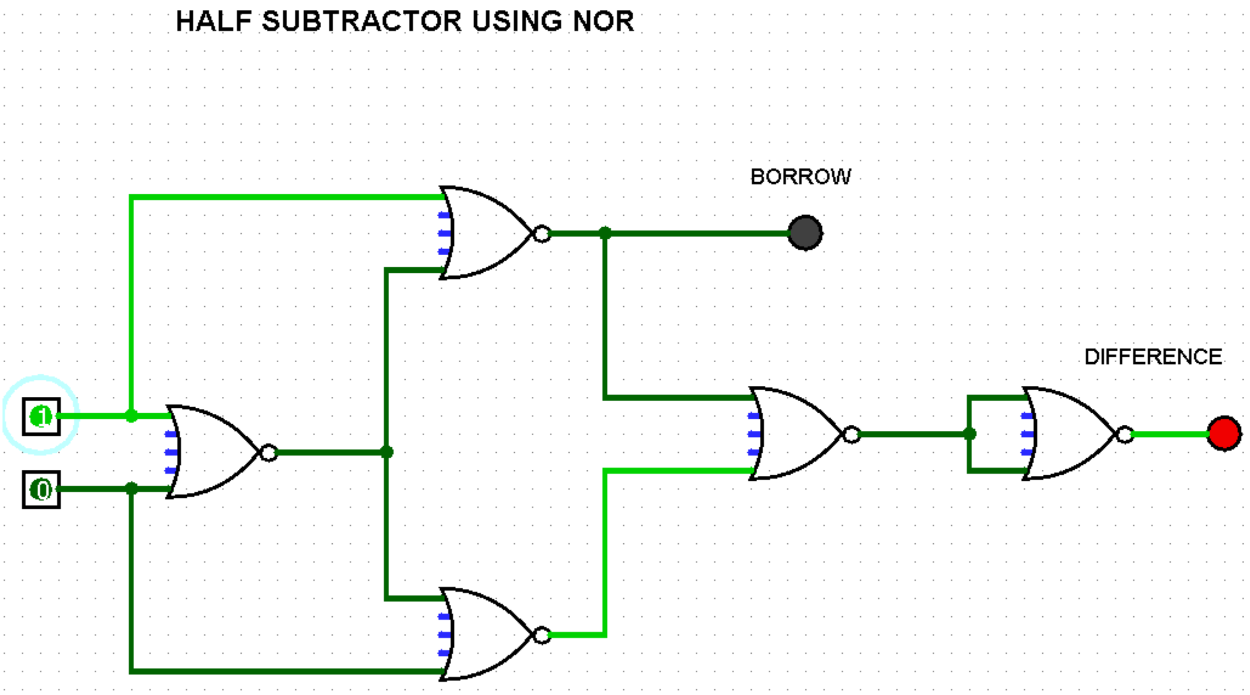
4)



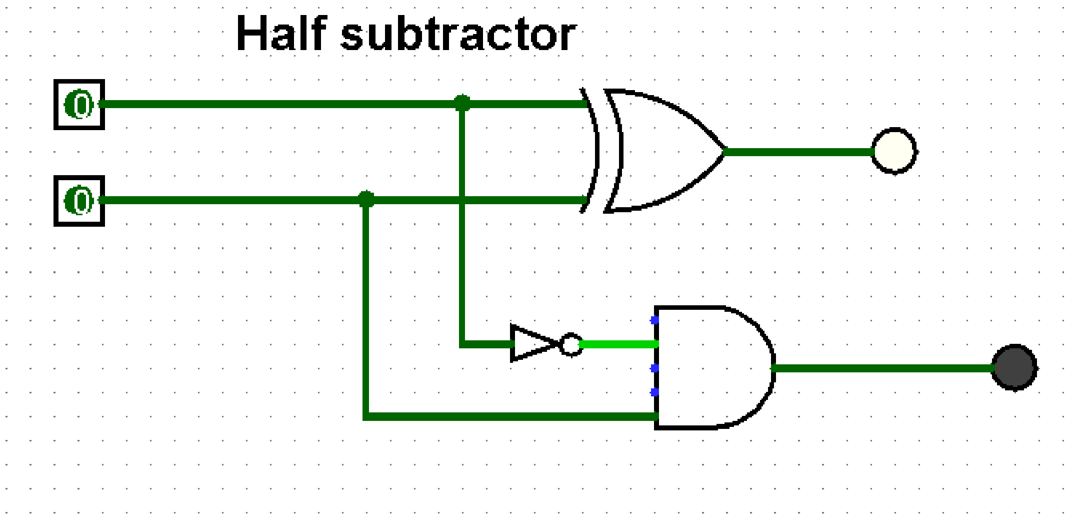


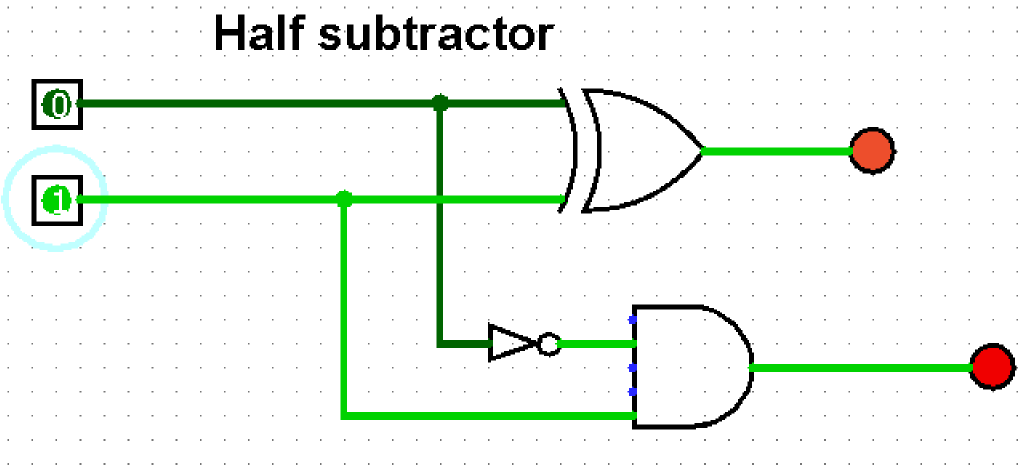
Aim: To construct and simulate FA/FS &HA/HS





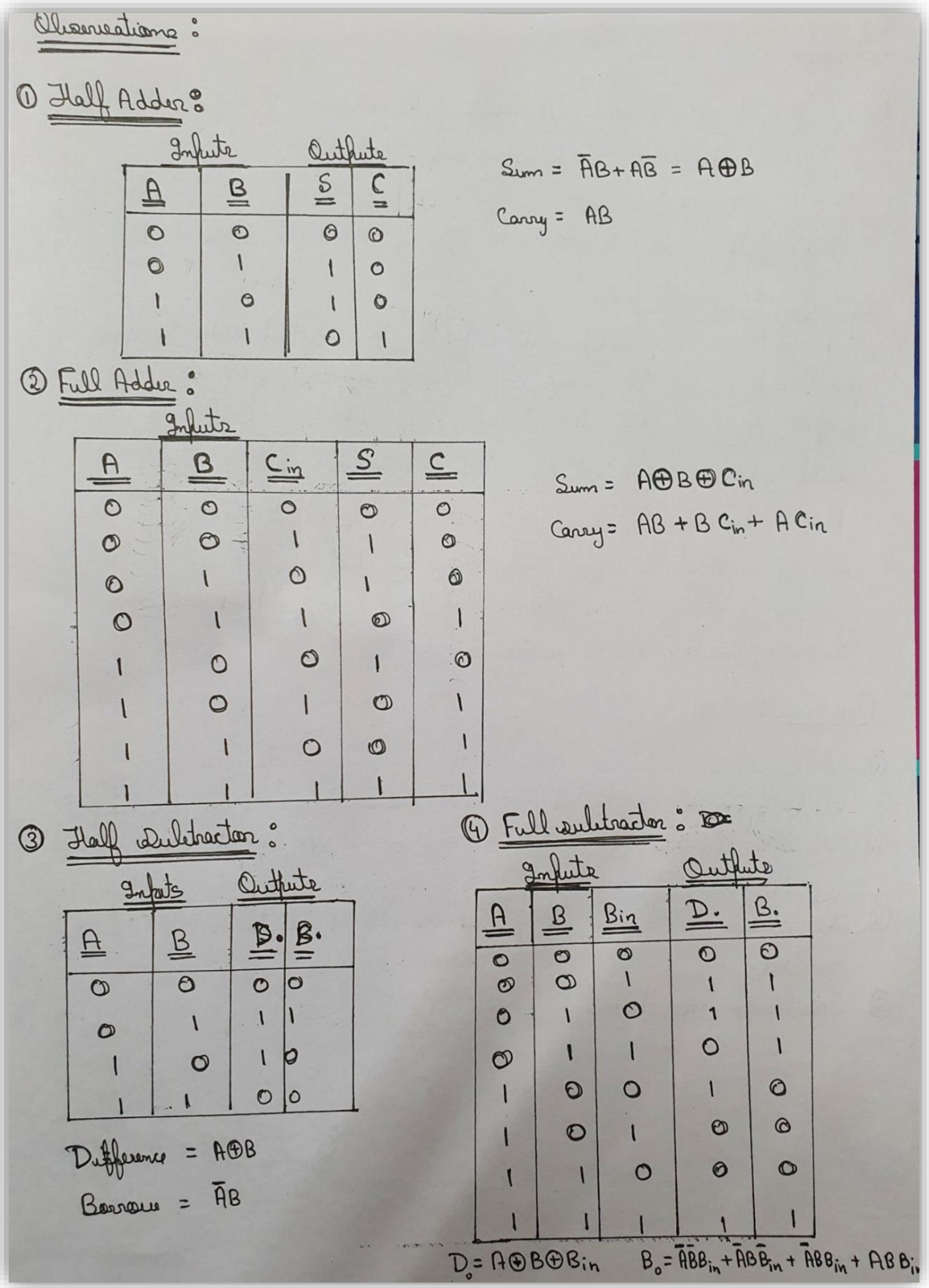
Aim: To construct and simulate FA/FS &HA/HS





Aim: To construct and simulate FA/FS &HA/HS

Observation:



Observations :

① Half Adder :

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum = $\bar{A}B + A\bar{B} = A \oplus B$

Carry = AB

② Full Adder :

Inputs				
A	B	C_{in}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum = $A \oplus B \oplus C_{in}$

Carry = $AB + BC_{in} + AC_{in}$

③ Half Subtractor :

Inputs		Outputs	
A	B	B.	B.
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Difference = $A \oplus B$

Borrow = $\bar{A}B$

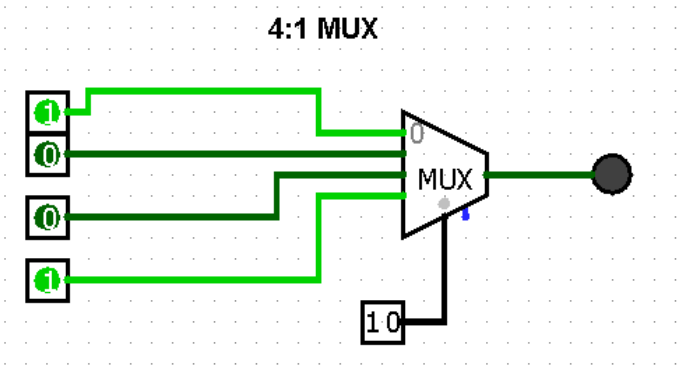
④ Full subtractor :

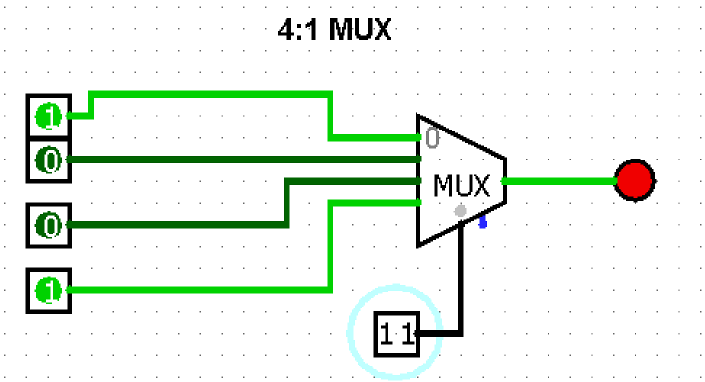
Inputs			Outputs	
A	B	Bin	D.	B.
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D_o = A \oplus B \oplus B_{in}$ $B_o = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + \bar{A}BB_{in} + ABB_{i}$

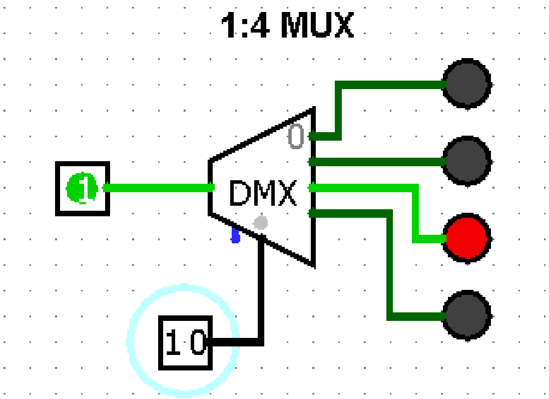
Aim: To simulate various MUX/DEMUX configs

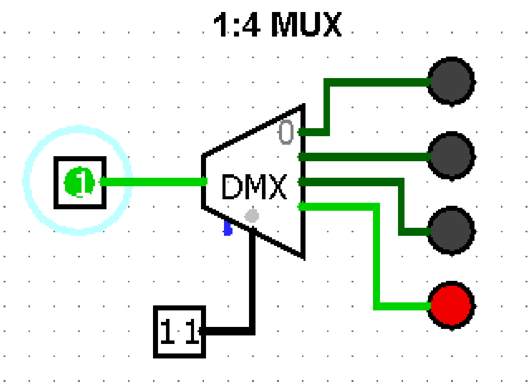
1.



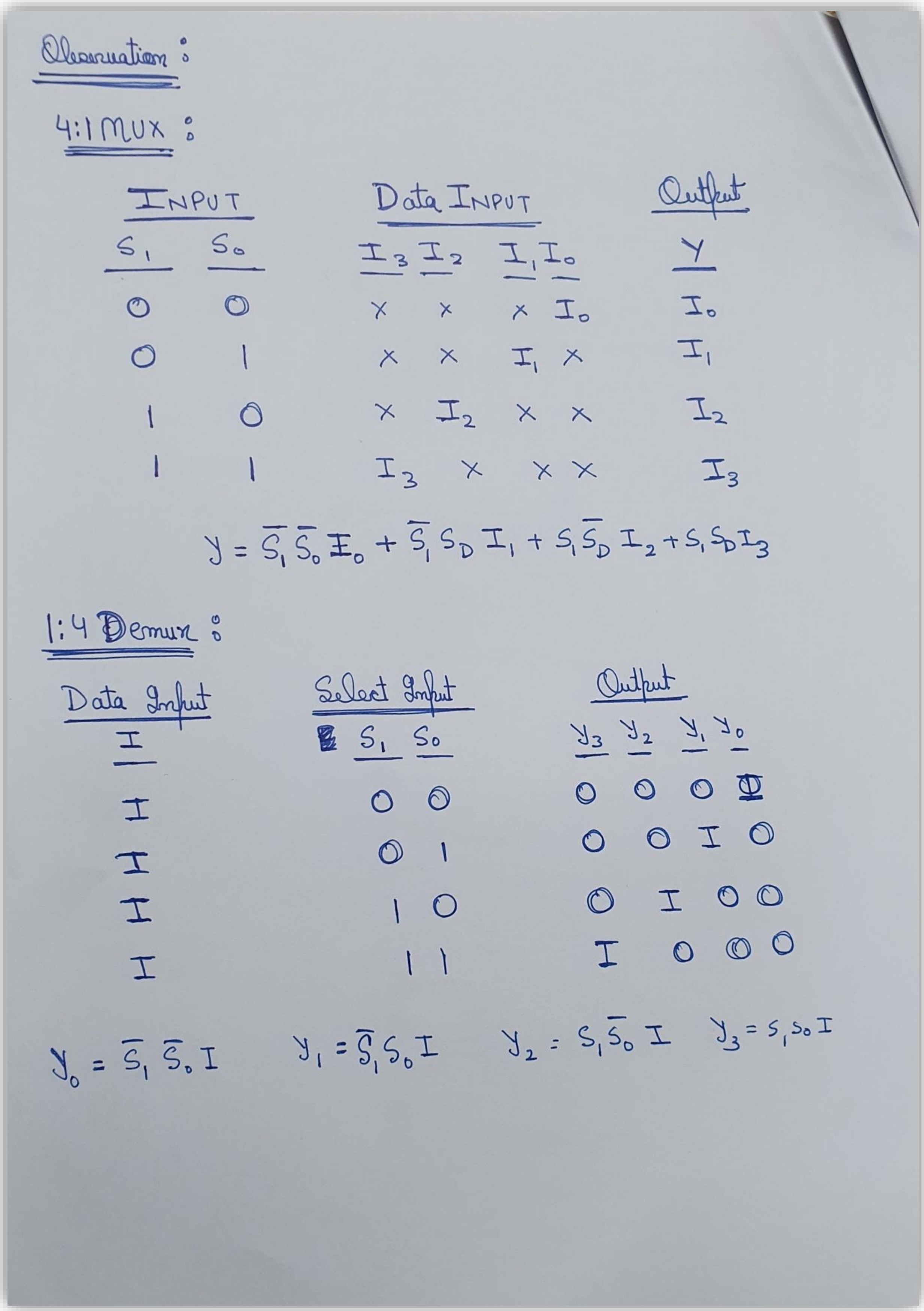


2.





Aim: To simulate various MUX/DEMUX configs



Observation :

4:1 MUX :

INPUT		Data INPUT				Output
S_1	S_0	I_3	I_2	I_1	I_0	Y
0	0	x	x	x	I_0	I_0
0	1	x	x	I_1	x	I_1
1	0	x	I_2	x	x	I_2
1	1	I_3	x	x	x	I_3

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_D I_1 + S_1 \bar{S}_D I_2 + S_1 S_D I_3$$

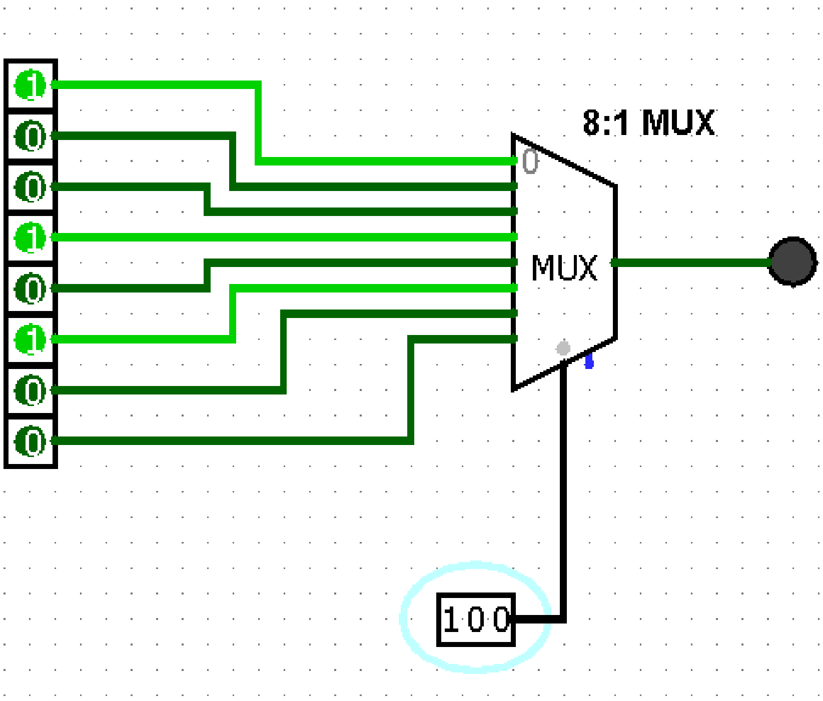
1:4 Demux :

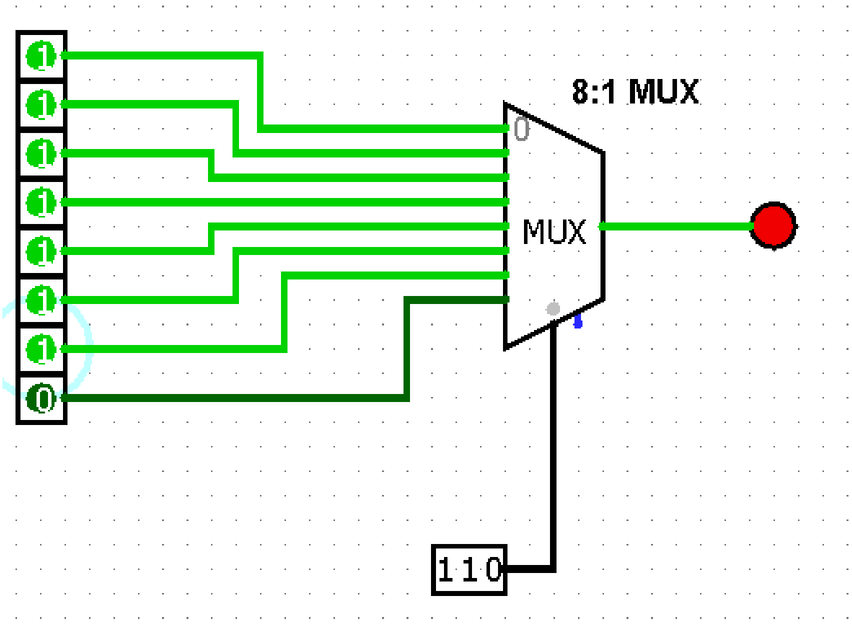
Data Input	Select Input		Output			
I	S_1	S_0	Y_3	Y_2	Y_1	Y_0
I	0	0	0	0	0	I
I	0	1	0	0	I	0
I	1	0	0	I	0	0
I	1	1	I	0	0	0

$Y_0 = \bar{S}_1 \bar{S}_0 I$ $\quad Y_1 = \bar{S}_1 S_0 I$ $\quad Y_2 = S_1 \bar{S}_0 I$ $\quad Y_3 = S_1 S_0 I$

Aim: To simulate various MUX/DEMUX configs

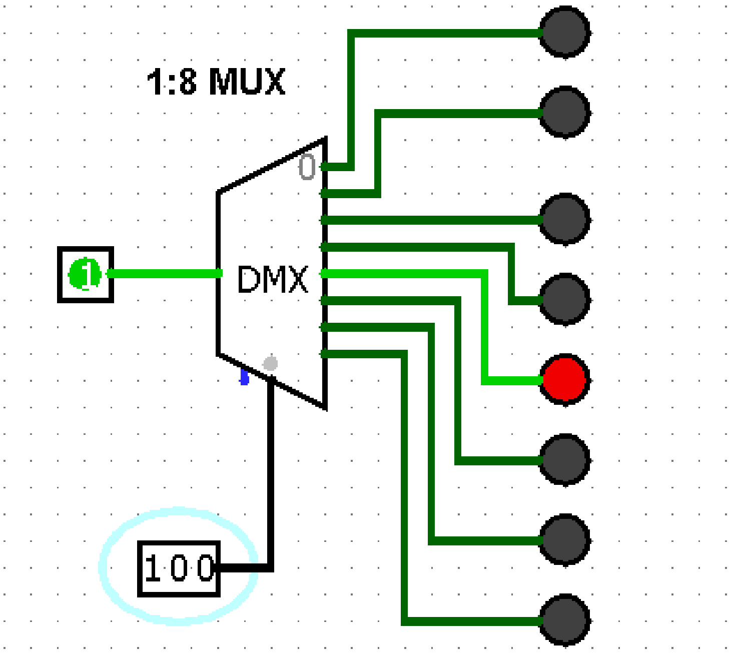
3.

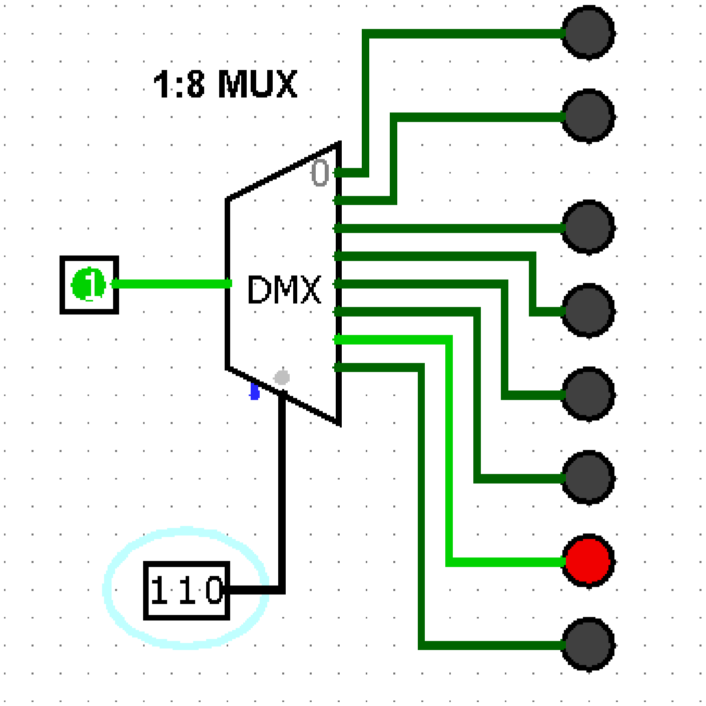




Aim: To simulate various MUX/DEMUX configs

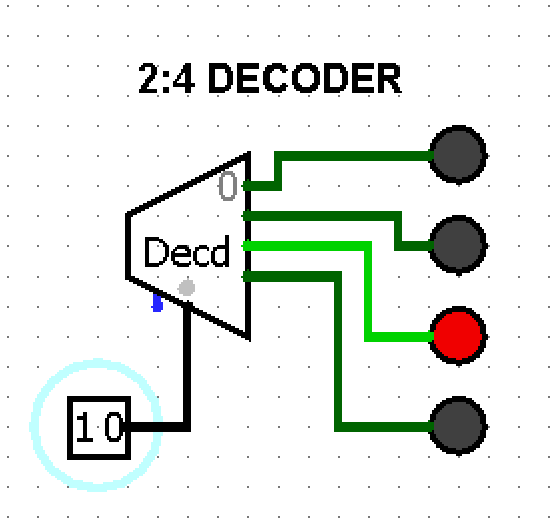
4.

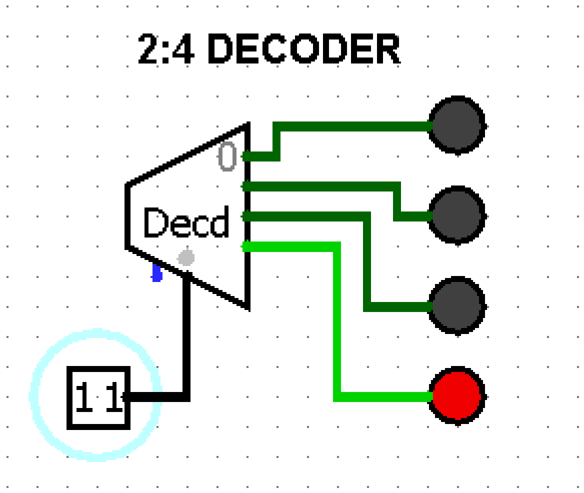




Aim: To simulate various MUX/DEMUX configs

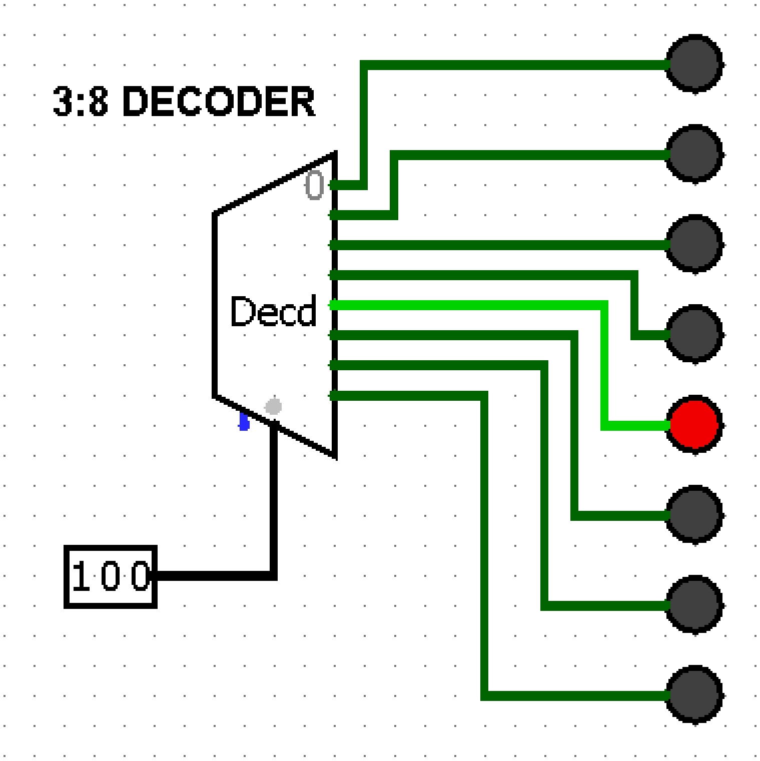
5.

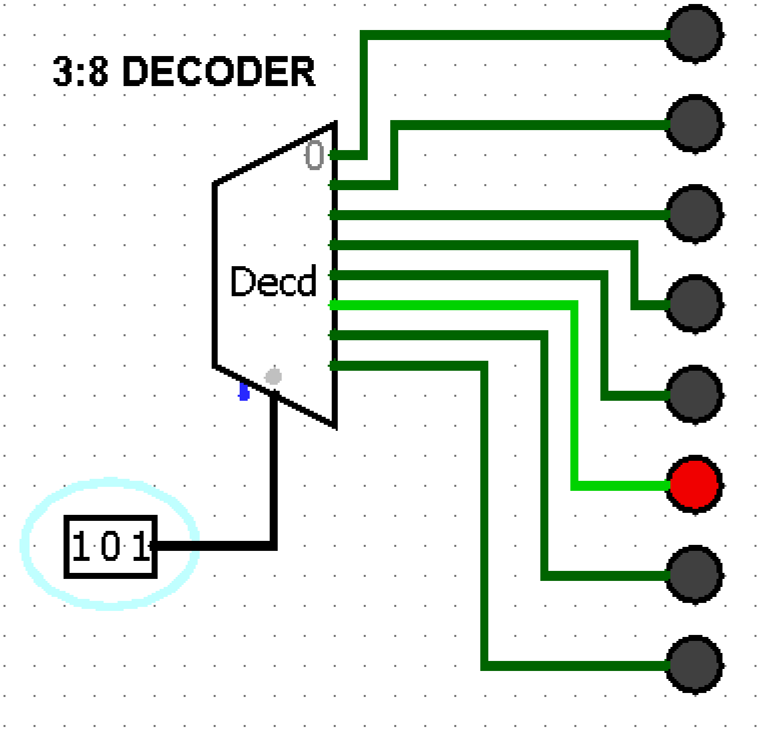




Aim: To simulate various MUX/DEMUX configs

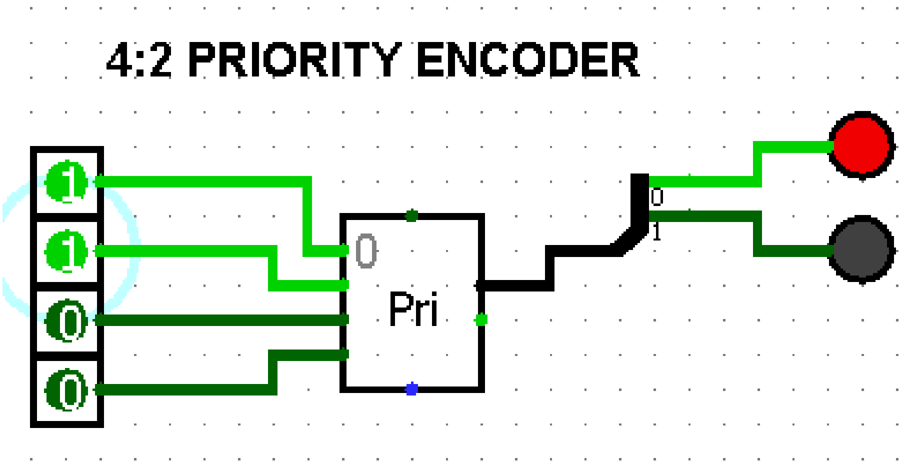
6.

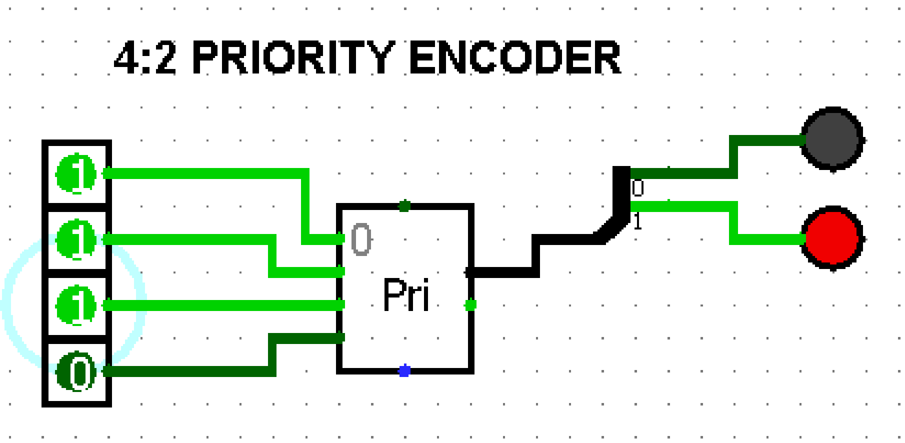




Aim: To simulate various MUX/DEMUX configs

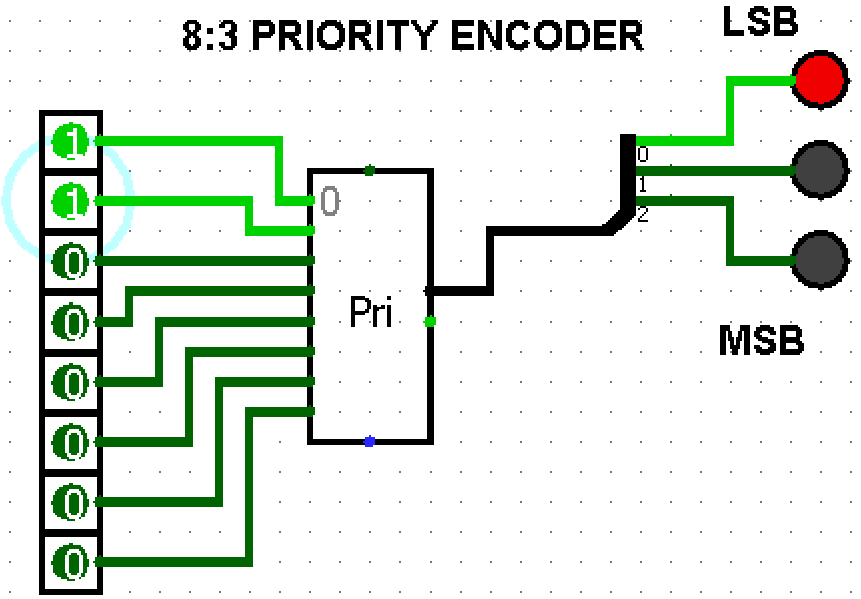
7.

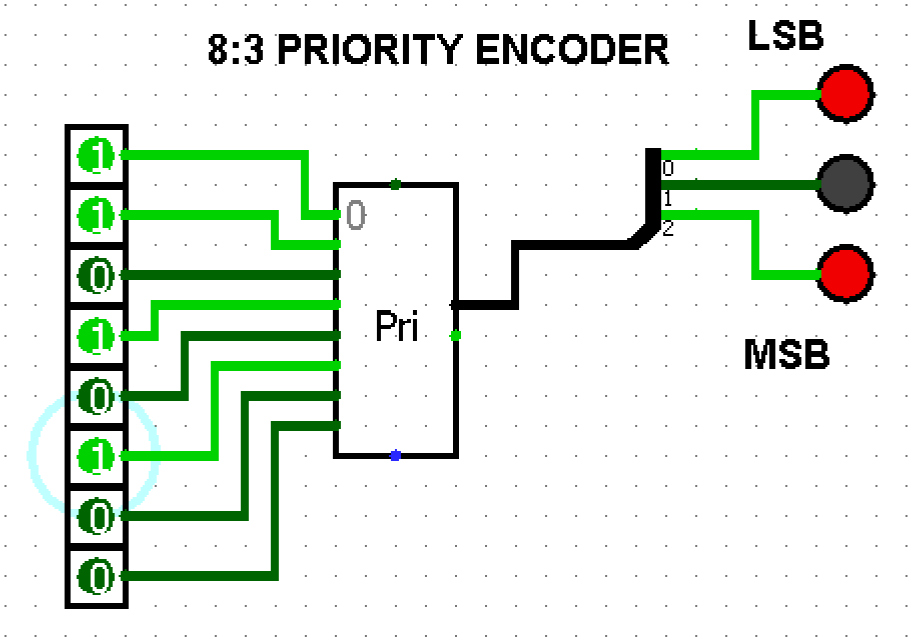




Aim: To simulate various MUX/DEMUX configs

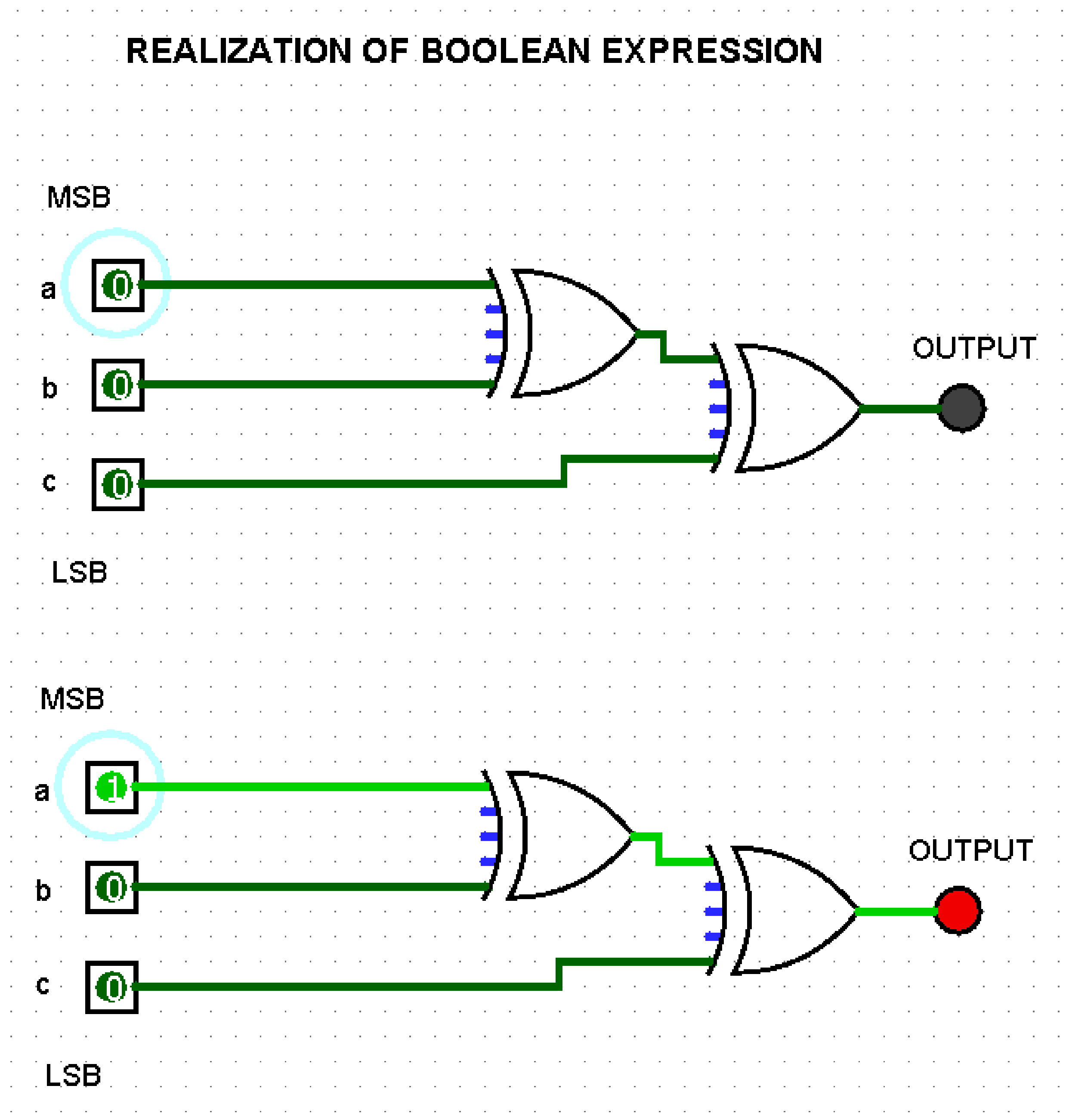
8.



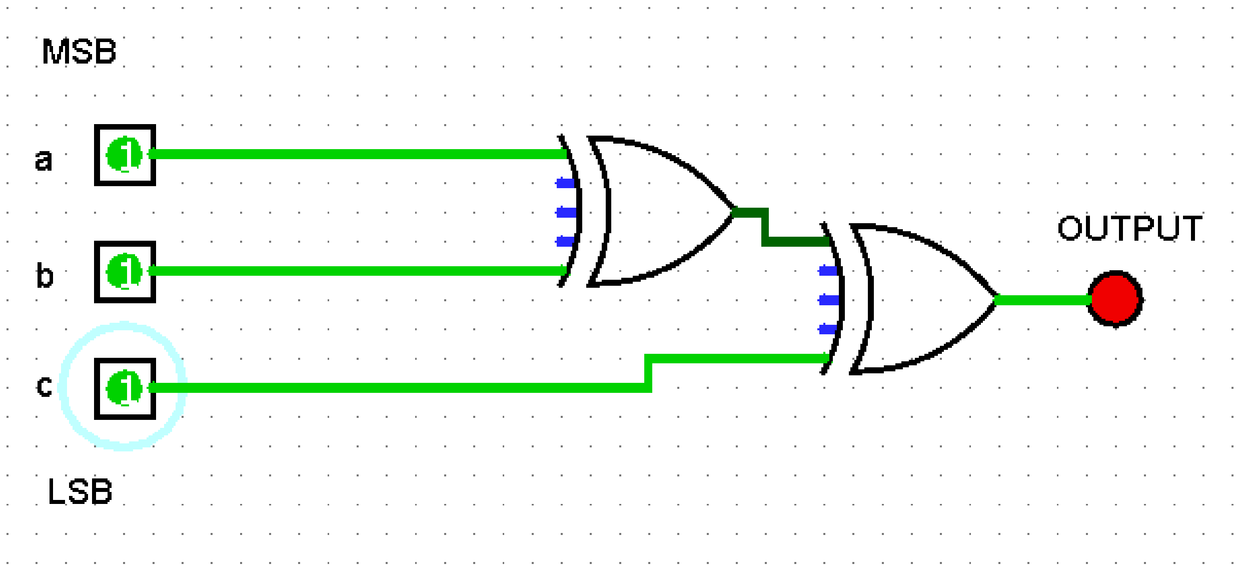


Aim: Realization of Boolean Expression/ MUX & Demux using Gates

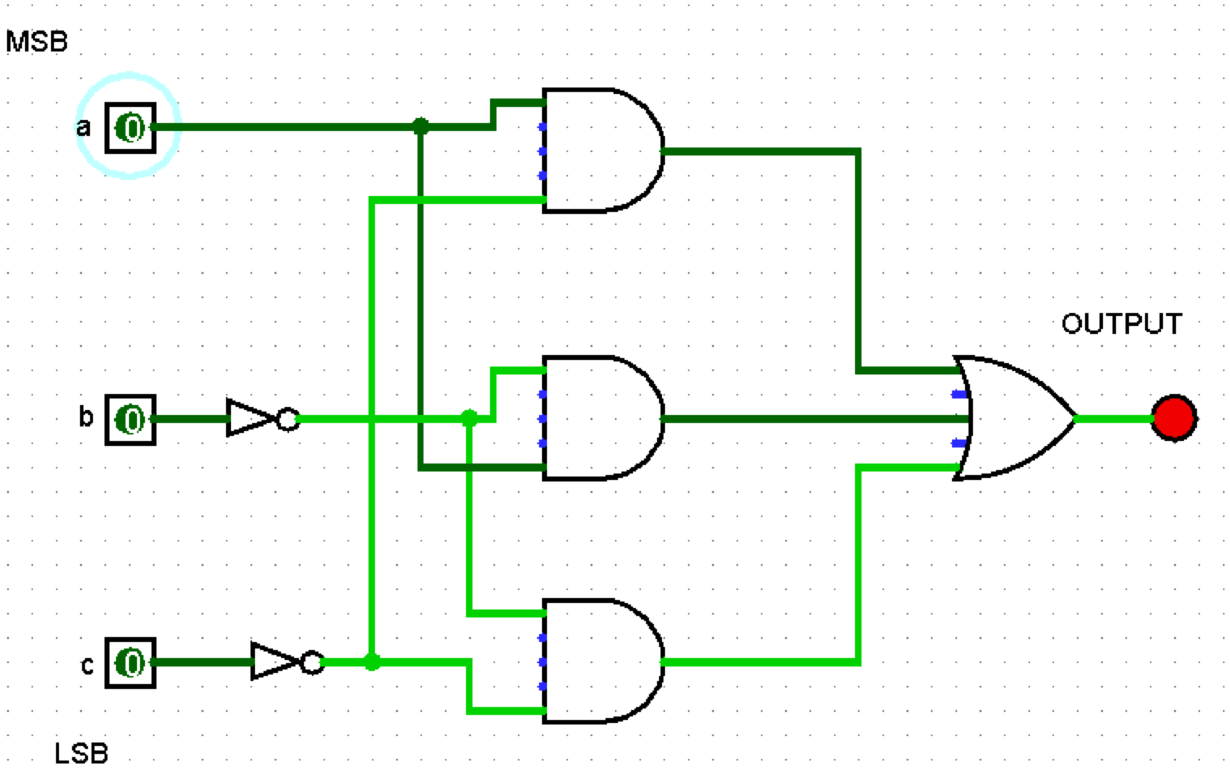
1.



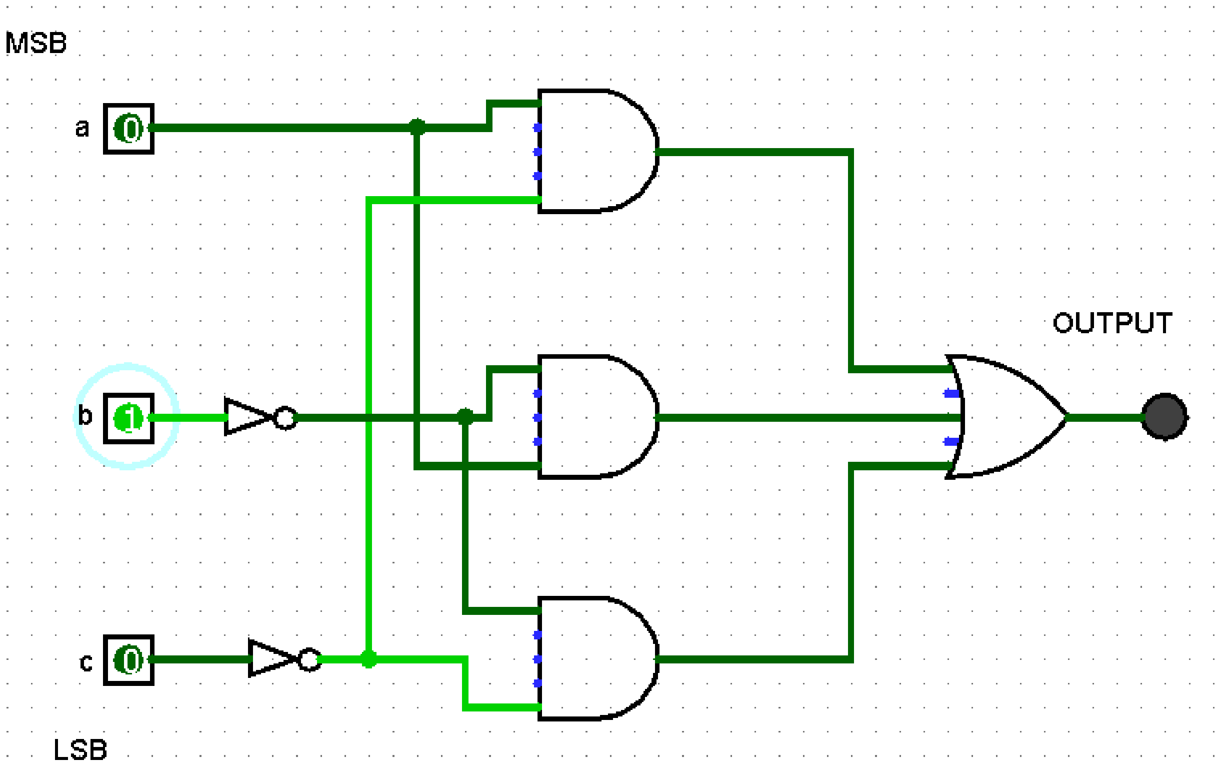
Aim: Realization of Boolean Expression/ MUX & Demux using Gates

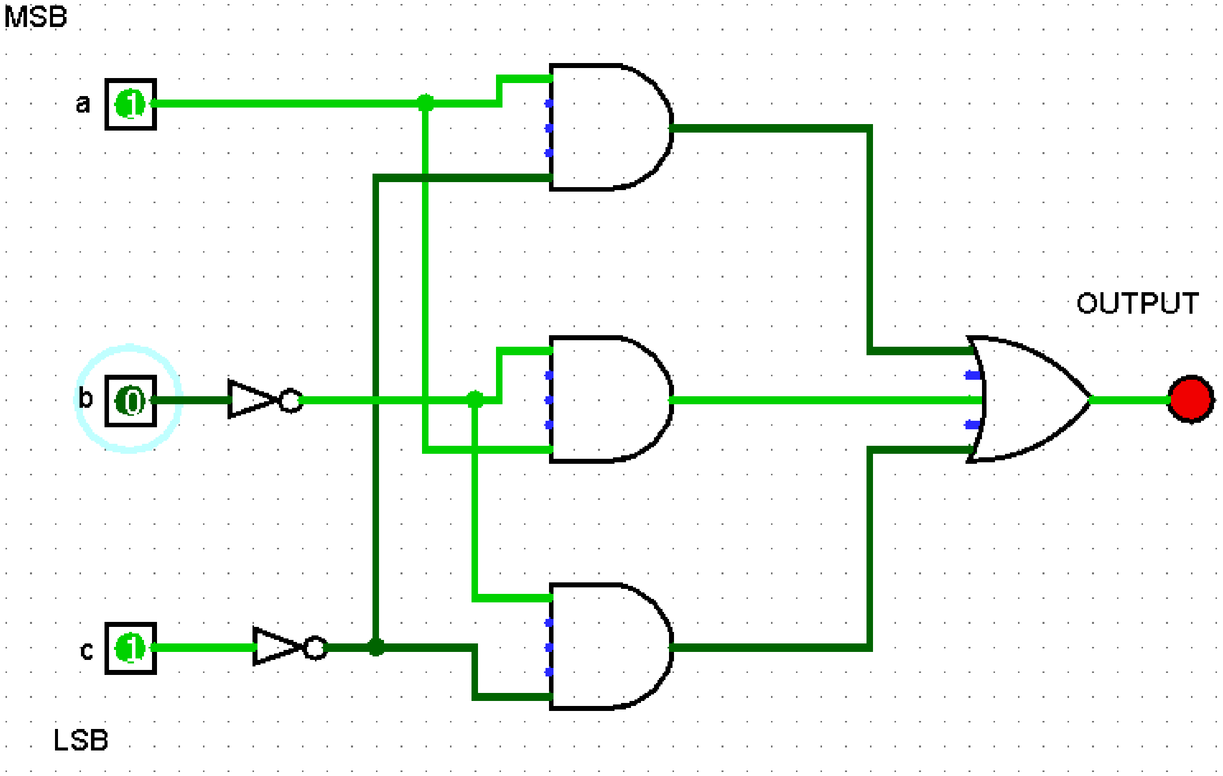


2.



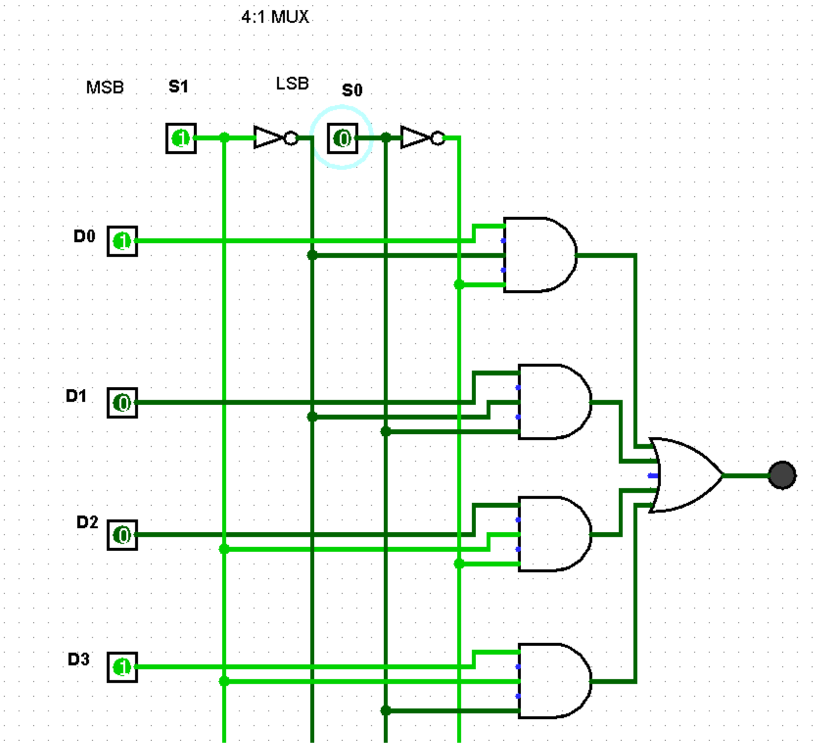
Aim: Realization of Boolean Expression/ MUX & Demux using Gates

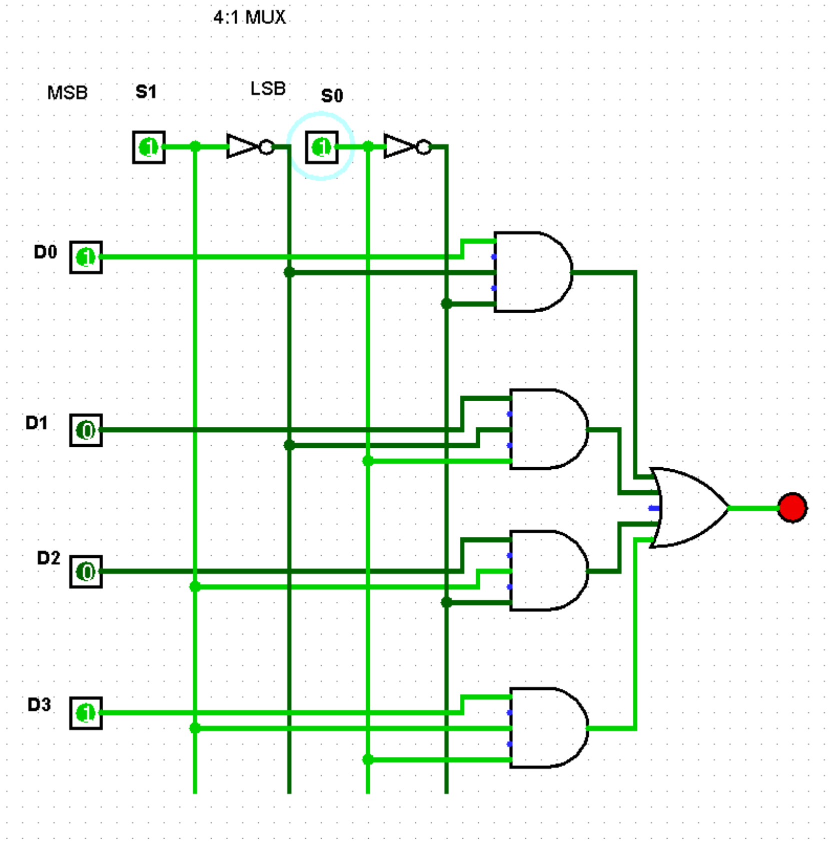




Aim: Realization of Boolean Expression/ MUX & Demux using Gates

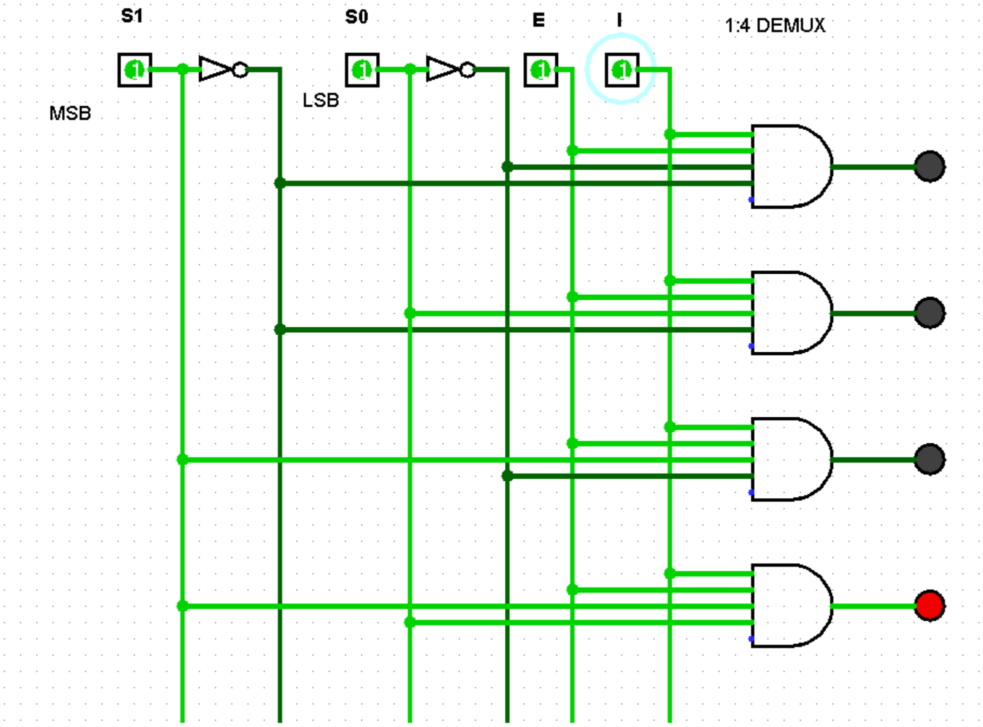
3.

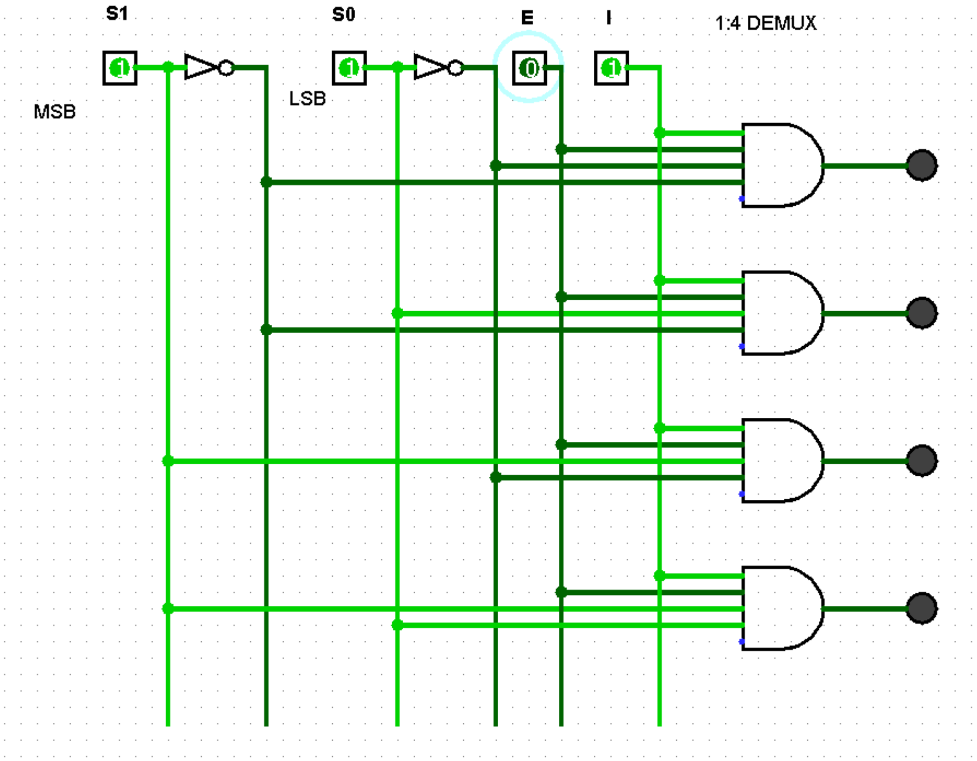




Aim: Realization of Boolean Expression/ MUX & Demux using Gates

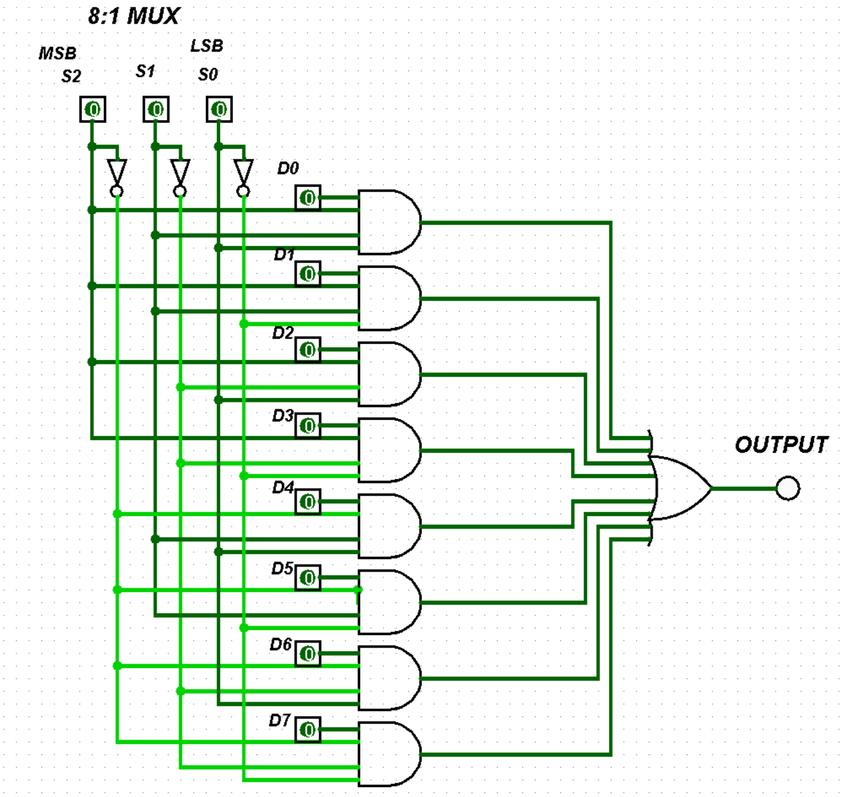
4.

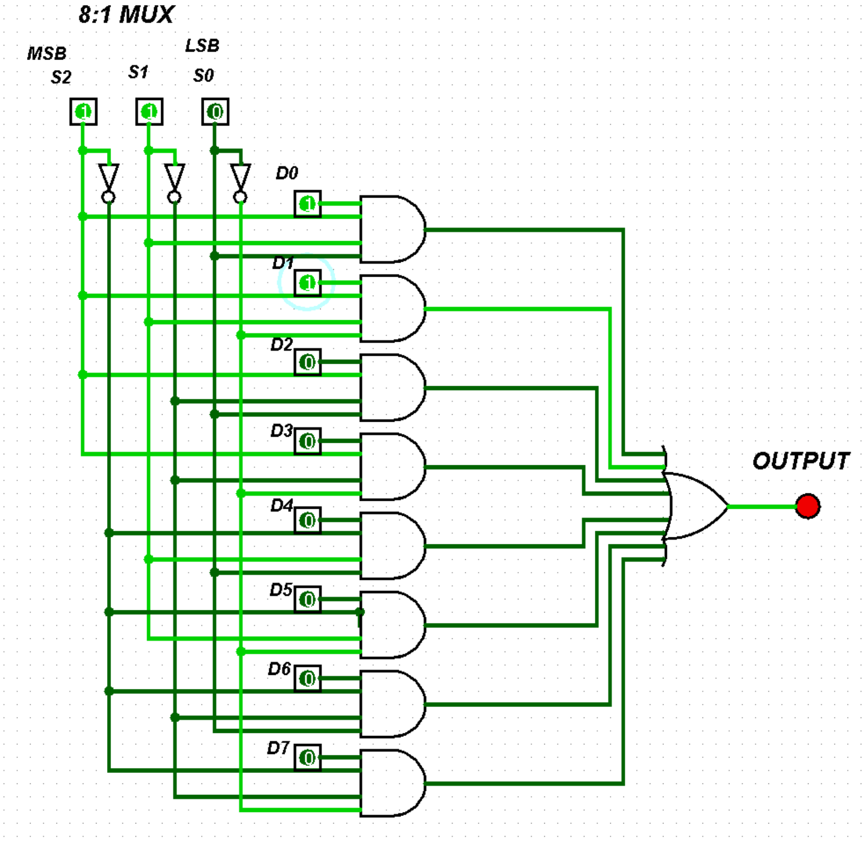




Aim: Realization of Boolean Expression/ MUX & Demux using Gates

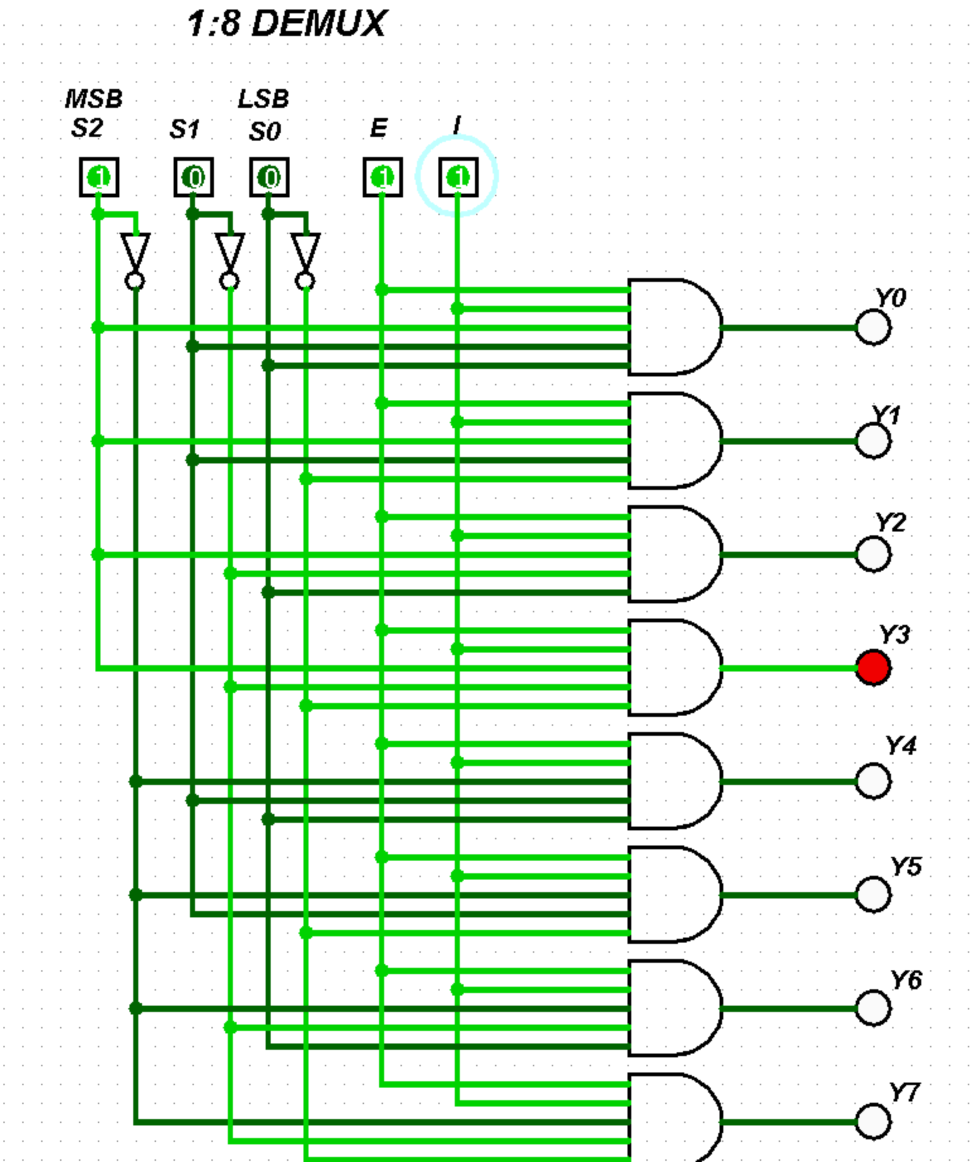
5.



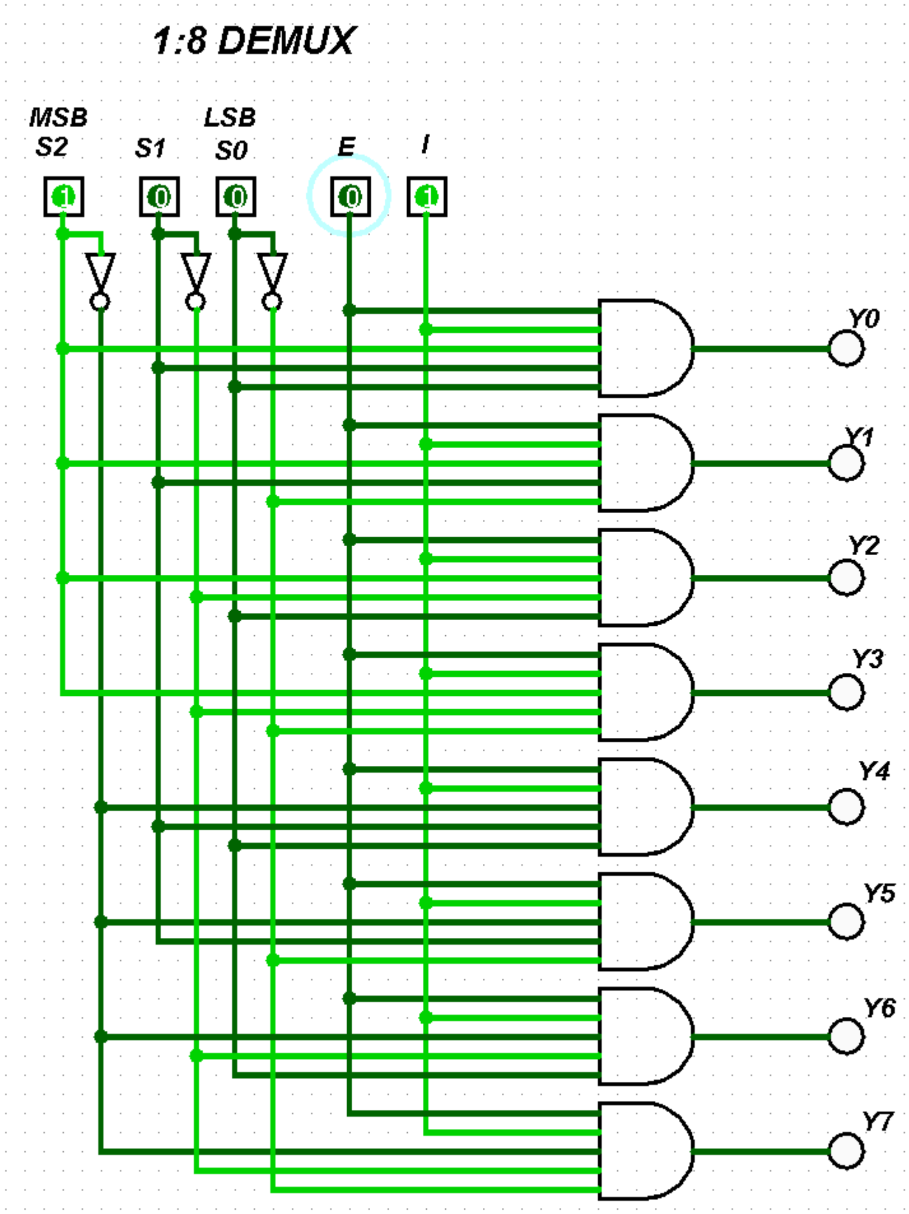


Aim: Realization of Boolean Expression/ MUX & Demux using Gates

6.

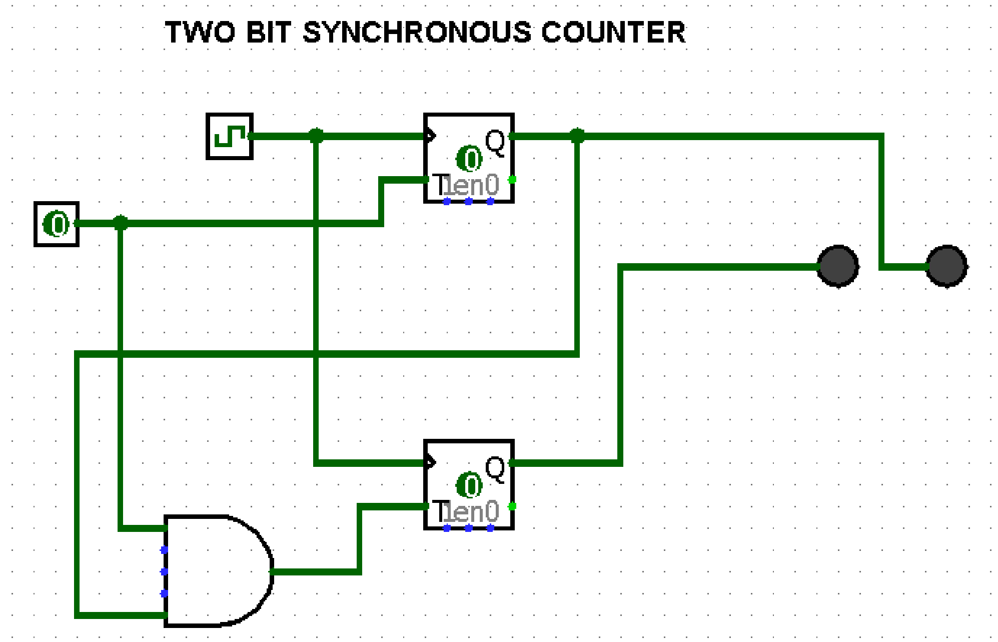


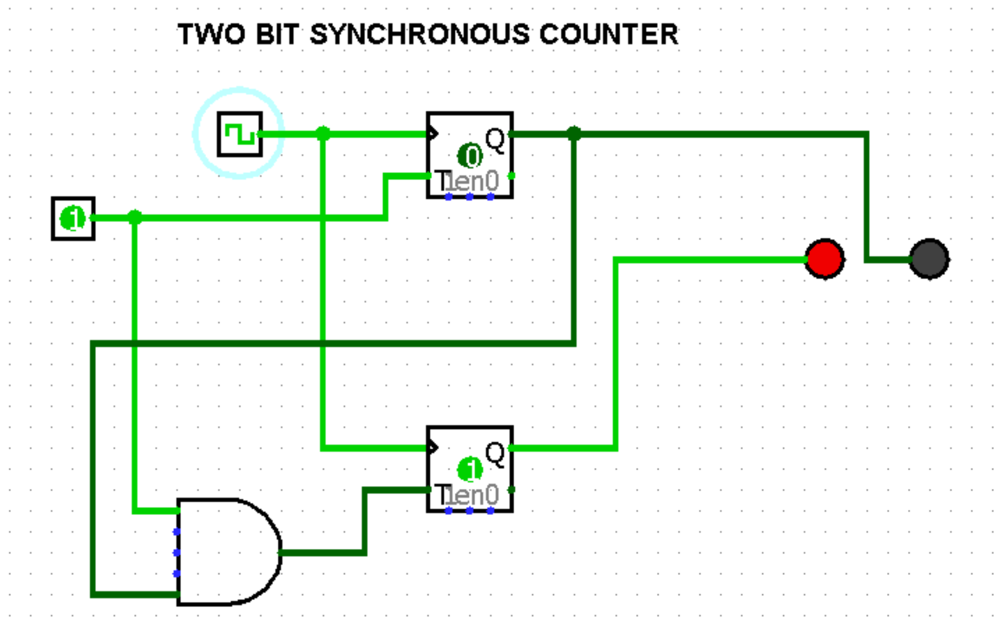
Aim: Realization of Boolean Expression/ MUX & Demux using Gates



Aim : To design and simulate various counters

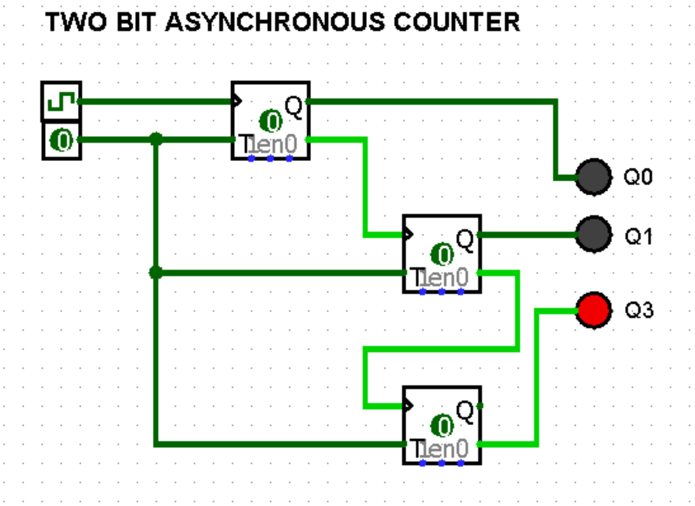
1.

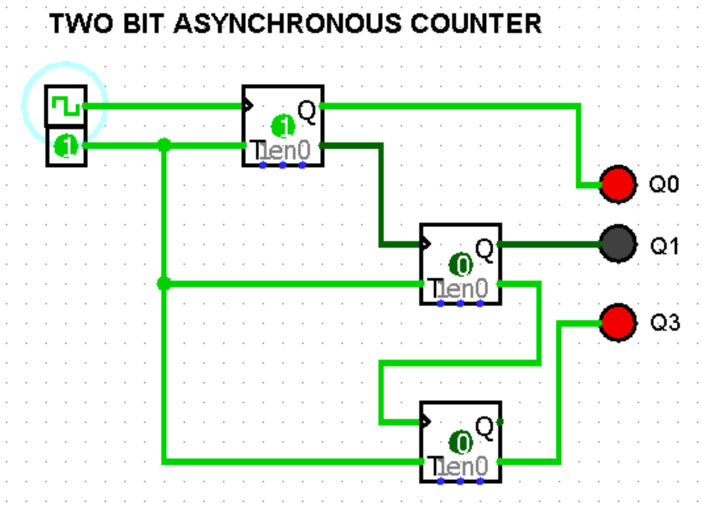


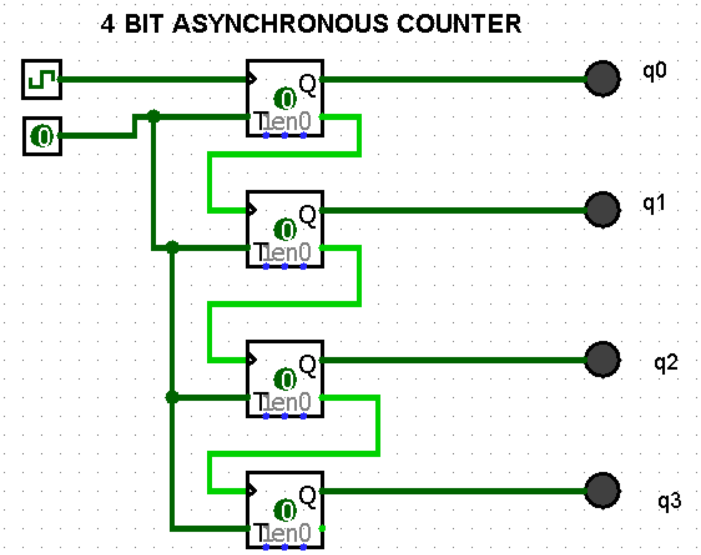


Aim : To design and simulate various counters

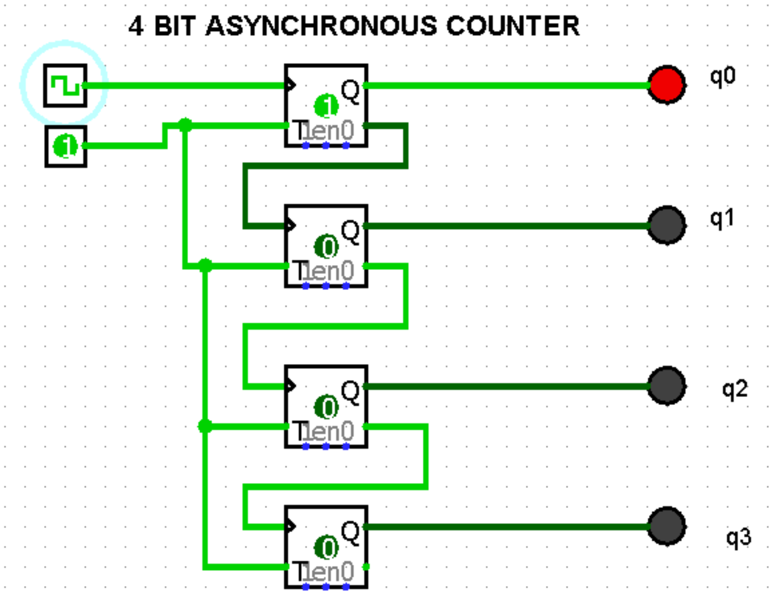
2.



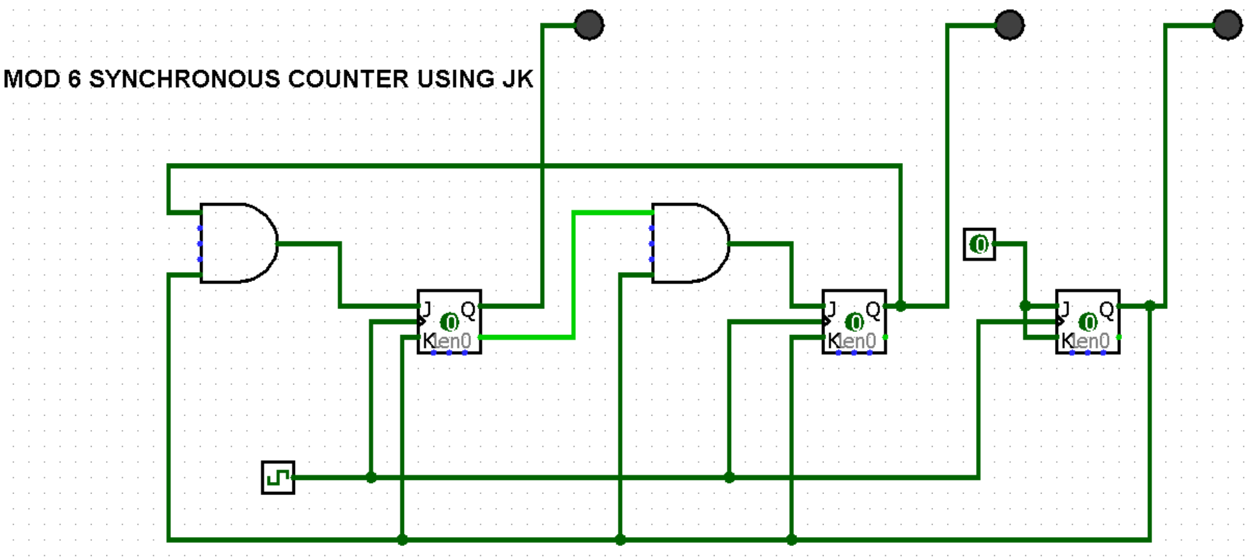




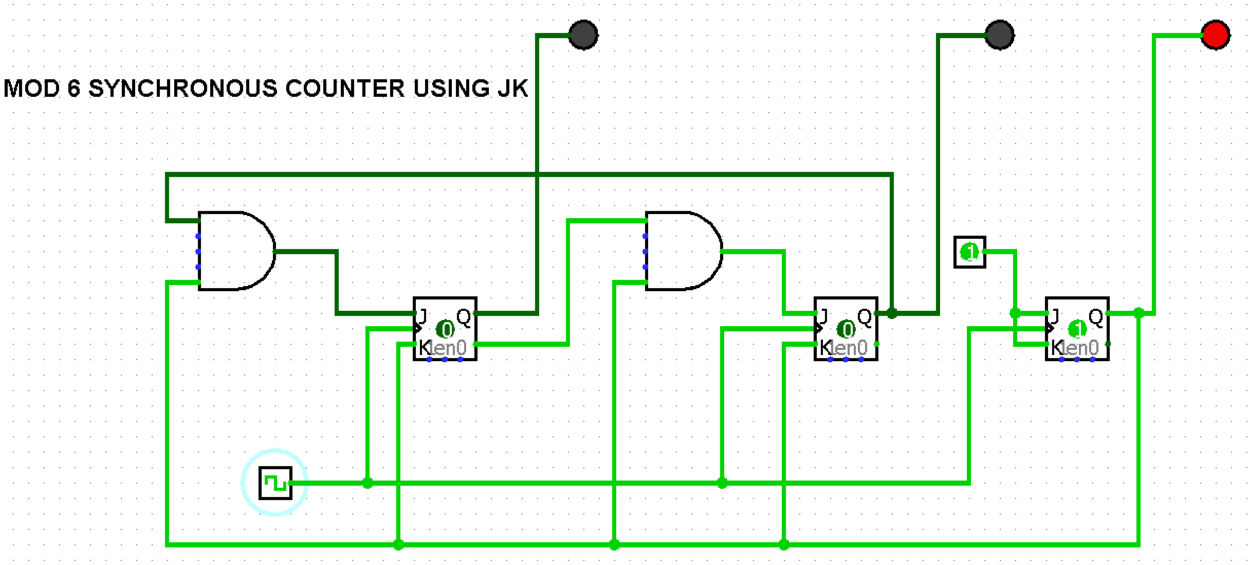
Aim : To design and simulate various counters



3.

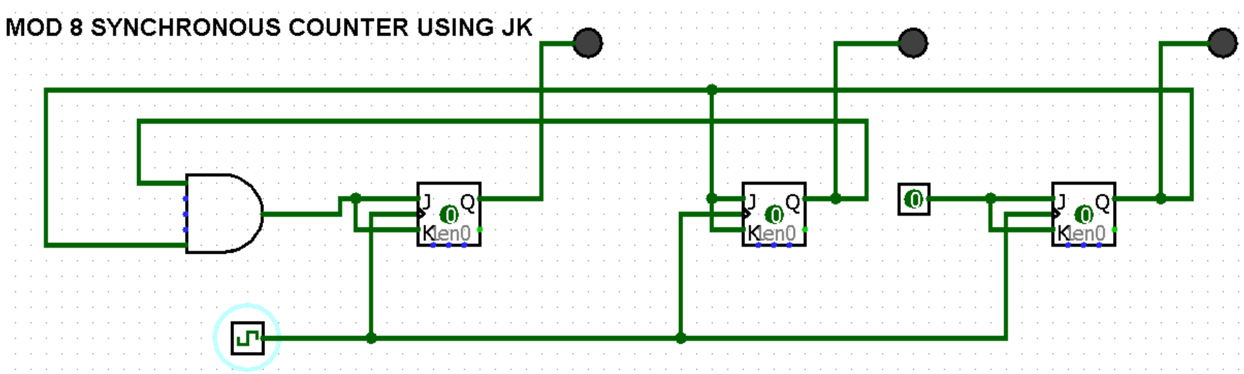


Aim : To design and simulate various counters

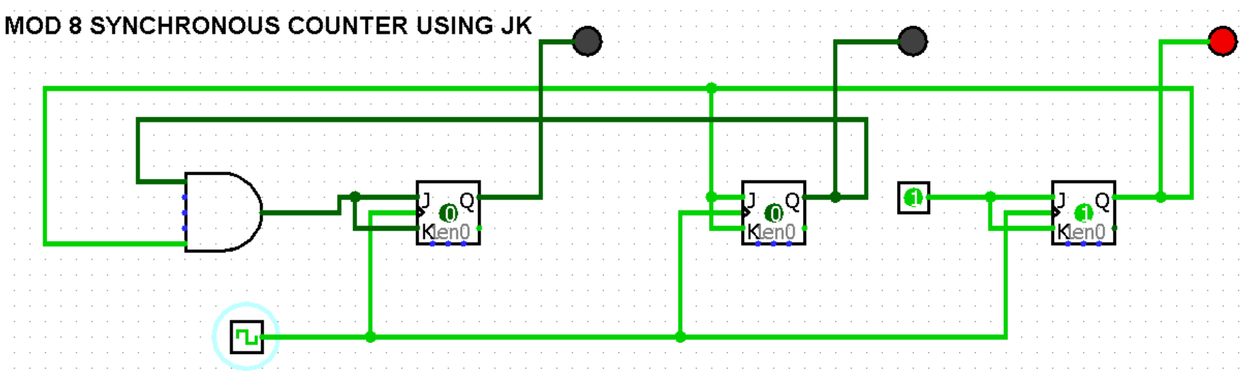


MOD 6 SYNCHRONOUS COUNTER USING JK

4.



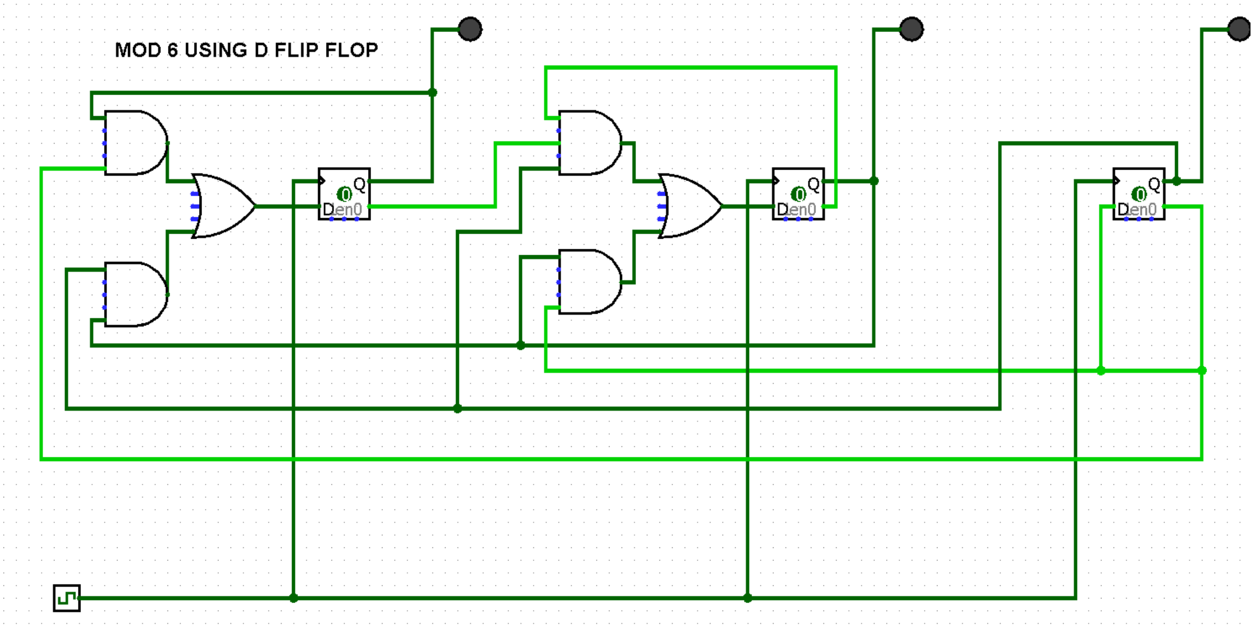
MOD 8 SYNCHRONOUS COUNTER USING JK

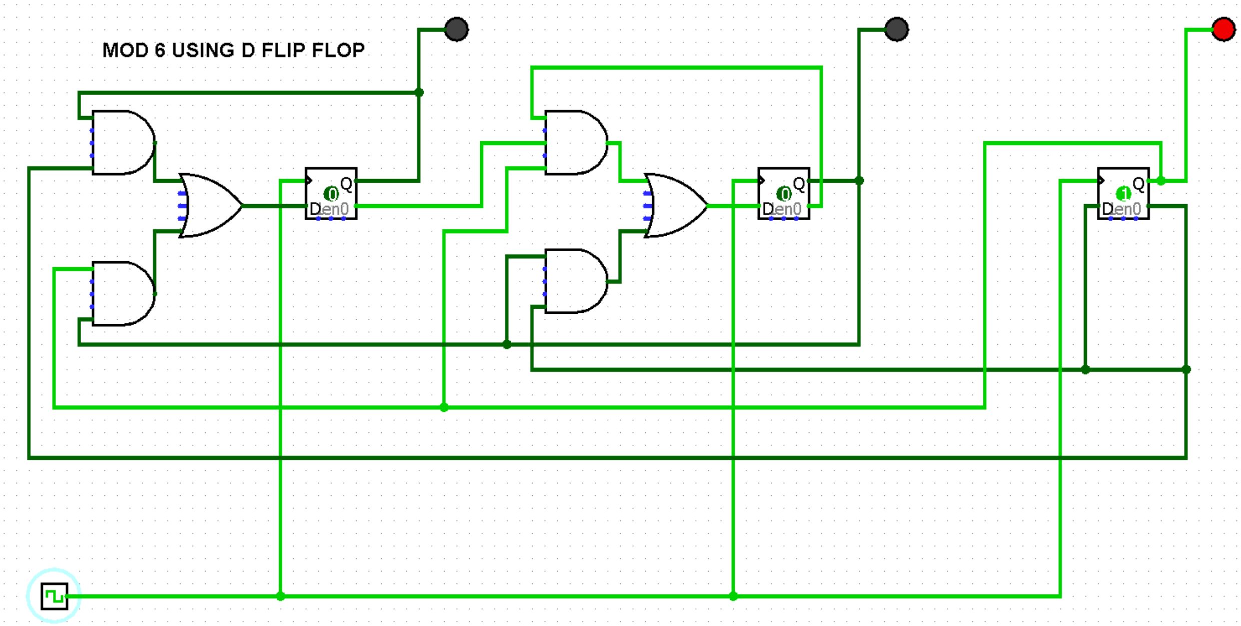


MOD 8 SYNCHRONOUS COUNTER USING JK

Aim : To design and simulate various counters

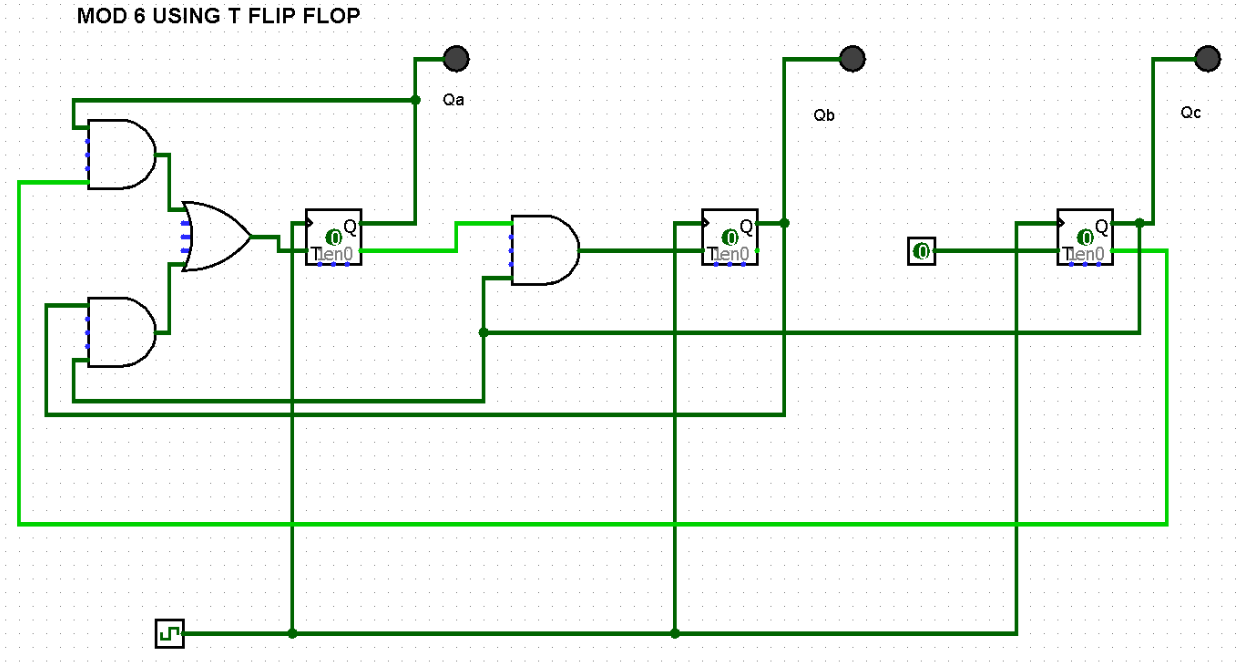
5.

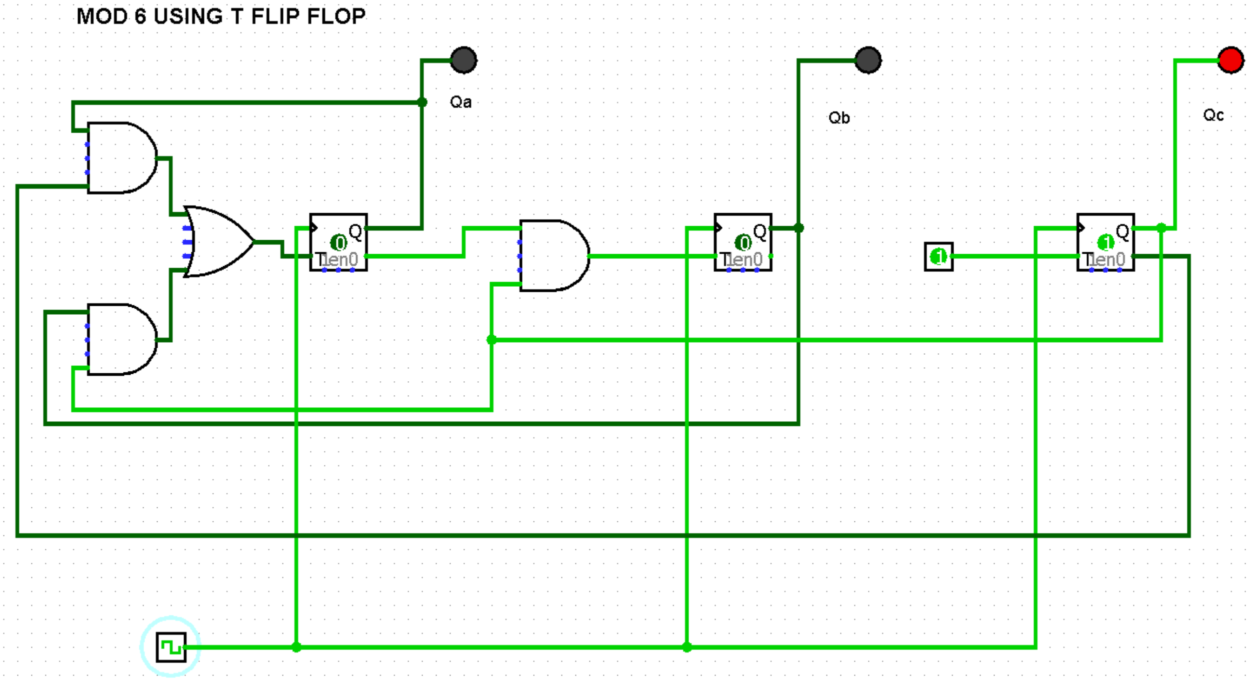




Aim : To design and simulate various counters

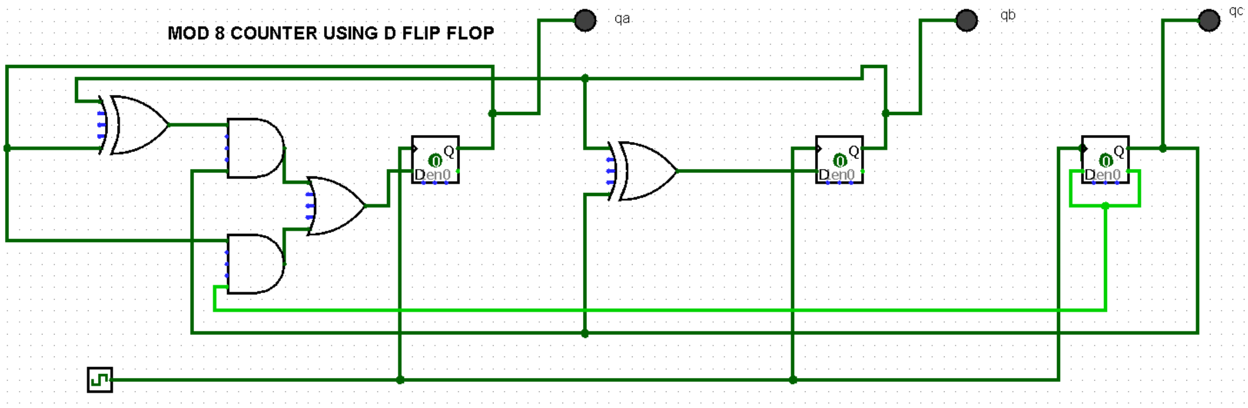
6.

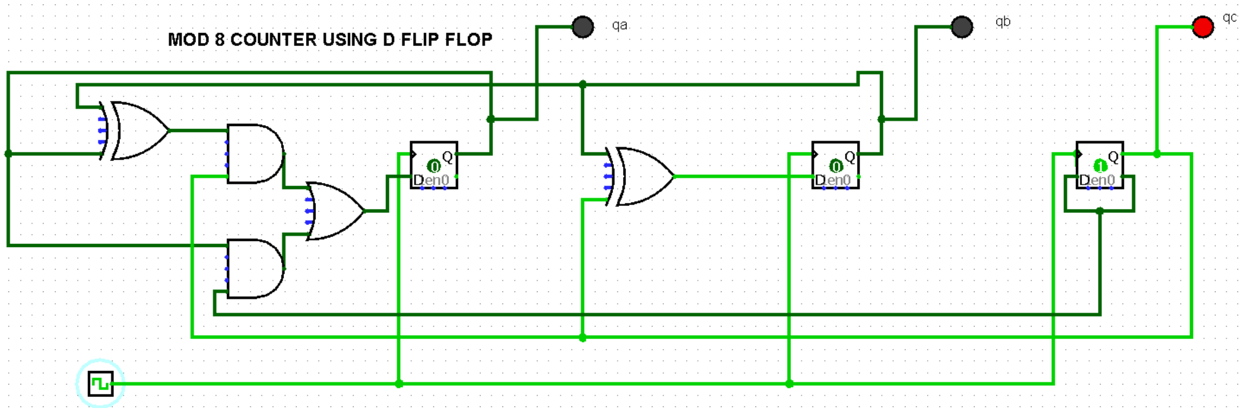




Aim : To design and simulate various counters

7.


MOD 8 COUNTER USING D FLIP FLOP
qa
qb
qc
0
Q
D en 0
0
Q
D en 0
0
Q
D en 0


MOD 8 COUNTER USING D FLIP FLOP
qa
qb
qc
0
Q
D en 0
0
Q
D en 0
1
Q
D en 0