**Non linear applications:- a) Astable Multivibrator b) Mono stable Multivibrator.**

**Astable Multivibrator**

**Aim:**

To design an astable multivibrator for a given frequency and duty cycle using NE555 timer.

**Components & Apparatus Required:**

NE555 Timer, Diode (IN4007) Resistors, Capacitors, power supply & CRO.

**Theory:**

A **multivibrator** is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. It is characterized by two amplifying devices (transistors, electron tubes or other devices) cross-coupled by resistors and capacitors. The most common form is the astable or oscillating type, which generates a square wave—the high level of harmonics in its output is what gives the multivibrator its common name.

There are three types of multivibrator circuit:

* **As table**, in which the circuit is not stable in either state—it continuously oscillates from one state to the other.
* **Monostable**, in which one of the states is stable, but the other is not—the circuit will flip into the unstable state for a determined period, but will eventually return to the stable state. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a **one shot**. A common application is in eliminating switch bounce.
* **Bistable**, in which the circuit will remain in either state indefinitely. The circuit can be flipped from one state to the other by an external event or trigger. Such a circuit is important as the fundamental building block of a register or memory device. This circuit is also known as a flip-flop.

**Design:**

Given frequency (f) = 1 KHz and duty cycle = 60% (=0.6)

The time period T =1/f = 1ms = tH + tL

Where tH is the time the output is high and tL is the time the output is low.

From the theory of astable multivibrator using 555 Timer, we have

tL= 0.693 RB C ------(1)

tH= 0.693 (RA + RB)C ------(2)

T = tH + tL  = 0.693 (RA +2 RB) C

Duty cycle = tH / T = 0.6.

Hence tH = 0.6T = 0.6ms and tL = T – tH = 0.4ms.

Let C=0.1μF and substituting in the above equations,

RB = 5.8KΩ (from equation 1) and RA = 2.9KΩ (from equation 2 & RB values).

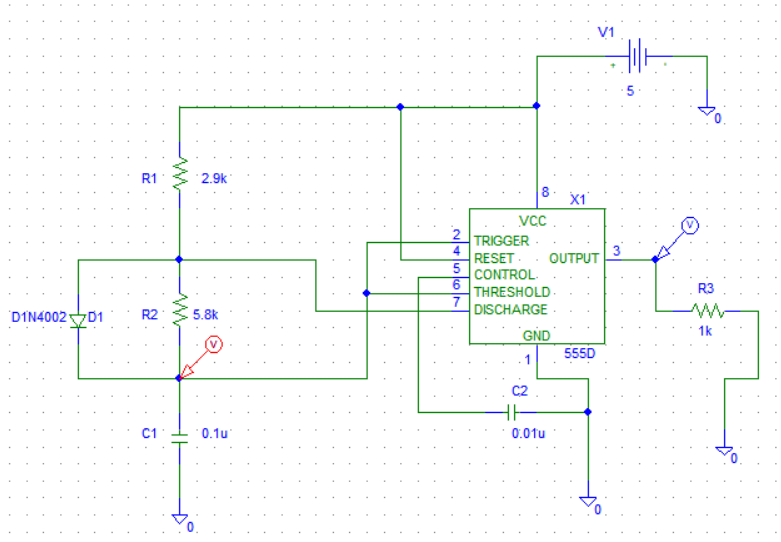
The Vcc determines the upper and lower threshold voltages (observed from the capacitor voltage waveform) as VUT = 2/3VCC  and VLT = 1/3 VCC

Note: The duty cycle determined by RA & RB can vary only between 50 & 100%. If RA is much smaller than RB, the duty cycle approaches 50%.

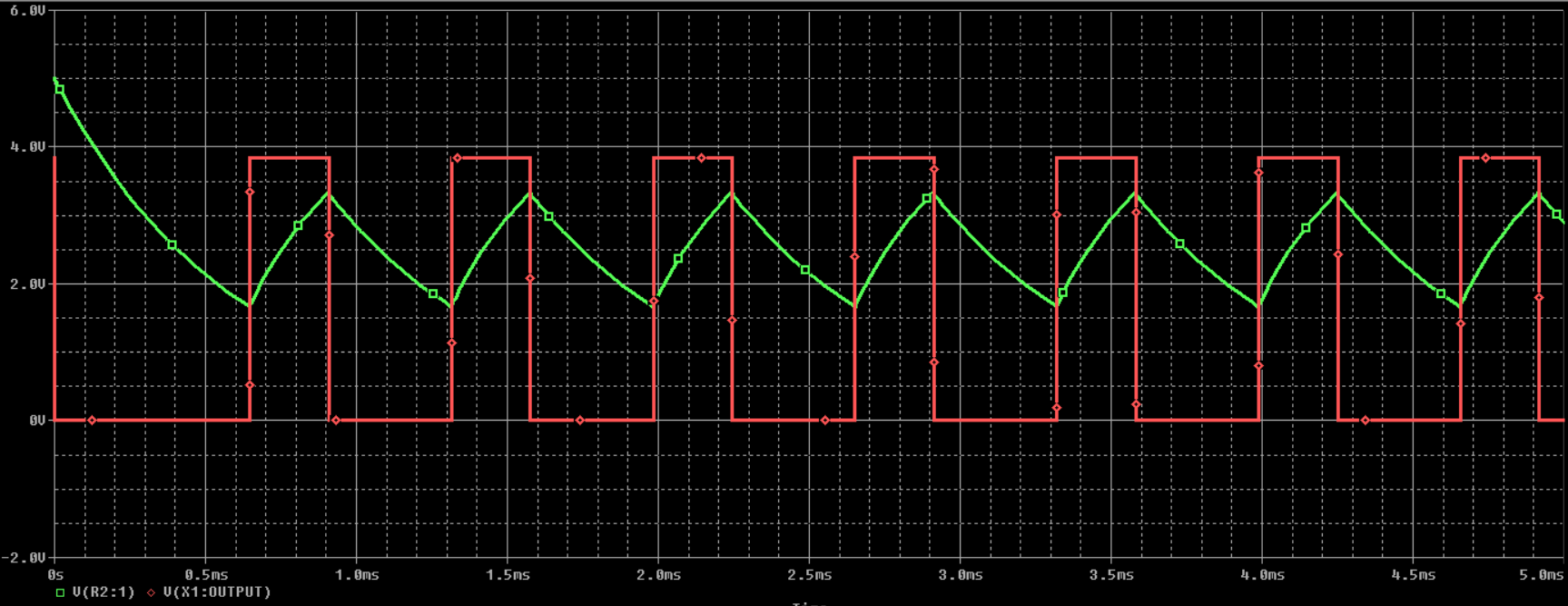
**Procedure for Circuit Connection:**

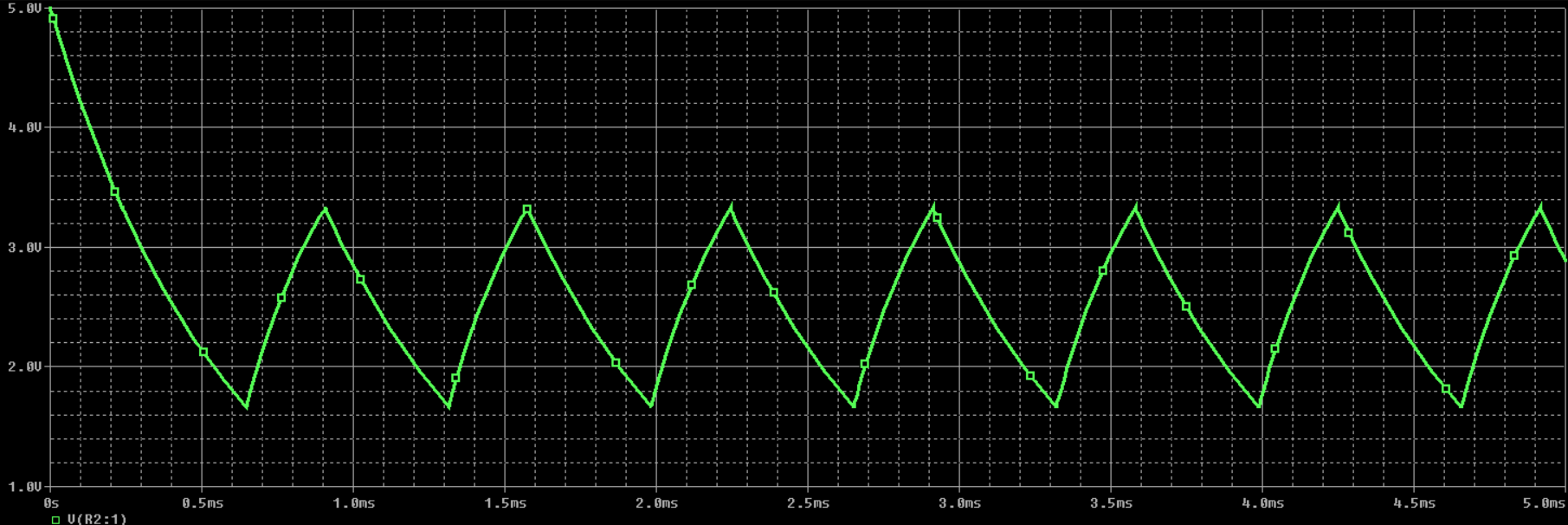
1. Rig up the circuit as shown in the circuit diagram.
2. Give a supply voltage of +5V.
3. Observe the capacitor voltage waveform at 6th pin of 555 timers on CRO.
4. Observe the output waveform at 3rd pin of 555 timers on CRO (shown below).
5. Note down the amplitude levels, time period and hence calculate duty cycle.
6. Draw output waveform & the corresponding capacitor voltage waveform.

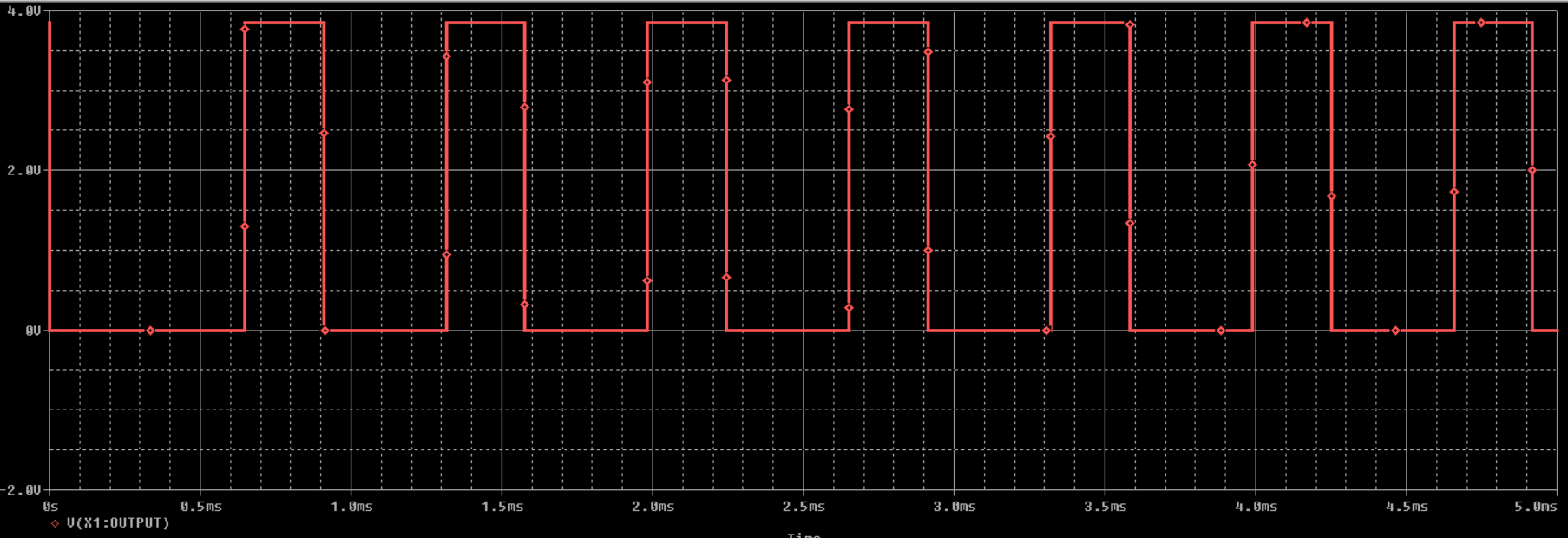
**Circuit diagram:**



**Graph:**







**Monostable multivibrator**

**Aim:**

To design a Monostable multivibrator for a given frequency using NE555 timer.

**Components & Apparatus Required:**

NE555 timer, Resistors, Capacitors, Power supply, and pulse generator.

**Theory:**

In the Monostable mode, the 555 timer acts as a “one-shot” pulse generator. The pulse begins when the 555 timer receives a trigger signal. The width of the pulse is determined by the time constant of an RC network, which consists of a capacitor (C) and a resistor (R). The pulse ends when the charge on the C equals 2/3 of the supply voltage. The pulse width can be lengthened or shortened to the need of the specific application by adjusting the values of R and C.

The pulse width of time t is given by

T= RC \* ln (3) ==1.1 RC

This is the time it takes to charge C to 2/3 of the supply voltage.

**Procedure for Circuit Connection:**

1. Rig up the circuit as shown in the circuit diagram.
2. Give a supply voltage of +5V.
3. Observe the capacitor voltage waveform at 6th pin of 555 timer on CRO.
4. Observe the output waveform at 3rd pin of 555 timer on CRO (shown below).
5. Note down the amplitude levels, time period and hence calculate duty cycle.
6. Draw output waveform & the corresponding capacitor voltage waveform.

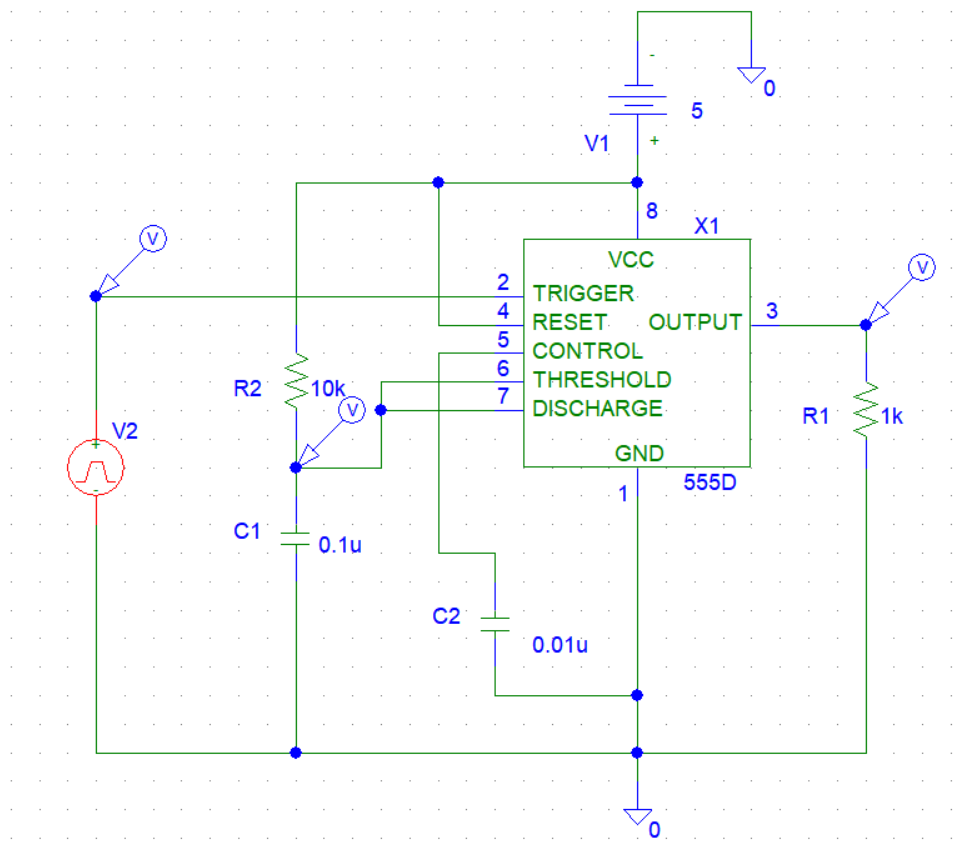
**Design:**

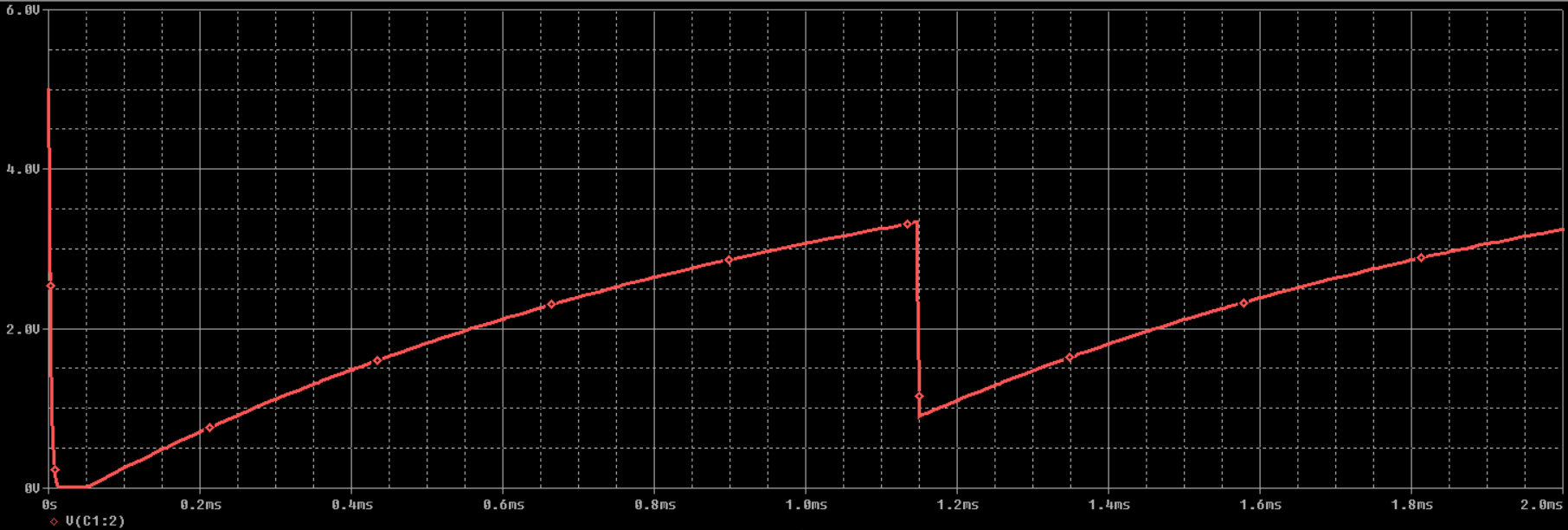
Pulse Width (tp) =1.1 RC

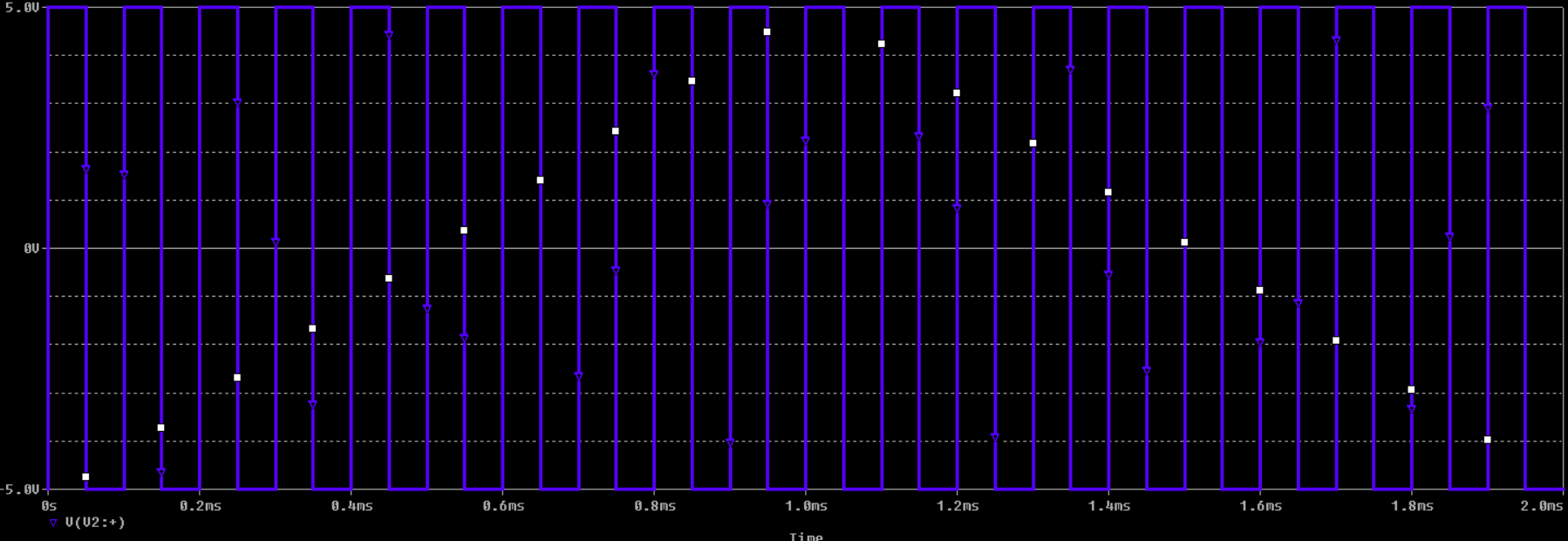
Let tp = 1ms, C = 0.1uF

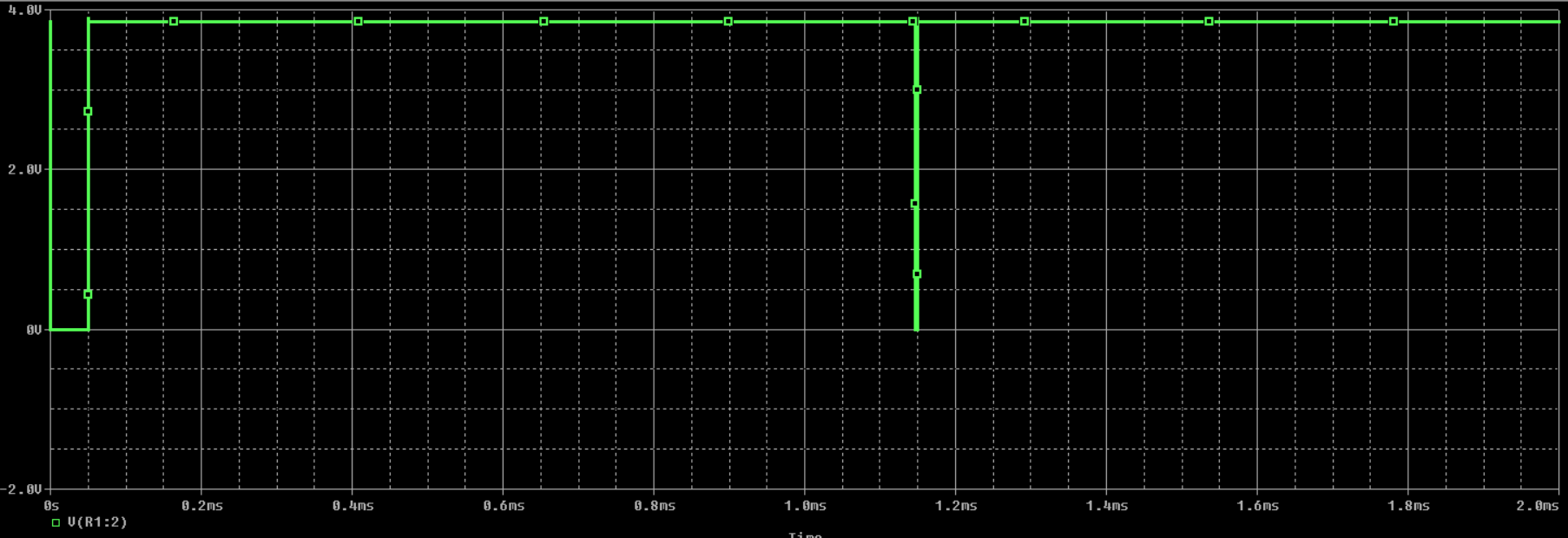
R = tp / 1.1C = 10 KΩ

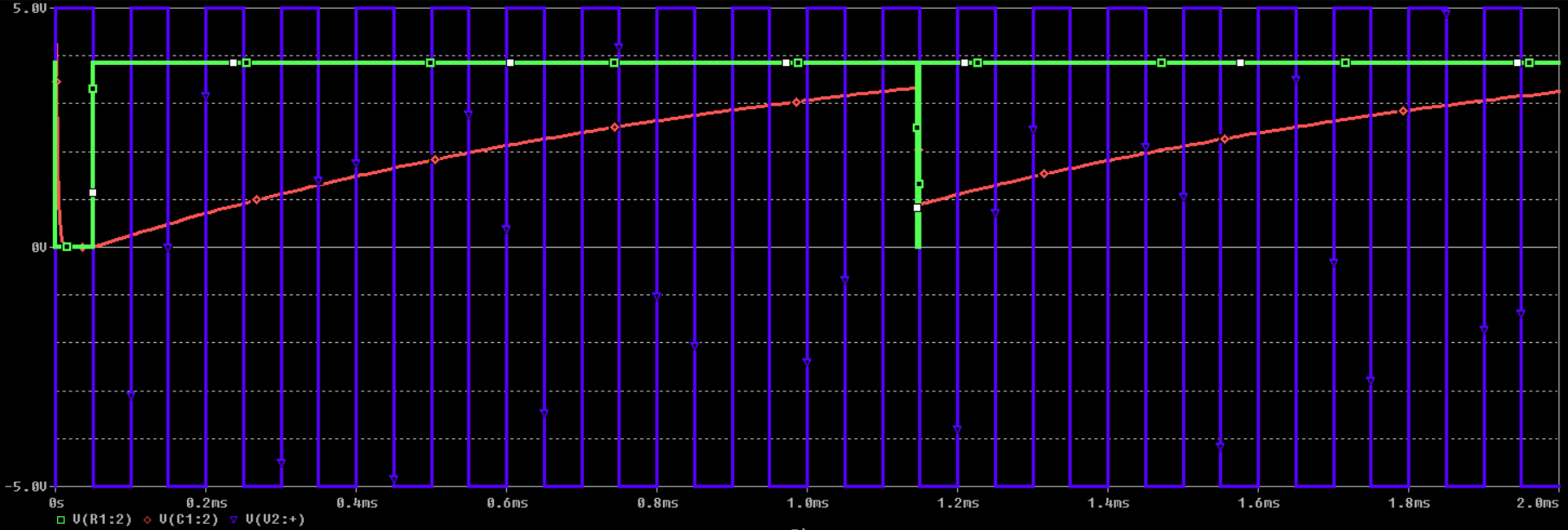
**Circuit Diagram:**

****

**Graphs:**

****

****

****

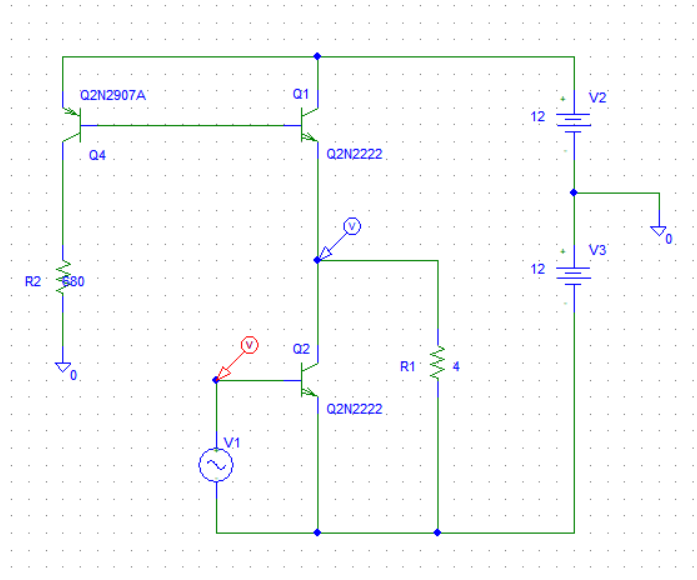
**Class A Power Amplifier**

**Aim:** To design a Common Emitter with Active Load, Class A Power Amplifier using BJT.

**Components Required:**

Q2N2907A PNP transistor, Q2N2222 NPN transistor, Resistors, Sinusoidal input, DC Voltage Source.

**Circuit:**

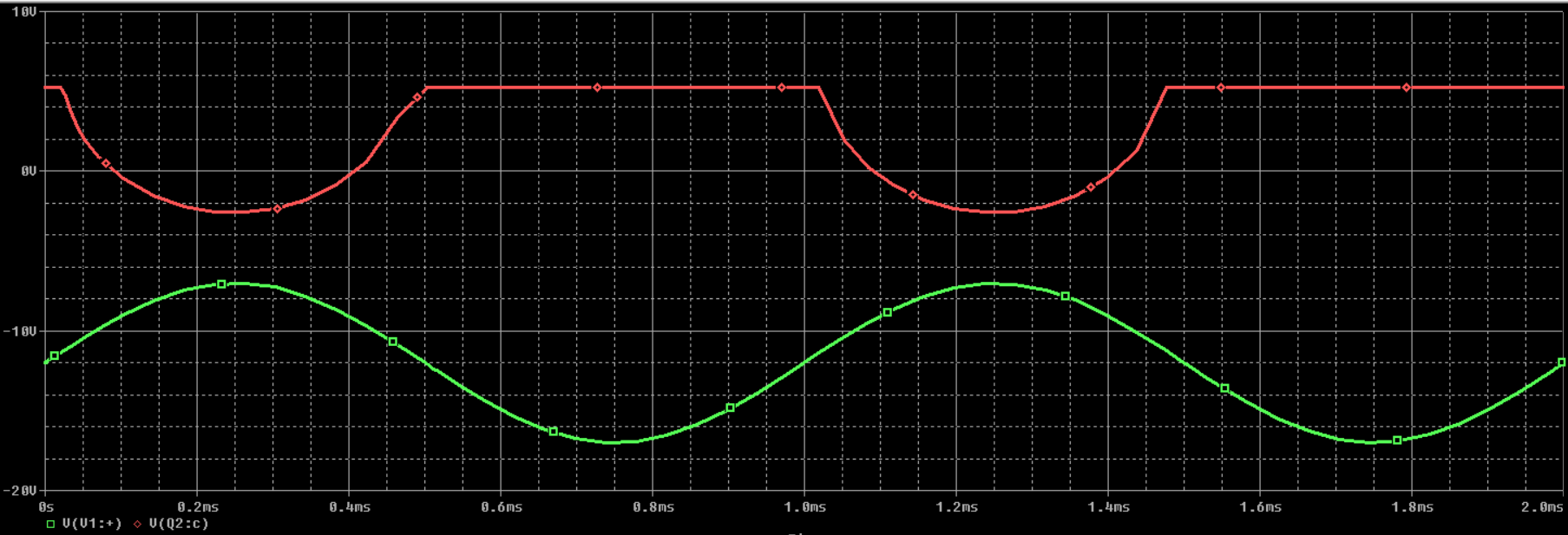
****

**Theory:**

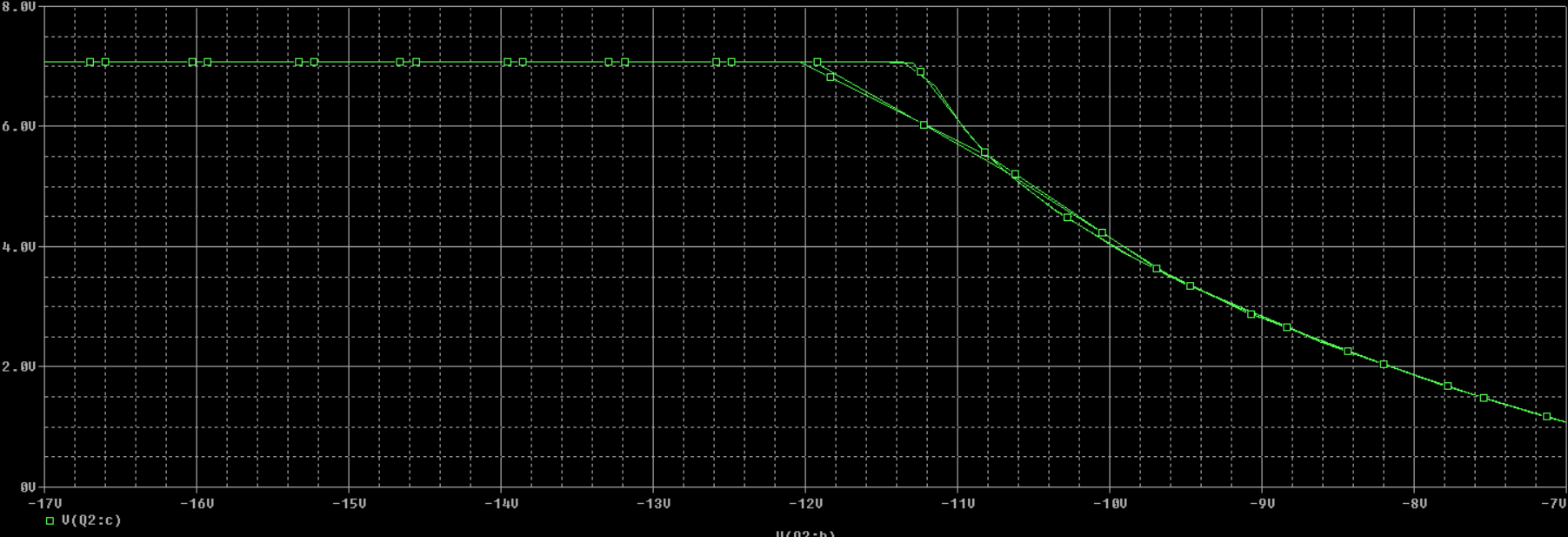
Power amplifiers are electronic circuits which are used to amplify the power of the input signal, so that it is capable of driving the load.

Class A power amplifiers is one such type whose angle of conduction is 3600, has an efficiency of 25 to 50%. This type of amplifier is considered to be the best class of amplifier due to their excellent linearity, high gain and low signal distortion levels. It finds its applications in high-fidelity audio amplifier designs. The duty cycle is 100% or 1.

**Graph:**

****

**Transfer Characteristics:**

****

**Procedure:**

1. Make the circuit connections as shown in the diagram.
2. Proceed for the simulation, observe the input and output waveforms.
3. Plot the transfer characteristics.

**Design:**

Given, RL = 4 Ω, β = 100, VCC = 12 V, VCE(Sat) = 0.7 V, PL(Max) = 10 W.

1. VCC = , VCE(Max) 2VCC or 24 V
2. Fm (Figure of Merit) = , PC(Max) 20 W
3. IC = = 1.67 A
4. IC(Max) = 2Ic = 3.33 A
5. IB = = 16.7 mA
6. RB = = 680 Ω

**Sample and Hold Circuit**

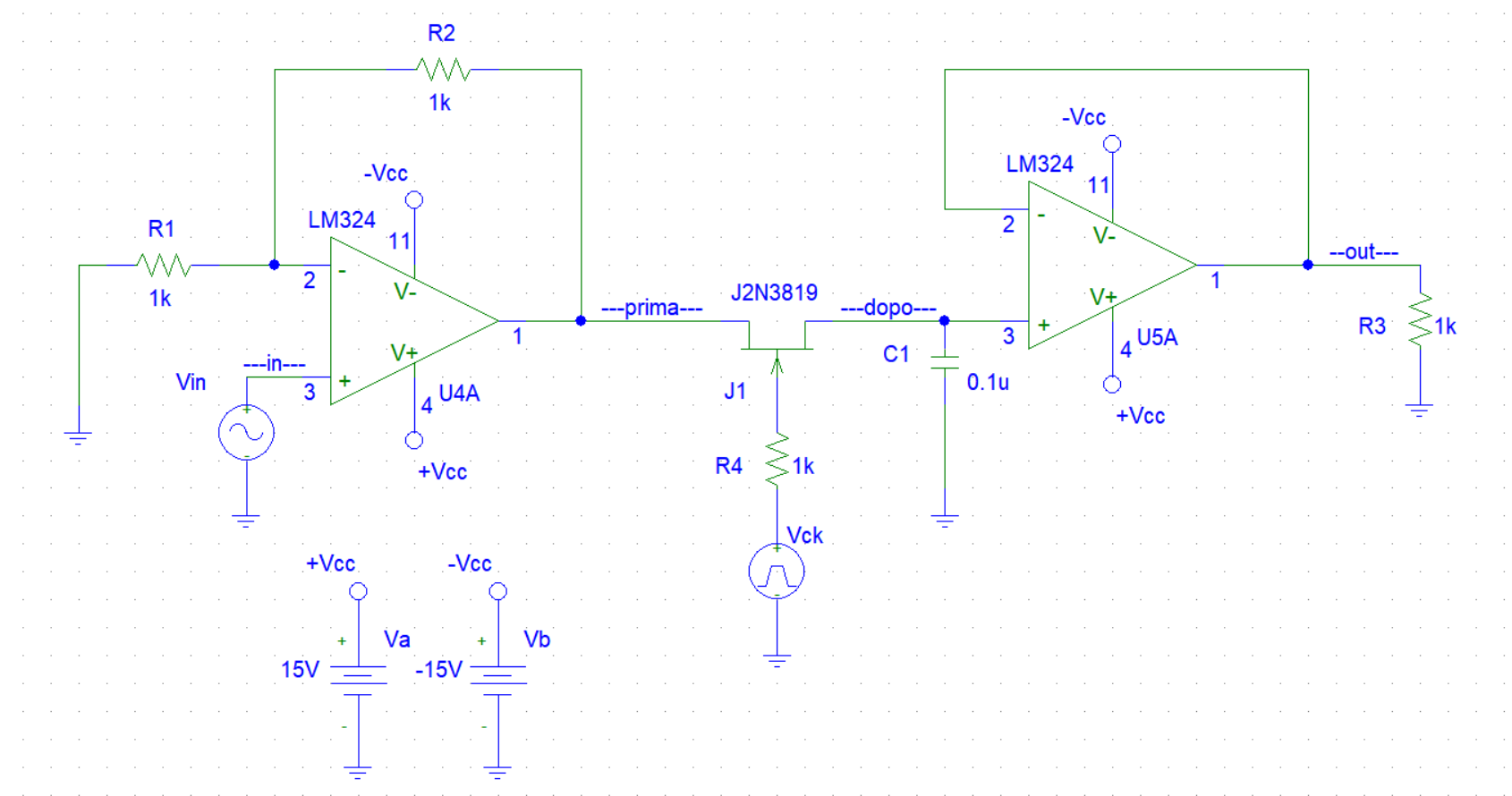
**Aim:** To design a Sample and hold circuit and simulate it. (Signal sampling by JFET)

**Theory:**

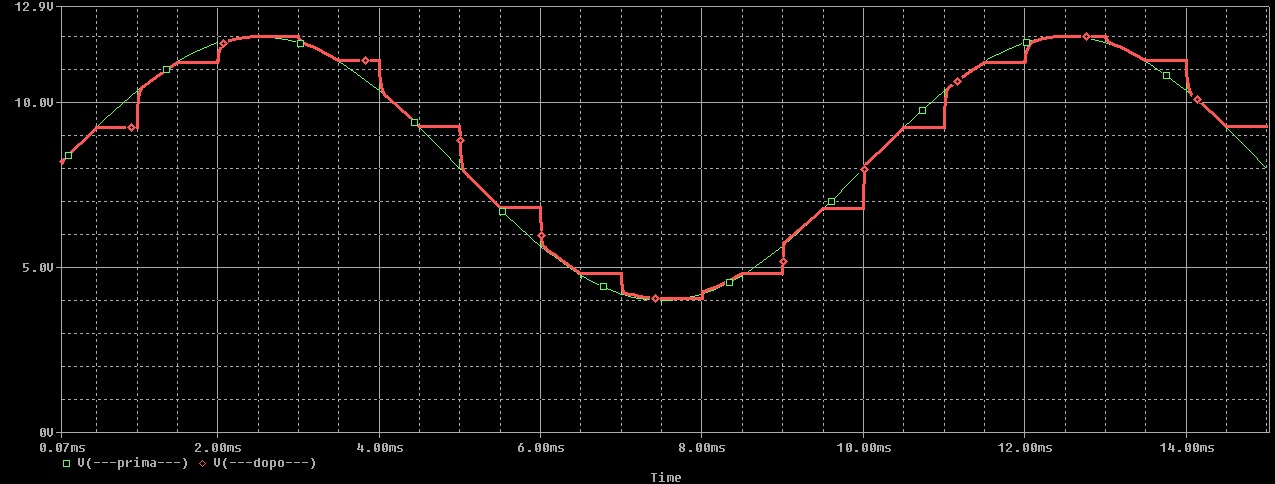
A circuit that is capable of sampling the input signal applied to its terminal as well as holding the sampled value up to the last sample for a particular time interval is known as sample and hold circuit. It basically utilizes an analog switch and a capacitor to perform the task.

The circuit samples the input signal in the time interval between 1 to 10 microseconds. Along with that holds the sampled value until another sampling command is provided to it.

**Circuit:**



**Graph:**



**Natural Sampling Circuit**

**Aim:**

To construct and simulate a natural sampling circuit

**Theory:**

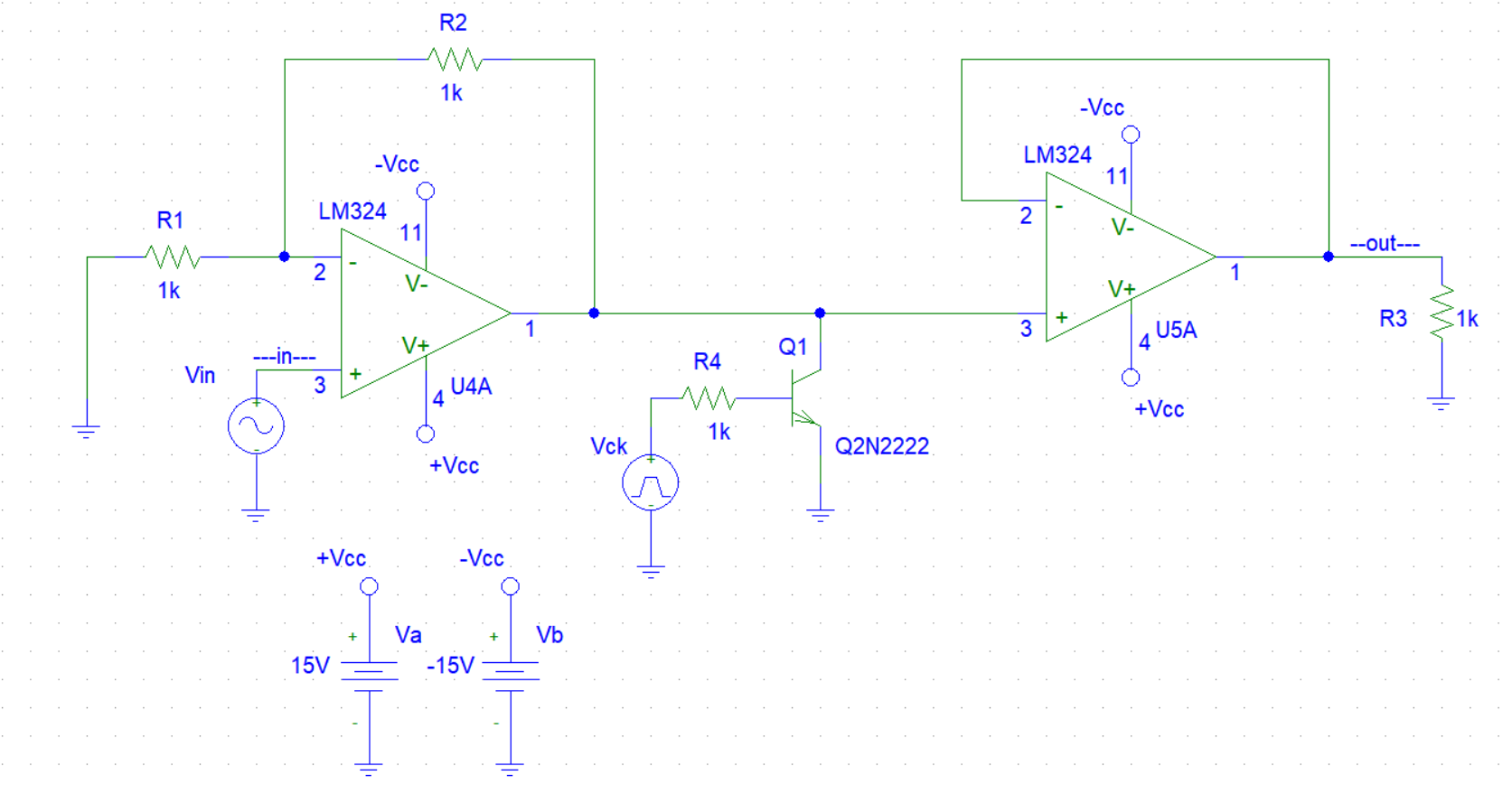
Natural Sampling is a practical method of sampling in which pulse have finite width equal to τ. Sampling is done in accordance with the carrier signal which is digital in nature.

Natural sampling is similar to impulse sampling, except the impulse train is replaced by pulse train of period T.

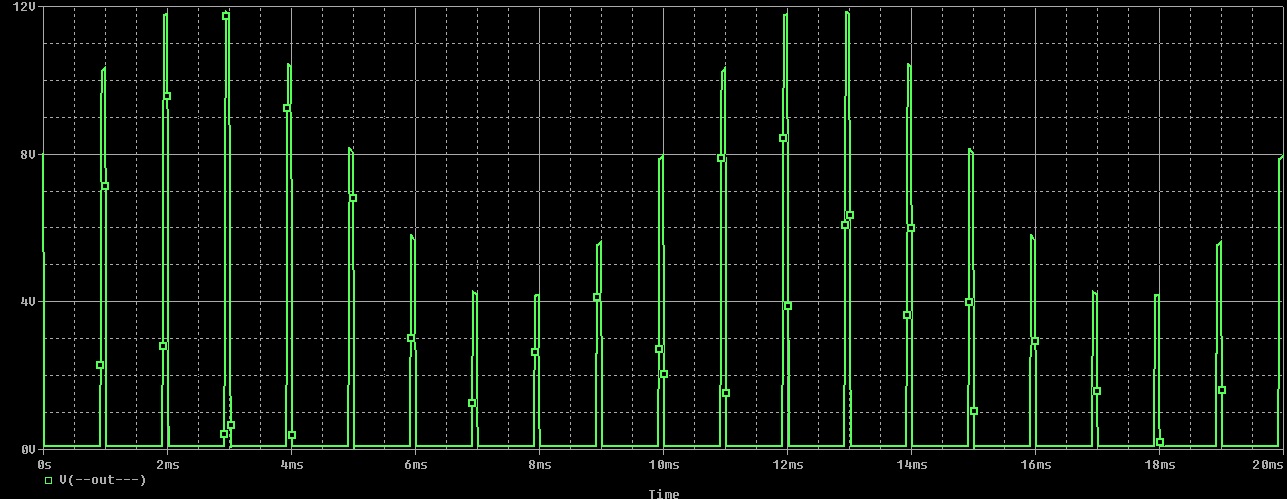
The output of sampler is:

y(t)=x(t)×pulse train

**Circuit:**



**Graph:**



**Hartley oscillator**

**Aim:** To construct a Hartley oscillator circuit and simulating it

**Theory:**

**Hartley Oscillator** is a type of harmonic [oscillator](https://www.electrical4u.com/what-is-an-oscillator/) which was invented by Ralph Hartley in 1915.

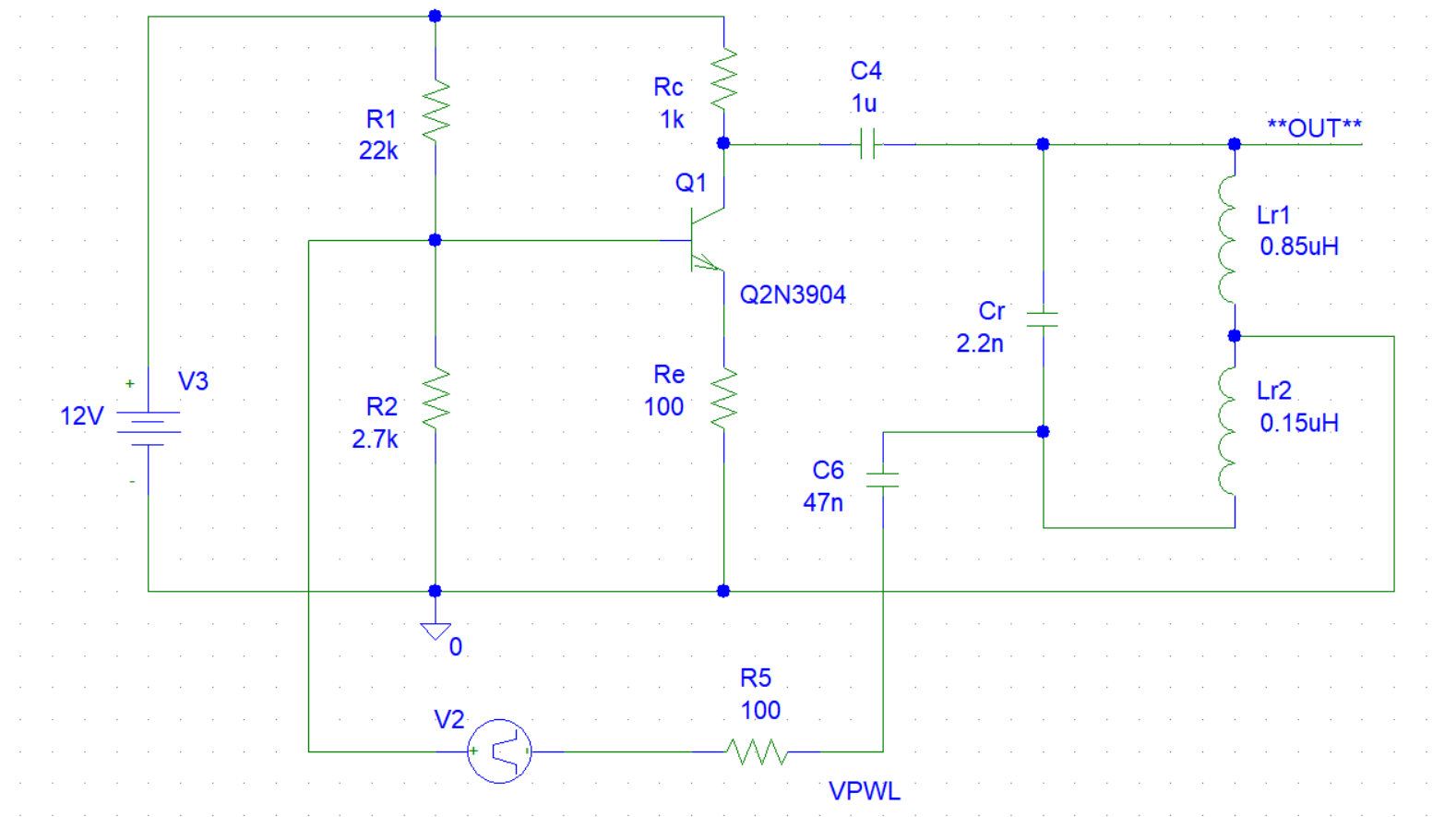
These are the Tuned Circuit Oscillators which are used to produce the waves in the range of radio frequency and hence are also referred to as RF Oscillators. Its frequency of oscillation is decided by its tank circuit which has a [capacitor](https://www.electrical4u.com/working-principle-of-a-capacitor/) connected in parallel with the two serially connected [inductors](https://www.electrical4u.com/what-is-inductor-and-inductance-theory-of-inductor/)

**Design:**

The oscillation frequency is given by:  
[](http://www.codecogs.com/eqnedit.php?latex=f_%7br%7d=\frac%7b1%7d%7b2\pi%20\sqrt%7bC_%7br%7d(L_%7br1%7d@plus;L%7b_%7br2%7d%5e%7b%7d%7d)%7d%7d)  
Taking the values Cr=2.2nF, Lr1=850nH, Lr2=150nH

The result is: fr=3.39MHz.

**Circuit:**



**Graph:**

