Inspiring Excellence

Project Title: "Digital Date and Time System"

Course Title: Digital Logic Design
Course Code: CSE260
Lab Section: 09
Semester: Fall-2021
Lab Instructors: Ramkrishna Saha Sir & Modhumonty Das Miss

Group Number: 07

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Introduction:

“Digital date and Time system” which is also known as the automated digital clock is one of the most popular systems nowadays. From the wristwatches we wear to the massive street clocks, we are all reliant on the information they provide. In the twenty-first century, we can't argue that time is money; rather, time is more valuable than money. As a result, our habits of checking the time every minute are significantly expanding. About 99 percent of today's digital clocks use microcontrollers, making them more user-friendly than the competition. We can set the time to begin at whatever minute or second we wish. Digital clocks are extremely helpful tools in our daily lives. As a result of this shift, the need for precise and simple materials is skyrocketing. The system that is anticipated to be built consists of a 14 digit clock including hours, minutes, seconds, days, months, and years using IC-74192 and DCLOCK.

Proposed Model:

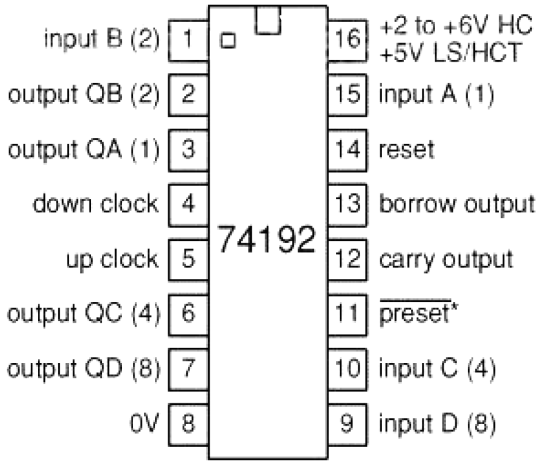
We created a digital clock with a 24-hour countdown in this project. The clock runs from 00:00:00 to 23:59:59, after which the system increases the day until it reaches 31 days, then the month, and finally the year (2020-2029). In addition, the 30-day case, leap year, and non-leap year cases are also monitored. This clock has 14 SEVEN-SEG displays, two for seconds, two for minutes, two for hours, two for days, two for months, and four for years. In this clock, we can set the time manually.

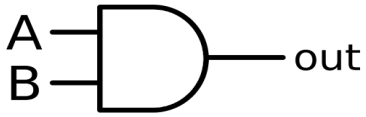
Experimental Setup:

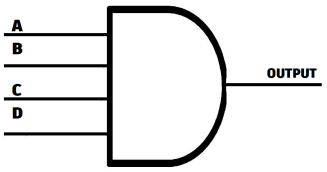
Component Used:

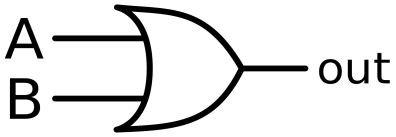
- 7SEG-BCD-GRN
- 7408
- IC-74192
- LED-BIBY
- SW-SPDT
- POWER
- GROUND
- DCLOCK
- WIRE
- Logic State
- NOT Gate
- AND Gate
- OR Gate

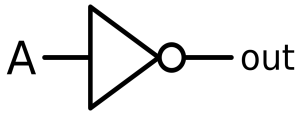
Circuit Diagram:

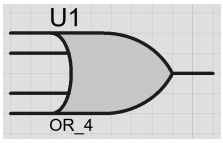


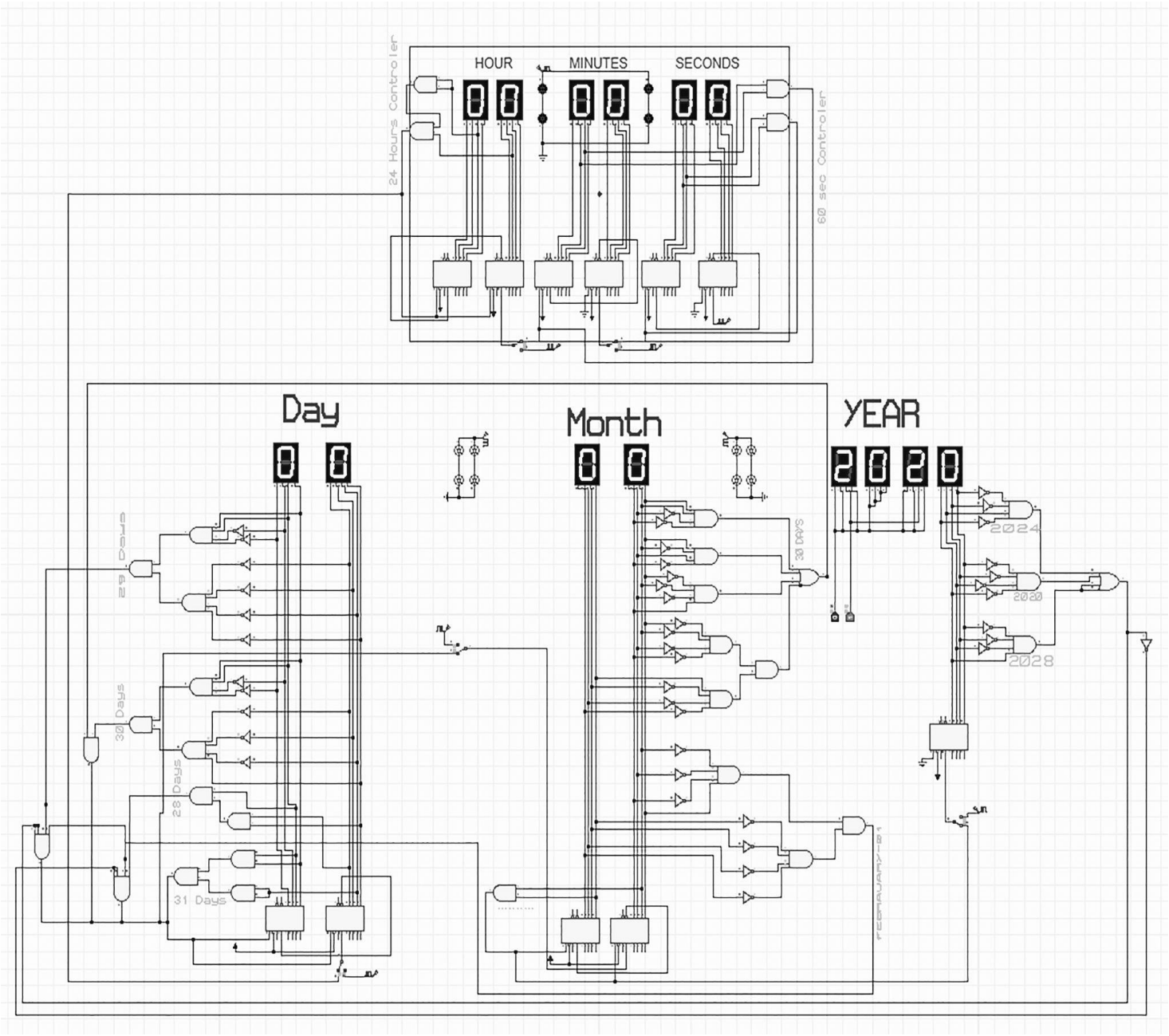












Description:

For Digital Time System:

Some components that are commonly used in logic circuits were employed to develop the digital clock system. To begin, we displayed the digits of our clock on six 7-segment BCD displays. Then, in tandem with those six screens, we constructed six presentable synchronous BCD decade up/down counters (IC 74192). Furthermore, we utilized counters since they may be preloaded with a particular number, count up and down, emit carry and borrow indications, and be rebooted to zero. As a result, we had to employ counters for this project. The clock is made up of three components that compute hours, minutes, and seconds. All of the counters' flip flop outputs are linked to the BCD display inputs in each area, and asynchronous parallel load inputs are added to the power. The rightmost counter's count-up clock pulse input has been coupled with an electronic clock generator, which is a form of a low-high-low clock, in the "seconds" section. It's utilized to generate a pulse every second, which is shown on the rightmost display. After 9 up counts, the terminal count up output creates carry, which is transferred to the following counter's clock pulse input(up) and changes its digit at the same time. Because the "seconds" portion must be reset every fifty-nine seconds, one AND gate (IC 7408) is employed to do this. The AND gate's output is linked to the master reset input of the leftmost counter, which resets this section's counting every time the display displays fifty-nine. The "minutes" part uses all of the logic that has been discussed so far. In these two portions, two AND gates are employed in addition. However, the AND gate's output is also linked to the up clock pulse input of the "minutes" rightmost counter, thus one value of the minute is incremented every fifty-nine seconds. For the same logic stated in the "hours" section, its output is also connected to the rightmost counter's up clock pulse input. Because this clock is based on the 24-hour clock, two AND gates are utilized. In this part, these two AND gates are connected to two counters' specific outputs in such a manner that they generate a larger voltage after every twenty-four-digit shown in the display (one). As a result, this output is linked to the master reset input of the two counters, and the clock is reset after twenty-four hours. Finally, two switches and two D-lock generators are connected to the counters of the "hours" and "minutes" sections, respectively, so that the values of these two sections may be manually changed when necessary.

For Digital Date System:

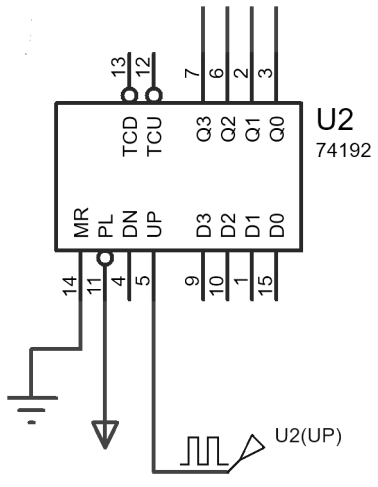
In the other section, the same logic circuits are being used to develop a digital calendar related to the digital clock system. Here, in this case, we have used eight 7-segment BCD displays. Then, along with those eight screens, we constructed five presentable synchronous BCD decade up/down counters (IC 74192). This subproject can display days, months, and years while being connected with the digital clock. Mostly the same way we have approached to create this project where we utilized counters since they may be preloaded with a particular number, count up and down, emit carry and borrow indications, and be rebooted to zero. In this case, just the days, months, and years are being changed through the counters. Though the logic used is the same, here we handled some exceptions which are, as there are varieties of days in every month of a year. So, for 28,30, and 31 days, we added the corresponding values with the help of AND, OR, and NOT gates so that the months get reset according to their corresponding days. Along with that, there were a few other exceptions that were handled which were leap-years. As we know, in leap years, February has 29 days so for that we added more AND gates in the corresponding leap years which are 2020,2024, and 2028 as we have created the project for 10 years. So, when these years arrive, the days of the month, February, gets a total of 29 days and then get reset on the same logic that we used before. Lastly, three switches and three D-lock generators are connected to the counters of the "days", "months" and “years” sections, respectively, so that the values of these three sections may be manually changed when necessary and there are a total of twelve LEDs for better showcasing of the project.

Result and Analysis:

Truth Table of IC-74192 (UP-DOWN COUNTER):

CPI	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Explanation:



For Digital Time System:

We'll look at how the digital time system or the digital clock works in this section, and we'll utilize the IC-74192 truth table to do it. Let's have a look at how the IC-74192 functions. The four input sections of this IC are D0, D1, D2, and D3, but we haven't used them for this project. The next question is how the IC will generate output. We used the clock pulse (DCLOCK) for this. The clock pulse generates the voltage for a specified frequency. The clock pulse is related to UP (5), as you can see. We didn't connect with the DN(4) since we want to display the time in SEVEN-SEGMENTS like (0,1,2,3,4,5...). If we have linked the clock pulse in DN(4), the time would have started at (9,8,7,6), that's why we didn't connect with the DN (4). Then you can see that we have connected power to the Parallel loader to run the IC, and to its left, we have MR, which stands for master reset, which is connected to the ground. Otherwise, the outputs would not work, and we cannot see any numbers in the SEVEN-SEG display if we do not connect it to the ground. TCU and TCD stand for Terminal Counter Up (TCU) and Terminal Counter Down (TCD), respectively (TCD). They serve as a carry bit in a nutshell. For this project, we only need to work with TCU. Now you can see Q3, Q2, Q1, Q0, which are our outputs, next to them. You'll notice a variety of outputs when the clock pulse generates voltage. The output will flash a red light when you run the proteus file, indicating that the output has a voltage of one. Let's go on to the explanation of the truth table. We've written CPI, which stands for Clock Pulse Input, on the left side of the table, and we already know which four are our outputs. If the clock pulse hasn't started yet, we'll get 0 volts for all outputs at first, which is apparent. For the initial higher voltage of the clock pulse, the D0 output will turn on, while the rest will remain off. We get the value -> 0001 (the decimal value of the binary) if we write it as a binary bit, and it will show 1 on the SEVEN-SEG display. The Q1 output is turned on and the other outputs are turned off for the second higher voltage (value-2) of the clock pulse, and if we write it to its binary bit, we get 0010, which is the decimal value of 2, which will be displayed on the SEVEN-SEG-display. This loop works normally up to the decimal value of 9, but beyond that, all of the outputs are turned off, which implies that for the decimal number of 10, all of the outputs are switched off. The Terminal Counter Up is the cause of this occurrence (TCU). The Terminal Counter Up, or simply the Carry bit, takes the next higher voltage after the 9th clock pulse higher voltage. In conclusion, we learned that the Clock Pulse (DCLOCK) works as an input and that we obtain different values for outputs (Q3, Q2, Q1, Q0), with the exception that when the value 10 is passed, all of the outputs are zero, and we determined the reason for this, which was TCU.

For Digital Date System:

Now, we'll look at how the digital date system or the digital calendar works in this section, and we'll utilize the same IC-74192 truth table to do it. We already know and discussed earlier how the IC-74192 functions. To be precise, the four input sections of this IC are D0, D1, D2, and D3, and we used the clock pulse (DCLOCK) for this just like earlier. The clock pulse generates the voltage for a specified frequency. The clock pulse is related to UP (5), as you can see. We didn't connect with the DN(4) since we want to display the day in SEVEN-SEGMENTS like (0,1,2,3,4,5...). If we have linked the clock pulse in DN(4), the day would have started at (9,8,7,6), that's why we didn't connect with the DN (4). Then you can see that we have connected power to the Parallel loader to run the IC and to its left, And like the previous circuit with the help of clock pulse and Terminal Counter Down (TCD), it will simultaneously go through the whole circuit increase 1 in month and years display respectively following the conditions we have set for that. Despite the fact that the logic is the same, we had to deal with several exceptions because each month of the year has a different number of days. As a result, we used AND, OR, and NOT gates to add the respective values for 28, 30, and 31 days, resetting the months to their corresponding days. There were also a few additional exceptions, such as leap

years, that were taken into account. We added extra AND gates in the appropriate leap years, which are 2020,2024, and 2028, as we have developed the project for ten years. As a result, when these years occur, February will have a total of 29 days and that’s how the whole circuit works.

Conclusion:

The knowledge of the CSE260 course was used to create and implement the project using basic gates and IC. The clock is required to display accurate time in a usual manner. Unfortunately, it does not display time with 100% accuracy, which is the project's fundamental shortcoming due to imperfect frequency. Furthermore, we cannot begin at 1 in the day, month, or year sector in the 7SEG-BCD-GRN display as we must always begin from 0. In the case of months, we showed 0 to 11 as 12 months, but in terms of handling the 28, 29, and 30 days exceptions would be much more difficult if we included days from 0 to 30. As a result, we kept it at 0 to 31 days, which is a flaw in our project. Moreover, the system only can represent 2020 to 2029. So those are the project's constraints. This project was built with very low-cost materials.