

## Peripherals Finals Preparation

Full Form: Inter-Integrated Circuit Bus

- Defn: Small Area Network.

connecting ICs and other electronic components in an embedding system

$I^2C$

Originally intended for operation on single PCB

Data Transfer Speeds

- Classic 100 Kbps

- Fast 400 Kbps

- High Speed 3.4 Mbps

~~Use~~ Advantages

- Reduce Board Space

- Reduce Cost

- ICs use less pins and smaller packages

- Reduces Interconnect Complexity.

### Characteristics

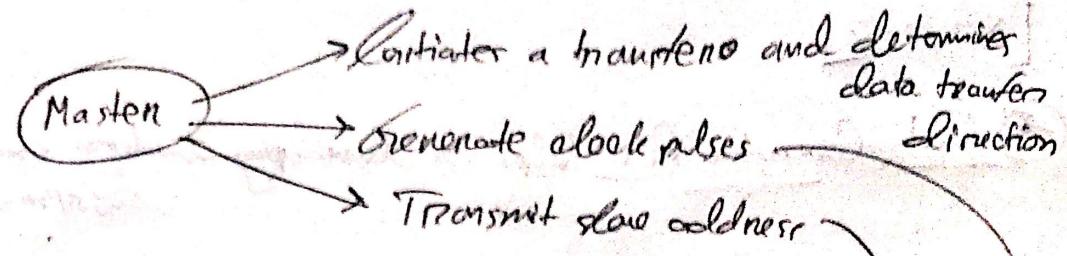
• (Electrical + Timing) Specifications  
Associated + Bus Protocol

• 2 wire → Serial Data (SDA)  
→ Serial Clock (SCL)

[For reliable comm. a third wire,  
common ground is used]

- Unique start and stop condition
- Slave selection protocol [7 bit slave address]
- Bi-directional data transfer
- Acknowledgement after each transfer.
- True Multi-Master Capability
- No fixed length transfer

— — —



Q: Why does in I<sup>2</sup>C bus

start-stop condition and data

transition signalling are opposite to each other? Timing controlled by clock line

Slave → Responds only when address is called by master

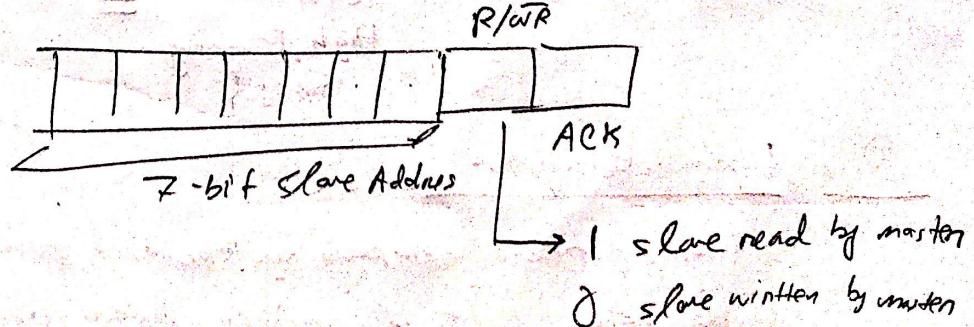
- ① Normal Data Transfer → [Changes state of data line when clock is (Low)]
- ② Start/Stop → [Change state of data line when clock is (HIGH)]

### Addressing

unique 7-bit address or 10 bit

[0000 and 1111] are special addresses

First byte



[Slide-7]

Q1 Computer Rev. helps for developing modern embedded systems.

Q2 Differentiate between Computer System and Embedded System

Q3 What is Embedded system.

Q4 Embedded control system block diagram

Q5 Implications of being embedded

Q1: → i) Dramatic change in processing power, memory and disk capacity in last decade.

ii) Previous high end PC performance can be achieved in small devices

iii) Wireless Revolution

iv) Wireless + Small MC with High Processing Speed = Rise of embedded systems.

Q3: Embedded system:

Specific-purpose computer systems that perform variety of tasks being part of another system and may be controlled by external environment.

Q5 Implications  $\rightarrow$  i) Low Cost Hardware

- Paired Memorization
  - i) Cost-Per-Unit
  - ii) Limited Storage Space  $\rightarrow$  [Complex Algorithms]
  - iii) Limited Processing Speed  $\rightarrow$  [Aggressive Optimization]
  - iv) Dev. Env. different from Execution Env.
  - v) Alien (uncontrolled env)  $\rightarrow$  Hard env.  
Needs to be reliable
  - vi) Long and uninterrupted running times
  - vii) Timeliness Expectations  
(Time complexity)
- Env. Constraint
- Time Constraint

Q2

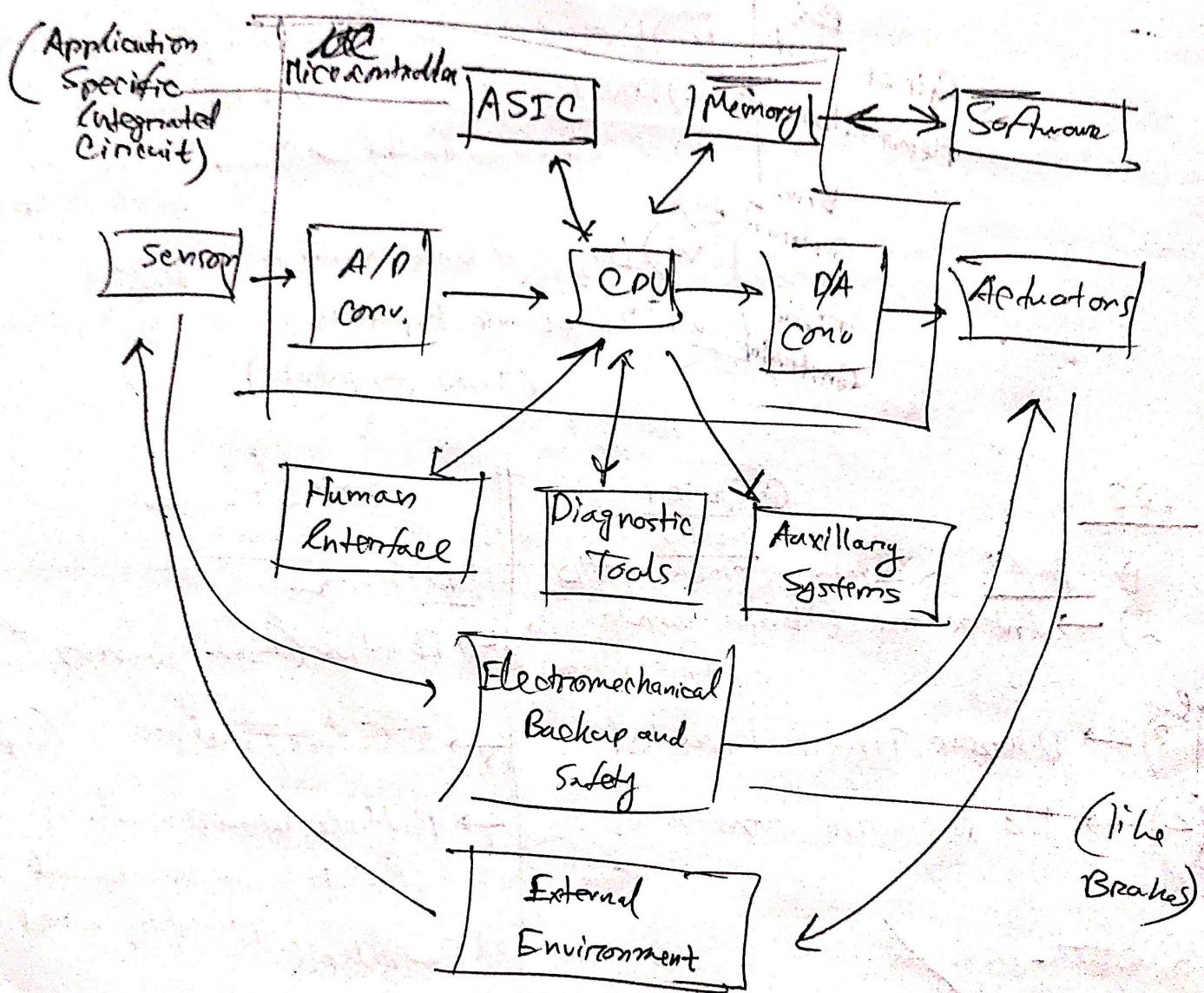
- 1) Definition: Memory + Processor + I/O
- 2)  $\rightarrow$  Interactive (Human Computer Interaction)
- 3)  $\rightarrow$  Discrete Time Not counted
- Resource
  - 4)  $\rightarrow$  No resource constraints
- 5) Stand-alone / networked
- 6) Isolated Environment

Embedded

- 1) Definition:
  - 2) Reactive (Event-driven)
  - 3)  $\rightarrow$  ~~Timeliness~~ Timeliness is important
  - 4) Multiple Resource constraints (Low HW cost, storage and processing speed).
  - 5) Controlled by external system
  - 6) Alien Environment

Q3

## Embedded control system block diagram



( ) is used for explanations, don't write in exams.

## Lec-8 CAN

- Q1) What is CAN bus and why is it called broadcast-type bus? ✓
- Q2) CAN bus can remove  $\frac{n(n-1)}{2}$  complexity of embedded system. ✓
- Q3) Bus length increment, transmission rate decreases - Explain.
- Q4) Draw Data Frame Format of CAN ✓
- Q5) Priority of Devices in CAN
- Q6) Remote Frame, error frame ✓
- Q7) Block diagram of CAN controller ✓
- Q8) Maximum length of CAN bus and justify its appropriateness.

### Q1

→ Embedded protocol for vehicle bus standard designed to allow microcontrollers and devices to communicate within a vehicle without host computer.

→ CAN sends message In CAN protocol the nodes send the message to the bus which can be received by all nodes.

: No way to send message to specific node, all nodes pick up traffic. Nodes "hear" all transmissions.

Q2

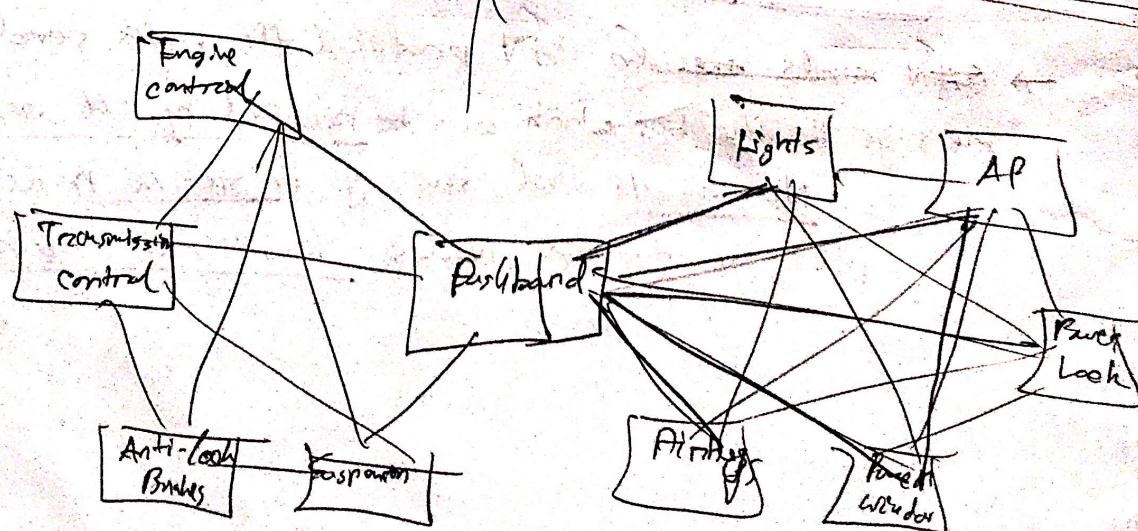
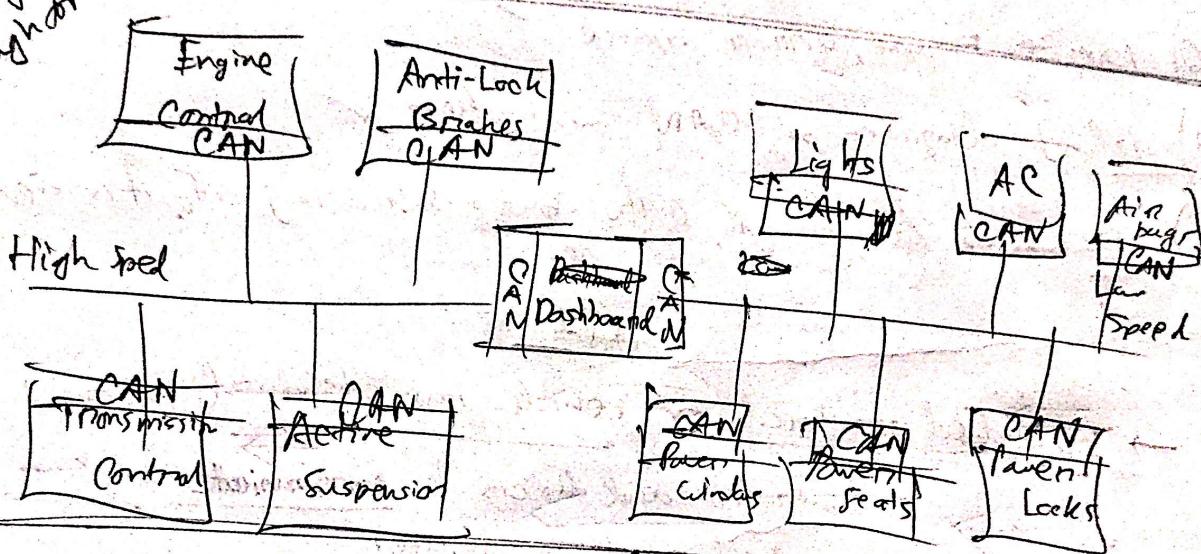
B) CAN connects via serial systems bus

Connects (all control systems) by (serial interface bus)

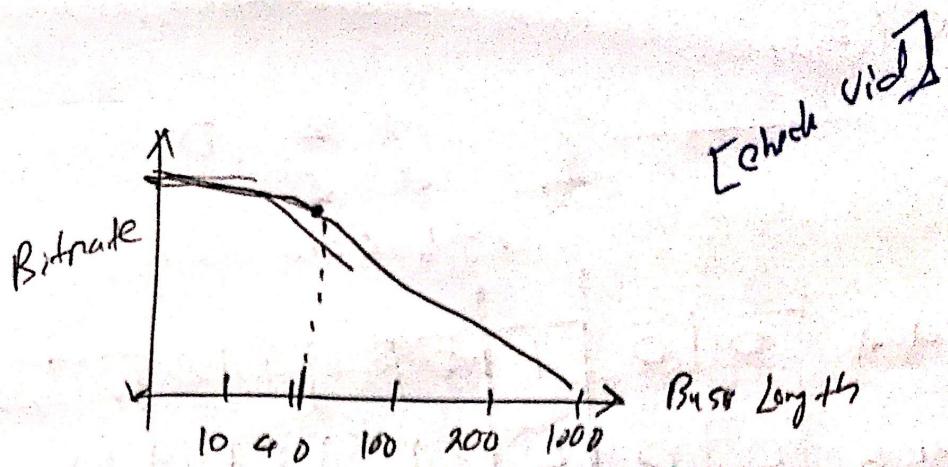
Accomplished by adding CAN specific H/W to each

control unit that provides code for  
transmitting and receiving info via bus.

This figure is  
enough for 5 marks



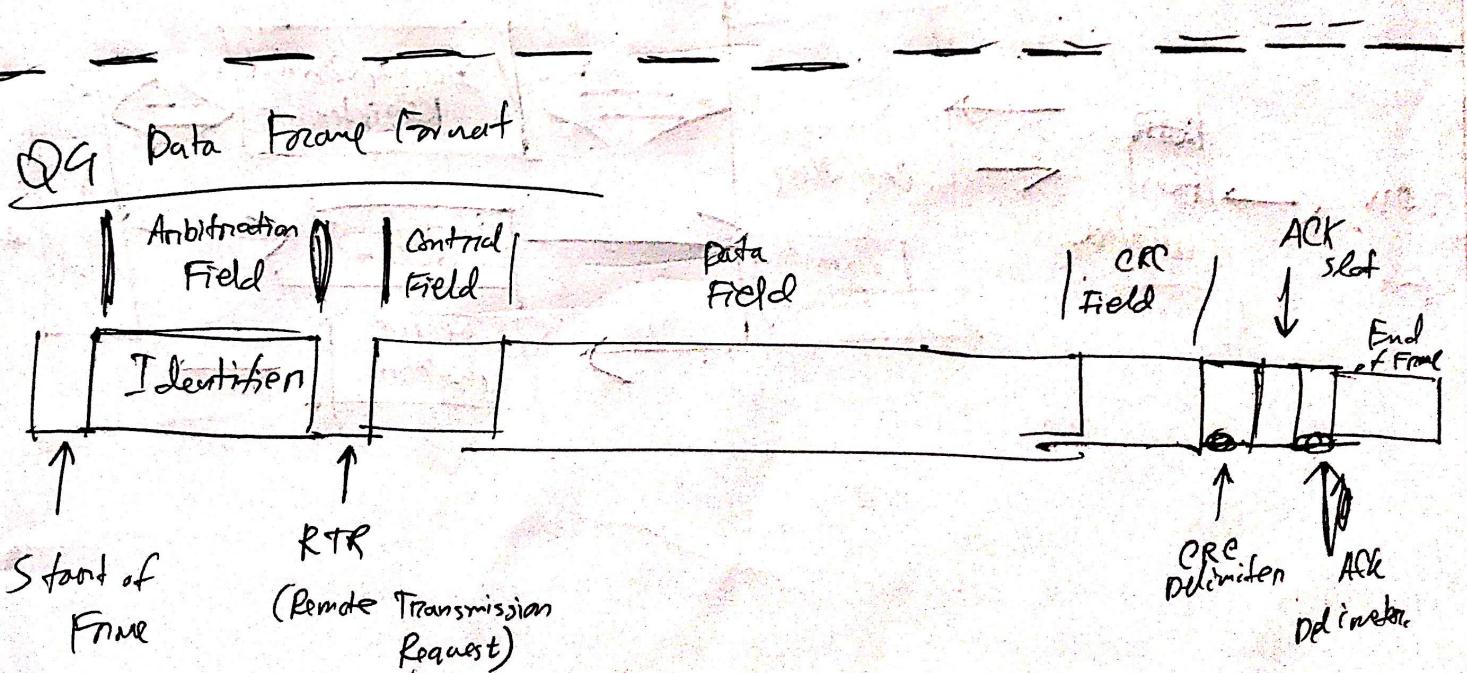
Q3



Due to resistance of cable

Reason: Propagation Delay of electric medium

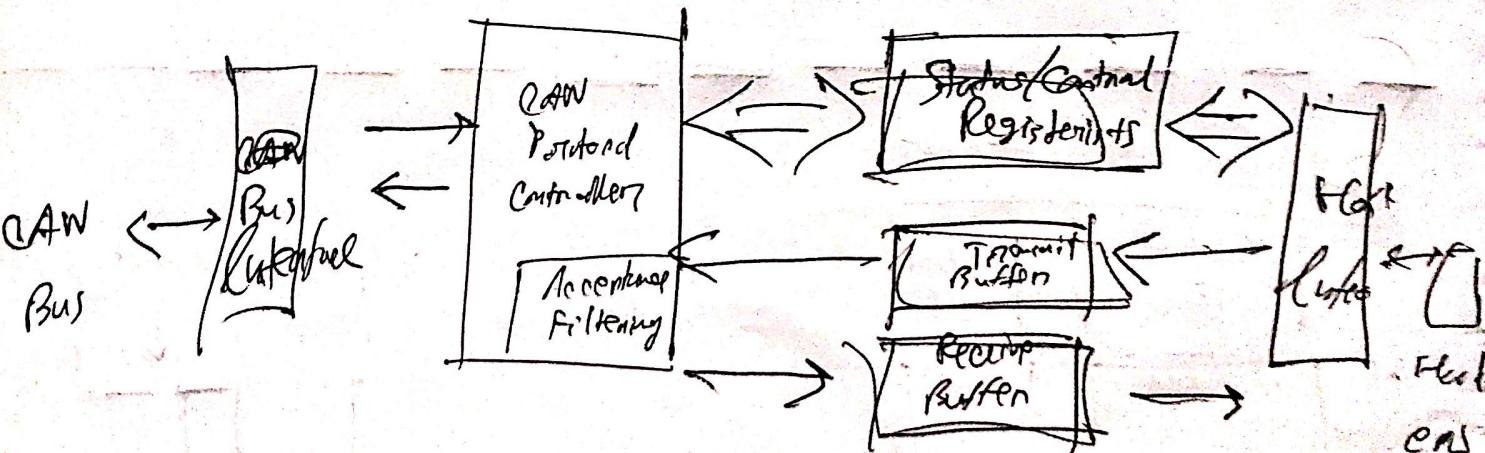
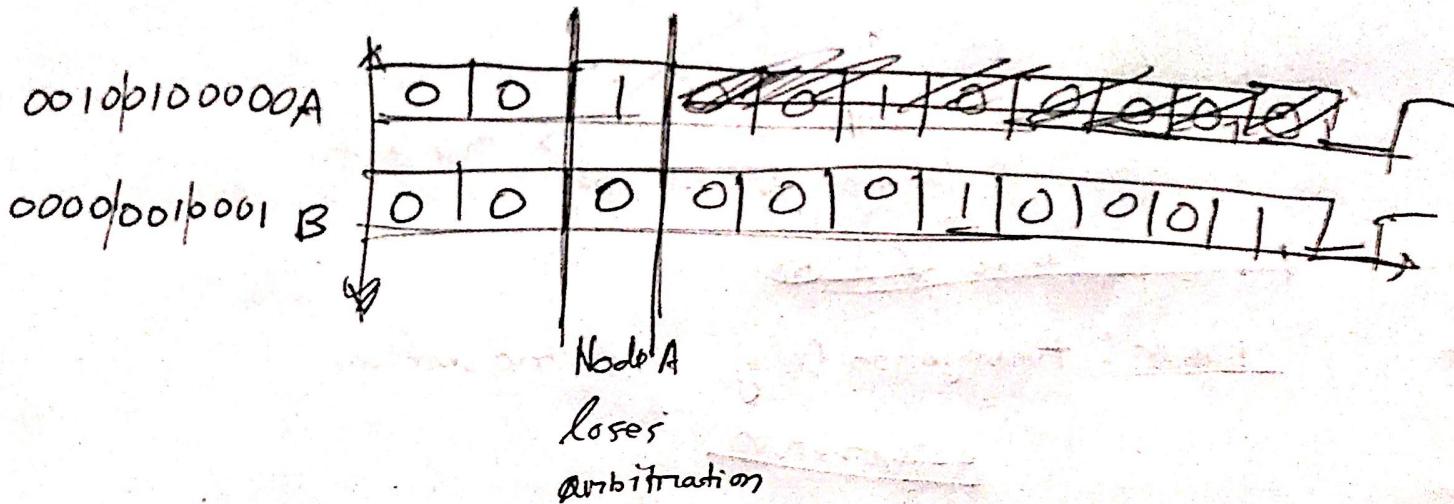
Attenuation



⊗ ACK doesn't mean intended receiver has received

## Quiz Solution

1 2 0  
 ↓ ↓ ↓  
 001 0010 0000



[Slide -13] LoRA → physical layer, modulation  
on wireless  
technique based on chirp spread spectrum.

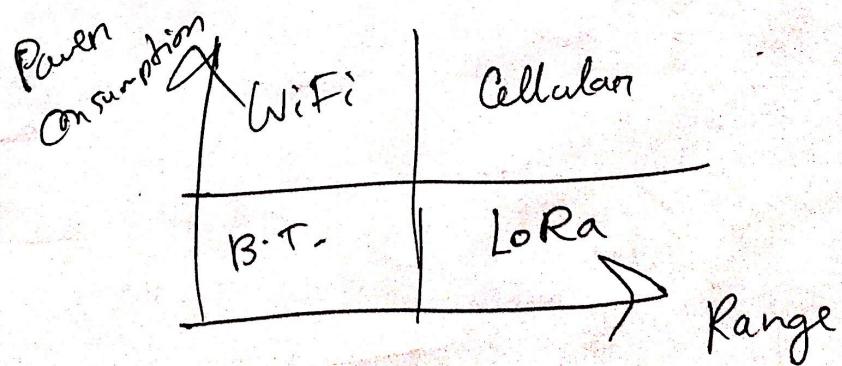
[low power + significant range]

- \* Single base station covers hundreds of ~~metres~~ <sup>km</sup>
- i) → Range → Robustness to interference
  - ii) → ~~Low Power~~ → Network Capacity  
(Under a network)
  - Security
  - Low Cost

Backhaul: 3G / Ethernet

(high speed) ~~short~~  
(long range) ~~far~~

~~better~~  
Energy Efficient ↑  
A Sensors  
B Sync with Beacon  
C ~~status~~ Actuators



8155

8255

8085

8086

No Bidirectional

Port C 8 bit

~~Programmer~~ timer  
(4 mode)

A is bidirectional

Port C 8 bit

No timer

D7 D6

Timer

D5

C

3

4

1

0

IEB FEA

PC

PS AD

IF

