

180041120

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Ans. to Q no. 1(a)

During analog to digital conversion, if the frequency of input signal is higher than sampling frequency, then there's loss of information and this problem is called Aliasing Problem.

Solution: To solve, the aliasing problem we use Nyquist's Rule—the sampling frequency must be greater than twice the input frequency.

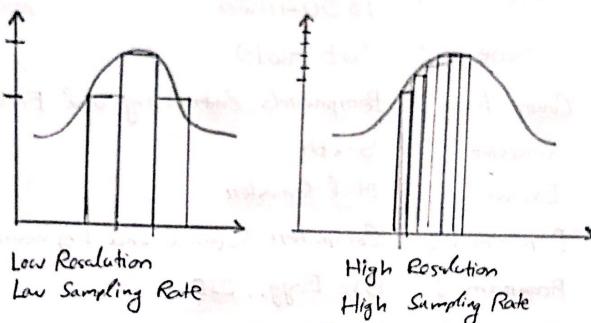
Ex—if input frequency is 25 Hz, the sampling frequency has to be 50 Hz at least.

Conditions for accurate and precise A/D conversion—

i) For better A/D conversion, we need high resolution.

Resolution is the number of discrete states, the A/D converter can produce as an output. Increasing the resolution increases the accuracy or precision of the converted as it can take a

value closer to the original input signal. Resolution,  $[Q = \frac{V_{max} - V_{min}}{N}]$



High Resolution ensures accurate and precise A/D conversion.

- ii) Increasing sampling rate, increases the accuracy of the conversion as more data is captured. This results in a more precise output. By increasing sampling rate, the behaviour of input is captured at a finer detail.

High Sampling Rate ensures accurate and precise A/D conversion.

Ans. to Q. no. 1(b)

Given,  $V_{in} = 10.75 \text{ V}$

$V_{ref} = 1 \text{ V}$

Step-1:  $V = V_{ref}/2 = 1/2 = 0.5 \text{ V}$

$V_{in} \geq V$  as  $0.75 > 0.5$

$\therefore \text{MSB is set to 1.}$

Step-2:  $V = V_{ref}/2 + V_{ref}/4 = 0.5 + 0.25 = 0.75$

$V_{in} \geq V$  as  $0.75 \geq 0.75$

$\therefore \text{MSB is set to 1.}$

Chennai

Since,  $V_{in} = V_{in}$  in this step, setting the other bits are not required as they will be zero.

So, rest of the bits are zero.

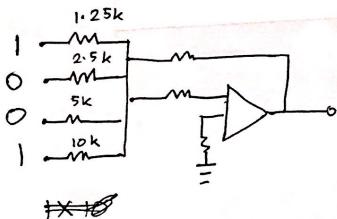
Bit	7	6	5	4	3	2	1	0
Value	1	1	0	0	0	0	0	0

MSB

LSB

Ans. to Q.no. 1(c)Weighted Sum

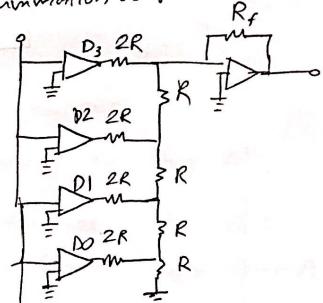
- i) Each bit is given a resistance, which gets doubled for lower bits. The output from each resistance is passed to a summation amplifier.



- ii) Increasing bits will increase the resistance which results in a more precise sum in summation amplifier. That is why number of bits can not be increased much. Can be used for small no. of bits only.

R-2R D/A

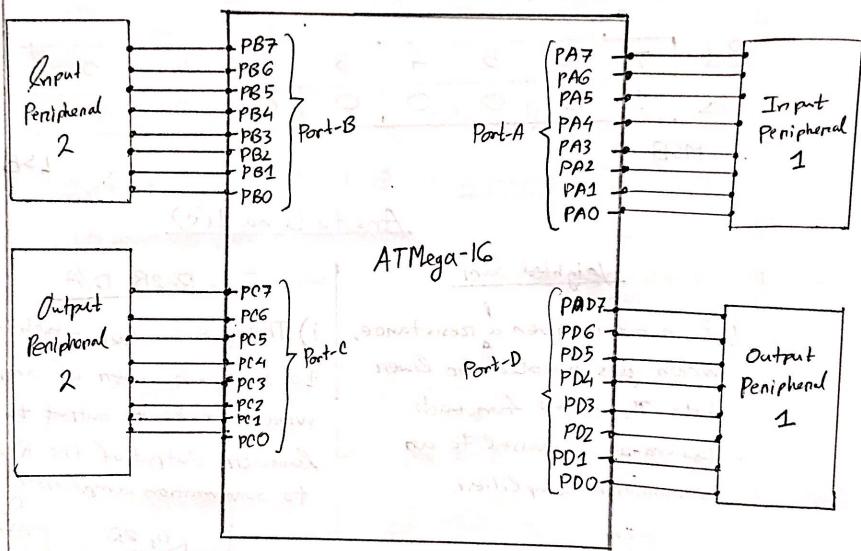
- i) There's a  $V_{ref}$  which is passed to a ~~more~~ number of amplifiers which feeds to output to R-2R ladders. Output of the R-2R is passed to summation amplifier.



- ii) The  $D_3, D_2, D_1, D_0$  outputs are 0, 1, so, the summation doesn't need to be precise. R-2R can be used for a large number of bits.

Ans. to Q.no. 2(a)

→ All 4 ports (A, B, C, D) are bidirectional 8-bit ports.



Ans to Q.no. 2(b)

$$(AB)_{16} \rightarrow 10101011$$

Pin	D7	DG	D5	D4	D3	D2	D1	DO
Function	Timer	IEB	IEA		PC	PB	PA	
Value	1	0	1	0	1	0	1	1

Interrupt for Port-B is enabled [D5=1]

Interrupt for Port-A is disabled [D4=0]

Port-B and Port-A are both taking outputs [D1=1  
DO=1]

$$PC = (10)_B$$

D3	D2	C5	C4	C3	C2	C1	CO
1	0	OUT			STBA <sub>A</sub> /SIBFA <sub>A</sub>	ACKA/OBF <sub>A</sub>	INTR <sub>A</sub>

The first 3 pins of ~~Port-C~~ Port-C, C5, C4 and C3 are set to Output, it can send output.

C2, C1, CO are used for handshaking for Port-A.

C2 → STB<sub>A</sub>/ACK<sub>A</sub> ~~store~~

store or acknowledgement for Port-A

C1 → IBF<sub>A</sub> / OBF<sub>A</sub>

Input Buffer Full or

Output Buffer Full for Port-A

CO → INTR<sub>A</sub>

Interrupt Request for Port-A.

18/04/1120  
Shrawan

### Ans to Q no 2(c)

Asynchronous - overhead for start = 1 byte = 8 bits  
overhead for stop = 1 byte = 8 bits  
overhead for parity = 1 bit

$$\text{total overhead} = (8+8+1) = 17 \text{ bits}$$

$$\text{total data sent} = 30 \times (5 \times 8 + 19) \text{ bytes} [5 \text{ bytes} = 8 \times 5 \text{ bits}] \\ = 1770 \text{ bits}$$

Synchronous - sync overhead =  $30/5 \times 1$  byte  
= 6 bytes

$$\text{total data sent} = (30 \times 5) + 6 \text{ bytes} \\ = 156 \text{ bytes}$$

$$= 1248 \text{ bytes} [156 \times 8 \text{ bytes} = 1248 \text{ bits}]$$

Asynch needs to send less data is better.

$$\text{The efficiency is } \left(1 - \frac{1248}{1770}\right) = 0.705$$

$$= 0.705 \text{ or}$$

$$= 70.5\%$$

more than asynchronous.

(Ans)

Ans to Q no. 3(a)

A1, AO will be (1,1) as they are used to access the control registers.

$48^{th}$  8255 means  $\rightarrow (48)_{10} = \underline{\underline{000}}(110000)_2$

As indexing starts from 0, the pin values will be

$$(48-1)_{10} = (47)_{10} = (101111)_2$$

A7	A6	A5	A4	A3	A2	A1	A0
1	0	1	1	1	1	1	1

$48^{th}$  interface

Access control register

The control Word format is

7	6	5	4	3	2	1	0
For A,B,C Port	Mode of Port-A	I/O of Port-A	I/O of Upper Port-C	Mode of Port-B	I/O of Port-B	I/O of Lower Port-C	
1	0	1	0	X	1	1	X

Hence, if set to Input then 1  
Output then 0. Mode - 01 = (01)

For A,B,C port programming, the  $7^{th}$  bit is set to 1.

$6^{th}$  and  $5^{th}$  bit are for Mode-1 and set to 01.

Port-A is in output mode, so  $4^{th}$  bit is 0.

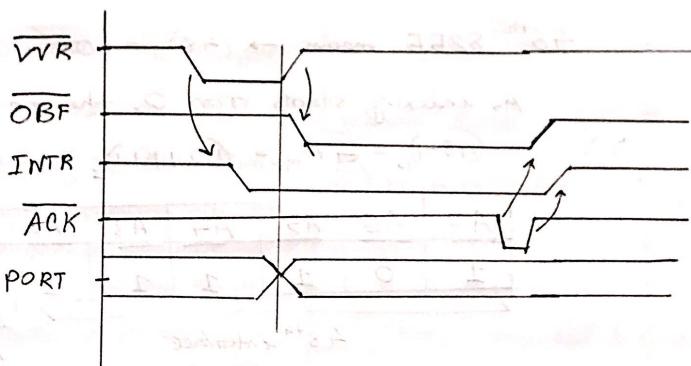
$\otimes$  2nd bit is 1 as port-B is in mode-1.

1st bit is 1 as port-B is used for output.

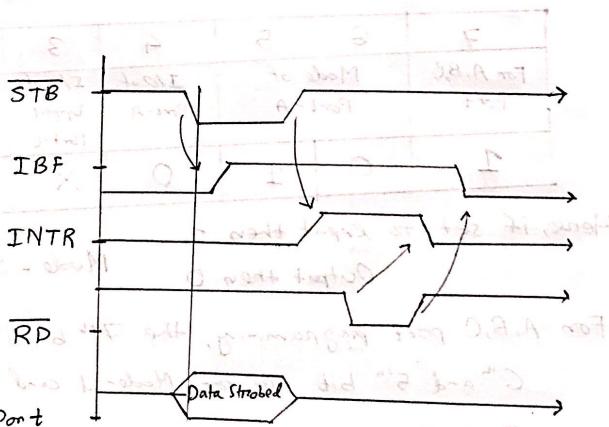
3rd and  $0^{th}$  bit are 'don't care' since they will be used for handshaking.

Ans. to Q.no. 3(b)

Port-A (output-port)



Port-B (input-port)



180041120

Fishman

Ans. to Q no. 3(c)

Flash ADC

- i) Uses a series of comparators and a priority encoder to produce digital signal.
- ii) Fast and efficient
- iii) Usually has low resolution because increasing bits needs to increase the number of comparators by twice.
- iv) Expensive as no. of comparators gets doubled for each bit.

Delta-Sigma

- i) Uses an integrator, and a summing amplifier to produce signal using oversampling.
- ii) Slow due to oversampling
- iii) High resolution with high accuracy.
- iv) Cheap compared to flash ADC.