CODE No.:16MC10101 SVEC16

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Anantapur)

M.C.A. I Semester (SVEC16) Regular/Supplementary Examinations January - 2018

COMPUTER ORGANIZATION

[MASTER OF COMPUTER APPLICATIONS]

Time: 3 hours **Max. Marks: 60**

Answer One Question from each Unit
All questions carry equal marks

UNIT-I

1. a) Modify the following decimal numbers to the bases indicated.
   i) 7562 to octal. 2 Marks
   ii) 1938 to hexadecimal. 2 Marks
   iii) 175 to binary 2 Marks
   b) Explain the floating-point representation. 6 Marks

(OR)

2. Discuss in detail the fixed-point representation. 12 Marks

UNIT-II

3. Draw and explain the logical configuration of shift registers with parallel load. 12 Marks

(OR)

4. a) Explain integrated circuits of digital components. 6 Marks
   b) Sketch the encoder and draw the truth table for it. 6 Marks

UNIT-III

5. Compare branch instruction, call subroutine instruction and a program interrupt. 12 Marks

(OR)

6. Explain data manipulation instructions of a computer. 12 Marks

UNIT-IV

7. List different phases of instruction cycle and explain the first phase in detail. 12 Marks

(OR)

8. Sketch and explain the control unit of a basic computer. 12 Marks

UNIT-V

9. Assess the DMA transfer technique with the block diagram. 12 Marks

(OR)

10. Define cache memory. Explain different mapping procedures in the organization of cache memory with suitable example. 12 Marks