BRAC UNIVERSITY

Department of Electrical and Electronic Engineering

CSE350: Digital Electronics and Pulse Techniques

Experiment No: 2

Implementing a DTL logic gate

Objective

1. Construct a DTL logic gate.
2. Understand the circuit operation.

Circuit Diagram

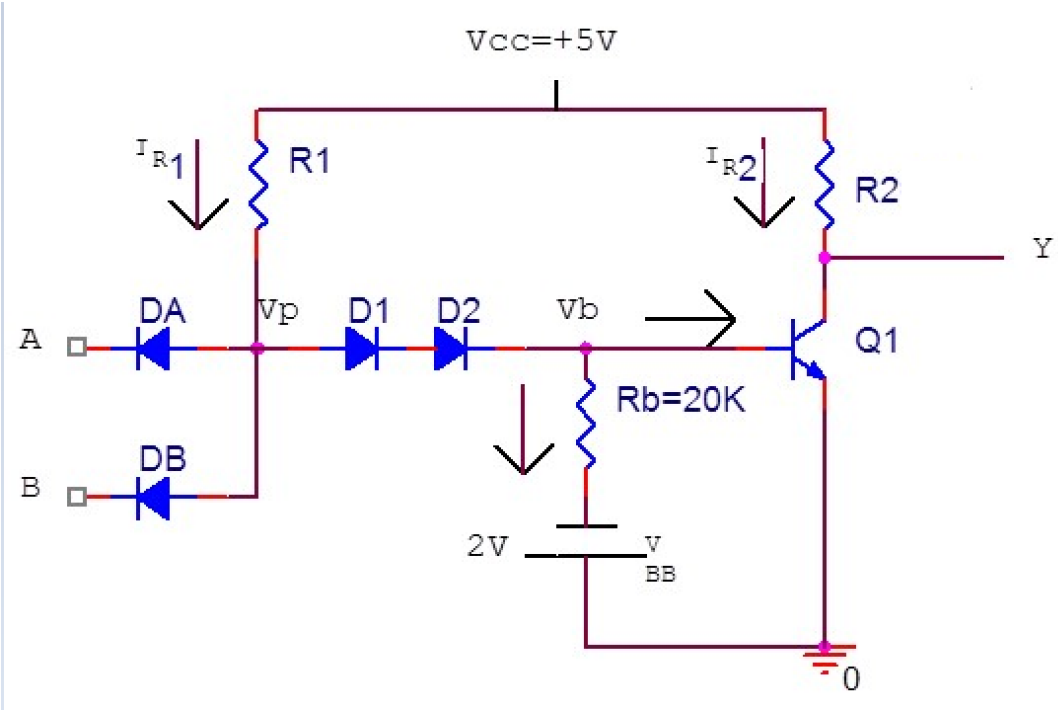

Fig: 1

Laboratory tasks

1. Connect the circuit as shown in Fig: 1 assuming that the values of R1 and R2 = XXXX where XXXX are the first 4 digits of your student ID
2. Observe the output for all possible inputs
3. Fill up the following table.

Input A	Input B	V_{DA}	V_{DB}	V_P	I_{R1}	Ir2	Vb	Output Y
0	0							
0	1							
1	0							
1	1							

4. Operate the gate in Fig 1 as an inverter by connecting either of the inputs to +5V and using the remaining one as input terminal. Fill up the following table.

Input A	Input B	V_P	Vb	Output Y
1	0			
1	1			

Report

1. Assume that Logic **HIGH** has been applied to both inputs of the circuit shown in Fig: 1, draw the partial circuit consisting of only those components which remain active.
2. Explain the logic operation in the table 2 (Laboratory task step 4). How did you reach that logic operation from NAND operation of figure 1 ?
3. Explain briefly how NAND operation is performed in the circuit.
4. Using proteus data Find the operation mode of Q1 when one of the inputs is **HIGH** and other one is **LOW**.
5. What is the maximum value of inputs A,B to keep the output **HIGH**? (use simulation data)