

**BRAC UNIVERSITY**  
**School of Engineering and Computer Science**  
**CSE-350: Digital Electronics and Pulse techniques**

**Experiment No: 3**

**Study of a TTL NAND gate with totem pole output**

**Objective**

1. Building standard TTL-NAND Gate.
2. Measure the voltages and verify the circuit.

**Circuit**

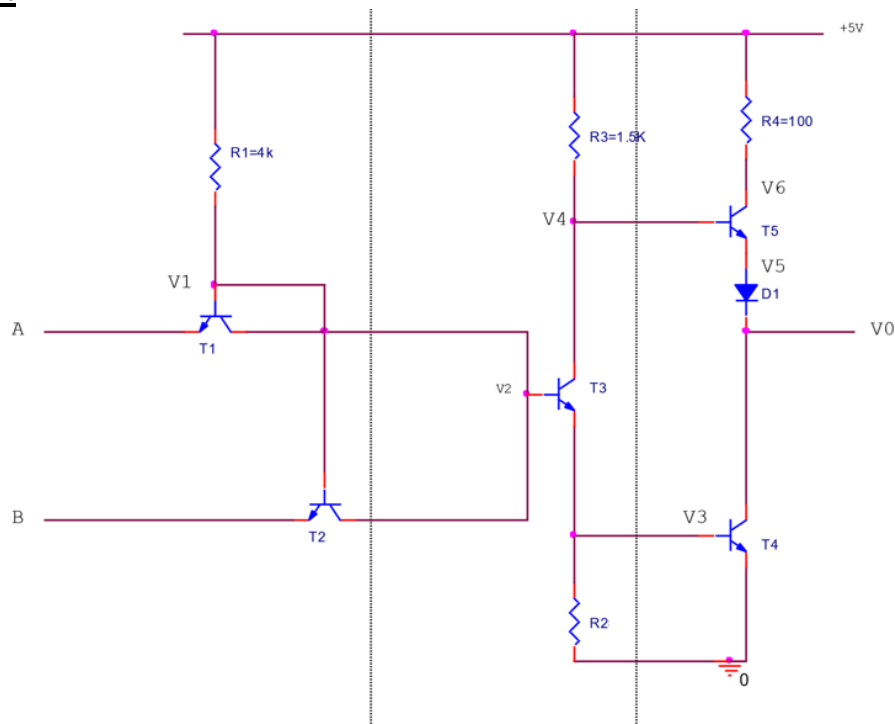
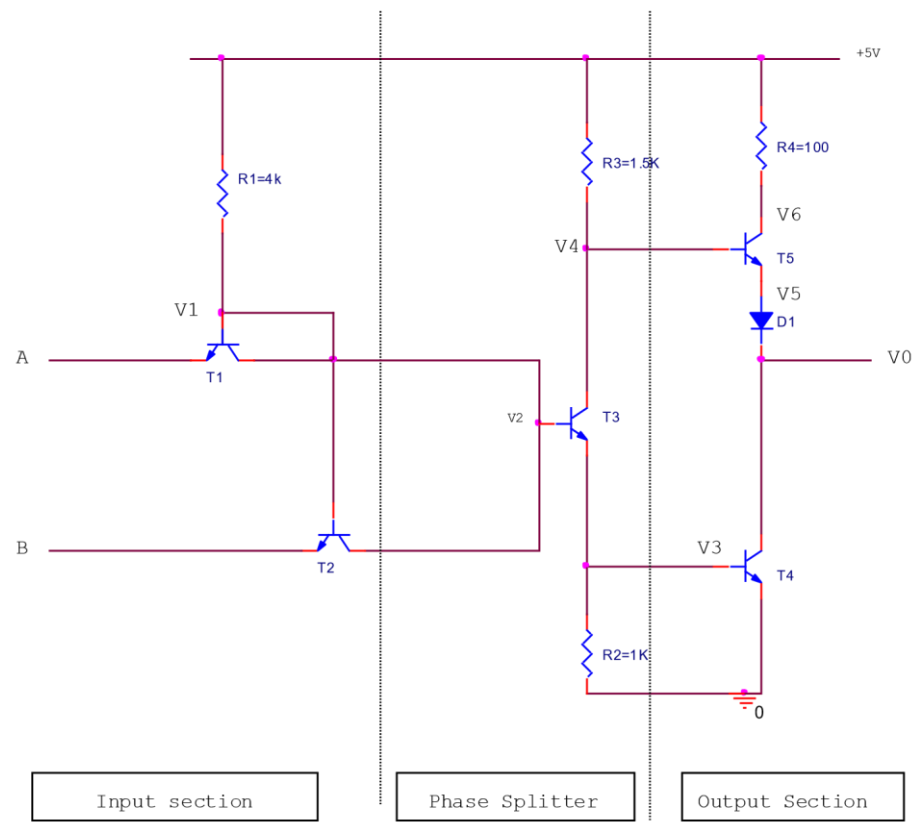


Figure 1: TTL NAND gate with Totem Pole output

## Procedure

1. Connect the circuit as shown in Fig: 1
2. Value of  $R_2 = \text{XXXX ohm}$  where XXXX is the last 4 digits of your student ID
3. Measure the  $V_0, V_1, V_2, V_3, V_4, V_5, V_6$  for all possible input combination.

Input A	Input B	Input (VA)	Input (VB)	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$	$V_6$
0	0									
0	1									
1	0									
1	1									



## **Report**

1. Explain how figure 1 circuit is working as NAND gate.
2. What do you understand by totem pole stage?
3. Draw the active portion of the circuit when both inputs are low.
4. What is the function of T3?
5. What may happen if diode D1 is not used in the circuit?
6. What is the mode of operation of the T5 transistor when at least one input is LOW? Verify it from Proteus data
7. Design a TTL NOR gate with Totem Pole Output Stage.

## **Reference**

Reference: Microelectronics: Digital and Analog Circuits and Systems by Jacob Millman