CSE 350

Digital Electronics and Pulse Techniques

Lab Report

Experiment No: 03

Study of a TTL NAND gate with totem pole output

Submitted by:

Name – Fariha Rahman

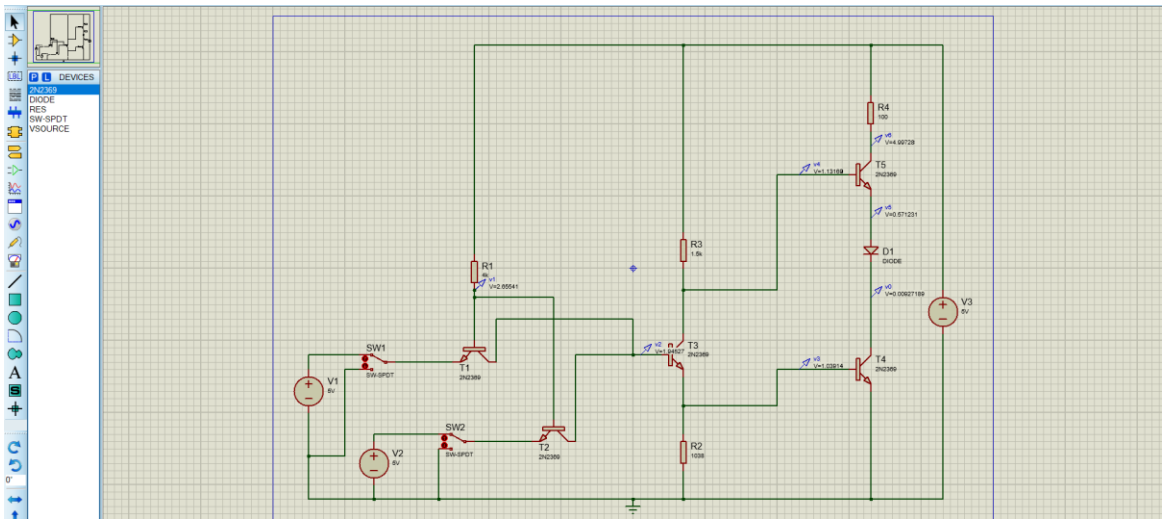
ID - 19101038

Section - 04

Department - CSE

Fall 2021

BRAC UNIVERSITY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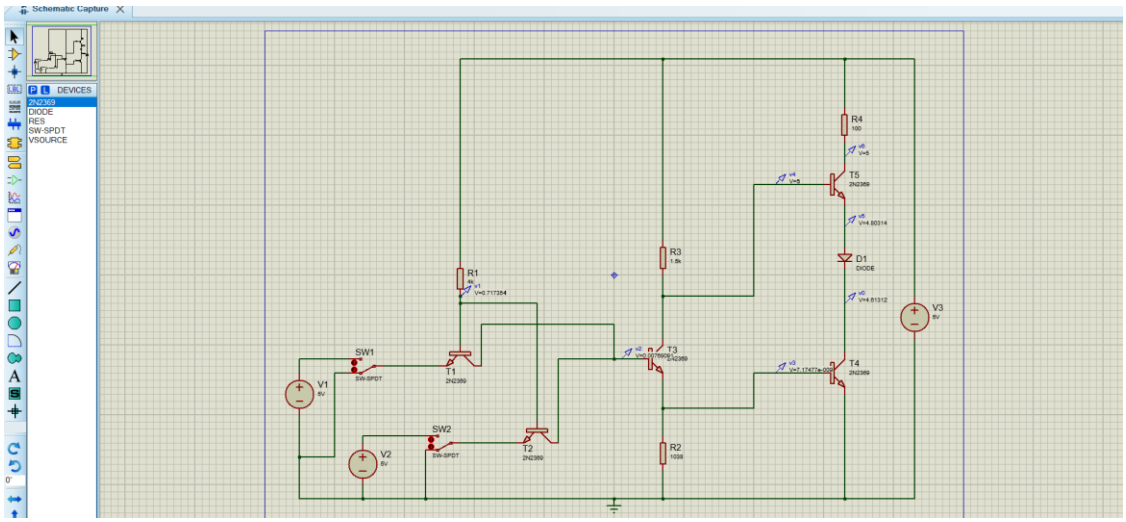
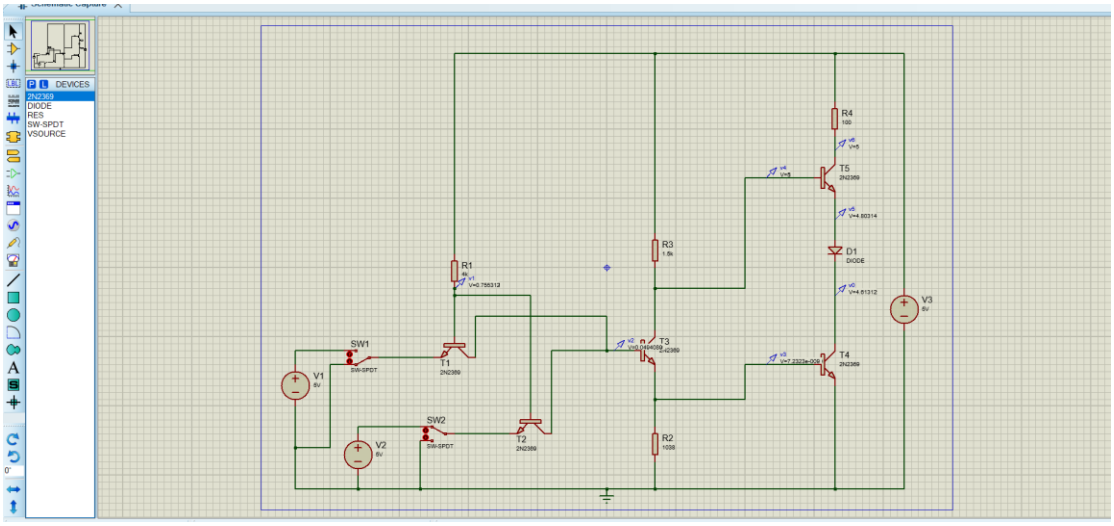
RES
SW-SPDT
VSOURCE
R1
R2
R3
R4
D1
T1
T2
T3
T4
T5
SW1
SW2
V1
V2
V3


Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
R1
R2
R3
R4
D1
T1
T2
T3
T4
T5
SW1
SW2
V1
V2
V3


DEVICES
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DIODE
RES
SW-SPDT
VSOURCE
R4
100
T5
2N2369
D1
DIODE
R3
1.5k
R1
4k
V=0.755313
T3
2N2369
T4
2N2369
SW1
SW-SPDT
T1
2N2369
V1
6V
SW2
SW-SPDT
T2
2N2369
V2
6V
R2
1036
V3
6V

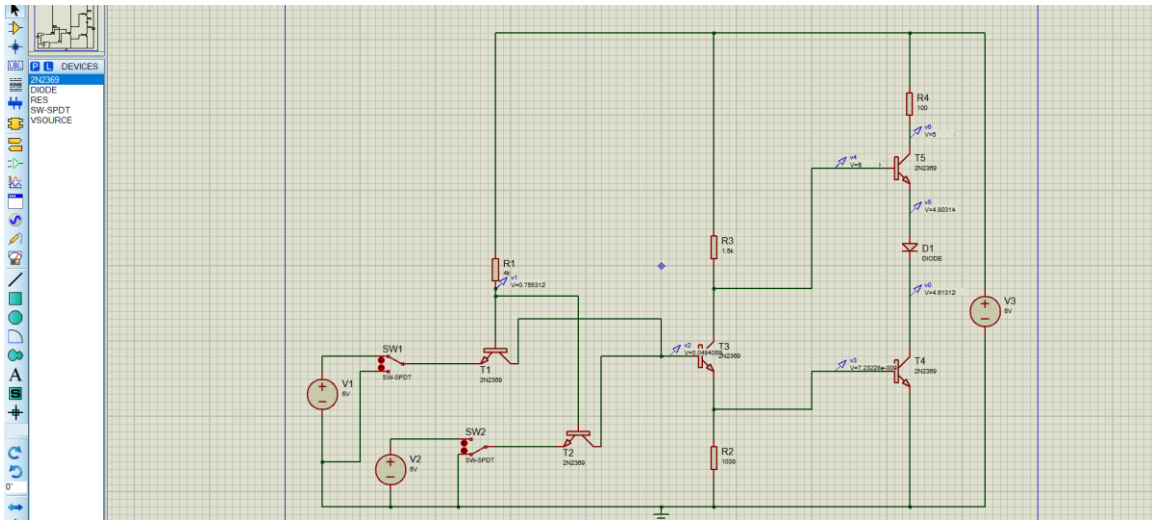

DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
R4
100
T5
2N2369
D1
DIODE
R3
1.5k
R1
4k
V=0.755312
T3
2N2369
T4
2N2369
SW1
SW-SPDT
T1
2N2369
V1
6V
SW2
SW-SPDT
T2
2N2369
V2
6V
R2
1036
V3
6V

Table:

Input A	Input B	Input V_A	Input V_B	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0	0	0	~~4.61312~~ ~~0.00927~~	~~0.717354~~ ~~1.94527~~ 2.65541	0.007691 ~~1.94527~~	7.175×10^{-9} ~~1.03914~~	5 ~~1.13169~~	~~4.80314~~ ~~0.57123~~	5 ~~4.997~~
0	1	0	5	4.61312	0.755312	0.04941	7.23×10^{-9}	5	4.80314	5
1	0	5	0	4.61312	0.755312	0.04941	7.23×10^{-9}	5	4.80314	5
1	1	5	5	0.00927	2.65541	1.94527	1.03914	1.13169	0.57123	4.997

Answer to the Question No-1

When one of the inputs are Low, T_1 or T_2 or both transistors will go in SATURATION Mode. and a small amount of current will flow from the base of T_3. So, T_3 will be in cut off mode and that will cause T_4 to be in cutoff mode too. T_5 will be in Active mode as 5V at base and positive voltage in emitter. So we will get "High" voltage from the output terminal.

Again, when both of the inputs are High, T_1, T_2 will be in reverse active Mode. T_3 will be in SAT and T_4 will also be in SAT, T_5 will be in cut off mode. So, the output will be Logic Low.

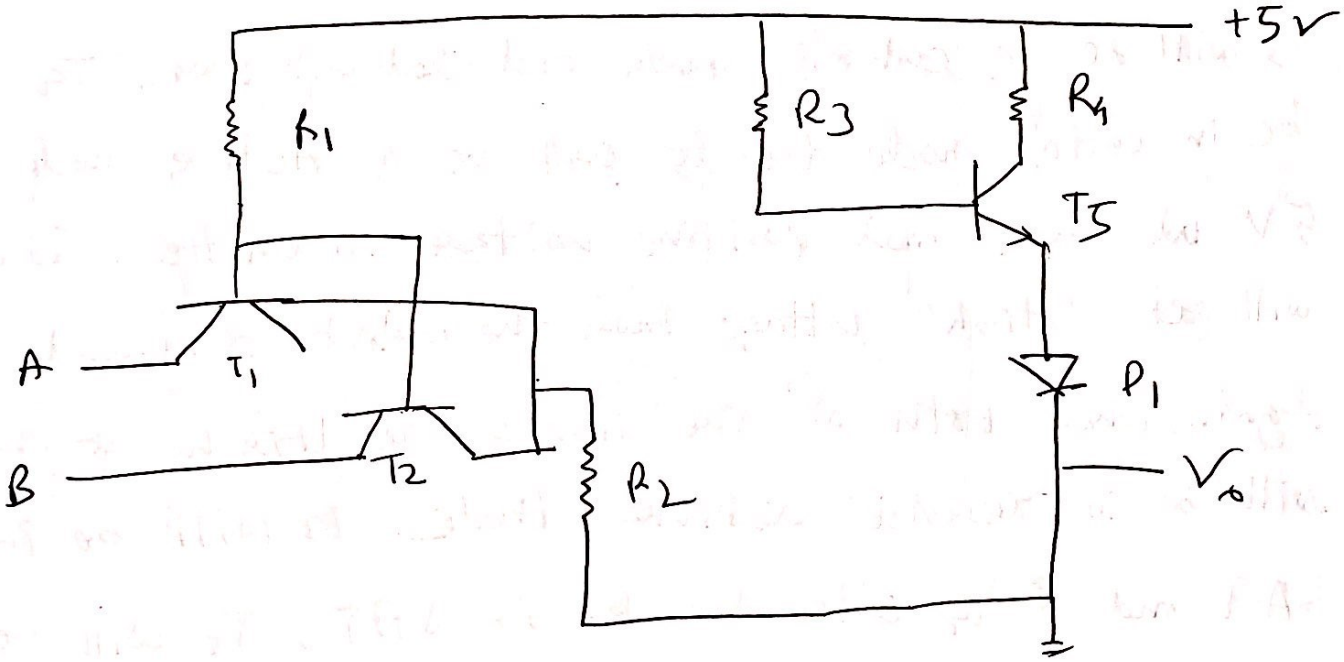
Therefore, the given circuit will be worked as a NAND gate. because in NAND gate when any of the input is Low, we get High and both inputs are High, we get Low in the output.

Answer to the Question No-2:

Totem pole stage refers to push-pull output consisting of two complementary transistors. Because of this push-pull configuration, the circuit configuration is known as totem pole totem pole structure. The advantage of totem pole output is, it decreases low to high transition time while not increasing power dissipation proportionately.

Answer to the Question No-3 :

When both the inputs are low, the active portion will be-



Answer to the Question No-4:

The function of T3 transistor is switching to supply voltage to one output transistor (T4 / & T5) at a time. When any of the input is low, T3 will be in cut-off. T4 will be cutoff and T5 will be in active mode.

When both inputs are High, T_3 will be in SAT. T_4 will also in SAT and T_5 will be cut off mode

Therefore, when one of the Transistor (T_4 / T_5) is in SAT mode, the other one will will be in cut off mode and vice versa.

Answer to the Question No-5:

If the diode D_1 is not used then the inputs are High T_5 will be in active mode and it cannot pull low to high output voltage. To keep it in cut off mode at that stage D_1 diode is used.

Answer to the Question No-6

When at least one input is low, the mode operation of T_5 transistor will be "active".

Answer to the Qustion No-7

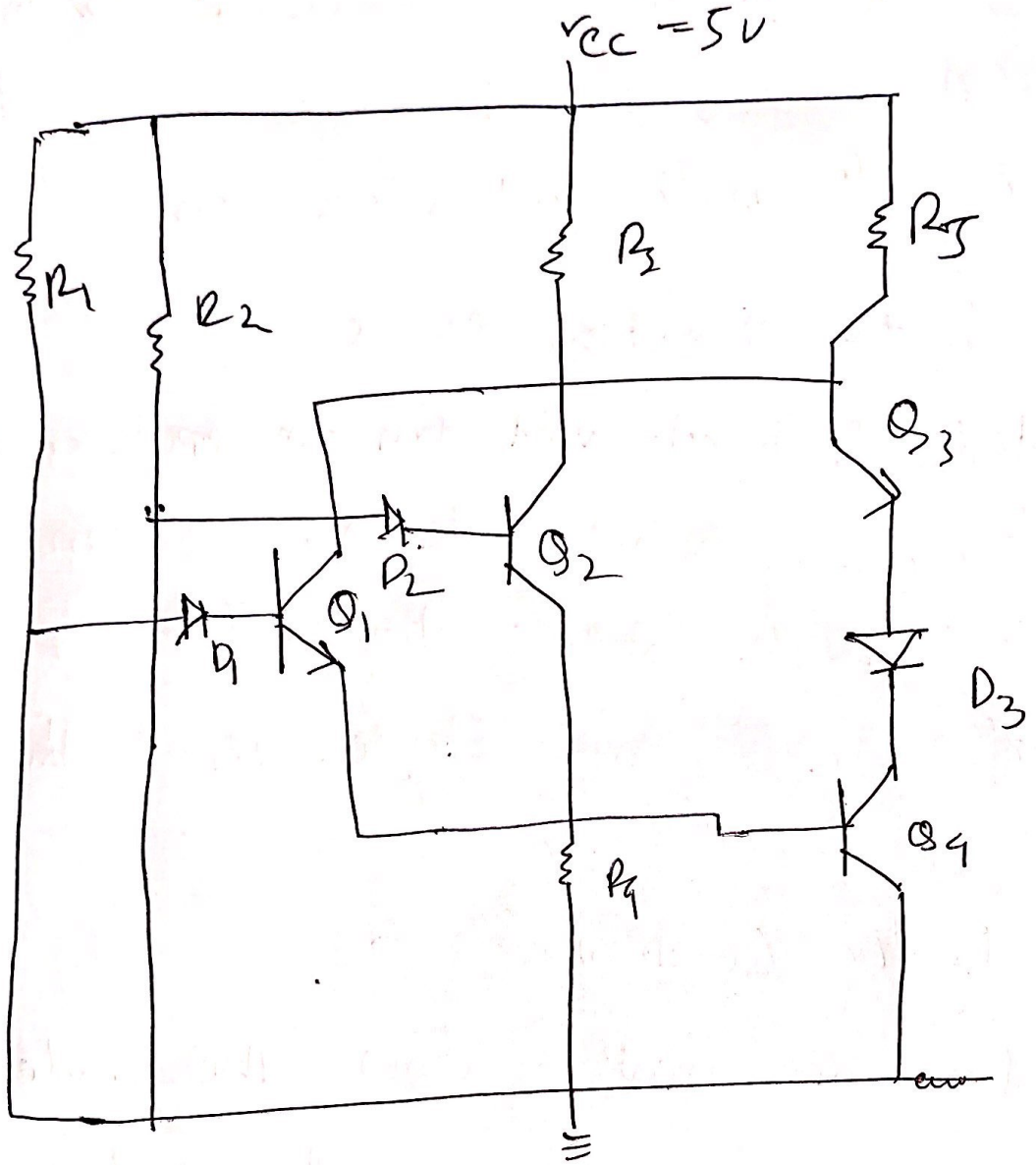


fig: TTL NOR gate with Totem pole output stage.