CSE350

Digital Electronics and Pulse Techniques

Lab Report

Experiment No: 04

Analysis of the binary weighted and R/2R ladder D/A converters

Submitted by:

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Section - 04
Department - CSE
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BRAC UNIVERSITY



Objective:

The objective of this experiment is to construct two different D/A converter and to verify that digital signal is converted into proportional analog signal.

Equipment:

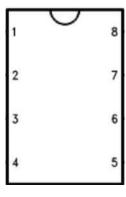
Resistance = 10K, 20K, 5K, 2.5K, 1.25K

Dc source

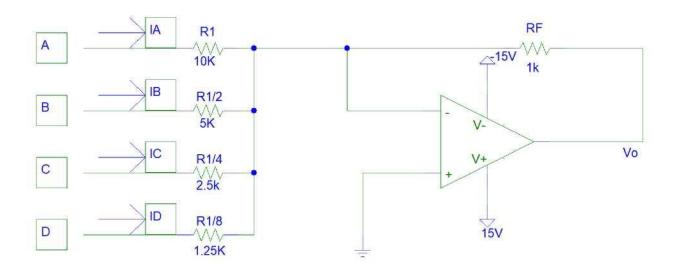
Operational Amplifier

Multimeter

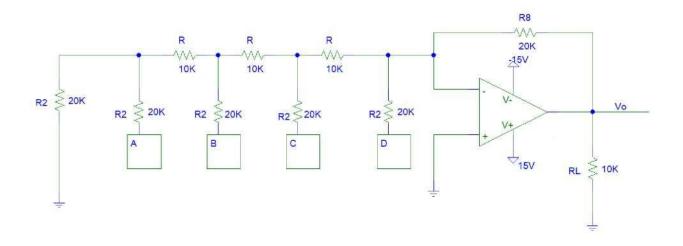
Circuit Diagram:

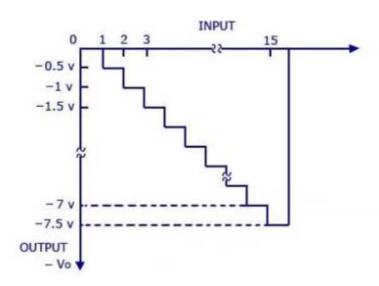


Circuit Diagram 01 Digital to Analog Converter using Binary-Weighted Resistors



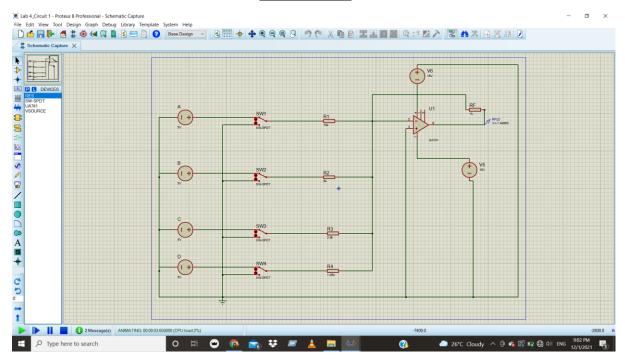
Circuit Diagram 02 Digital to Analog Converter with R and 2R Resistors



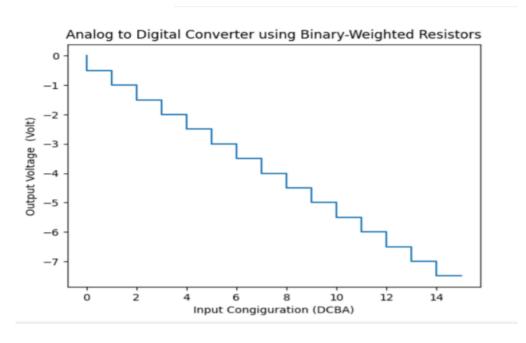


Circuits:

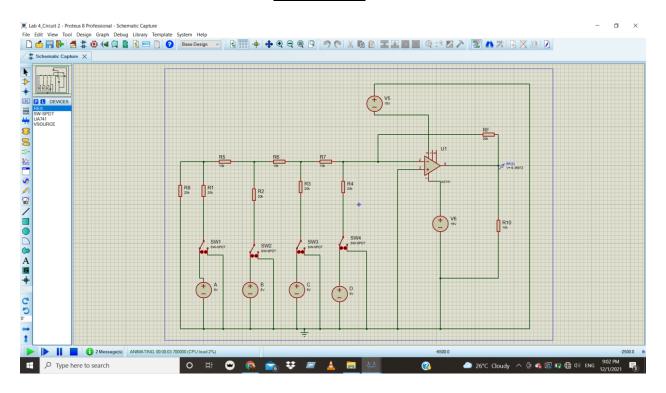
Circuit 01



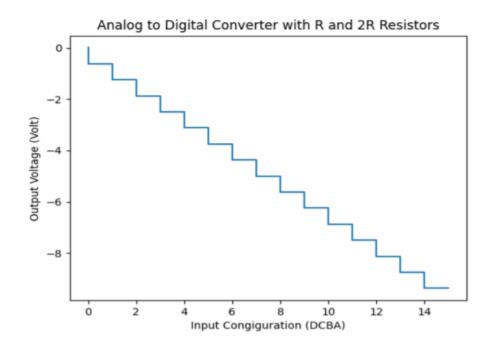
Graph For Circuit 1:



Circuit 02



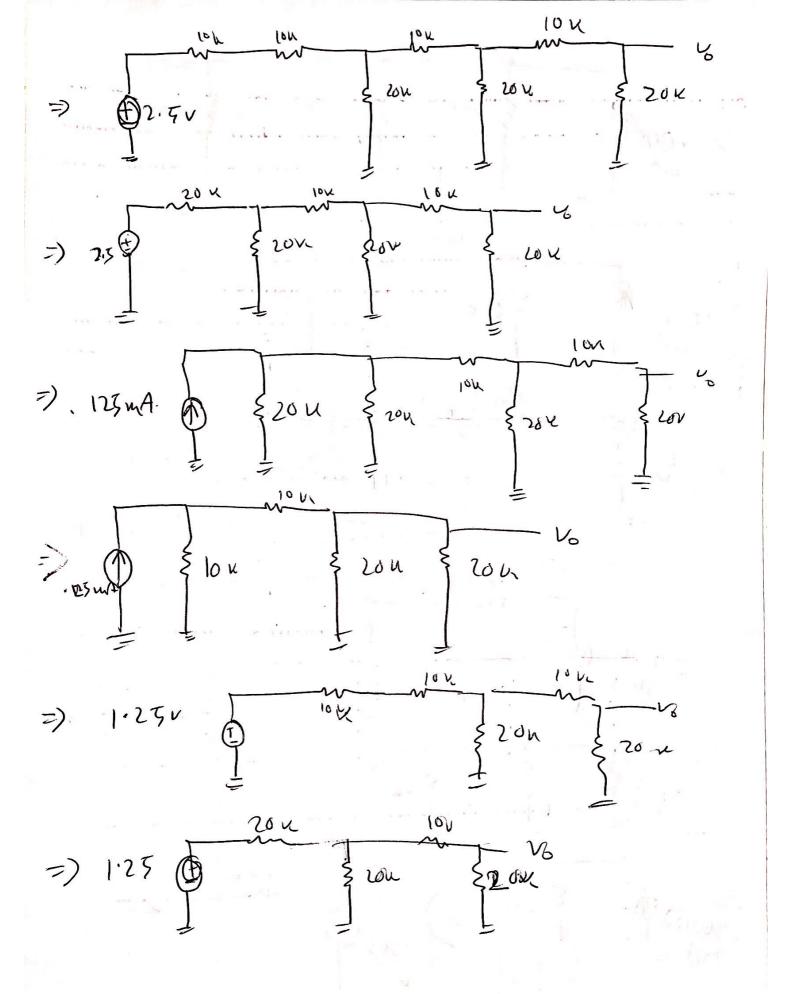
Graph For Circuit 2:

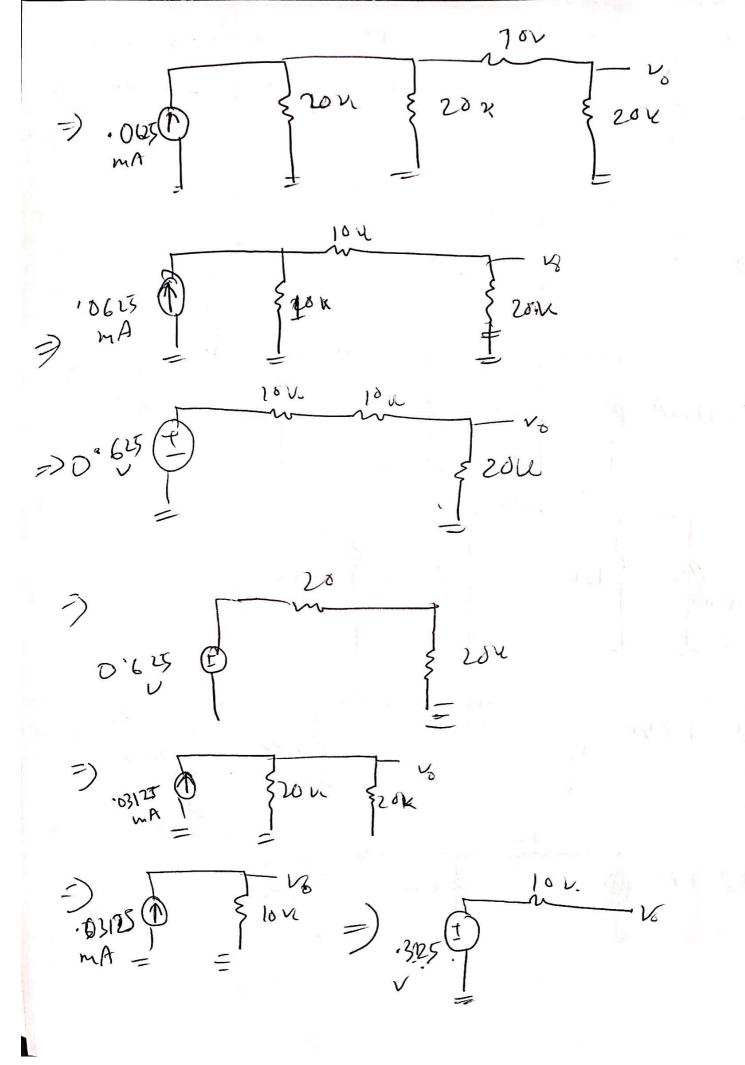


Dorbe tuble: Circuit -1:

Input Configuration	0	B C	B	M	Output voltage, Volu
	0	6	0	0	0.00272
3	0	6	6		-0.497259
3	0	0		0	0,777299
7	0	0			-0.99723
5	0		0	^	-1.4972
6	0		0	1-0	-1.99714
7	0	The same of the sa			-2,49712
8	O			0	-2.9971
7	water the second second	The section of the se	THE RESERVE OF STREET		- 3,49708
The second second second second		0	0	6	-3.99685
10		D	0		-4-49683
		0		^	-4.9968
اک	(0	1	The state of the s	-3,49678
13	1		0	^	-5,99672
14	1		0)	-6.4967
15		Agricultura de la companya de la com	(0	-6.99667
16			1		-7.49665
Circuit-2					
1 1	0	6	0	0	0.00495
2	0	0	٥		-1.24501
3	0	0		6	-1.86999
4	The second second second second second		0	Ø	-2.49496
5	0	THE SECOND CONTRACTOR OF THE SECOND S	0		-3.11994
6	6			0	-3.77 492
7	0			1	-4.3699 -4.99487
8	0			0	-4.99487
3		0	0		-5-67 985
10		0		0	-6.24 483
11		0		l.	-6.86981 -67.49478
11			0	0	- 9: 11976
13	1'	(0		- 8: 11976 - 8: 74479
14				0	- 9. 36972
THE REAL PROPERTY.		and the same of th		41	

Answer to the Question No-L: By Champing, the value of RF we can change the value of the step size, But they only one condition and that is we need to set the step value in such a way that for any input our analog value must be less than (15 1), meaning output voltage should exceed saturation levels of the opamo So, it is not possible to get higher than 15 V in 62A convertes Answer to the Question No-2: We know, full step output = Reterence wittage X vo (LIB) For, Binony weighted DLA, reduce = 1 - 4971 = 497 : full step output = 15 x . 497 = 7. 95561+ For, Rand 2h RZA, Newsler = 1:6201 = "620 :, full step output = 15 x, 620 = 9.3 Volt Answer to the Question No-3: -Taking input > 0001 Now, Applying source transformedion : DÖZ5MA Fred Fred \$ 20 K \$ 20 K





The closed loop voltage goin of an inventing amplifier is:

$$\frac{-7}{10}$$
 Vow = $\frac{-20}{10}$ x (.3125)

= - 0.623 U

Answer to the Question No- 4 &

ID-19101038: VA=VB=VP=Vp=3+8=11V

Input Configuration	D	C	B	I A	Outrut Kittage		
	Ō	6	6	6	0.0627218		
2	0	6	D		-1.09729		
3	0	0	The second straight respective interesting or the product of the second straight.	0	-2.17717		
4	Q	6	The second secon	1	-3,29713		
5	0		0	6	-4.39698		
6	0	1	0	The state of the s	-5.49694		
7	٥			G	-6.59688		
8	Ð		A XA DATE OF THE PARTY OF THE P		-7.69689		
9		0	0	0	-8-79634		
10		O	0		-9.8963		
11		Q	l	٥	-10.9962		
12		0		١	-12-0962		
13		1	0	0	-13.196		
14		1	0	4	-13.49 45		
15				0	-13. 4959		
16	1	١		(-13.493		

Arswer to the Q. Fo

We know, Step siee = (KF) VHIGH From this formula, it can be said that, by Changing the walre of Re, R; and WHILE We can control the ster size- It is seen that, the relationship between Re and step size is propontional. That means If we increase RF, the stepsice will increase too and it we decrease the le and stellize will decrease as well, but when the value of Ri and is unchanged. VHIGH