CSE 350

Digital Electronics and Pulse Techniques

Lab Report

Experiment No: 02

Implementing Diode Logic (DL) gates

Submitted by:

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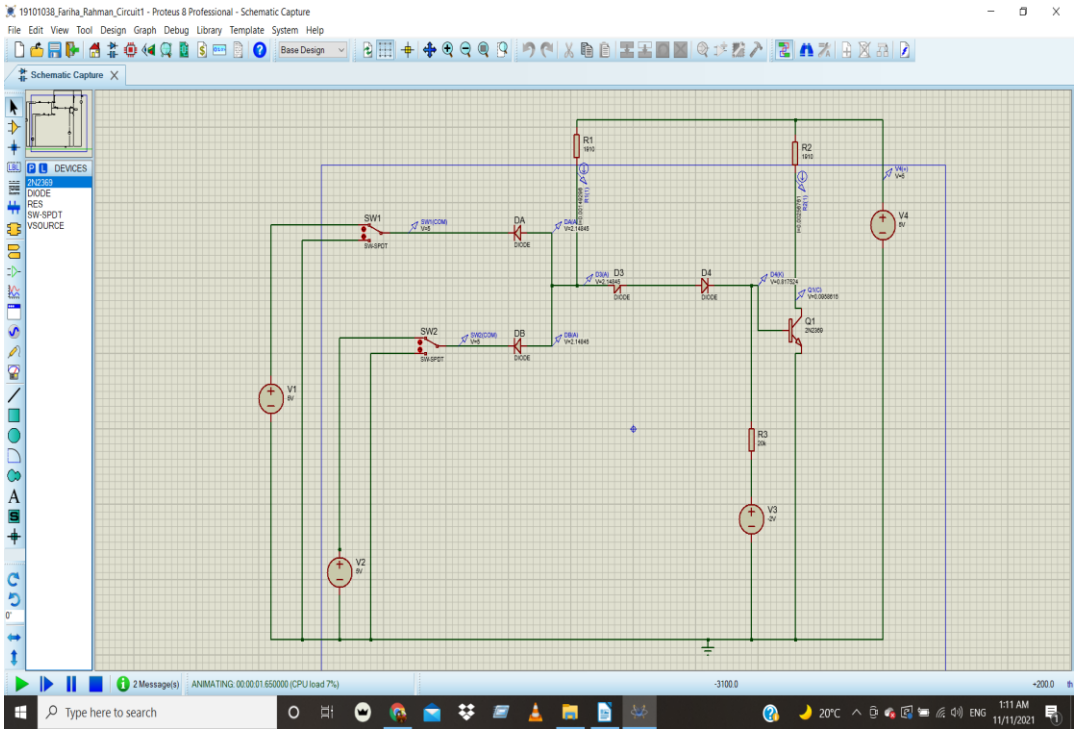
Section - 04

Department - CSE

Fall 2021

BRAC UNIVERSITY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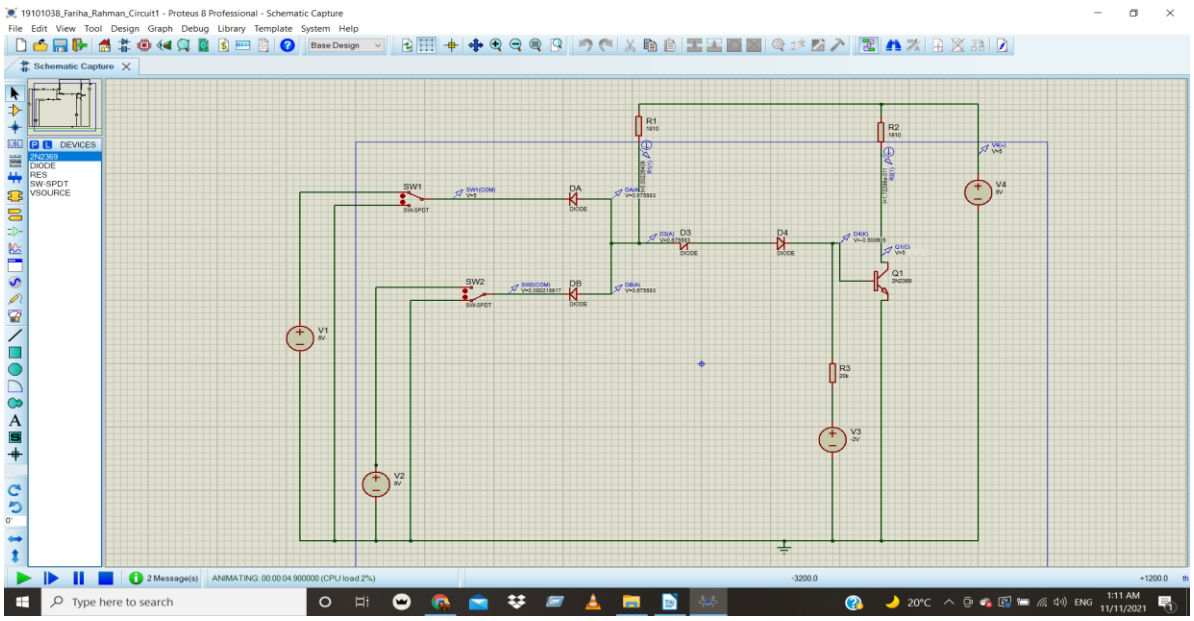
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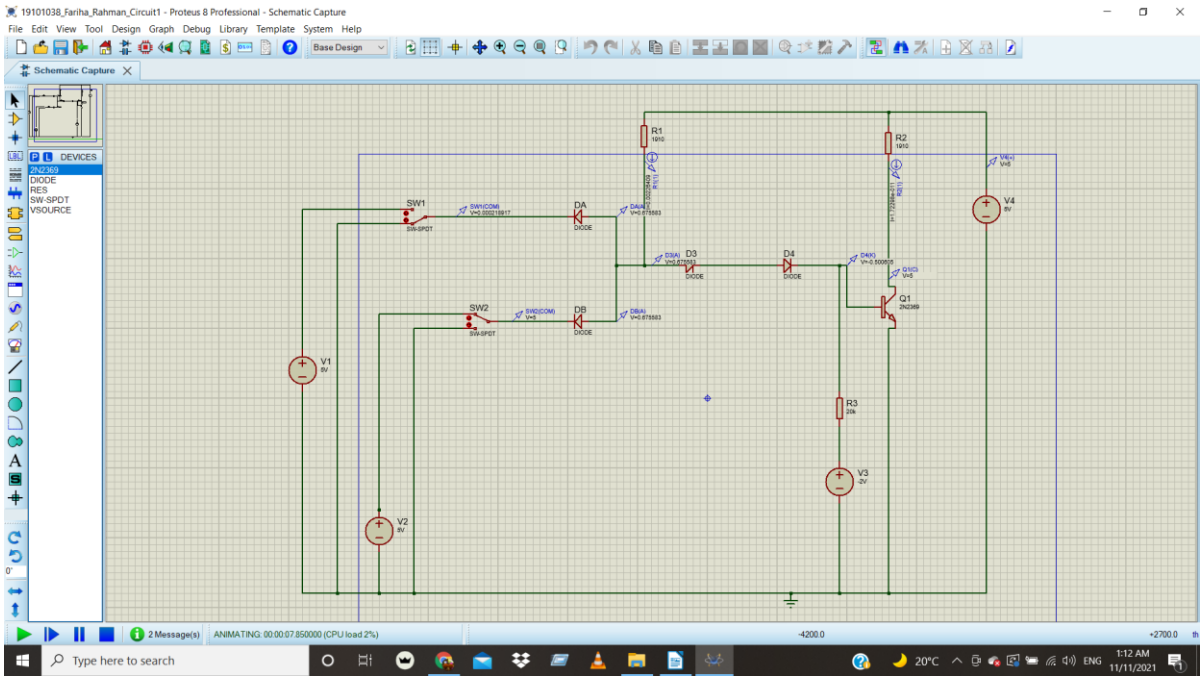
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Base Design
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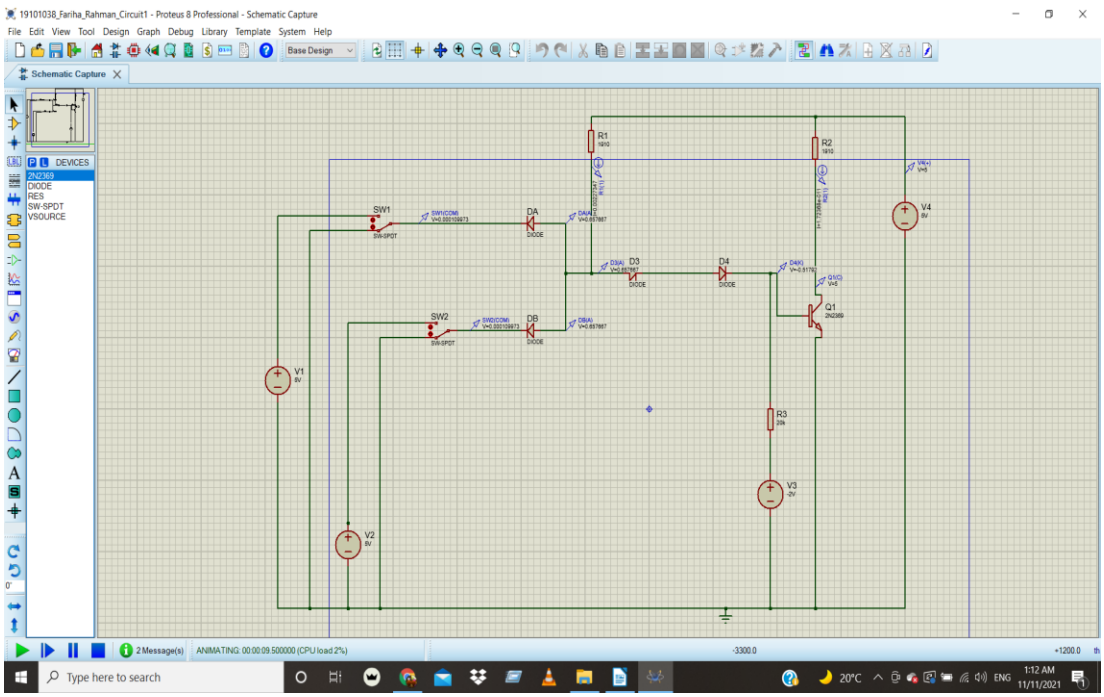
19101038_Fariha_Rahman_Circuit1 - Proteus 8 Professional - Schematic Capture
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Base Design
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FARIHA (19101038)
350 - Lab 2

Nand Gate (Table 1)

Input A	Input B	V_{DA}	V_{DB}	V_p	I_{R_1}	I_{R_2}	V_b	Y
0	0	0.657	0.657	0.657	.002	1.72×10^{-11}	-.517	5
0	1	0.675	-4.33	0.675	.002	1.72×10^{-11}	-.5	5
1	0	-4.33	0.675	0.675	0.002	1.72×10^{-4}	-.5	5
1	1	-2.851	-2.851	2.148	0.001	.002	.817	.095

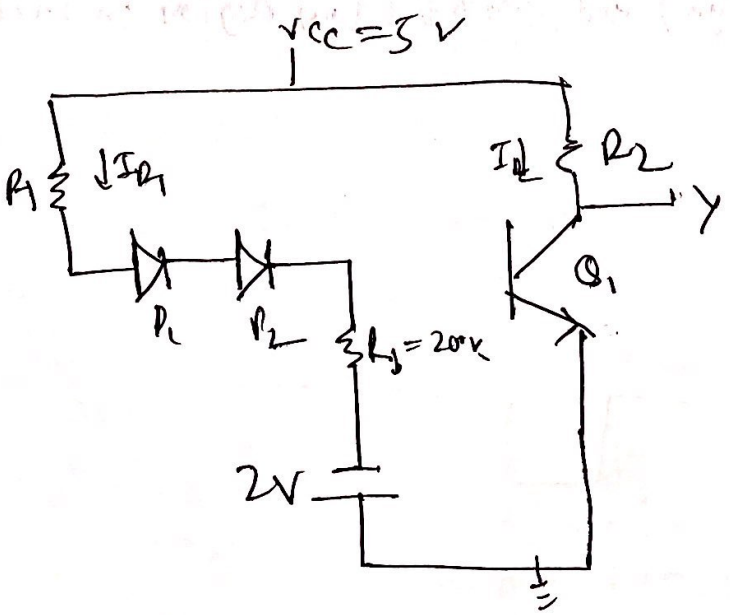
NAND Gate As Inverter (Table 2)

Input A	Input B	V_p	V_b	Y
1	0	.675	-.5	5
1	1	2.148	.817	.095

Report

Answer to the Question No-1

When both of the inputs of the circuit are HIGH then the active part is shown below—



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Ans to the Question No 2

In Table 2, when we set Input A = HIGH and when Input B is LOW, D_A was OFF and diode D_B was turned ON. So, at p node the voltage, vp was approximately 0.7 V. As we know to turn on the Q_1 transistor we have to strike at least 2.1 volt at p node P. But, we did not achive it in this case. Which conclude Q_1 was on Cut off mode and we get 5 / HIGH in the output.

Also, when Input B = HIGH, diode D_A, D_B will be off. So, vp will be approximately 2.1 v. That means the transistor is in saturation mode. When transistor is in saturation mode we get 0.1 / 0.2 v from the collector - emitter junction (close to 0). So, we get 0 / Low from output. This is why ~~An Inverter can be made~~ NAND gate can be used as An Inverter.

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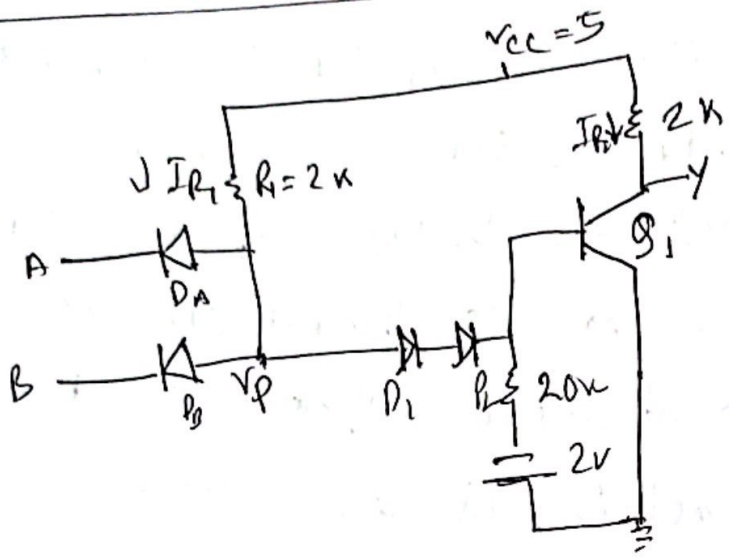
Answer to the Question – 3



When the both inputs are low 0 volt, D_A, D_B will be ON. So, V_p will be approximately 0.7 V which is less than $(.8+.7+.7)V = .22$ volt.
0.8 v is base emitter voltage. 0.7 v is conducting voltage for diode. So, Q_1 will be on Cut off mode. so, no current will pass and the output will be 5V/ High.

: When any of the input B high. Lets consider, A= High and B = low, So, D A = OFF, D_B = ON.
So, V_p ~ 0.7 V which is less than 2V
So, we can say that Q_1 will be in Cut off mode
So, No current will pass and the output will be High / 5V.

Same will happen when A= Low and B= High

Therefore, when both of the inputs are high, then $D_A = D_B = OFF$. So, the I (current) will go through D_1 and D_2 diode and Q1 transistor. So, Q1 will be in Saturation Mode. So, output = Low.

This is how NAND operations are performed

Ans to the question No-4 :

From Proteus simulation, 1 of the input is high then, $V_B = -0.5$ V. So, $V_B = -0.5$ [$V_E = 0$ V] and $V_C = 5$ V. So, $V_E < V_B$ and $V_C > V_B$.

So, Q1 will be cutoff.

Ans. to the Question No-5

When one of the inputs one High which is 5V. We get an output of 5V which is High.

So, the maximum input is 5Volts.