CSE 350

Digital Electronics and Pulse Techniques

Lab Report

Experiment No: 01

Implementing Diode Logic (DL) gates

Submitted by:

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Section - 04

Department - CSE

Fall 2021

BRAC UNIVERSITY

Objective:

1. Construction of DL gates.
2. Understanding the Circuit Operation.

Circuit Diagram:

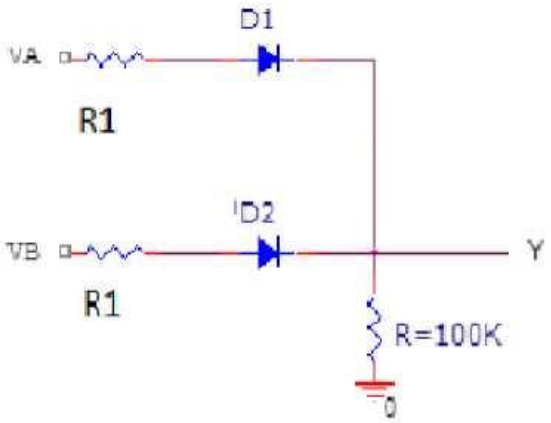


Fig 1: OR gate

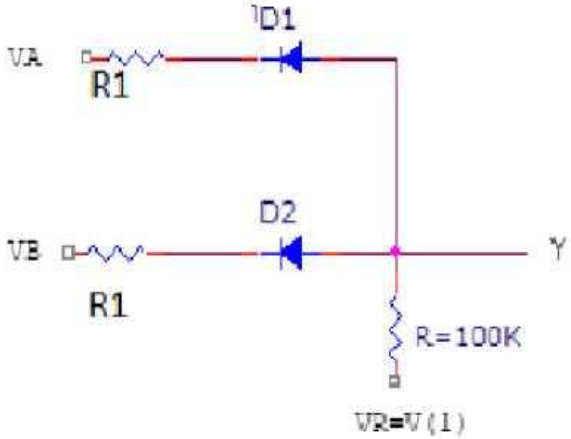


Fig 2: AND gate

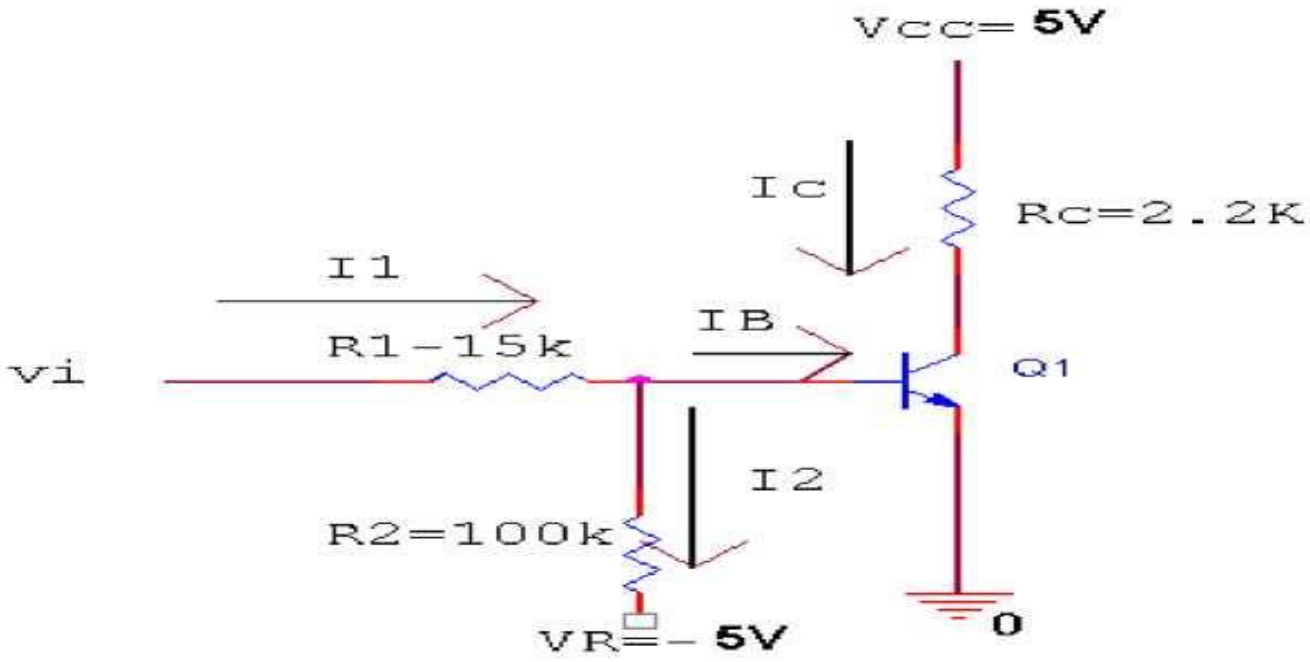
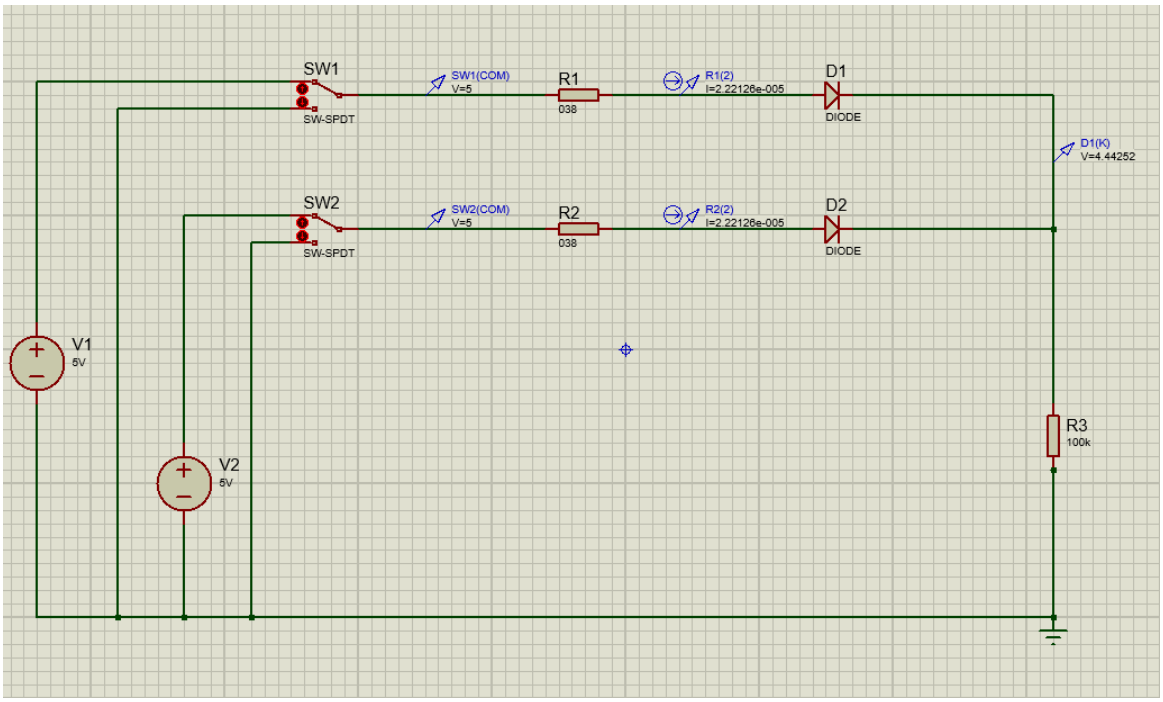
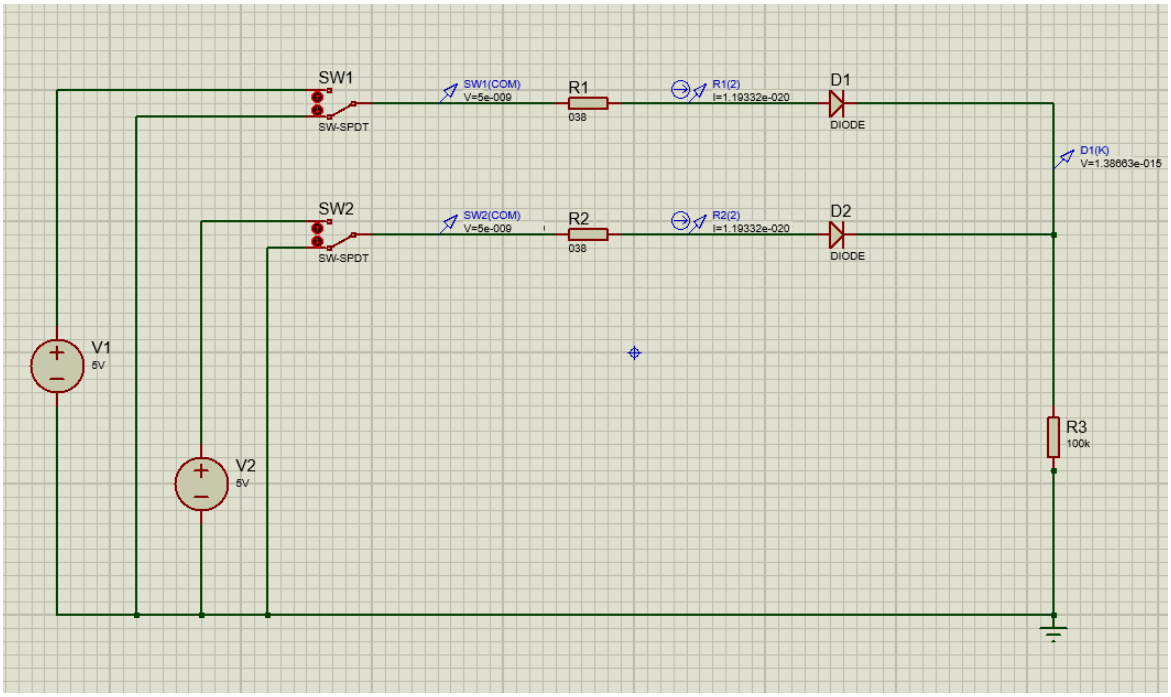


Fig 3: INVERTER for positive logic

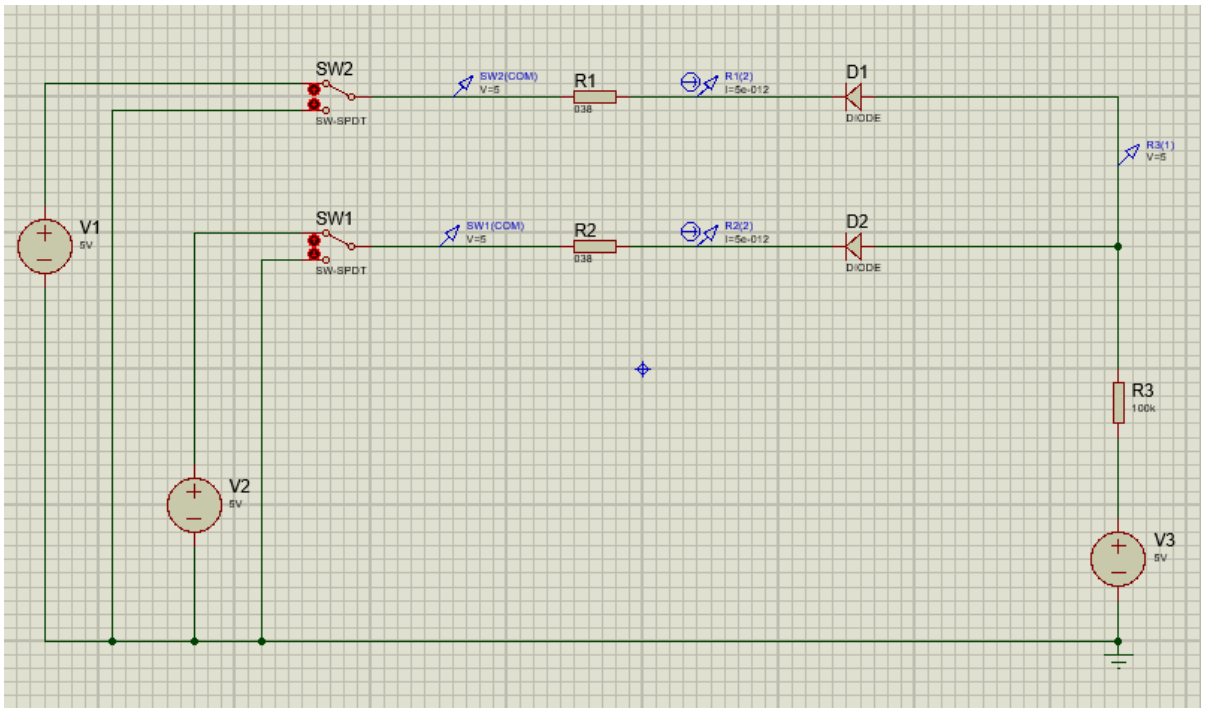
Circuits:

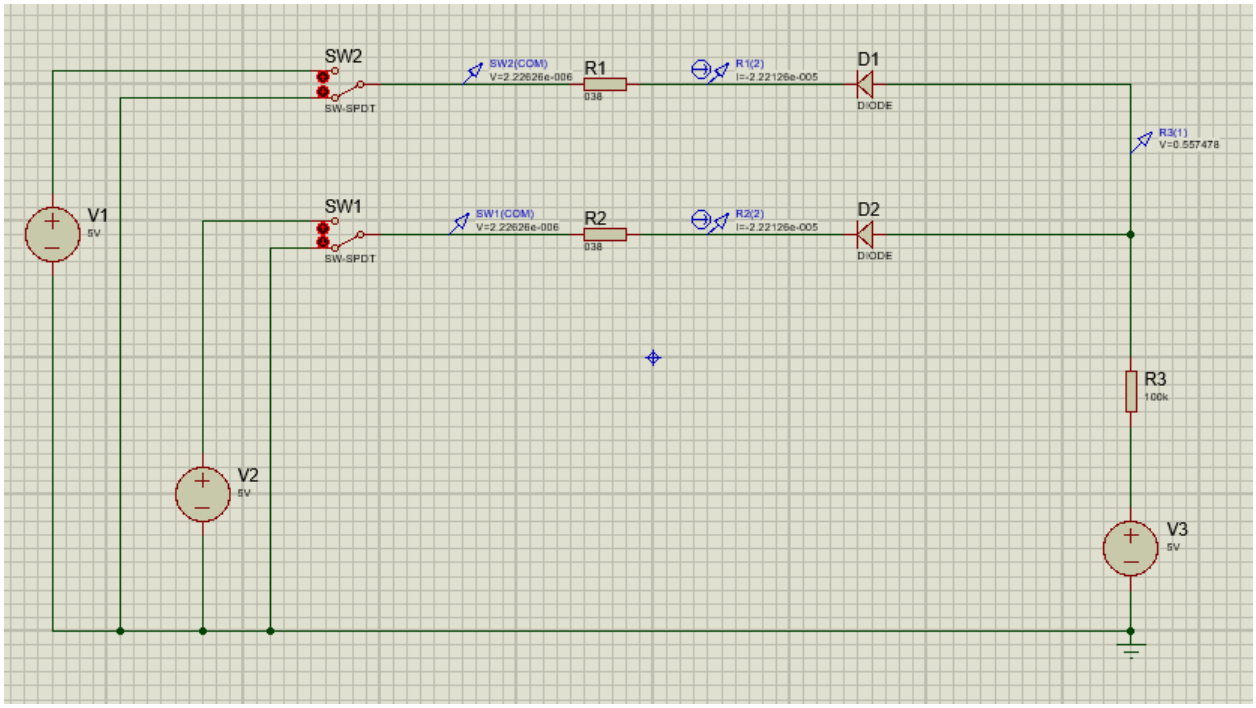
OR GATE



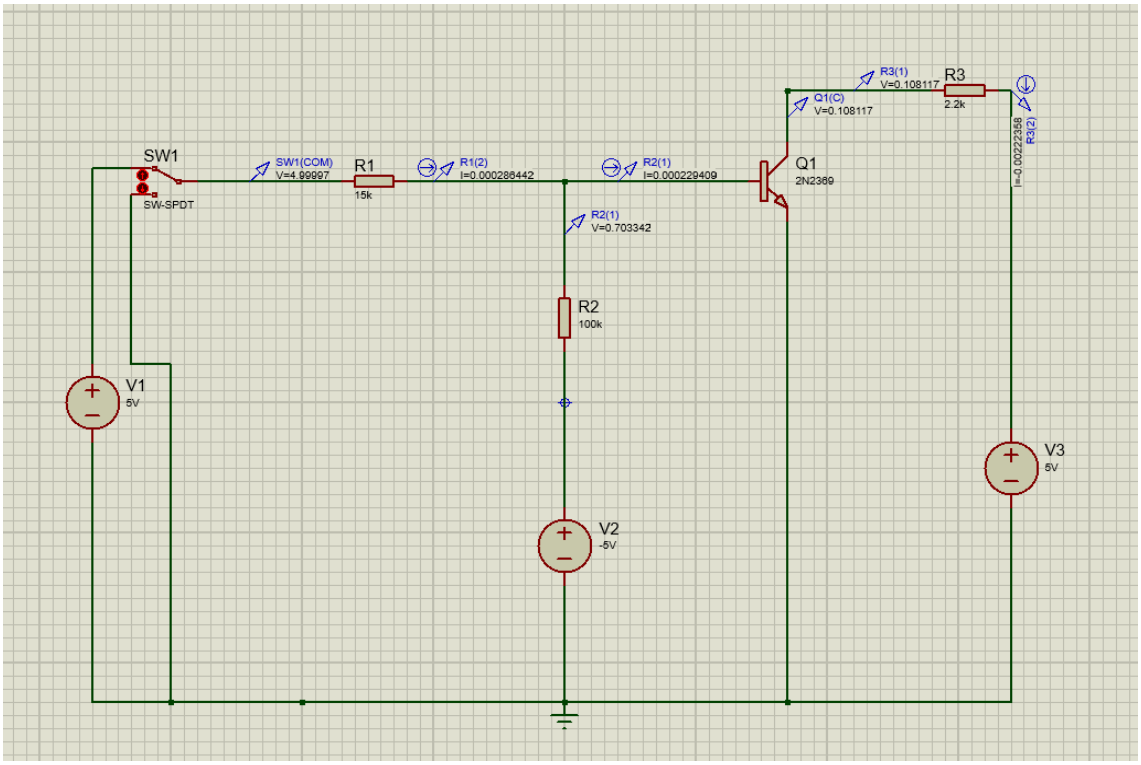


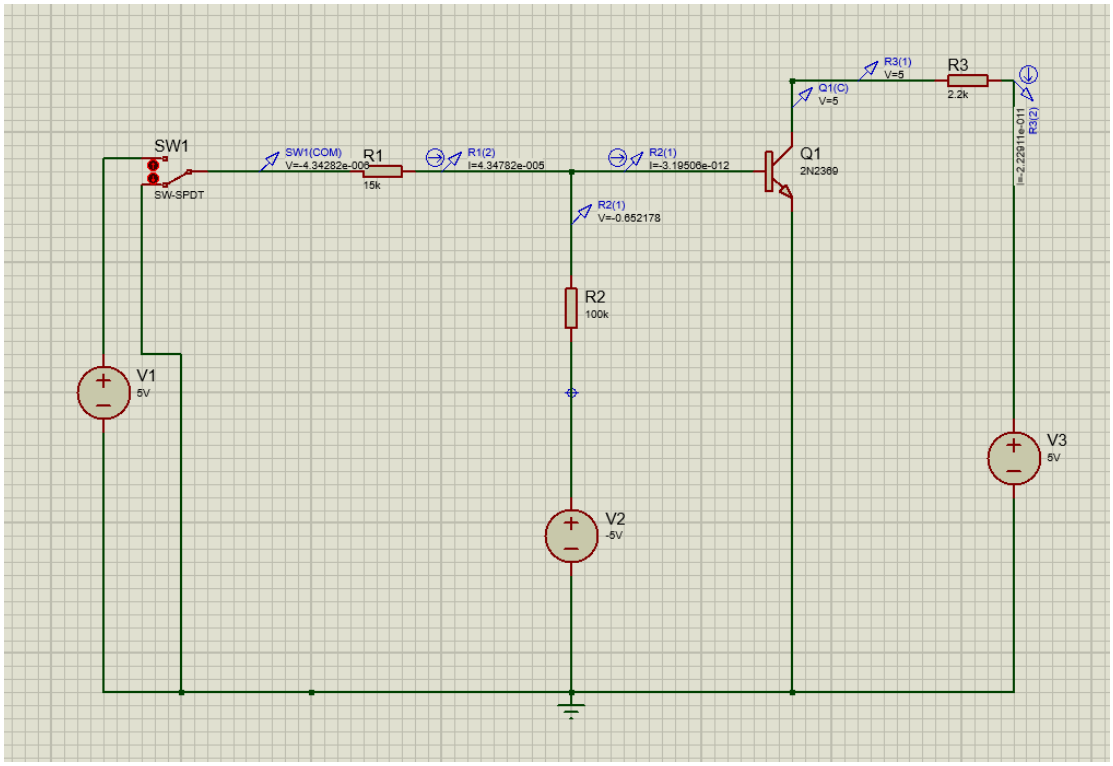
AND GATE


SW2
SW2(COM)
V=5
R1
038
R1(2)
I=5e-012
D1
DIODE
R3(1)
V=5
V1
5V
SW1
SW1(COM)
V=5
R2
038
R2(2)
I=5e-012
D2
DIODE
SW-SPDT
R3
100k
V2
5V
V3
5V


SW2
SW2(COM)
V=2.22626e-006
R1
038
R1(2)
I=-2.22126e-005
D1
DIODE
R3(1)
V=0.557478
V1
5V
SW1
SW1(COM)
V=2.22626e-006
R2
038
R2(2)
I=-2.22126e-005
D2
DIODE
SW-SPDT
R3
100k
V2
5V
V3
5V

INVERTER


SW1
SW-SPDT
SW1(COM)
V=4.99997
R1
15k
R1(2)
I=0.000288442
R2(1)
I=0.000229409
Q1
2N2369
R3(1)
V=0.108117
R3
2.2k
Q1(C)
V=0.108117
R3(2)
I=-0.00222358
R2(1)
V=0.703342
R2
100k
V1
5V
V2
-5V
V3
5V


SW1
SW-SPDT
SW1(COM)
V=-4.34282e-006
R1
15k
R1(2)
I=4.34782e-005
R2(1)
I=-3.19506e-012
Q1
2N2369
R3(1)
V=5
R3
2.2k
Q1(C)
V=5
R3(2)
I=-2.22911e-011
R2(1)
V=-0.652178
R2
100k
V1
5V
V2
-5V
V3
5V

Data Table:

OR Gate:

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	$Y = V_R$
0	0	5×10^{-9}	5×10^{-9}	1.19332×10^{-20}	1.19332×10^{-20}	1.3866×10^{-15}
0	5	5.0004×10^{-9}	0.01	4.43386×10^{-12}	4.4238×10^{-5}	4.42386
5	0	0.01	5.0004×10^{-9}	4.4238×10^{-5}	4.43386×10^{-12}	4.42386
5	5	0.01	0.01	2.221×10^{-5}	2.221×10^{-5}	4.44252

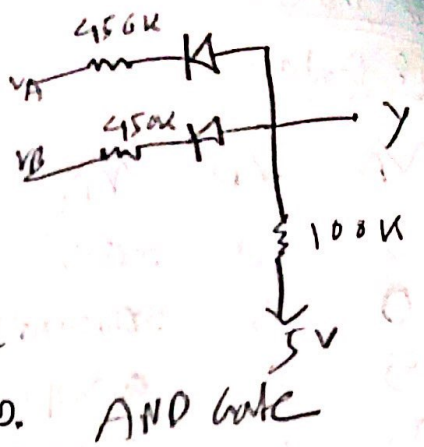
AND GATE:

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	$Y = V_r$
0	0	2.226×10^{-6}	2.26×10^{-6}	2.221×10^{-5}	2.2216×10^{-5}	0.557478
0	5	4.426×10^{-6}	5	4.424×10^{-5}	9.433×10^{-12}	0.576135
5	0	5	4.428×10^{-6}	9.433×10^{-12}	4.423×10^{-5}	0.576136
5	5	5	5	5×10^{-12}	5×10^{-12}	5

Inverter:

V_i	V_{R_1}	V_{R_2}	V_{RC}	I_1	I_2	I_3	I_{RC}	V
0	4.34×10^{-6}	0.652	5	4.34×10^{-5}	4.34×10^{-5}	3.49×10^{-12}	2.229×10^{-11}	5×10^{-11}
5	4.99	0.703	0.104	0.000286	5.1×10^{-5}	0.0002294	$\frac{0.00222}{258}$	0.108817

Report:



AND Gate

(1) When both inputs are 0 (Low), both of the diode will be on forward bias. So, they will conduct current. The output will be closer to zero. When one input high (1) and another low (0) which can make D_1 into reverse bias and D_2 into forward bias. So, it will conduct current. So, therefore, the output will be closer to zero. In another case, if we take one case input as low (1) and another high (1) then the output will also be the same as the previous case. Hence, for the 4th scenario if we take both High (1), then it will make the diodes in reverse bias so, the output will be closer to 5

(2) If $V_A = V_B = 6v$, $V_R = 5v$

OR Gate:

V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	V_R
0	0	0	0	1.43×10^{-20}	1.43×10^{-20}	1.66×10^{-15}
0	6	4.09×10^{-16}	4×10^{-3}	-5.42×10^{-12}	5.42×10^{-9}	5.41619
6	0	4×10^{-3}	4.09×10^{-16}	5.42×10^{-9}	-5.42×10^{-12}	5.41619
6	6	2.07×10^{-3}	2.07×10^{-3}	2.72×10^{-5}	2.72×10^{-5}	5.43603

It is observed that it doesn't change the functionality of the OR gate. It will work as before.

And Gate:

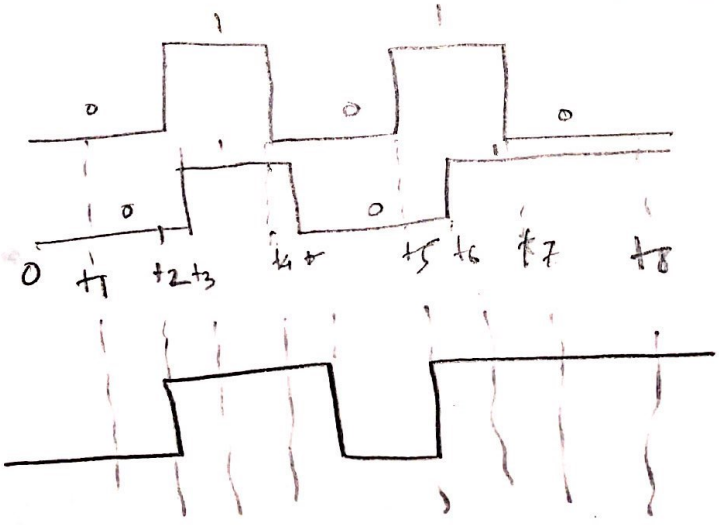
V_A	V_B	V_{R_1}	V_{R_2}	I_{R_1}	I_{R_2}	V_R
0	0	1.68×10^{-3}	1.69×10^{-3}	-2.2×10^{-5}	-2.221×10^{-5}	0.558318
0	6	4.42464	0	-4.42×10^{-5}	1.14×10^{-14}	0.557806
6	0	0	4.42464	1.14×10^{-11}	-4.4×10^{-5}	0.557806
6	6	0	0	7.01×10^{-12}	7.101×10^{-12}	5

It is also doesn't change the functionality so it will work.

(3) The function of $R_L = 100K$ is to control the current value of I_B at the base emitter junction. It fixed the mode of the transistor. ~~The reused emitter~~ save as it prevents excessive current to flow through the base emitter function. So, for this 100K resistance one portion of the I_1 current is going through I_2 and other portion of it is going through the base emitter junction of the transistor.

(4) In the inverter circuit, when input is high (5), $V_{BE} = 0.703$ V which is closer to 0.8. And, $V_{CE} = 0.108$ which is closer to 0. So, we can say that when input is high, the transistor will be operating in saturation mode. However, when input is low(0), $I_B = -3.9 \times 10^{-12}$ mA, $I_C = 1.72 \times 10^{-11}$ mA, $I_E = 5.4 \times 10^{-12}$ which are closer to zero. We know, in Cut-off mode, all current = 0 mA, and $V_B(0.7) > V_E(0)$, $V_B(0.7) > V_C(0.1)$ V when the input is high. So, we can say from our proteus observation that transistor will be operating in Saturation (high) and cut-off (low) region in inverter circuit.

(5)



OR: