BRAC UNIVERSITY

VLSI DESIGN

CSE460

SECTION: 10L

Lab Test 1

Time: 40 minutes (+5 minutes submission time)

Problem 1:
Write down the Verilog HDL code for a 8 to 3 priority encoder with priority: 4>6>5>7>0>2>1>3 and verify the output from the timing diagram.

Problem 2:
Design a **Mealy** type FSM that has one input *w* and one output *z*. The FSM is a sequence detector that produces *z = 1*, if the previous three values of w were *010*, otherwise *z = 0.*

Submission Guidelines:
For each of the problems, copy-paste the codes in a doc, add screenshots (fullscreen) of compilation report and simulation report. Finally, export the doc as pdf and submit it in the following link:
https://docs.google.com/forms/d/e/1FAIpQLScizk4B1oZwd_9c2P9plj-WuQC1FBxY_kfQxdmZTq5h0NUlgQ/viewform?usp=sf_link