VLSI DESIGN
CSE460
SECTION : 10L
Assignment 1 [Lab]
Deadline: 07/03/2022 11:59 pm

Rules:

1. You need to submit the code, the compilation report and the simulation report with a brief description for each of the problems.
2. Prepare your assignment in a doc file. For each of the problems, paste the code in the doc file (Not screenshot, copy-paste the code), add screenshots (full screen) of the compilation and simulation report and give a brief description of how your timing diagrams manifest expected outputs.The explanation can either be typed or scanned. Next, export the doc as pdf and rename it as **ID_LabAssignment1_CSE460.pdf.**
3. Finally, submit the pdf within the deadline.

Problem 1:
Design a 4 to 2 priority encoder (0>1>3>2) using Verilog HDL and verify using timing diagram.

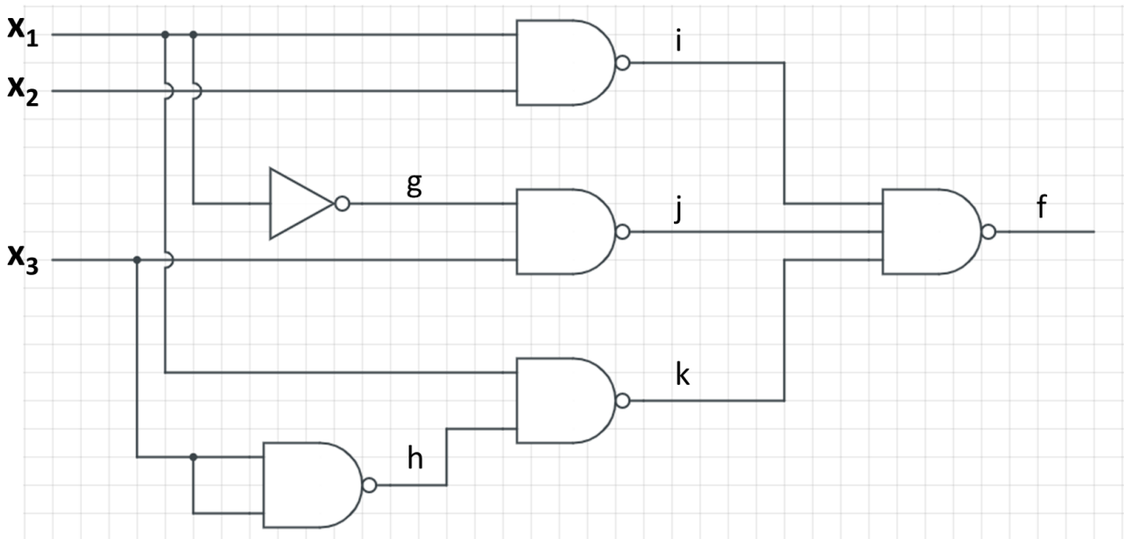
Note:

1. Show and discuss the case when multiple input bits are high.

Problem 2:
Write Verilog code (both in **structural representation** and **procedural representation using case statement**) to realize the following circuit. Verify both the representations using timing diagrams. **Your timing diagrams must include all the possible combinations (eight) of the three inputs (x_1, x_2, & x_3).** You may synchronize the inputs with clocks to keep all the combinations within a suitable simulation end time, as demonstrated in the class. Don't forget to select **'Functional'** as the simulation mode.

Note:

- Derive the expressions for the wires (g, h, I, j, & k) and for the output (f).
- Derive a truth table including only the inputs (x_1, x_2, & x_3) and the output (f).
- From the timing diagram, explain one timestamp where f=0 and another where f=1. Verify these values with your theoretical values calculated from the logic expressions.



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