VLSI DESIGN
CSE460 (Spring 2022)
SECTION : 10L
Assignment 3 [Lab]
Deadline: 25/04/2022 11:59 pm

Rules:

1. You need to submit the code, the compilation report, and the simulation report with a brief description for each of the problems.
2. Rename the project/directory/top-level-design-entity/module for each problem as: **problem#_StudentID** [# = 1/2/4/..]. If not, your submission will not be accepted.
3. Prepare your assignment in a doc file. For each of the problems, add screenshots (full screen) of the circuits, timing diagram and give a brief description of how your timing diagrams manifest expected outputs.The explanation can either be typed or scanned. Next, export the doc as pdf and rename it as **Section_StudentID_assignment3.pdf.** For example: 2_1406066_assignment3.pdf
1. Finally, submit the pdf within the deadline.

Submission link:
https://docs.google.com/forms/d/e/1FAIpQLSd1UxrAKJcbAWBY2rvOq5Tar18fnFv_vmE61-3lka5L2nwEZA/viewform?usp=sf_link

Problem 1

Using DSCH2, design a 4 bit Serial In Serial Out (SISO) shift register using 1 bit positive edge triggered D flip-flops. You may use blocks/sub-circuits made using CMOS technology but **cannot use readily available logic gates.**

Clock frequency: 100 Hz.

D_in: 80 Hz

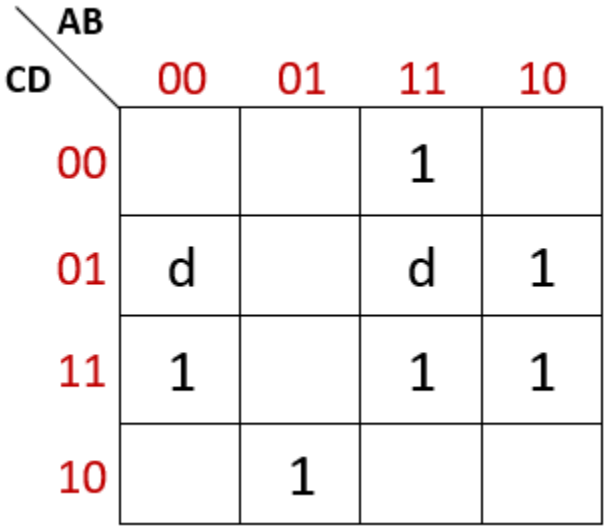
Your report must include the following

1. Full-screen screenshots of all the hierarchical blocks (CMOS NAND gate, D Latch, D flip flop and Shift register). Adjust the zoom level appropriately so that the blocks are clearly visible.
2. Timing diagram of 4 bit Shift register. Show all the input and outputs (D_in, Q0, Q1, Q2, and Q3)

Please turn over

Problem 2

Derive the Boolean logic expression from the following K-Map and implement the logic function in DSCH2 using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but **cannot use readily available logic gates.**



CD \ AB	00	01	11	10
00			1	
01	d		d	1
11	1		1	1
10		1		

Your report must include the following

1. Full-screen screenshots of all the hierarchical blocks/circuits (CMOS NAND/NOT/AND/OR gate and final schematic). Adjust the zoom level appropriately so that the blocks are clearly visible.
2. Simulated timing diagram with verification discussion for any two timestamps where f = 0 and f = 1.