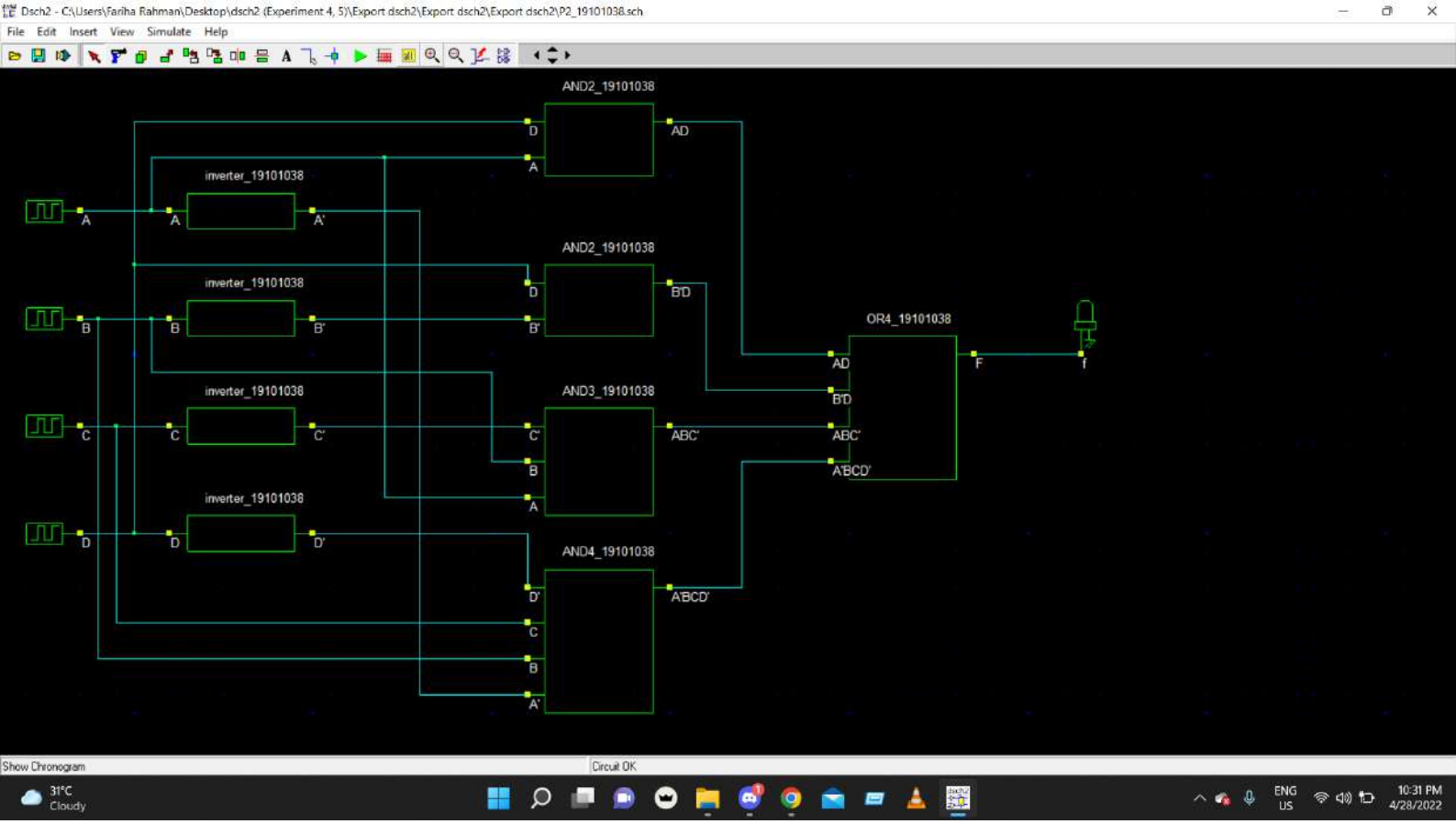
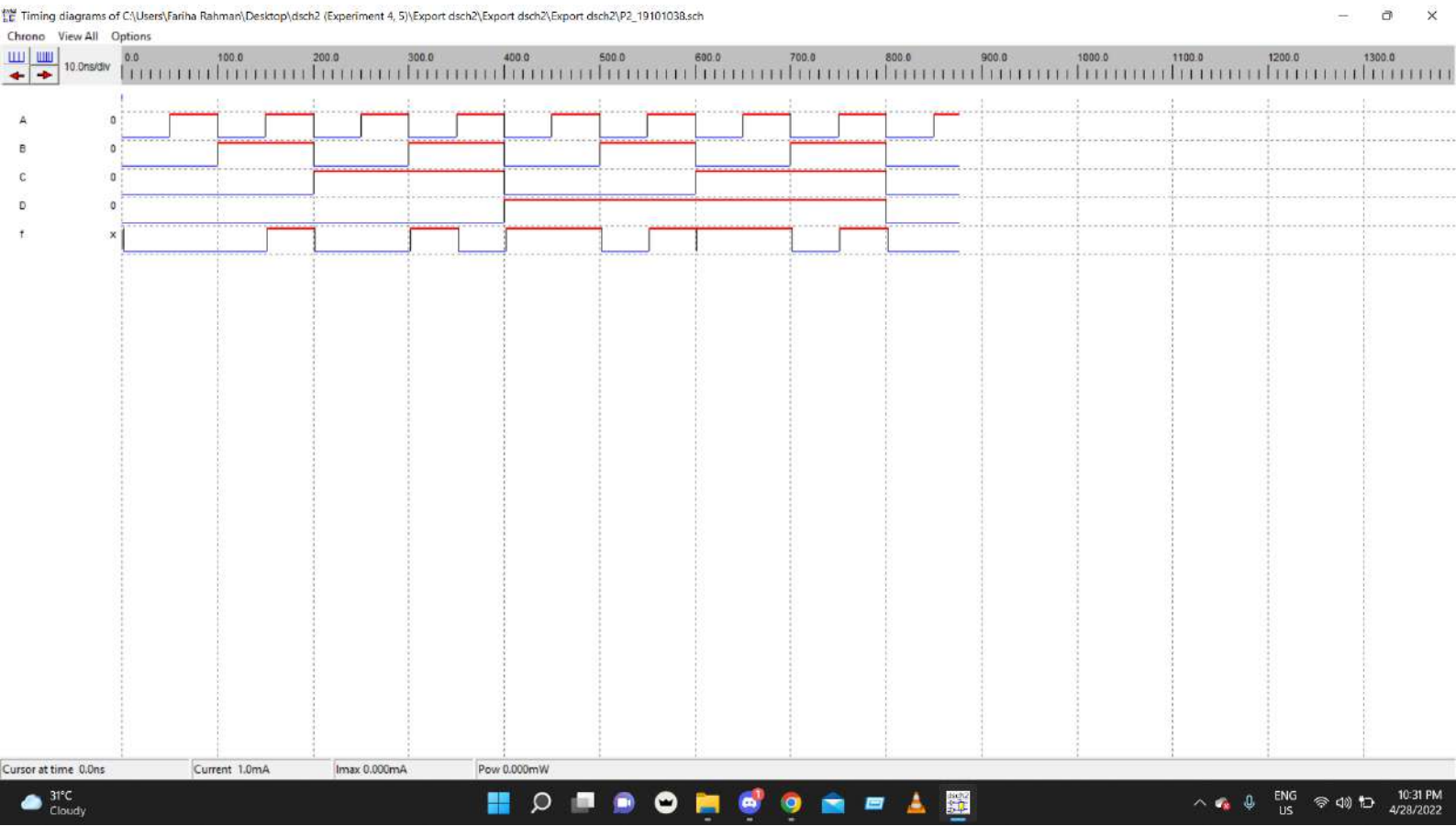
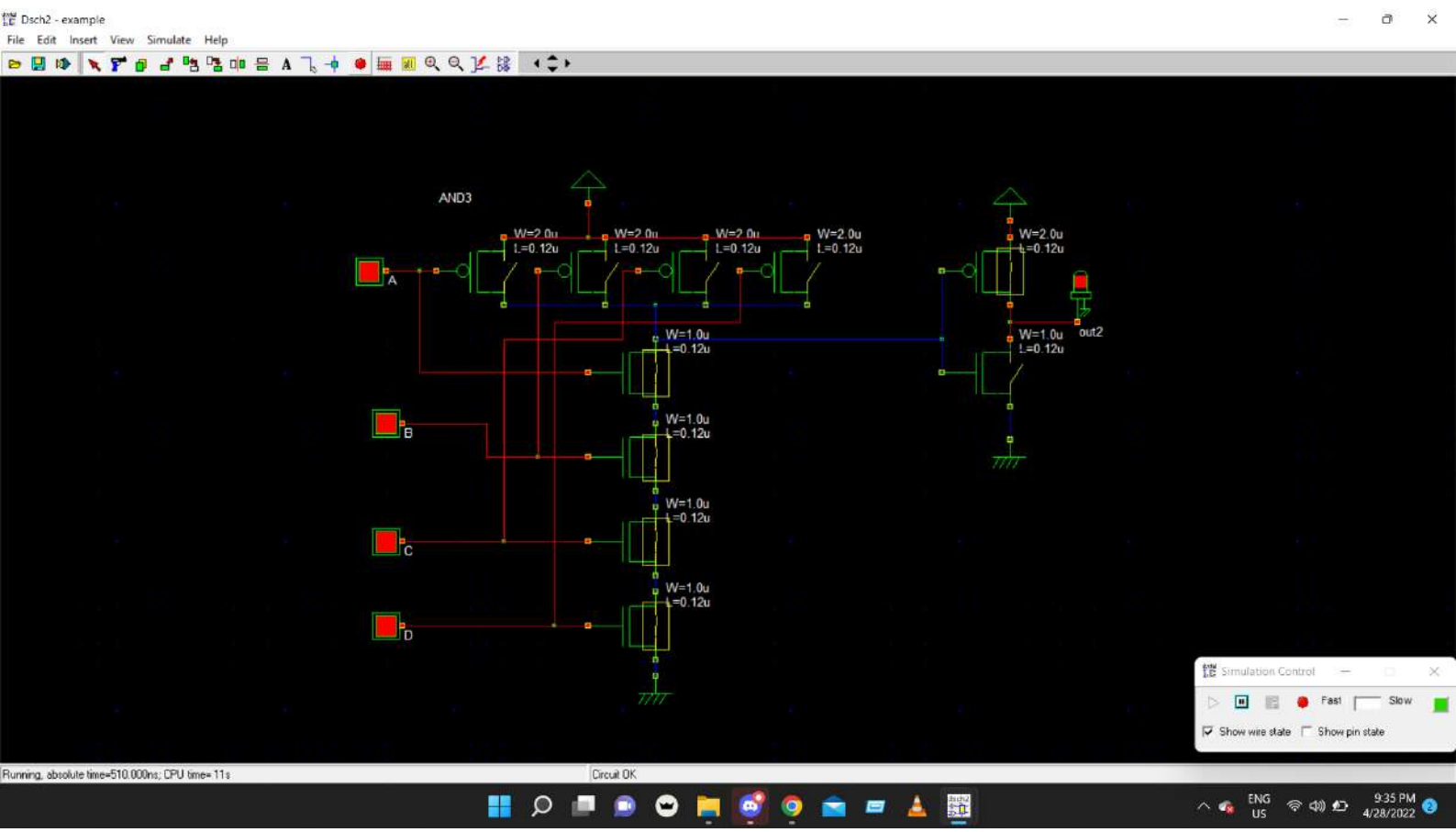
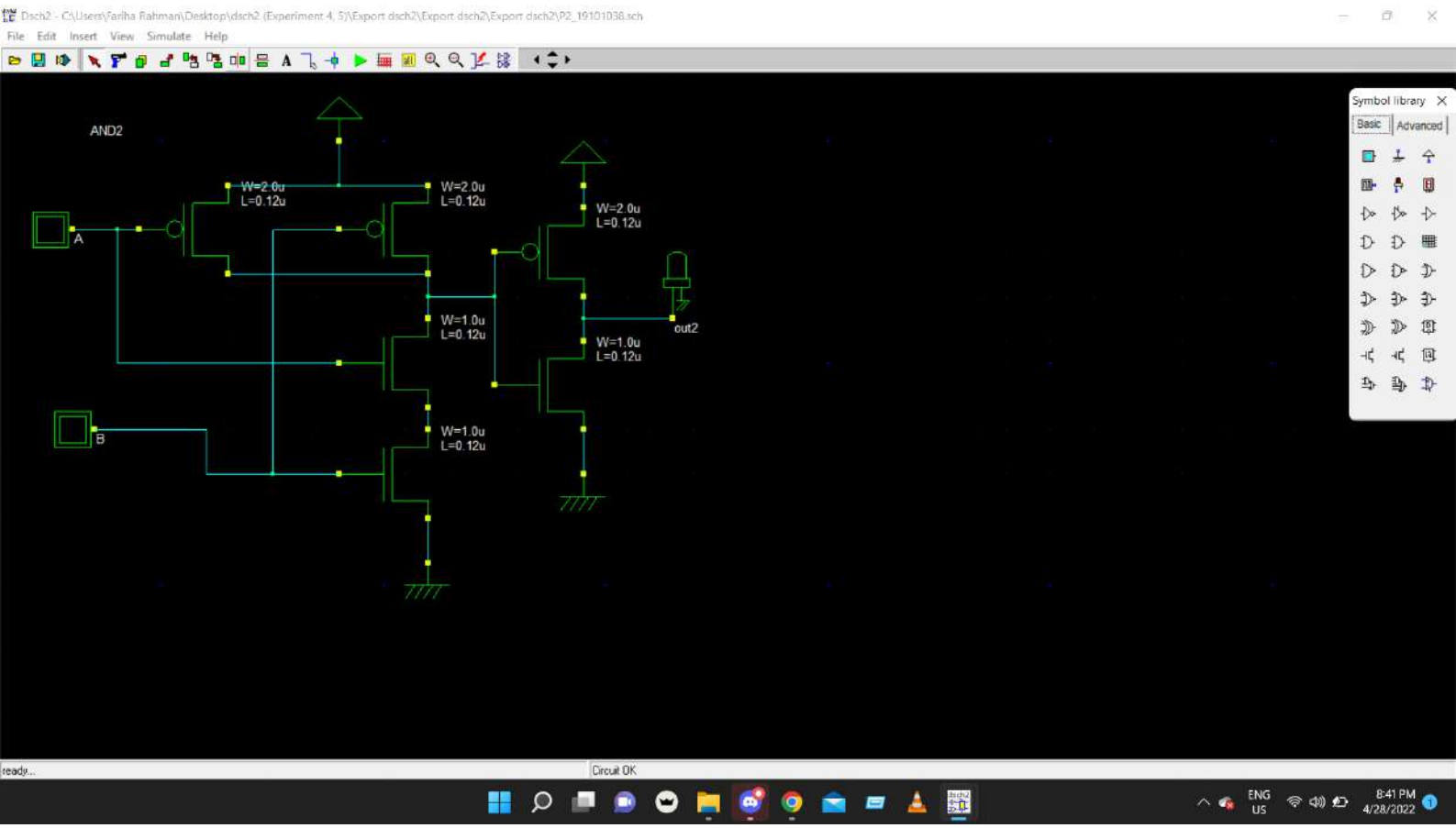
Fariha Rahman
ID: 19101038
Section 10
Lab Assignment 3

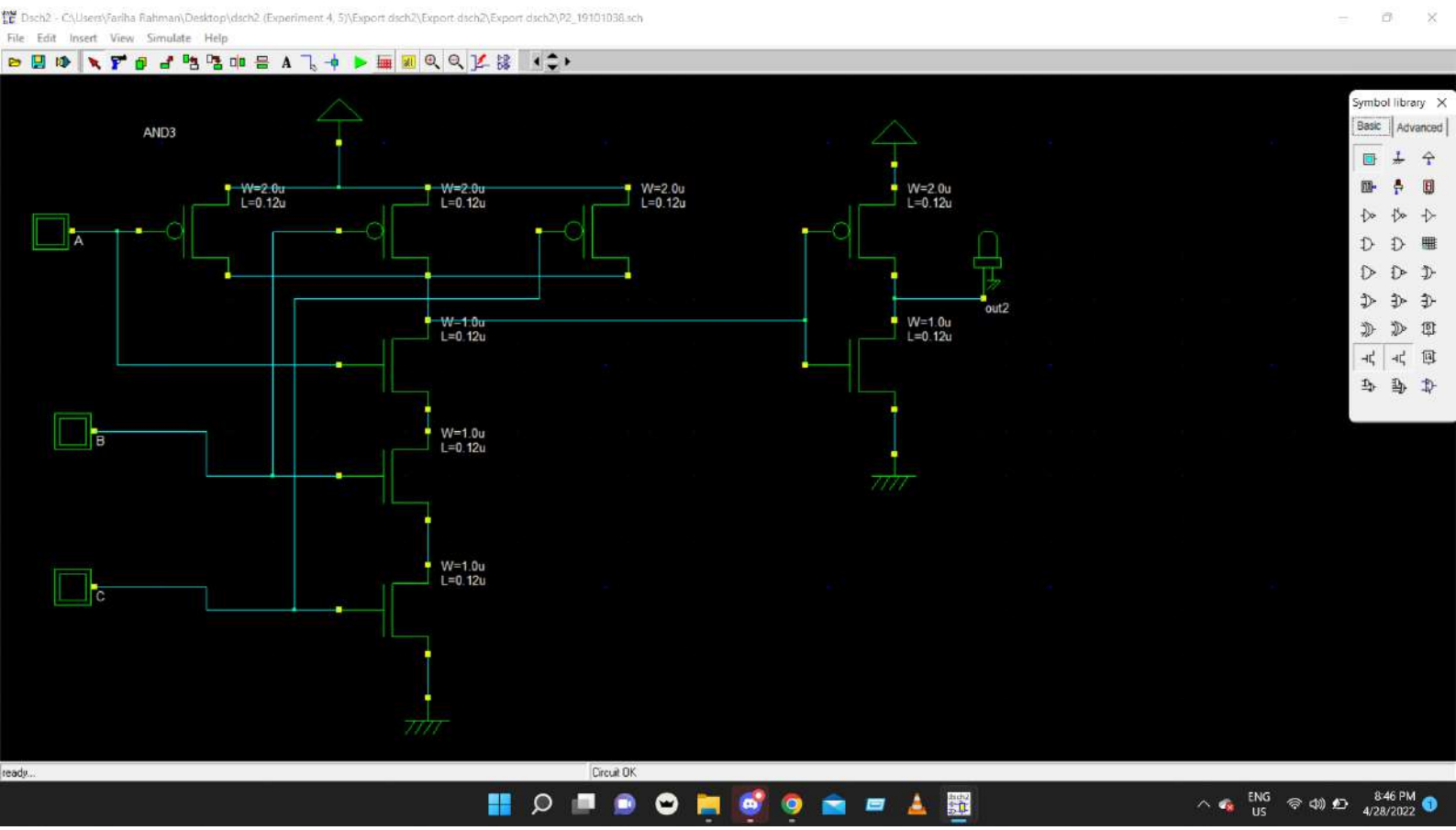
Problem 2

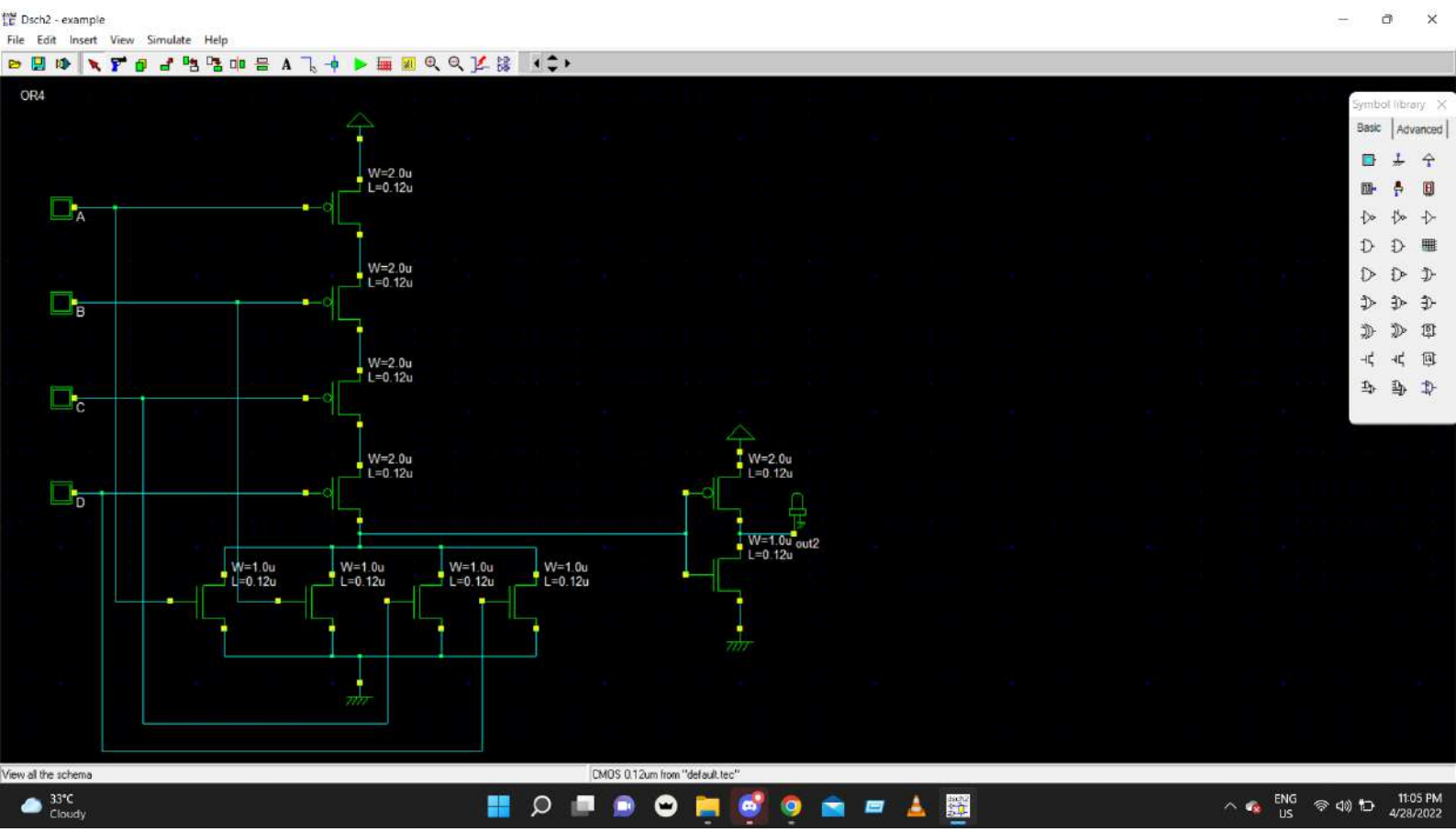





Dsch2 - example
File Edit Insert View Simulate Help
AND3
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
W=1.0u
L=0.12u
B
W=1.0u
L=0.12u
C
W=1.0u
L=0.12u
D
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
out2
Simulation Control
Fast
Slow
Show wire state
Show pin state
Running, absolute time=510.000ns; CPU time= 11s
Circuit OK
ENG
US
9:35 PM
4/28/2022


Dsch2 - C:\Users\Fariha Rahman\Desktop\dsch2 (Experiment 4, 5)\Export dsch2\Export dsch2\Export dsch2\P2_19101038.sch
File Edit Insert View Simulate Help
AND2
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
W=1.0u
L=0.12u
out2
W=1.0u
L=0.12u
B
W=1.0u
L=0.12u
Symbol library
Basic
Advanced
ready...
Circuit OK
ENG
US
8:41 PM
4/28/2022


Dsch2 - C:\Users\Fariha Rahman\Desktop\dsch2 (Experiment 4, 5)\Export dsch2\Export dsch2\Export dsch2\P2_19101038.sch
File Edit Insert View Simulate Help
AND3
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
W=1.0u
L=0.12u
B
W=1.0u
L=0.12u
C
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
out2
Symbol library
Basic
Advanced
ready...
Circuit OK
ENG
US
8:46 PM
4/28/2022


Dsch2 - example
File Edit Insert View Simulate Help
OR4
A
B
C
D
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u out2
L=0.12u
Symbol library
Basic
Advanced
View all the schema
CMOS 0.12um from "default.tec"
33°C
Cloudy
ENG
US
11:05 PM
4/28/2022

FARIHA RAHMAN
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SECTION:10

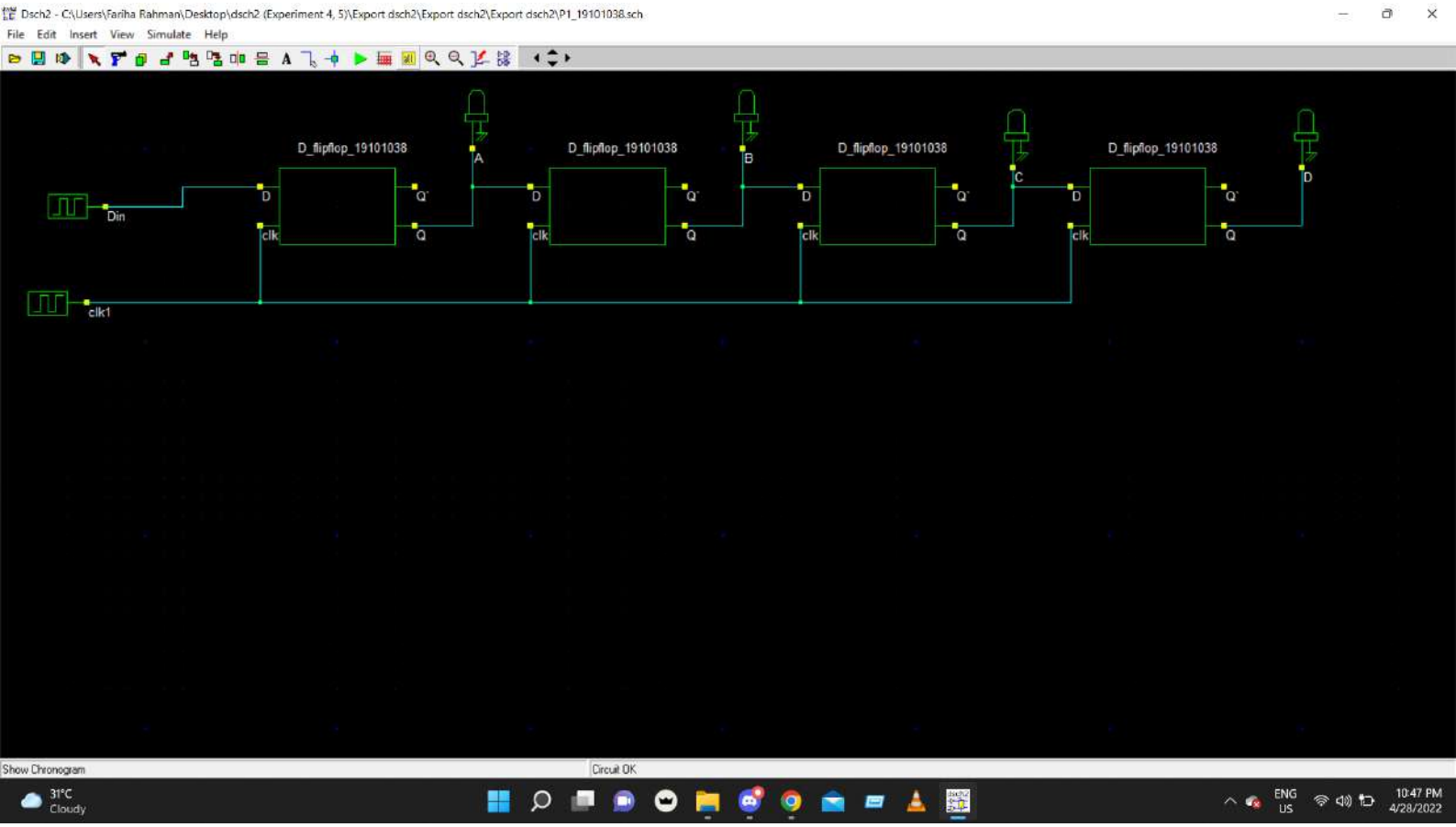
PROBLEM2:

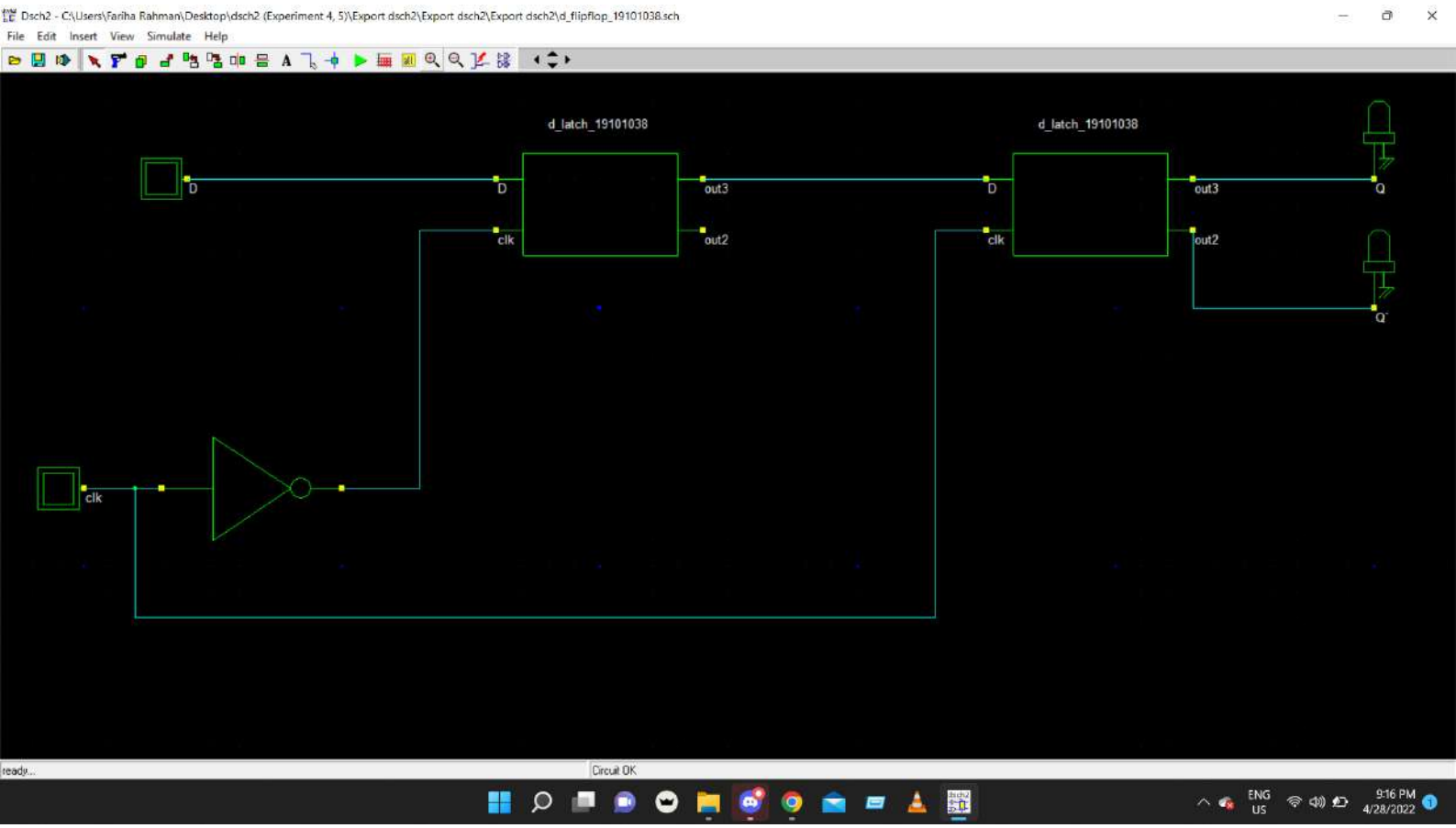
From these groups we get the expression,
Y=A'BCD'+AD+B'D+ABC'

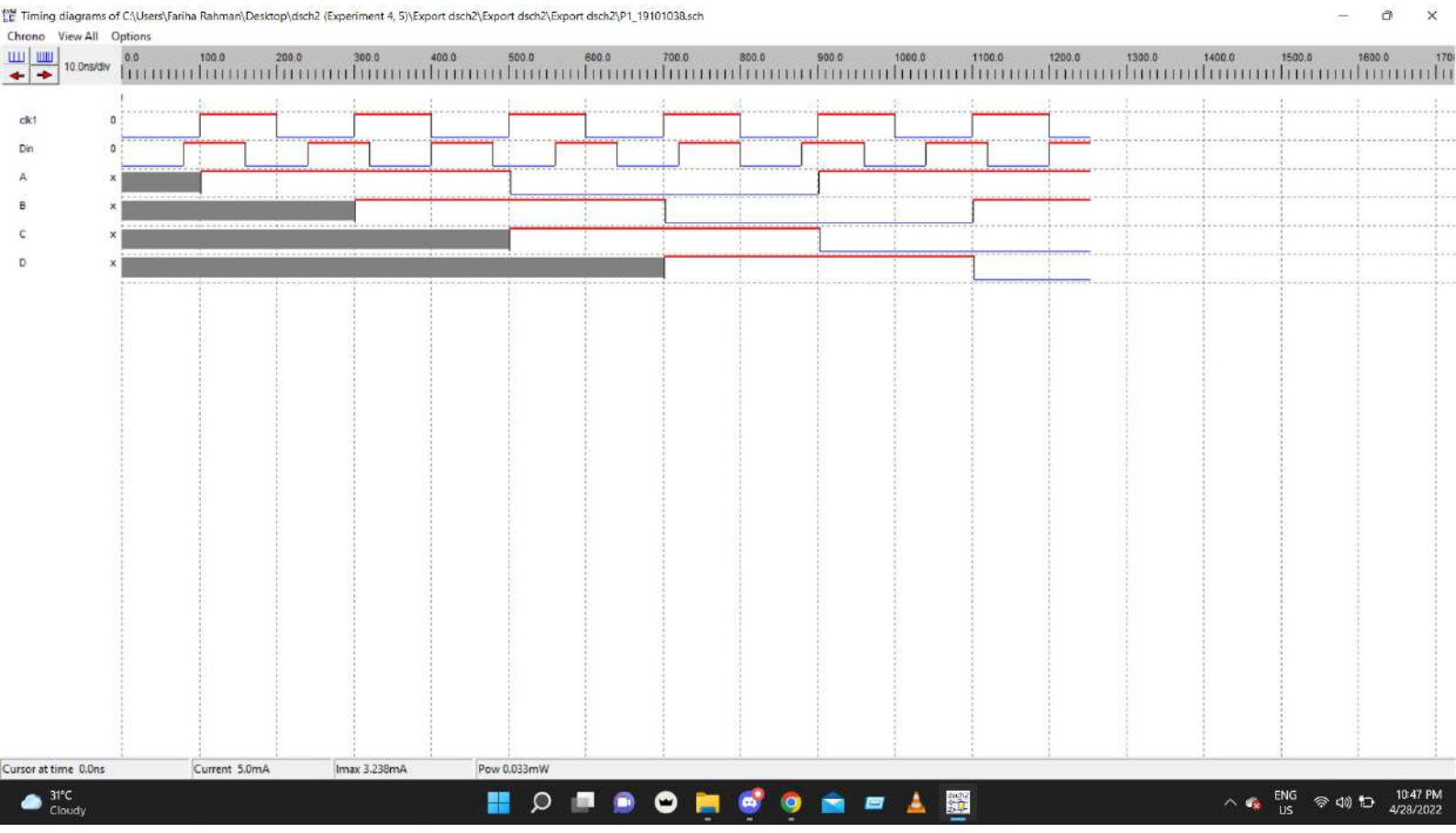
Now from the timing diagram, lets choose two timestamp that is t=150ns where output Y=1 and t=200ns where Y=0 for the explanation.

At t=150ns from timing diagram A=1, B=1, C=0, D=0 and Y=1. In this case we see from the K-map at position CDAB=0011, the cell value is 1. That means here we have an output high.
Now from logic function,
Y=A'BCD'+AD+B'D+ABC'=1
So, both the logic expression's value and timing diagram value are matched for Y=1 case.
At t=200ns from timing diagram A=0, B=0, C=1, D=0 and Y=0. In this case we see from the K-map at position CDAB=1000, the cell value is 0. That means here we have an output low.
Now from logic expression,
Y=A'BCD'+AD+B'D+ABC' =0
So, both the logic expression's value and timing diagram value are matched for Y=0 case also.

Problem 1


Dsch2 - C:\Users\Farlha Rahman\Desktop\dsch2 (Experiment 4, 5)\Export dsch2\Export dsch2\Export dsch2\P1_19101038.sch
File Edit Insert View Simulate Help
D_flipflop_19101038
D_flipflop_19101038
D_flipflop_19101038
D_flipflop_19101038
A
B
C
D
Din
clk1
D
clk
Q
Q'
Show Chronogram
Circuit OK
31°C
Cloudy
ENG
US
10:47 PM
4/28/2022


Dsch2 - C:\Users\Fariha Rahman\Desktop\dsch2 (Experiment 4, 5)\Export dsch2\Export dsch2\Export dsch2\d_flipflop_19101038.sch
File Edit Insert View Simulate Help
d_latch_19101038
d_latch_19101038
D
D
clk
out3
out2
D
clk
out3
out2
Q
Q'
clk
ready...
Circuit OK
ENG
US
9:16 PM
4/28/2022


Timing diagrams of C:\Users\Fariha Rahman\Desktop\dsch2 (Experiment 4, 5)\Export dsch2\Export dsch2\Export dsch2\P1_19101038.sch
Chrono
View All
Options
10.0ns/div
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
900.0
1000.0
1100.0
1200.0
1300.0
1400.0
1500.0
1600.0
clk1
Din
A
B
C
D
Cursor at time 0.0ns
Current 5.0mA
Imax 3.238mA
Pow 0.033mW
31°C
Cloudy
ENG
US
10:47 PM
4/28/2022