BRAC UNIVERSITY

VLSI DESIGN

CSE460

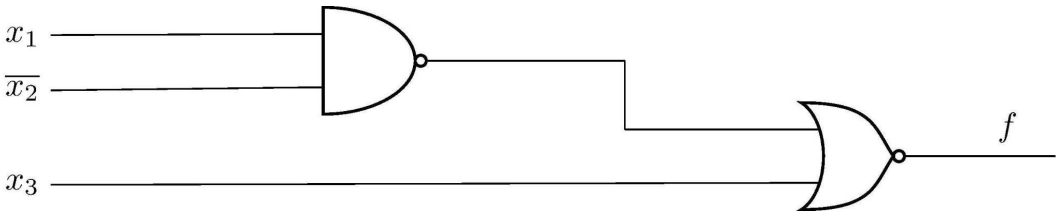
SECTION: 10L

Lab Test 2

Time: 40 mins (+5 mins submission time)

Problem 1:

Design CMOS implementation of the following circuit in dsch2. You **cannot** use readily available gates. **Do not use sub-circuits**. Add full-screen ss of design and output in the submission pdf.



Problem 2:

Design the layout of the following function in Microwind, and demonstrate the output by selecting proper input clock signals (A, B, C, D). Use the **"Design Rule Check"** function to ensure that your layout has no design rule error.

$$F = \overline{(A + B + C + D)}$$

Note: You cannot use Verilog code to implement the function. You may use **"MOS Generator"** in microwind to facilitate your layout workflow.

Submission Link:
https://docs.google.com/forms/d/e/1FAIpQLSflZtSUlm6G_XWnOPrX4rkPenrY6iQn9vi9n7h80NSyHWtt2g/viewform?usp=sf_link