CSCE-312 | Summer 2019

GRADING SHEET

Project 3: Sequential Chips

Demo Date: Bring this Grading document to your next lab for Demo. No make-up unless university-excused.

Grading

(A) Project Submission [100%]: **Friday, 07/19**

You will be graded for correctness of the chips (hdl) you have designed and coded. All your HDL codes will be run using Nand2tetris software (Hardware Simulator) by the TA.. The same simulator you would have used to check your chips in the project. So, make sure to test and verify your codes before finally submitting on eCampus.

Full Name: Jorge Farinacci **UIN:** 125008668 **Section:** 701

Any assignment turned in without a fully completed cover page will NOT BE GRADED.
Please list all below all sources (people, books, web pages, etc) consulted regarding this assignment:

CSCE 312 Students	Other People	Printed Material	Web Material (URL)	Other
1.	1.	1.	1.	1.
2.	2.	2.	2.	2.
3.	3.	3.	3.	3.
4.	4.	4.	4.	4.
5.	5.	5.	5.	5.

Please consult the Aggie Honor System Office for additional information regarding academic misconduct – it is your responsibility to understand what constitutes academic misconduct and to ensure that you do not commit it.

I certify that I have listed above all the sources that I consulted regarding this assignment, and that I have not received nor given any assistance that is contrary to the letter or the spirit of the collaboration guidelines for this assignment.

eCampus Submission Date: 7/19/2019

Printed Name (in lieu of a signature): Jorge Farinacci

The points division for all the chips are listed in the table below:

Category	Chip	Working?
A	Bit	_____/ 5
	Register	_____/ 5
B	RAM8	_____/ 15
	RAM64	_____/ 10
	RAM512	_____/ 10
C	RAM4K	_____/ 15
	RAM16K	_____/ 15
D	PC	_____/ 25