A Temperature Detector with Process Compensation and Non-linear Calibration for Battery Management Systems with HV ESD Protection

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***Abstract*—This paper presents a temperature detector with process compensation and non-linear calibration for battery management systems (BMS) with HV ESD protection. The proposed temperature detector attains process compensation and calibration by using the proposed CTAT and PTAT sensors. The proposed temperature detector must be protected using HV ESD protection in BMS. The proposed temperature detector is implemented using a typical 0.25 μm 1P3M 60V BCD process. The core area of the proposed design is 0.1 mm^2. In the range from -40 ^{o}C to 140 ^{o}C, the worst deviation of the temperature detector is -2.16 ^{o}C $\sim$ +1.98 ^{o}C at FF, TT, and SS corners. The maximum non-linearity reduction of CTAT and PTAT sensors are 9% and 41%, respectively.**

***Index Terms*—non-linear calibration, process compensation, PTAT sensor, CTAT sensor, temperature detector, BMS, ESD.**

I. Introduction

Nowadays, electrical vehicle (EV) is considered as a possible solution to replace conventional fossil-energy-powered vehicles in the future. Battery modules are the major electrical energy storage device in the EV. Due to the demand of safety and reliability, the EV battery modules must be protected, and properly managed [1]. For instance, FlexRay has become a widely used car electronics standard which might be used to co-operate with battery modules in the EV [2], where the operating temperature range is from -40 ^{o}C to 125 ^{o}C, while the ESD protection is required to be over 4 KV, as shown in Table I. Besides the temperature and ESD, the state of charge (SOC) and state of health (SOH) of EV battery modules are basics to monitor the status of EV BMS. Thus, reliable temperature detectors are needed in EV BMS, as shown in Fig. 1.

The temperature detector must be designed to resist the process variation, which particularly affects the accuracy when the nanometer CMOS technology is used to realize the design [3]. However, most of the prior temperature detectors did not consider process variation effect [4]-[6]. Although Jeong *et al*. has proposed a method to cancel the process offset by applying the same circuit architecture to realize temperature sensors [3], the temperature range was not wide enough to meet certain car electronics specifications, e.g., FlexRay, which is up to -40 ^{o}C $\sim$ 125 ^{o}C [3]-[8]. Meanwhile, most of the prior temperature detectors also did not consider the body effect of the temperature sensor, which introduces serious offsets at very low and high temperatures [3]-[8].

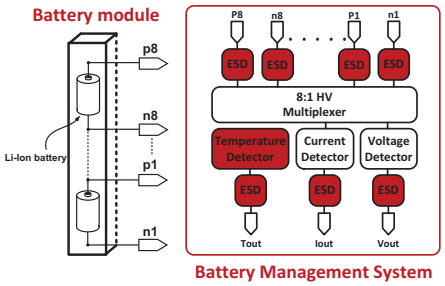

Fig. 1. Simplified diagram of a BMS [1].

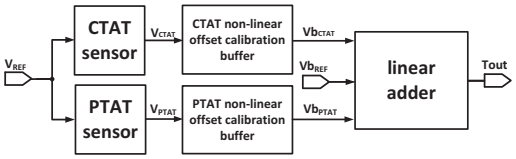

Fig. 2. The block diagram of the proposed temperature detector.

In this study, we propose a temperature detector with process compensation and non-linear calibration for BMS with HV ESD protection. The proposed temperature detector attains process compensation and calibration by using the proposed CTAT and PTAT sensors. In this work, the temperature range sensed by the temperature detector is -40 ^{o}C $\sim$ 140 ^{o}C. The worst deviation of the temperature detector is -2.16 ^{o}C $\sim$ +1.98 ^{o}C at FF, TT, and SS corners. Notably, the maximum non-linearity reduction of the CTAT and PTAT sensors are 9% and 41%, respectively.

II. Temperature Detector

Fig. 2 shows the block diagram of the proposed temperature detector, which is composed of 5 major blocks, i.e., PTAT sensor, CTAT sensor, CTAT non-linear offset calibration buffer, PTAT non-linear offset calibration buffer, and linear adder. The output voltages of CTAT and PTAT sensors using the

TABLE I
FLEXRAY ELECTRICAL PHYSICAL LAYER SPECIFICATION

	Min	Max
Ambient temperature	-40 °C	125 °C
uESD$_{Ext}$ (ESD protection on pins that lead to ECU external terminals)	4 KV	N/A
uESD$_{Int}$ (ESD on all other pins)	2 KV	N/A

same circuit attain reciprocal characteristics vs. FF, TT, and SS corners [3]. Thus, the process compensation method in this paper is to raise the output voltages of CTAT and PTAT sensors to cancel process offsets. The proposed linear adder to carry out the summation of the voltages attains a temperature compensation feature by combining resistors made with different materials. Notably, the CTAT and PTAT non-linear offset calibration buffers are used to calibrate body effect of the CTAT and PTAT sensors. The details of these function blocks are given in the following text.

A. CTAT & PTAT sensors

Fig. 3 (a) and (b) show the schematics of the proposed CTAT and PTAT sensors, respectively. The linearity of CTAT and PTAT sensors will be improved by using series MOSs provided that Vths of MN2 and MN5 are equal to those of MN3 and MN4, respectively [6]. In fact, the proposed CTAT and PTAT sensors have very serious body effect.

According to [6], Vthn0 is the zero-bias threshold voltage,

$$\mathrm{Vthn0} = \mathrm{V_{FB}} - 2\mathrm{Vfn} + \frac{\mathrm{Q'_{bo}}}{\mathrm{C_{ox}}} \tag{1}$$

where $\mathrm{V_{FB}}$ is the flatband voltage, $\mathrm{Q'_{bo}}$ is the negative charge under the gate oxide, Vfn is the bulk surface potential, and $\mathrm{C_{ox}}$ is oxide capacitance. Referring to [6], Vthn of MOS with body effect will drift depending on Vthn0 and the variation of Vbs, which is the voltage difference between bulk (= GND) and source voltage of MOS.

$$\mathrm{Vthn} = \mathrm{Vthn0} + \gamma_\mathrm{p}(\sqrt{2|\mathrm{Vfn}| + \mathrm{Vbs}} - \sqrt{2|\mathrm{Vfn}|}) \tag{2}$$

where γ_p can be written as $\gamma_\mathrm{p} = \frac{\sqrt{2q\varepsilon_s N_A}}{\mathrm{C_{ox}}}$, q is electronic charge, ε_s is silicon dielectric constant, γ_p is the body effect coefficient, Vbs is the voltage difference between bulk and source of MOS, and N_A is doping concentration. N_A will be changed by the mobility of q, which is related to temperature. Notably, the Vthn and Vthn0 are drastically deviated at very low or high temperatures. Fig. 4 (a) and (b) are the output voltage plots of the CTAT and PTAT sensors, respectively, which show an important issue. That is, the deviation of the real output voltage from the ideal voltage is very large at both high and low temperatures, namely non-linear offsets. Thus, the proposed CTAT and PTAT sensors have to calibrate the body effect of the MOSs.

B. CTAT & PTAT non-linear offset calibration buffers

Fig. 5 (a) and (b) show the schematics of the proposed CTAT and PTAT non-linear offset calibration buffers, respectively. The proposed buffers have the same circuitry, which is basically composed of an OPA, a silicide resistor, and a polysilicon resistor. As addressed previously, the output voltages of CTAT

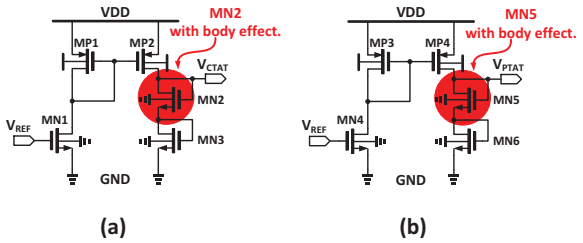

Fig. 3. Schematics of (a) CTAT sensor ; and (b) PTAT sensor.

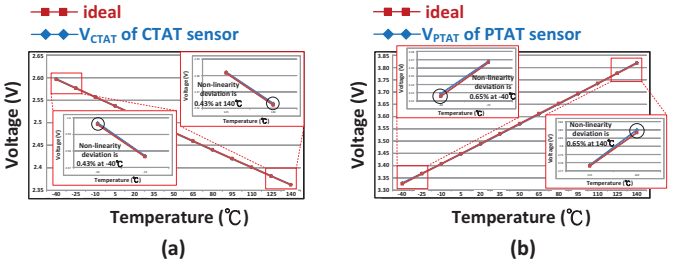

Fig. 4. Simulation waveforms of (a) CTAT sensor and (b) PTAT sensor.

and PTAT sensors show a significant non-linearity at very low and high temperatures. That is, the non-linearity deviations of CTAT and PTAT sensors are relatively symmetrical with respect to the middle of the temperature range. Thus, polysilicon resistor is used to provide calibrated currents, namely $\mathrm{I_{R2}}$ and $\mathrm{I_{R4}}$. Meanwhile, the silicide resistor is used to calibrate the deviations of $\mathrm{V_{CTAT}}$ and $\mathrm{V_{PTAT}}$. The function descriptions of these buffers are given as follows.

- $\mathrm{V_{CTAT}}$ and $\mathrm{V_{PTAT}}$ are are coupled to the CTAT and PTAT non-linear offset calibration buffers, respectively.
- $\mathrm{I_{R2}}$ and $\mathrm{I_{R4}}$ are equal to $\frac{\mathrm{V_{CTAT}}}{\mathrm{R2}}$ and $\frac{\mathrm{V_{PTAT}}}{\mathrm{R4}}$, respectively.
- $\mathrm{Vb_{CTAT}}$ and $\mathrm{Vb_{PTAT}}$ are $\mathrm{I_{R2}}\times\mathrm{R1}+\mathrm{V_{CTAT}}$ and $\mathrm{I_{R4}}\times\mathrm{R3}+\mathrm{V_{PTAT}}$, respectively.

$\mathrm{I_{R2}}\times\mathrm{R1}$ and $\mathrm{I_{R4}}\times\mathrm{R3}$ are calibration terms to cancel the non-linear offsets of CTAT and PTAT sensors, respectively. By thorough simulations using 0.25 μm 1P3M 60V BCD process, when R1 and R3 are selected to 6 KΩ, R2 and R4 will be 60 KΩ. Fig. 6 (a) and (b) show the $\mathrm{V_{CTAT}}$ and $\mathrm{V_{PTAT}}$ vs. resistance characteristics of a silicide resistor in series with a polysilicon resistor, respectively. Fig. 7 (a) and (b) show the calibrated simulation results of CTAT and PTAT sensors, respectively. Thus, we use the same temperature characteristic of CTAT and PTAT sensors and a silicide resistor in series with a polysilicon resistor to calibrate non-linear offset of CTAT and PTAT sensors. The output ranges of $\mathrm{Vb_{CTAT}}$ and $\mathrm{Vb_{PTAT}}$ are found to be 2.84 V $\sim$ 2.61 V and 3.64 V $\sim$ 4.22 V, respectively.

C. linear adder

Fig. 8 shows the schematic of the proposed linear adder composed of an OPA and four resistors. The linear adder is used to sum up the output voltages of temperature sensors. Thus, the linear adder must be designed with temperature compensation capability. R7 is the only silicide resistor, and the other 3

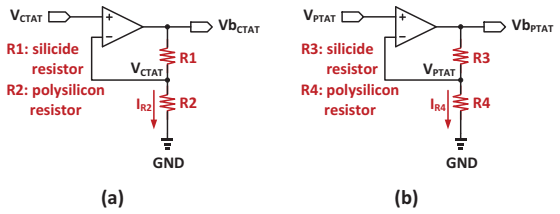

Fig. 5. Schematics of (a) CTAT non-linear offset calibration buffer ; and (b) PTAT non-linear offset calibration buffer.

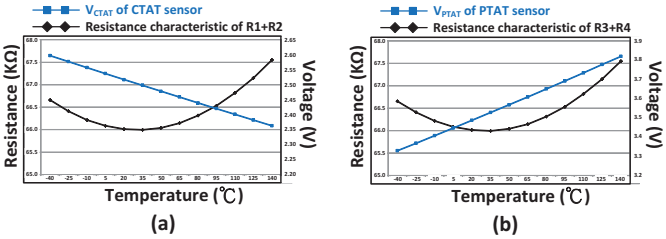

Fig. 6. Simulation of (a) V_{CTAT} and (b) V_{PTAT} vs. resistance characteristics of a silicide resistor in series with a polysilicon resistor with temperature, respectively.

resistors are all polysilicon. The function description of this linear adder is given as follows.

- Both Vb_{CTAT} and Vb_{PTAT} are coupled to the minus input of the linear adder. Vb_{REF} is 3 V at the plus input.
- I_{R5} and I_{R6+R7} are equal to $\frac{Vb_{REF}-Vb_{CTAT}}{R5}$ and $\frac{Vb_{PTAT}-Vb_{REF}}{R6+R7}$, respectively.
- The R5 (60 KΩ) is equal to R6 (59 KΩ) + R7 (1 KΩ), since the overall resistance is selected to match the 60 KΩ of R2, R4. Notably, Vb_{PTAT} is 3.64 V ∼ 4.22 V, and Vb_{CTAT} is 2.84 V ∼ 2.61 V. I_{R5} and I_{R6+R7} are $\frac{3\text{ V}-(2.84\text{ V}\sim 2.61\text{ V})}{60\text{ K}\Omega} = 2.667\text{ uA} \sim 6.5\text{ uA}$ and $\frac{(3.64\text{ V}\sim 4.22\text{ V})-3\text{ V}}{59\text{ K}\Omega + 1\text{ K}\Omega} = 10.67\text{ uA} \sim 20.33\text{ uA}$, respectively.

When I_{R6+R7} is significantly larger than I_{R5}, the offset of the Vb_{PTAT} will be a major factor to T_{out} especially at very low and high temperatures. According to resistance characteristic of the silicide resistor, which is roughly proportional to temperature, the silicide resistor is used to reduce I_{R6+R7} when the mismatch between I_{R6+R7} and I_{R5} is happened. The offset of Vb_{PTAT} will then be reduced.

D. HV ESD protection

Fig. 9 (a) shows the schematic of the HV ESD protection design required in Fig. 1. The function description of this HV ESD protection circuit is given as follows.

1) When electrostatic surge enters VDD, the V_P−VDD is lower than Vthp of M5 to turn on M5.
2) M5 then provides a current path to R21 to raise V_N.
3) When V_N is higher than Vth of M6, the M6 is turned on to discharge the surge current.
4) When the electrostatic surge is fully discharged, the V_N is lower than Vth of M6 to turn off M6.

Fig. 9 (b) shows the simulated function of the HV ESD protection circuit when VDD is 40 V, which is also the BMS

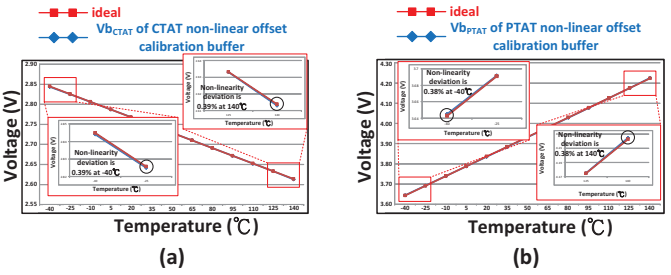

Fig. 7. Simulation waveforms of (a) CTAT sensor calibrated results ; and (b) PTAT sensor calibrated results.

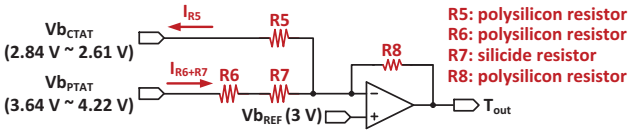

Fig. 8. Schematic of the linear adder.

supply voltage. Notably, the maximum limitation voltage of C1 is only 5 V required by the 0.25 μm 1P3M 60V BCD process. Thus, we use these resistors (R18, R19, and R20) to reduce the voltage drop of R20 such that V_{R20} is smaller than 5 V. Then, by the current mirrors composed of MOSs (M1, M2, M3, and M4) , V_{R20} is mapped to the voltage drop of C1 to keep it under 5 V voltage drop.

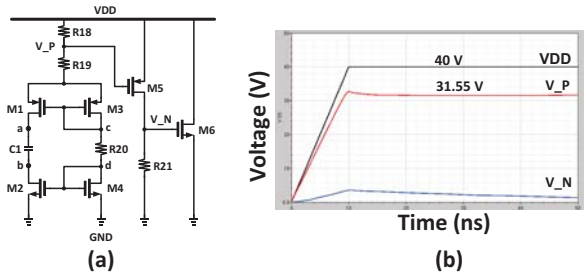

Fig. 9. Schematic of the (a) ESD protection and (b) simulated function of ESD protection.

III. Implementation and Simulation Results

Fig. 10 shows the layout of this work, where the core area of the proposed temperature detector is 0.1 mm^2. The power of the proposed temperature detector is 17 mW. Table II compares the non-calibrated and calibrated simulation results, where the maximum non-linearity reduction is 41%. The proposed temperature detector is also simulated at FF, TT, and SS corners, as shown in Fig. 11. Fig. 12 summarizes the deviation distribution of the proposed temperature detector at FF, TT, and SS corners. The performance comparison of the proposed design and several prior works is tabulated in Table III. In the range from -40 °C to 140 °C, the worst deviation of the temperature detector is -2.16 °C ∼ +1.98 °C at all process corners. The worst-case deviations of the calibrated CTAT and PTAT sensors are only 0.39% and 0.38%, respectively. Besides,

TABLE III
PERFORMANCE COMPARISON OF TEMPERATURE DETECTOR

	[8]	[5]	[7]	[4]	[3]	This work
Year	2007	2009	2010	2011	2012	2013
Process (μm)	N/A(FPGA)	0.13	0.065	0.065	0.18	0.25
Supply Voltage (V)	N/A	1.2	1	1	1.8	5
Temperature Range	0 °C ~ 75 °C	0 °C ~ 100 °C	0 °C ~ 100 °C	0 °C ~ 60 °C	-40 °C ~ 85 °C	-40 °C ~ 140 °C
Error (°C)	-1.5/0.8	-1.8/+2.3	-10/+10	-5.1/+3.4	-0.9/+1.8	-2.16/+1.98
Core Area (mm^2)	N/A	0.16	0.01	0.01	0.04	0.1
Power (mW)	0.084	12	0.55	0.015	0.478	17

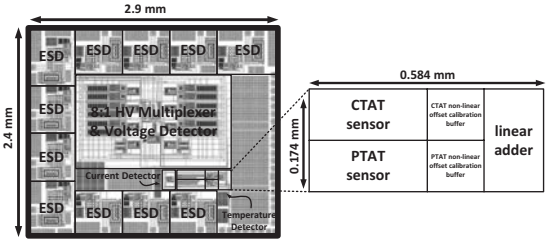

Fig. 10. Layout of the proposed design.

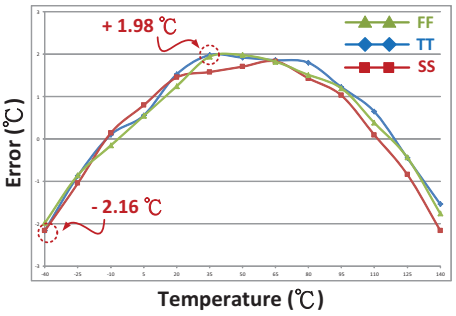

Fig. 12. Error distribution of the proposed temperature detector at FF, TT, and SS corners.

the maximum non-linearity reduction of the CTAT and PTAT sensors are 9% and 41%, respectively.

TABLE II
CALIBRATION RESULTS AT CTAT SENSOR & PTAT SENSORS

	non-calibrated	calibrated	Linearity improvement
CTAT sensor @ -40 °C / 140 °C	0.43% / 0.43%	0.39% / 0.39%	9% / 9%
PTAT sensor @ -40 °C / 140 °C	0.65% / 0.65%	0.38% / 0.38%	41% / 41%

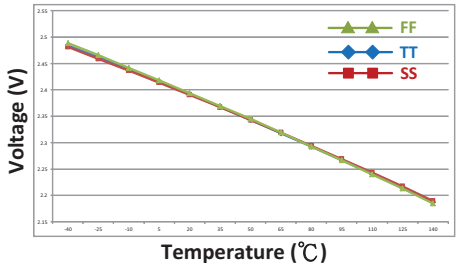

Fig. 11. Simulation results of the proposed temperature detector performance at FF, TT, and SS corners.

IV. CONCLUSION

In this work, the temperature detector attains process compensation and calibration by using the proposed CTAT and PTAT sensors. Notably, the usage of resistors made with different materials carries out the cancellation of offsets caused by temperature drifting. In this work, the temperature detector is composed of 3 OPAs and 8 resistors using a typical 0.25 μm 1P3M 60V BCD process. Notably, our design attains the advantages of accuracy and reliability ensured by HV ESD protection circuit at the expense of power and area overhead.

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REFERENCES

[1] K. W. E. Cheng, B. P. Divakar, H. Wu, K. Ding, and H. F. Ho, "Battery-management system (BMS) and SOC development for electrical vehicles," *IEEE Trans. Vehicular Tech.*, vol. 60, no. 1, pp. 76-88, Jan. 2011.

[2] FlexRay Communications System-Protocol Specification V2.1 (http://www.flexray.com), 2005.

[3] Y. Jeong and F. Ayazi, "Process compensated CMOS temperature sensor for microprocessor application," in *Proc. IEEE Int. Conf. on Circuits and Syst.*, pp. 3118-3121, May 2012.

[4] C.-C. Chung and C.-R. Yang, "An autocalibrated all-digital temperature sensor for On-chip thermal monitoring," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 2, pp. 105-109, Feb. 2011.

[5] K. Woo, S. Meninger, T. Xanthopoulos, E. Crain, D. Ha, and D. Ham, "Dual-DLL based CMOS all-digital temperature sensor for microprocessor thermal monitoring," *IEEE ISSCC Dig.*, pp. 68-69, Feb. 2009.

[6] C. Zhao, J. He, S.-H. Lee, K. Peterson, R. Geiger, and D. Chen, "Linear Vt-based temperature sensors with low process sensitivity and improved power supply headroom," in *Proc. IEEE Int. Conf. on Circuits and Syst.*, pp. 2553-2556, May 2011.

[7] C.-C. Chung and C.-R. Yang, "An all-digital smart temperature sensor with auto-calibration in 65nm CMOS technology," in *Proc. IEEE Int. Conf. on Circuits and Syst.*, pp. 4089-4092, May 2010.

[8] P. Chen, M.-C. Shie, Z.-Y. Zheng, Z.-F. Zheng, and C.-Y. Chu, "A fully digital time-domain smart temperature sensor realized with 140 FPGA logic elements," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2661-2668, Dec. 2007.