

Electric Circuit & Electronics

Chapter 2 Diode Applications

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OBJECTIVES

- Understand the concept of **load-line analysis** and how it is applied to diode networks.
- Become familiar with the use of equivalent circuits to analyze **series, parallel, and series-parallel** diode networks.
- Understand the process of **rectification** to establish a dc level from a sinusoidal ac input.
- Be able to predict the output response of a **clipper** and **clamper** diode configuration.
- Become familiar with the analysis of and the range of applications for **Zener diodes**.

2.1 INTRODUCTION

- This chapter will develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application
- By chapter's end, the fundamental behavior pattern of diodes in **dc and ac networks** should be clearly understood.
- The analysis of electronic circuits can follow one of two paths: using the **actual characteristics** or applying **an approximate model** for the device.

2.2 LOAD-LINE ANALYSIS

The circuit of Fig. 2.1 is the simplest of diode configurations. It will be used to describe the analysis of a diode circuit using its actual characteristics

In the next section we will replace the characteristics by an **approximate model** for the diode and compare solutions.

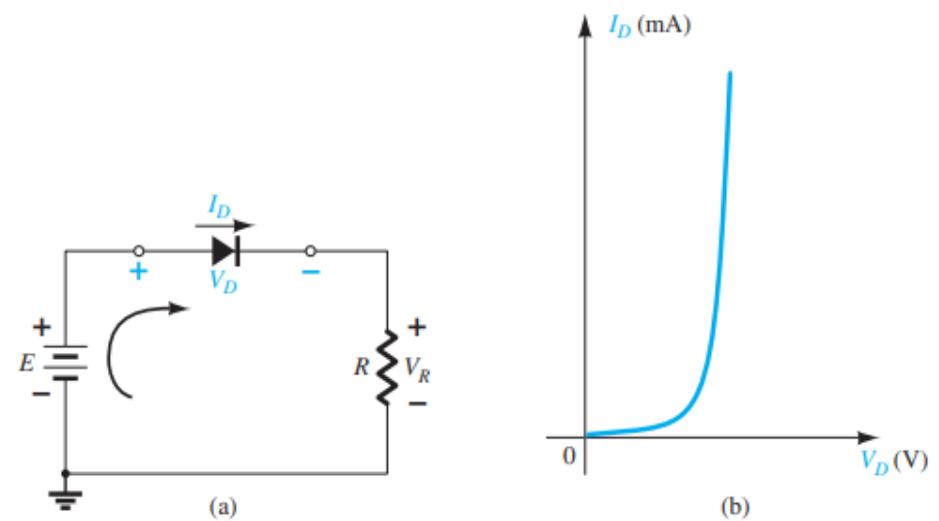
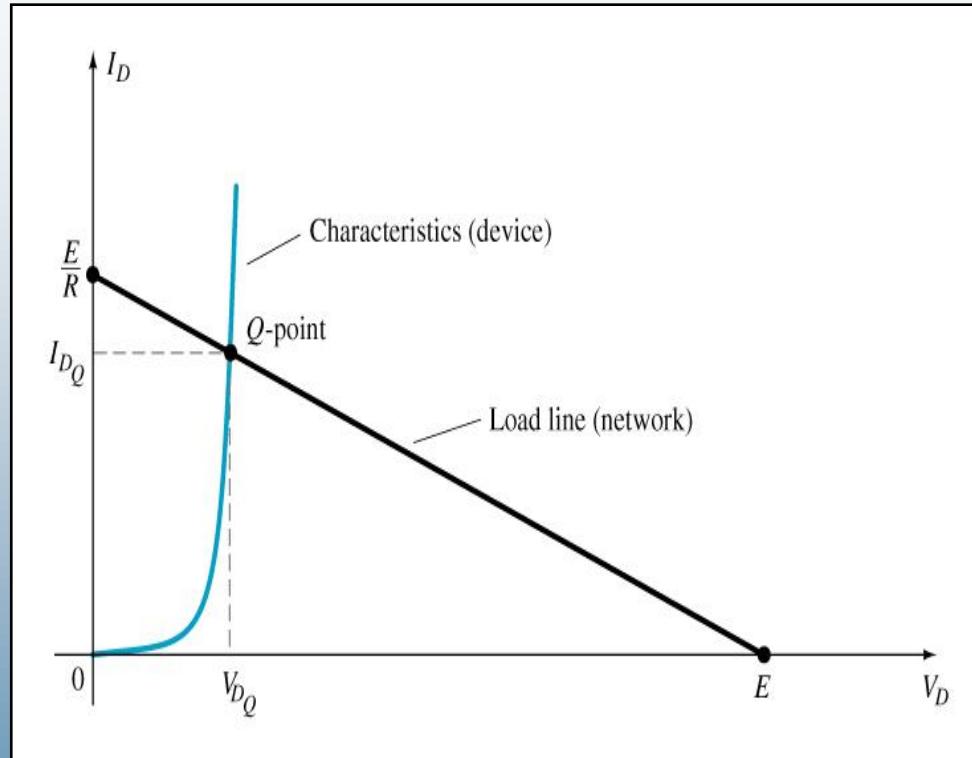


FIG. 2.1

Solving the circuit of Fig. 2.1 is all about finding **the current and voltage** levels that will satisfy both the characteristics of the diode and the chosen network parameters at the same time.

Load-Line Analysis

The straight line is called a load line because the intersection on the vertical axis is defined by the applied load R . The load line plots all possible combinations of diode current (I_D) and voltage (V_D) for a given circuit. The maximum I_D equals E/R , and the maximum V_D equals E .



The point where the load line and the characteristic curve intersect is the Q-point, which identifies I_D and V_D for a particular diode in a given circuit.

2.2 LOAD-LINE ANALYSIS

The intersections of the load line on the characteristics of Fig. 2.2 can be determined by first applying Kirchhoff's voltage law $+E - V_D - V_R = 0$

$$E = V_D + I_D R \quad (2.1)$$

If we set $V_D=0$ V in Eq. (2.1) and solve for I_D , we have the magnitude of I_D on the vertical axis. Therefore, with $V_D=0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0 \text{ V} + I_D R \end{aligned}$$

$$I_D = \frac{E}{R} \Big|_{V_D=0 \text{ V}} \quad (2.2)$$

2.2 LOAD-LINE ANALYSIS

as shown in Fig. 2.2 . If we set $I_D = 0 \text{ A}$ in Eq. (2.1) and solve for V_D , we have the magnitude of V_D on the horizontal axis. Therefore, with $I_D=0 \text{ A}$, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0 \text{ A})R \end{aligned}$$

$$V_D = E|_{I_D=0 \text{ A}} \quad (2.3)$$

As shown in Fig. 2.2 . A straight line drawn between the two points will define the load line as depicted in Fig. 2.2 . Change the level of R (the load) and the intersection on the vertical axis will change

2.2 LOAD-LINE ANALYSIS

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of operation for this circuit.

By simply drawing a line down to the horizontal axis, we can determine the diode voltage V_{DQ} , whereas a horizontal line from the point of intersection to the vertical axis will provide the level of ID_Q . The current ID is actually the current through the entire series configuration

2.2 LOAD-LINE ANALYSIS

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a , employing the diode characteristics of Fig. 2.3b , determine:

- V_{DQ} and I_{DQ} .
- V_R .

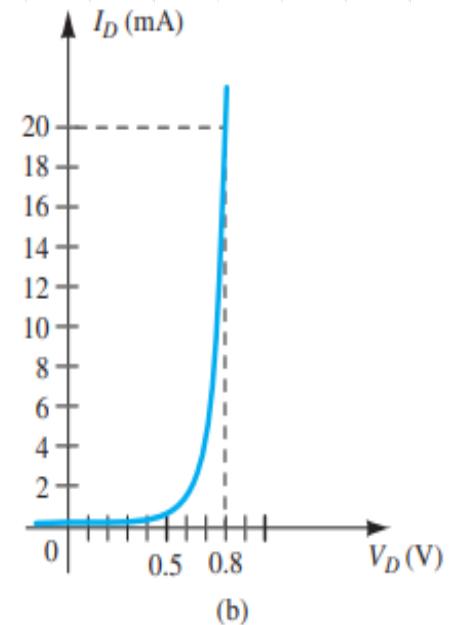
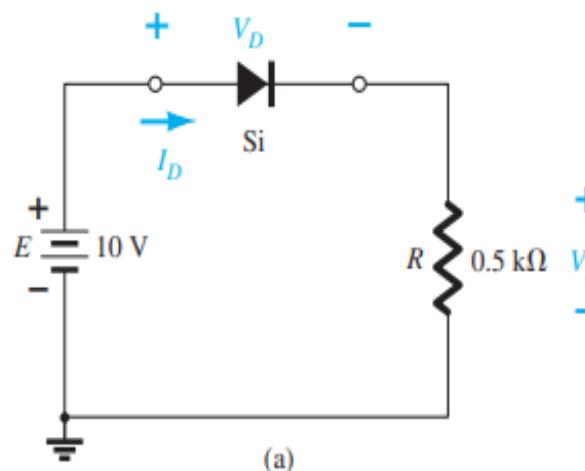


FIG. 2.3

2.2 LOAD-LINE ANALYSIS

Solution:

a. Eq. (2.2): $I_D = \frac{E}{R} \Big|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$

Eq. (2.3): $V_D = E \Big|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.4 . The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong 0.78\text{ V}$$

$$I_{D_Q} \cong 18.5\text{ mA}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = 9.22\text{ V}$

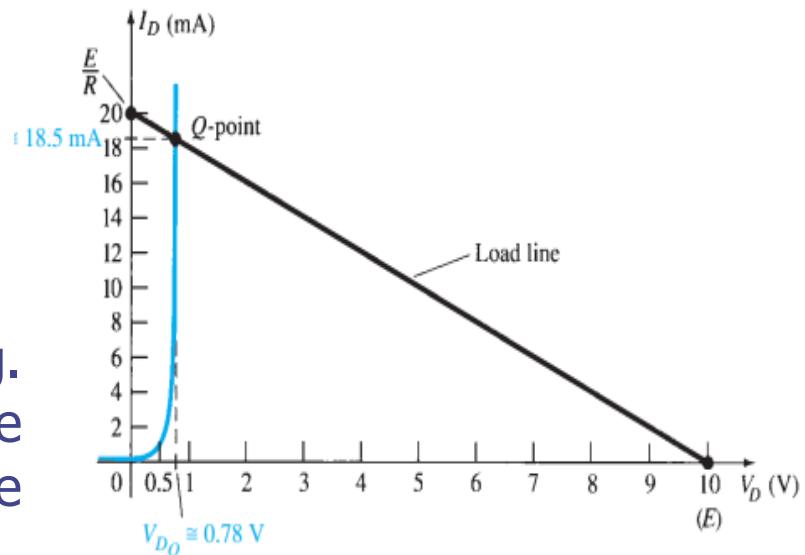


FIG. 2.4

2.2 LOAD-LINE ANALYSIS

Using the Q-point values, the dc resistance for Example 2.1 is

$$R_D = \frac{V_{DQ}}{I_{DQ}} = \frac{0.78 \text{ V}}{18.5 \text{ mA}} = 42.16 \Omega$$

An equivalent network (for these operating conditions only) can then be drawn as shown in Fig. 2.5

The current

$$I_D = \frac{E}{R_D + R} = \frac{10 \text{ V}}{42.16 \Omega + 500 \Omega} = \frac{10 \text{ V}}{542.16 \Omega} \cong 18.5 \text{ mA}$$

$$V_R = \frac{RE}{R_D + R} = \frac{(500 \Omega)(10 \text{ V})}{42.16 \Omega + 500 \Omega} = 9.22 \text{ V}$$

matching the results of Example 2.1 .

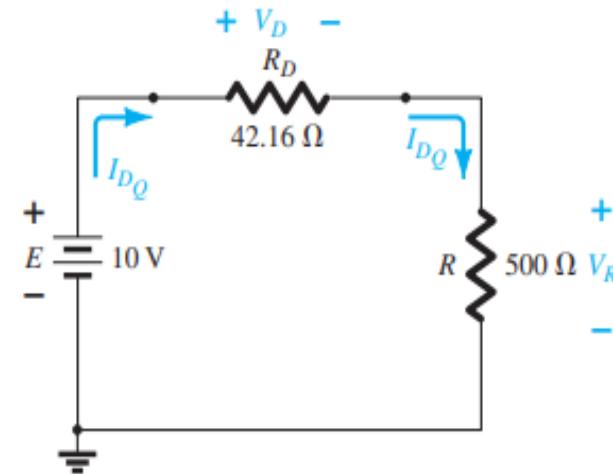


FIG. 2.5

2.2 LOAD-LINE ANALYSIS

EXAMPLE 2.2 Repeat Example 2.1 using the approximate equivalent model for the **silicon** semiconductor diode

Solution: The load line is redrawn as shown in Fig. 2.6 with the same intersections as defined in Example 2.1 . The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting Q-point is

$$V_{D_Q} = 0.7 \text{ V}$$

$$I_{D_Q} = 18.5 \text{ mA}$$

For this situation the dc resistance of the Q -point is

$$R_D = \frac{V_{D_Q}}{I_{D_Q}} = \frac{0.7 \text{ V}}{18.5 \text{ mA}} = 37.84 \Omega$$

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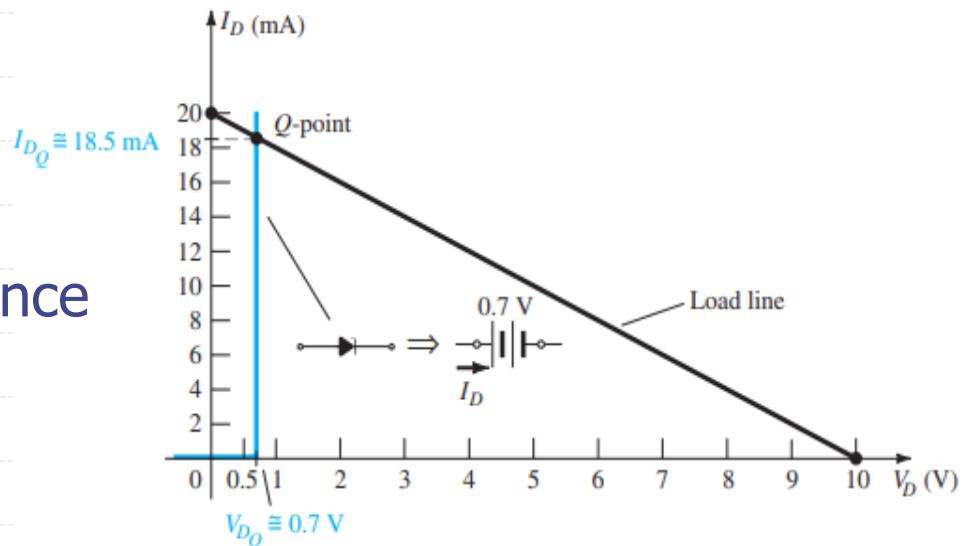


FIG. 2.6

2.2 LOAD-LINE ANALYSIS

EXAMPLE 2.3 Repeat Example 2.1 using the ideal diode model.

Solution: As shown in Fig. 2.7 , the load line is the same, but the ideal characteristics now intersect the load line on the vertical axis. The Q-point is therefore defined by

$$V_{DQ} = 0 \text{ V}$$

$$I_{DQ} = 20 \text{ mA}$$

$$R_D = \frac{V_{DQ}}{I_{DQ}} = \frac{0 \text{ V}}{20 \text{ mA}} = 0 \Omega \text{ (or a short-circuit equivalent)}$$

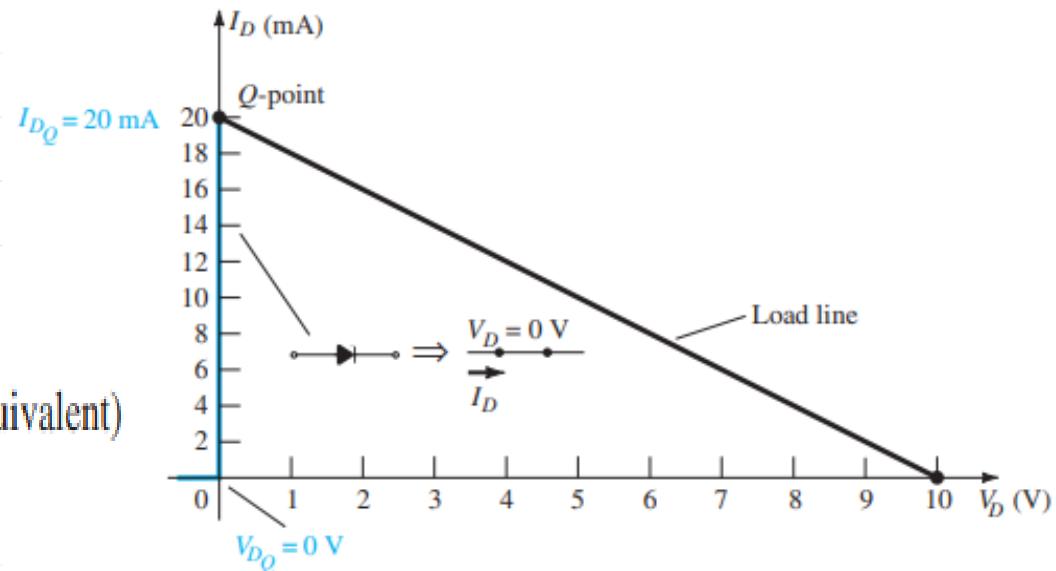


FIG. 2.7

2.3 SERIES DIODE CONFIGURATIONS

Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified.

2.3 Series Diode Configurations

Forward Bias

Constants

Silicon Diode: $V_D = 0.7 \text{ V}$

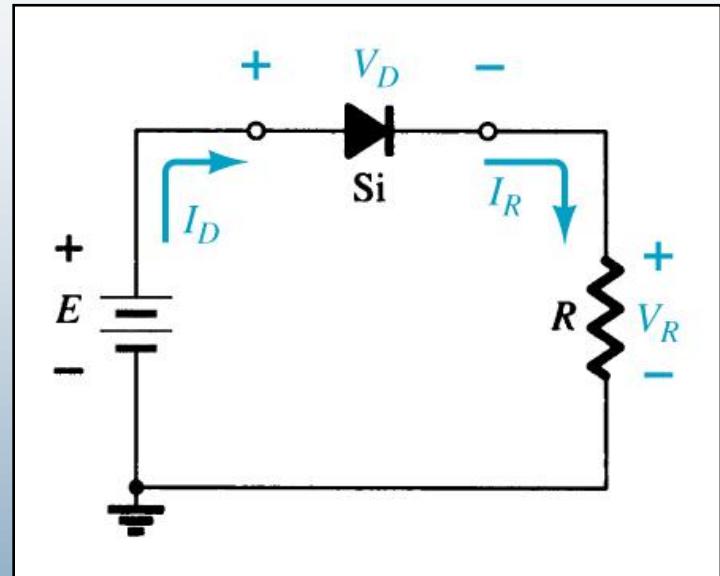
Germanium Diode: $V_D = 0.3 \text{ V}$

Analysis (for silicon)

$$V_D = 0.7 \text{ V} \text{ (or } V_D = E \text{ if } E < 0.7 \text{ V})$$

$$V_R = E - V_D$$

$$I_D = I_R = I_T = V_R / R$$



2.3 Series Diode Configurations

Reverse Bias

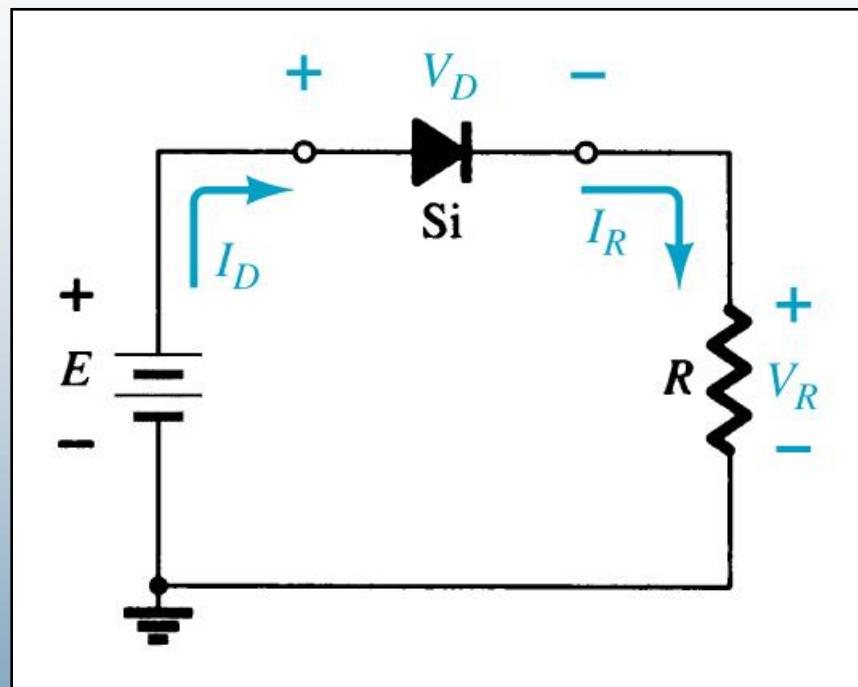
Diodes ideally behave as open circuits

Analysis

$$V_D = E$$

$$V_R = 0 \text{ V}$$

$$I_D = 0 \text{ A}$$



2.3 SERIES DIODE CONFIGURATIONS

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13 , determine V_D , V_R , and I_D .

Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the “on” state,

$$V_D = 0.7 \text{ V}$$

$$V_R = E - V_D = 8 \text{ V} - 0.7 \text{ V} = 7.3 \text{ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3 \text{ V}}{2.2 \text{ k}\Omega} \cong 3.32 \text{ mA}$$

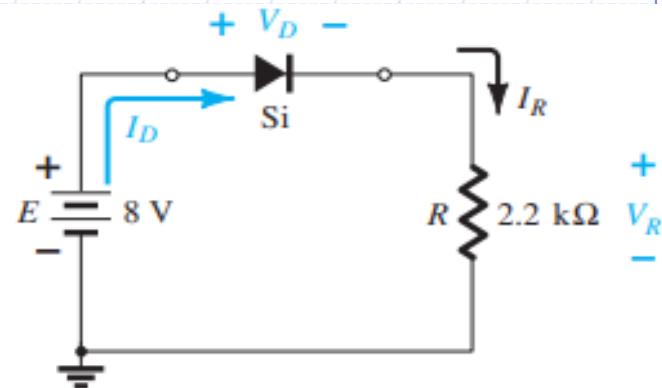


FIG. 2.13

2.3 SERIES DIODE CONFIGURATIONS

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit. The result is the network of Fig. 2.14 , where $I_D = 0 \text{ A}$ due to the **open circuit**. Since $V_R = I_R R$, we have $V_R = (0)R = 0 \text{ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

$$V_D = E - V_R = E - 0 = E = 8 \text{ V}$$

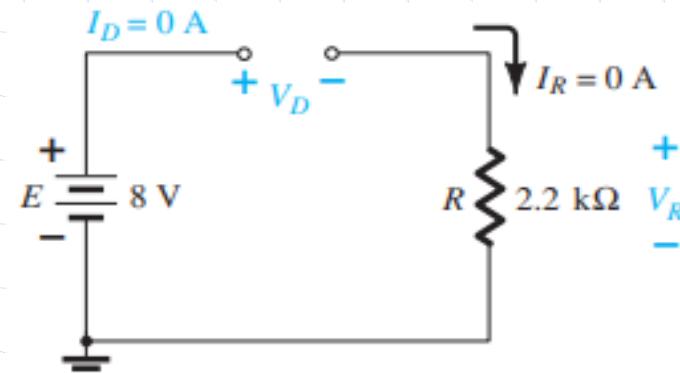


FIG. 2.14

2.3 SERIES DIODE CONFIGURATIONS

EXAMPLE 2.6 For the series diode configuration of Fig. 2.16 , determine V_D , V_R , and I_D .

Solution: The level of applied voltage is insufficient to turn the silicon diode “on.” The point of operation on the characteristics is shown in Fig. 2.17 , establishing the open circuit equivalent as the appropriate approximation, as shown in Fig. 2.18 . The resulting voltage and current levels are therefore the following:

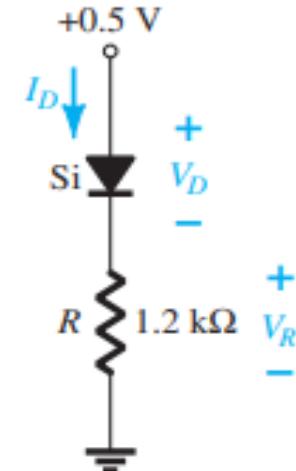


FIG. 2.16

$$I_D = 0 \text{ A}$$

$$V_R = I_R R = I_D R = (0 \text{ A}) 1.2 \text{ k}\Omega = 0 \text{ V}$$

$$V_D = E = 0.5 \text{ V}$$

2.3 SERIES DIODE CONFIGURATIONS

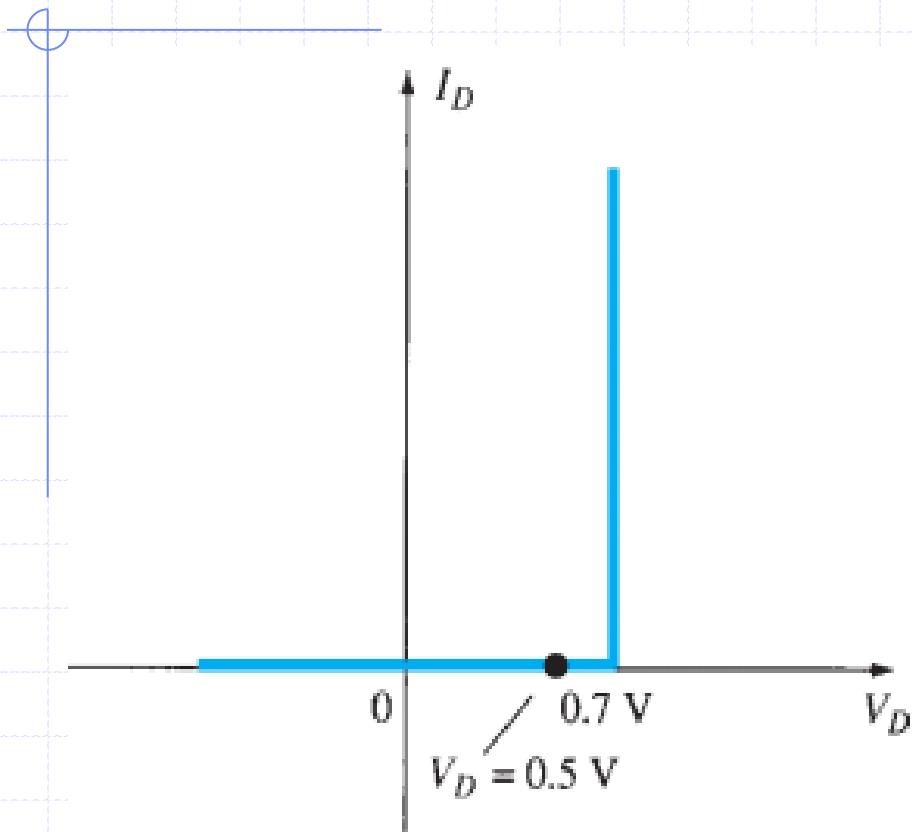


FIG. 2.17

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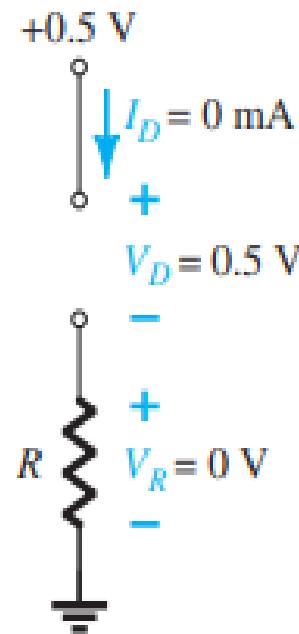


FIG. 2.18

2.3 SERIES DIODE CONFIGURATIONS

EXAMPLE 2.7 Determine V_o and I_D for the series circuit of Fig. 2.19 .

Solution

The network of Fig. 2.20 results because $E = 12V > (0.7 V + 1.8V [Table 1.8]) = 2.5V$. Note the redrawn supply of 12 V and the polarity of V_o across the 680Ω resistor. The resulting voltage is

$$V_o = E - V_{K_1} - V_{K_2} = 12V - 2.5V = 9.5V$$

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5V}{680\Omega} = 13.97mA$$

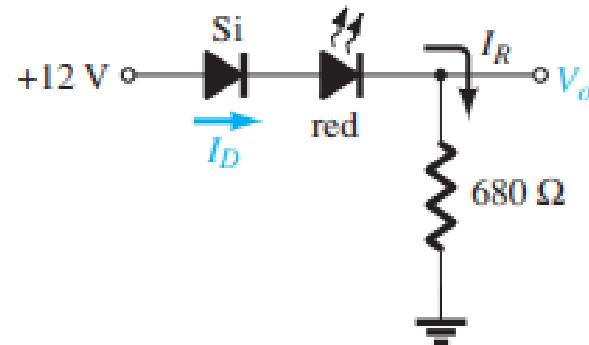


FIG. 2.19

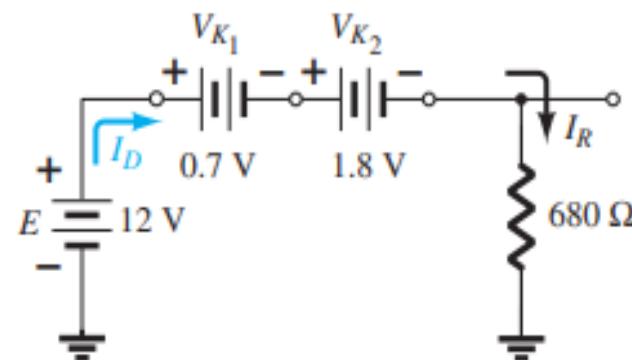


FIG. 2.20

2.3 SERIES DIODE CONFIGURATIONS

EXAMPLE 2.8 Determine I_D , V_{D2} , and V_o for the circuit of Fig. 2.21.

Solution: Removing the diodes and determining the direction of the resulting current I result in the circuit of Fig. 2.22

$I_D=0A$ and $V_{D1} = 0 V$ are indicated in Fig. 2.24

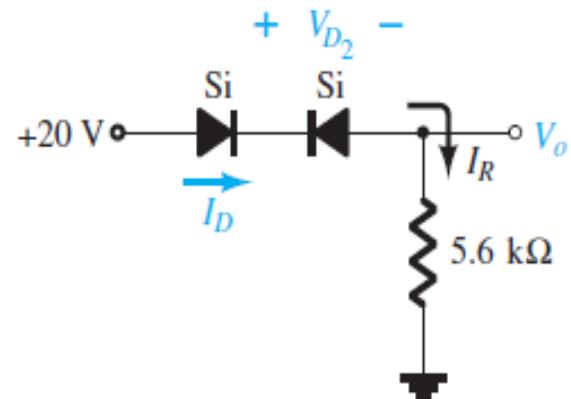


FIG. 2.21

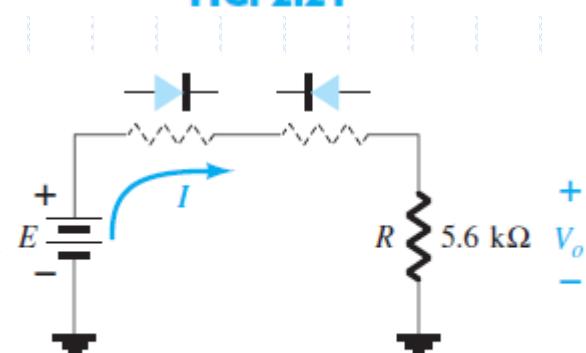


FIG. 2.22

2.3 SERIES DIODE CONFIGURATIONS

$$V_o = I_R R = I_D R = (0 \text{ A})R = 0 \text{ V}$$

$$V_{D_2} = V_{\text{open circuit}} = E = 20 \text{ V}$$

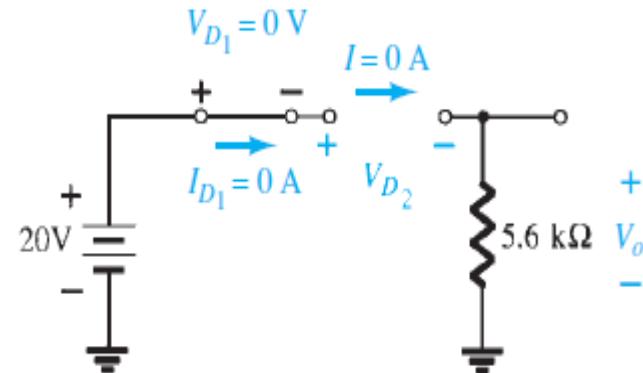


FIG. 2.24

Applying Kirchhoff's voltage law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

$$V_{D_2} = E - V_{D_1} - V_o = 20 \text{ V} - 0 - 0 = 20 \text{ V}$$

$$V_o = 0 \text{ V}$$

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

The methods applied in **Section 2.3** can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.10 Determine V_o , I_1 , I_{D1} , and I_{D2} for the parallel diode configuration of Fig. 2.28 .

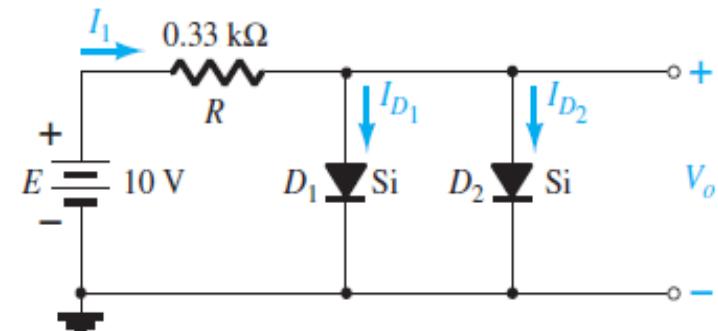


FIG. 2.28

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

Solution: For the applied voltage the “pressure” of the source acts to establish a current through each diode in the same direction as shown in Fig. 2.29. $V_o = 0.7 \text{ V}$

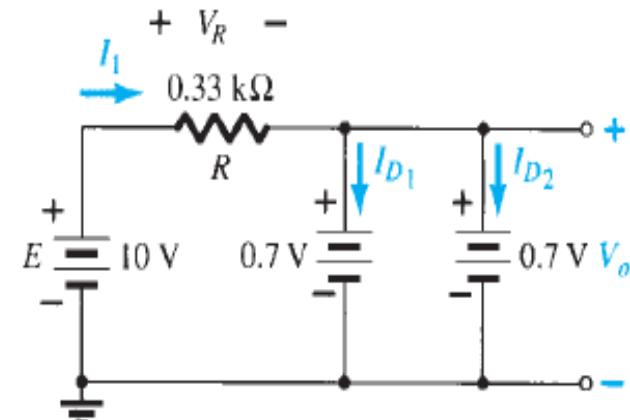


FIG. 2.29

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10 \text{ V} - 0.7 \text{ V}}{0.33 \text{ k}\Omega} = 28.18 \text{ mA}$$

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18 \text{ mA}}{2} = 14.09 \text{ mA}$$

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

EXAMPLE 2.11 there are two LEDs that can be used as a polarity detector. Apply a positive source voltage and a green light results. Negative supplies result in a red light. Packages of such combinations are commercially available. Find the resistor R to ensure a current of 20 mA through the “on” diode for the configuration of Fig. 2.30. Both diodes have a reverse breakdown voltage of 3 V and an average turn-on voltage of 2 V.

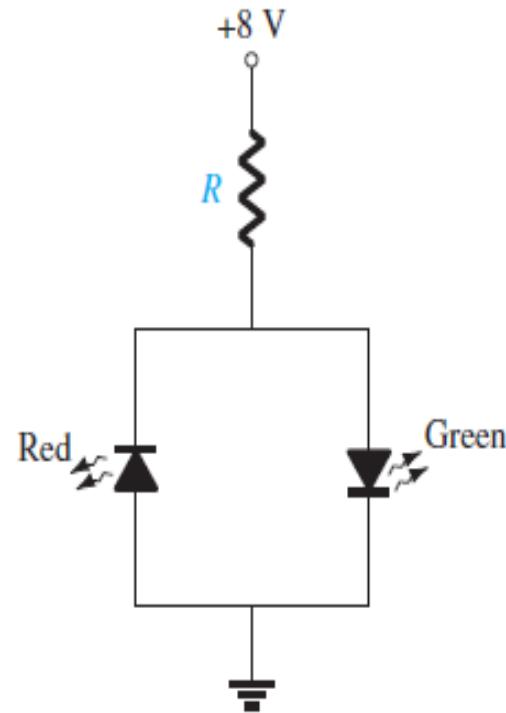


FIG. 2.30

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

$$I = 20 \text{ mA} = \frac{E - V_{\text{LED}}}{R} = \frac{8 \text{ V} - 2 \text{ V}}{R}$$

$$R = \frac{6 \text{ V}}{20 \text{ mA}} = 300 \Omega$$

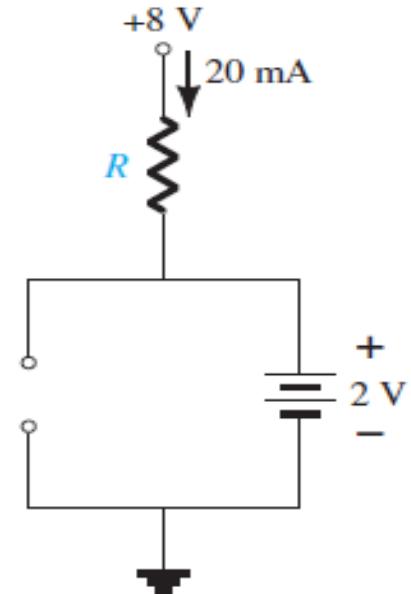


FIG. 2.31

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

EXAMPLE 2.12 Determine the voltage V_o for the network of Fig. 2.35 .

Solution: Initially, it might appear the applied voltage will turn both diodes “on” because the applied voltage is trying to establish a conventional current through each diode that would suggest the “on” state. However, if both were on, there would be more than one voltage across the parallel diodes, violating one of the basic rules of network analysis: The voltage must be the same across parallel elements.

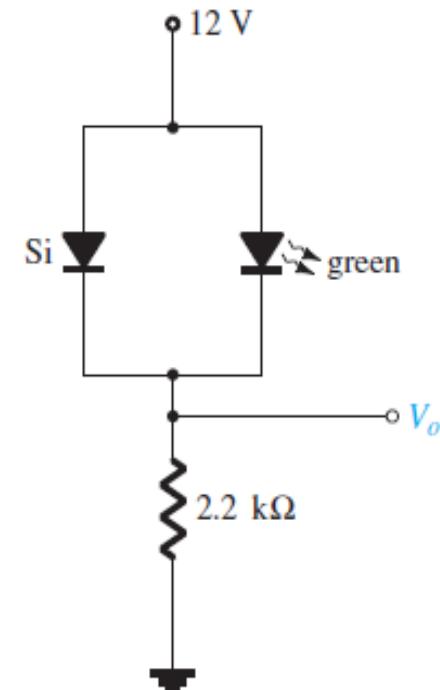


FIG. 2.35

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

the silicon diode will turn “on” and maintain the level of 0.7 V since the characteristic is vertical at this voltage the current of the silicon diode will simply rise to the defined level. The result is that the voltage across the green LED will never rise above 0.7 V and will remain in the equivalent open-circuit state as shown in Fig. 2.36 .

$$V_o = 12 \text{ V} - 0.7 \text{ V} = 11.3 \text{ V}$$

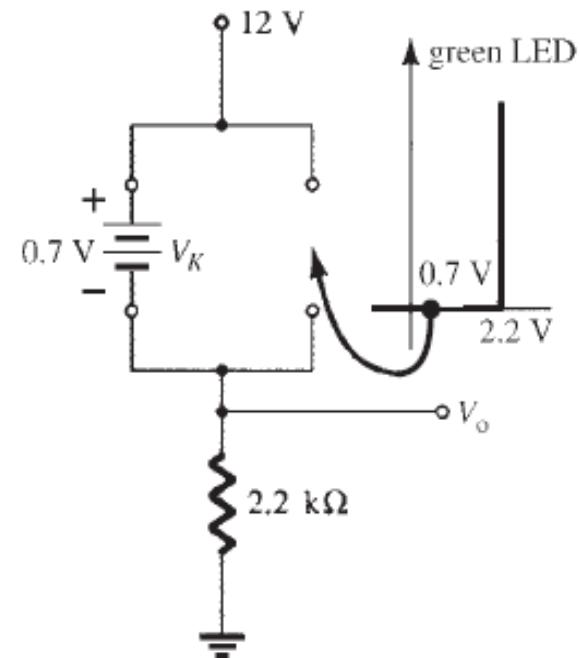


FIG. 2.36

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

EXAMPLE 2.13 Determine the currents I_1 , I_2 , and I_{D2} for the network of Fig. 2.37

Solution:

The applied voltage is such as to turn both diodes on, as indicated by the resulting current directions in the network of Fig. 2.38. The solution is obtained through an application of techniques applied to dc series-parallel networks.

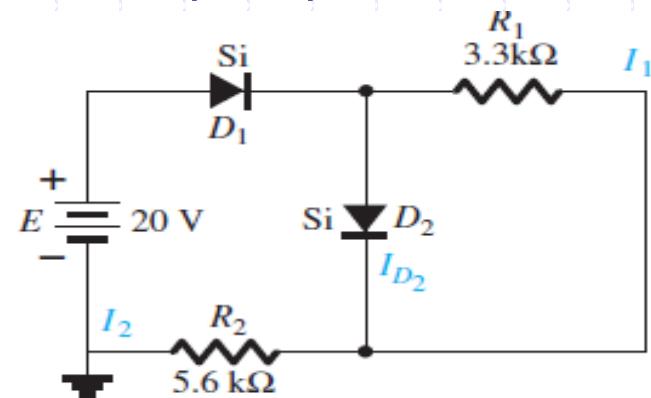


FIG. 2.37

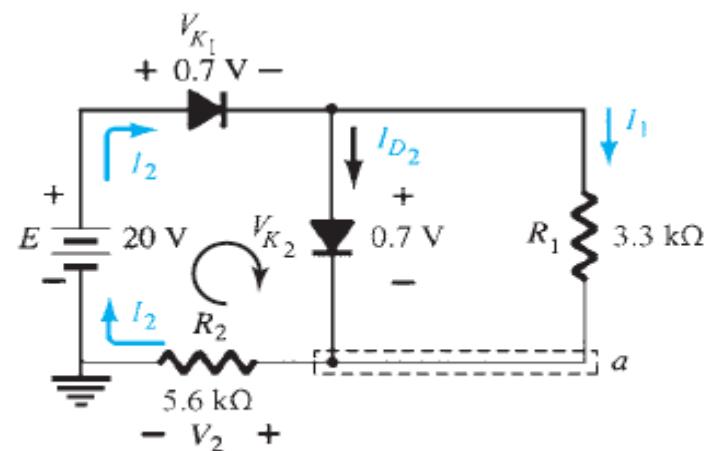


FIG. 2.38

2.4 PARALLEL AND SERIES-PARALLEL CONFIGURATIONS

$$I_1 = \frac{V_{K_2}}{R_1} = \frac{0.7 \text{ V}}{3.3 \text{ k}\Omega} = 0.212 \text{ mA}$$

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{K_1} - V_{K_2} = 0$$

$$V_2 = E - V_{K_1} - V_{K_2} = 20 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V} = 18.6 \text{ V}$$

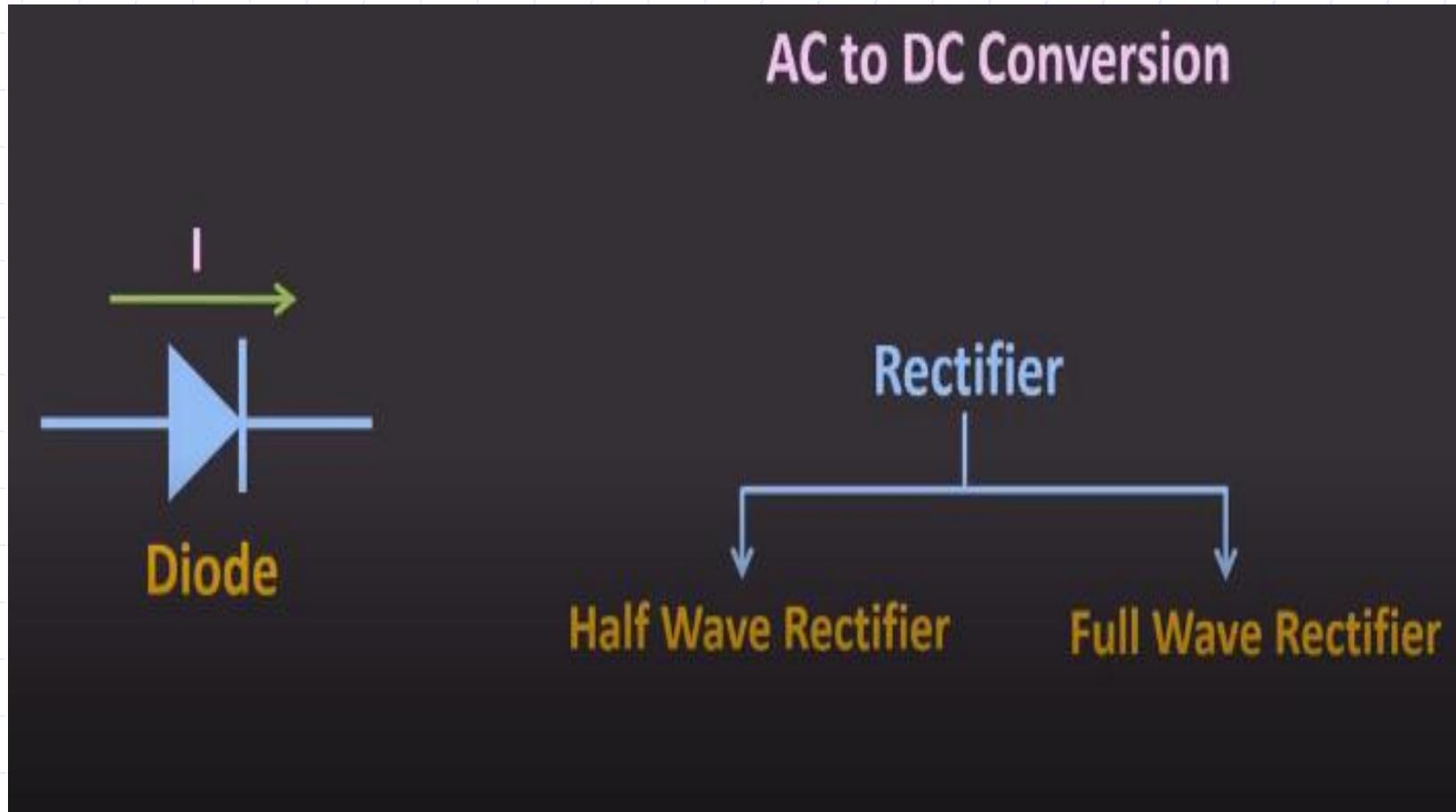
$$I_2 = \frac{V_2}{R_2} = \frac{18.6 \text{ V}}{5.6 \text{ k}\Omega} = 3.32 \text{ mA}$$

At the bottom node a

$$I_{D_2} + I_1 = I_2$$

$$I_{D_2} = I_2 - I_1 = 3.32 \text{ mA} - 0.212 \text{ mA} \approx 3.11 \text{ mA}$$

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION



2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include **time-varying functions** such as the sinusoidal waveform and the square wave. The simplest of networks to examine with a time-varying signal appears in Fig. 2.44.

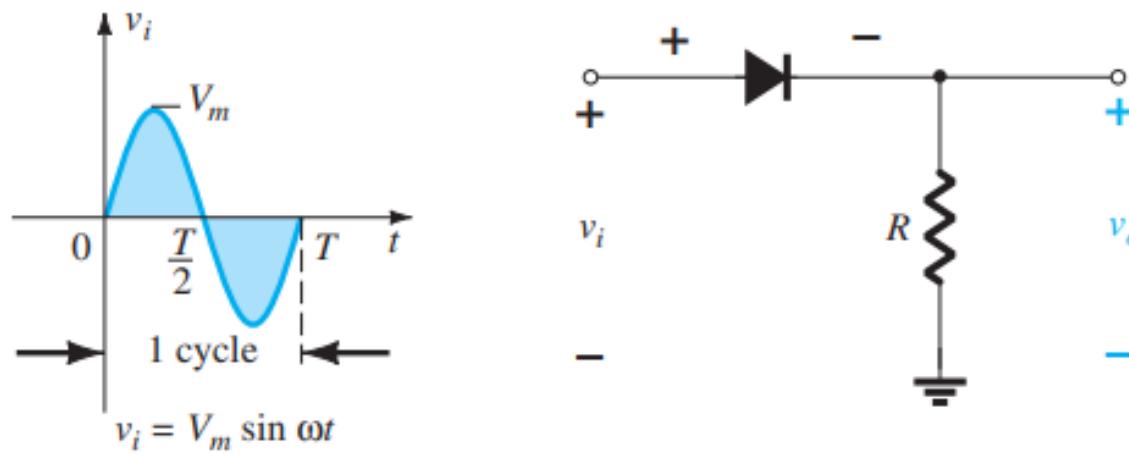
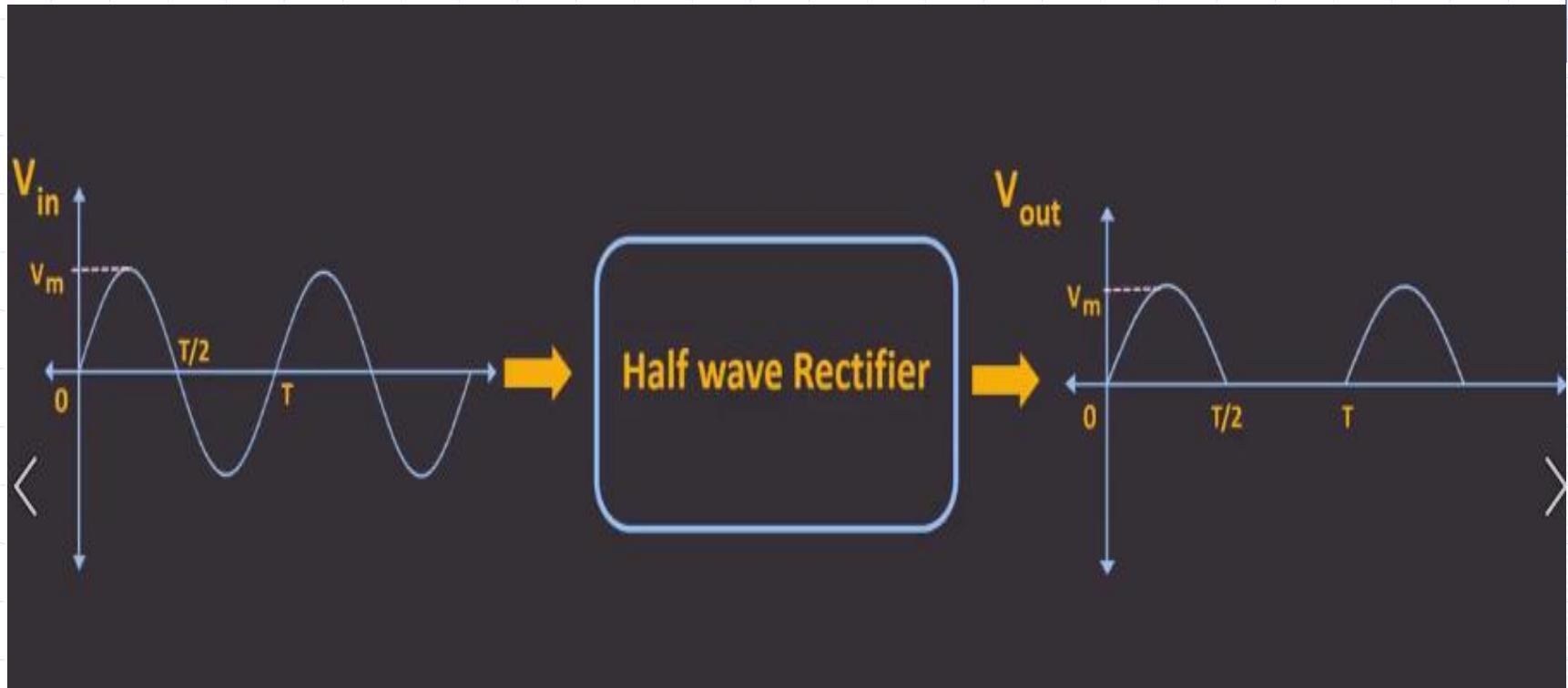


FIG. 2.44

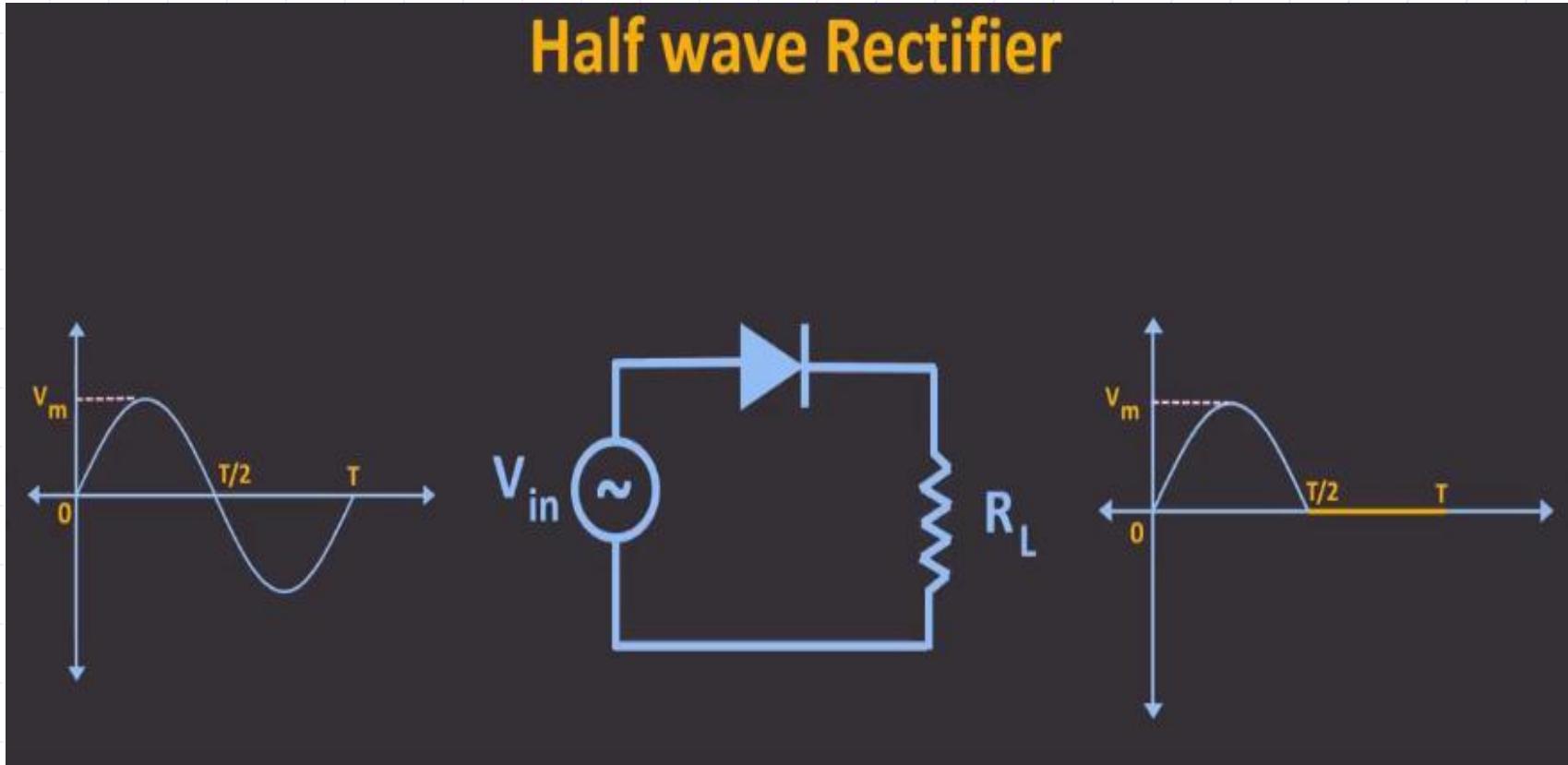
2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

- Over one full cycle, defined by the period T of Fig. 2.44, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.44 , called a half-wave rectifier , will generate a waveform v_o that will have an average value of particular use in the ac-to-dc conversion process.
- When employed in the rectification process, a diode is typically referred to as a rectifier. Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

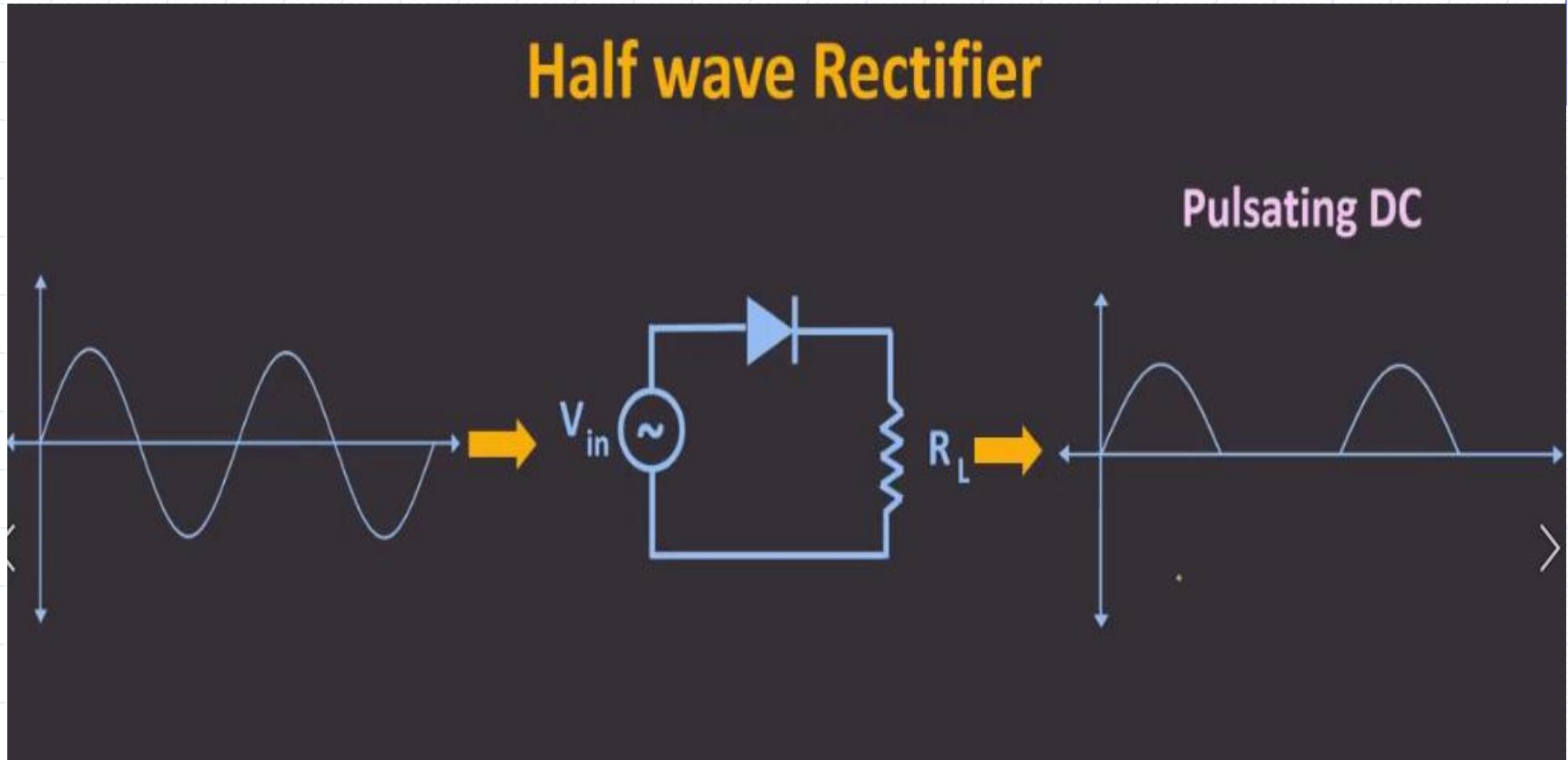
2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION



2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

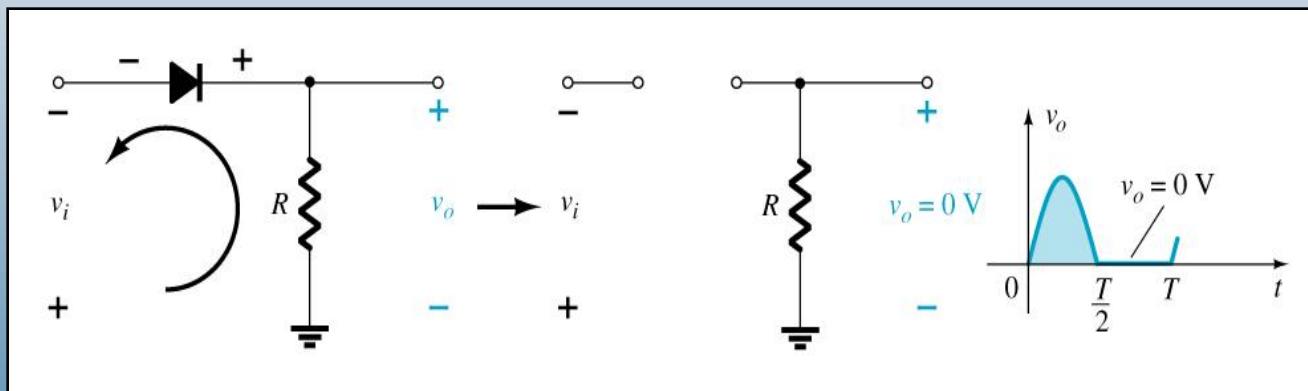
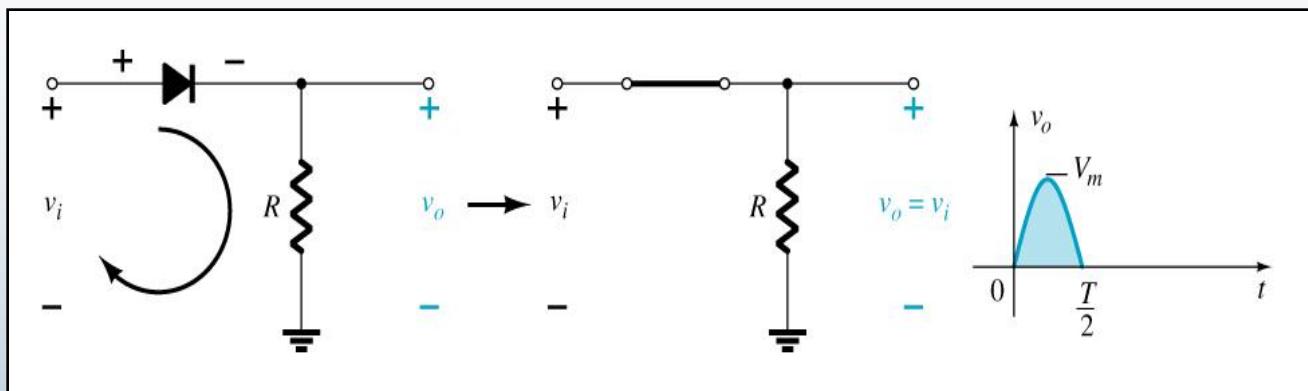


2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION



Half-Wave Rectification

The diode conducts only when it is **forward biased**, therefore only half of the AC cycle passes through the diode to the output.



The DC output voltage is $0.318 V_m$, where V_m = the peak AC voltage.

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The input v_i and the output v_o are sketched together in Fig. 2.47 for comparison purposes. The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = 0.318 V_m$$

half-wave

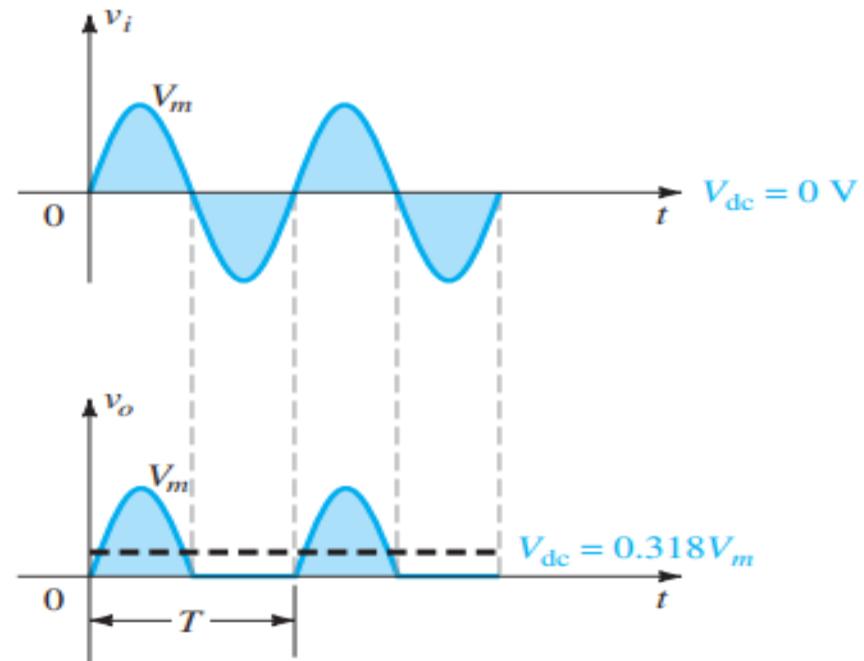


FIG. 2.47

(2.7)

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The effect of using a silicon diode with $V_K = 0.7\text{ V}$ is demonstrated in Fig. 2.48 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V , the diode is still in an open-circuit state and $v_o = 0\text{ V}$

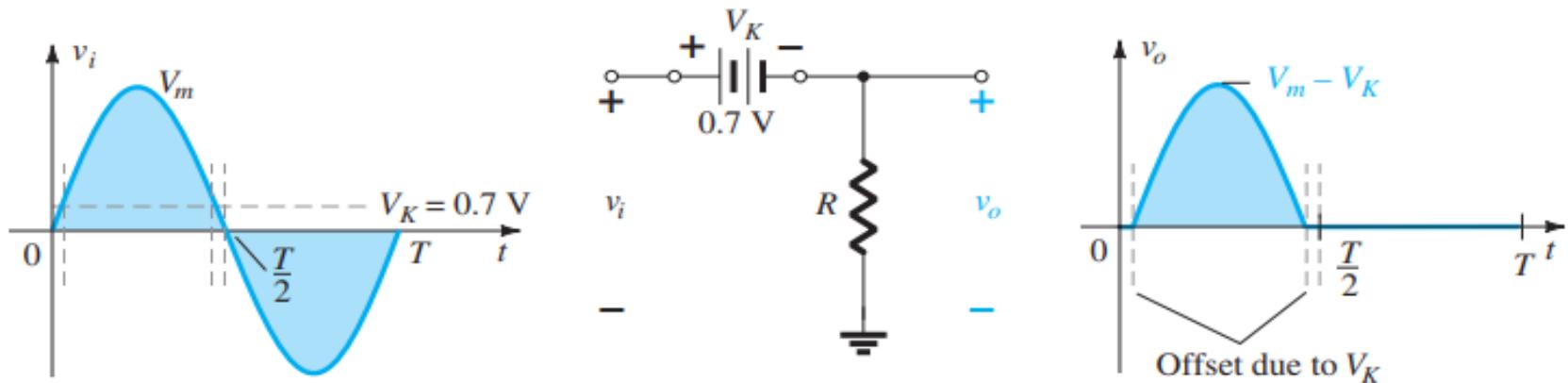
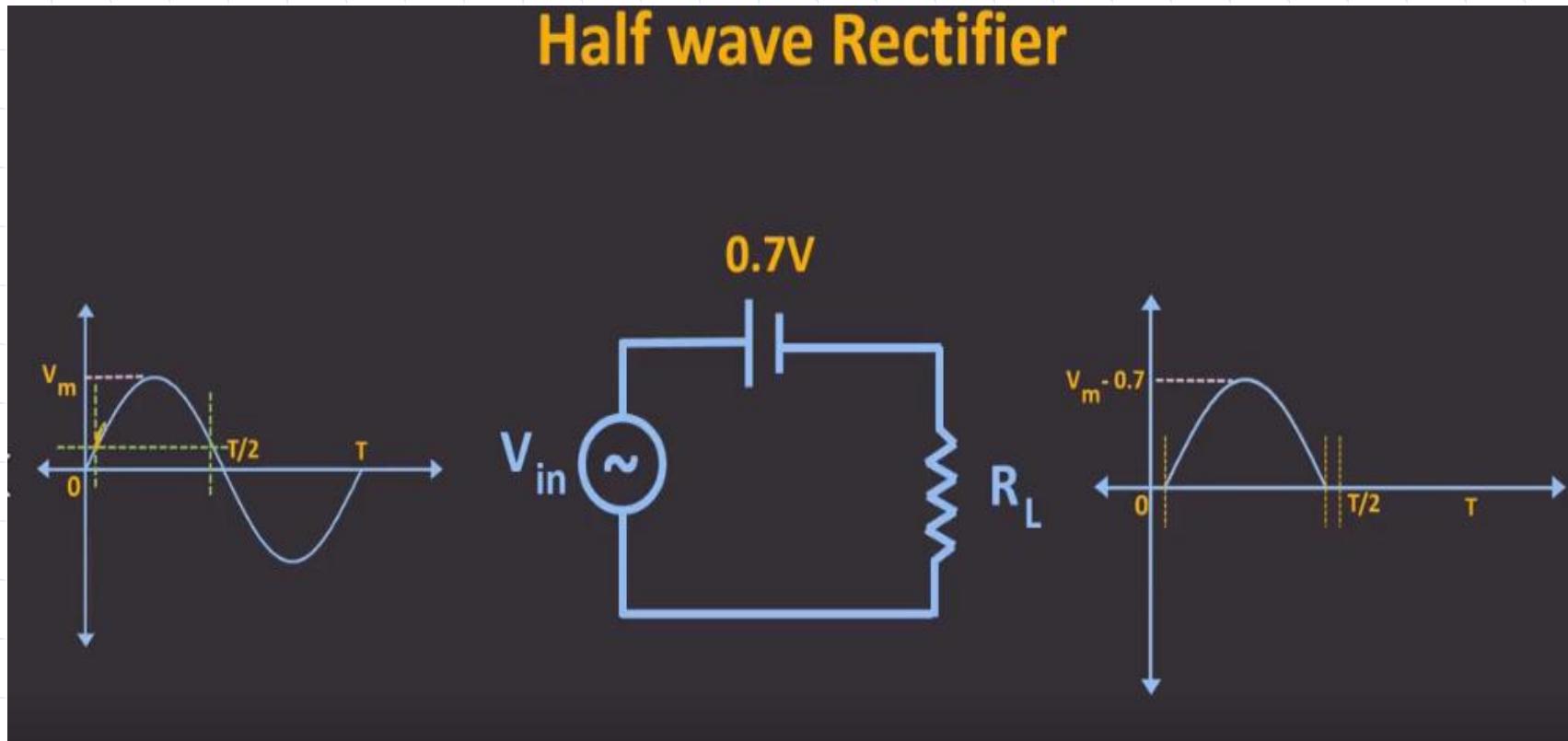


FIG. 2.48

$$V_{dc} \cong 0.318(V_m - V_K)$$

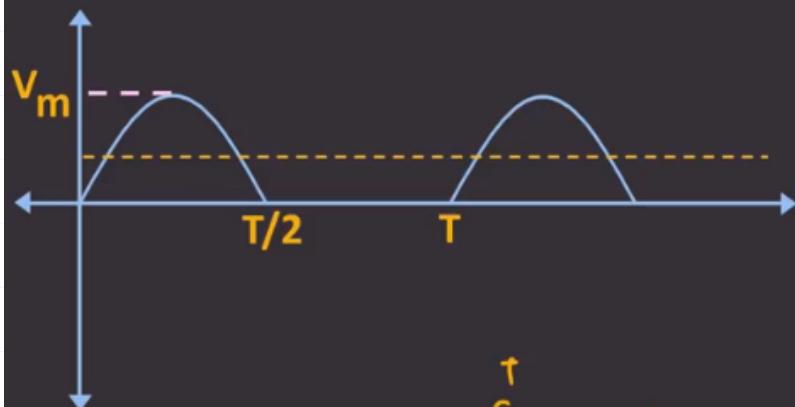
$$(2.8)$$

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION



2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

Average Value



$$V(t) = \begin{cases} V_m \sin(\omega t) & ; 0 < t < T/2 \\ 0 & ; T/2 < t < T \end{cases}$$

$$V_{avg} = \frac{1}{T} \int_0^T V(t) dt = \frac{1}{T} \int_0^{T/2} (V_m \sin(\omega t)) dt = \frac{V_m}{\pi}$$

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

EXAMPLE 2.16

- Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49 .
- Repeat part(a) if the ideal diode is replaced by a silicon diode.
- Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs.(2.7) and (2.8).

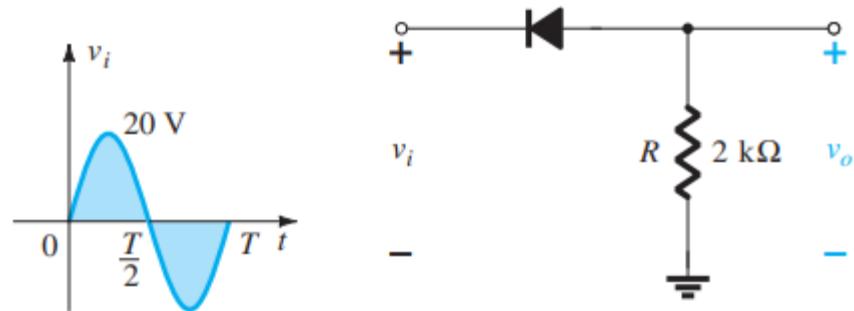


FIG. 2.49

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

Solution:

- A. In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.50, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20 \text{ V}) = -6.36 \text{ V}$$

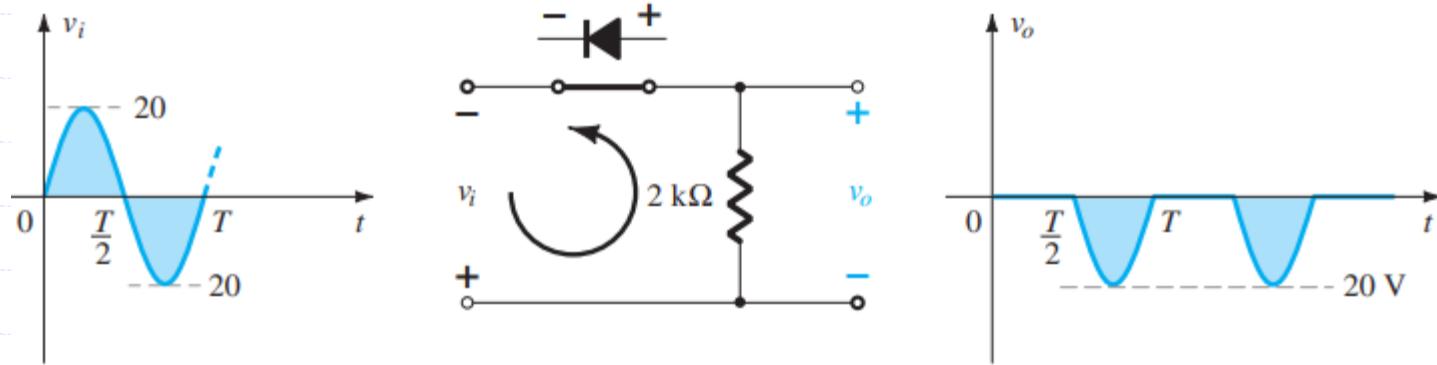


FIG. 2.50

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

- B. For a silicon diode, the output has the appearance of Fig. 2.51, and $V_{dc} \approx -0.318(V_m - 0.7 \text{ V}) = -0.318(19.3 \text{ V}) = -6.14 \text{ V}$ The resulting drop in dc level is 0.22 V, or about 3.5%.
- C. Eq. (2.7): $V_{dc} = -0.318 V_m = -0.318(200 \text{ V}) = -63.6 \text{ V}$
Eq. (2.8): $V_{dc} = -0.318(V_m - V_k) = -0.318(200 \text{ V} - 0.7 \text{ V}) = -(0.318)(199.3 \text{ V}) = -63.38 \text{ V}$

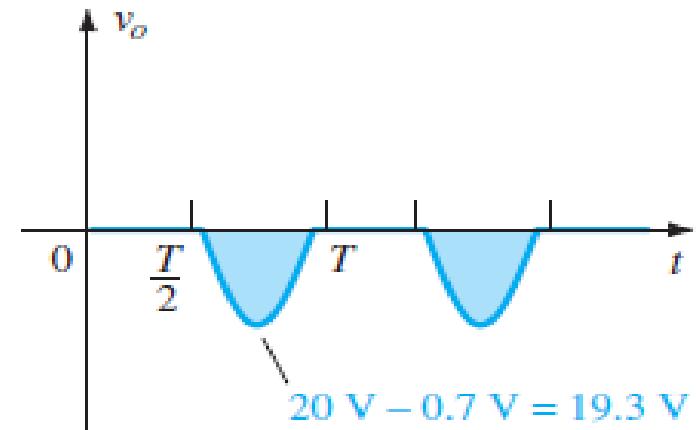


FIG. 2.51

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.52 , which displays the reverse-biased diode of Fig. 2.44 with maximum applied voltage. Applying KVL, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geq V_m$$

half-wave rectifier

(2.9)

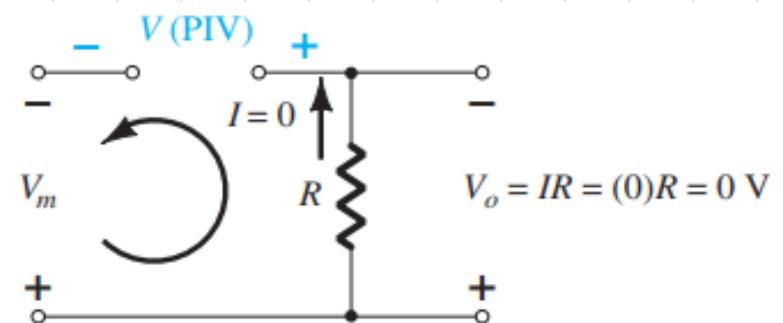
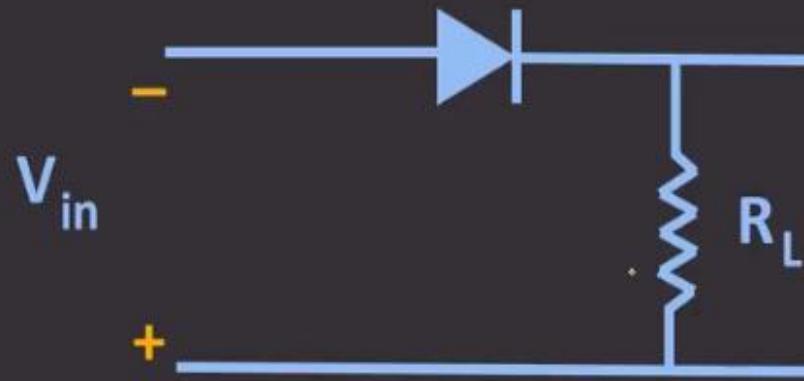
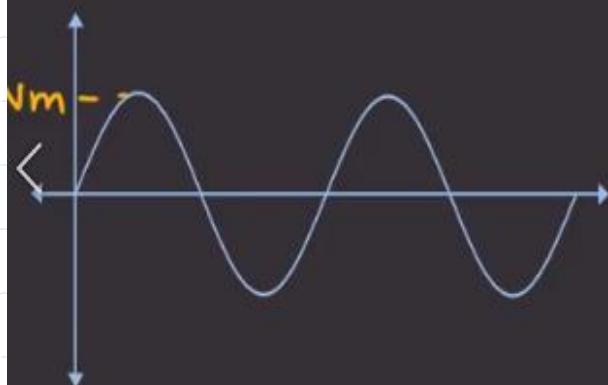


FIG. 2.52

2.6 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

Peak Inverse Voltage (PIV)



$$PIV = V_m$$

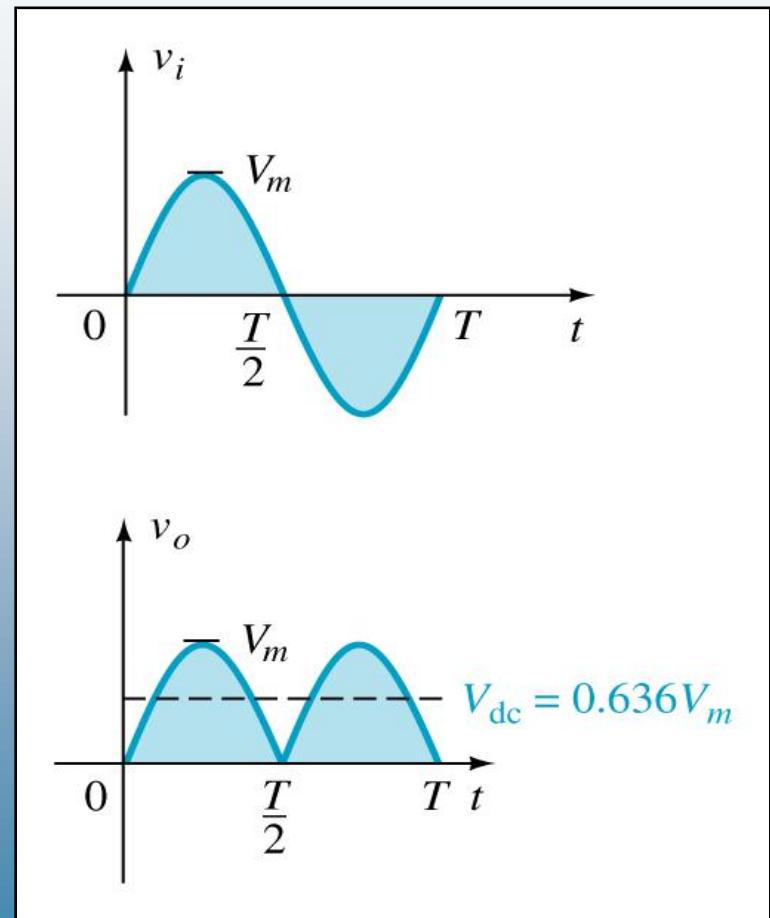
2.7 Full-Wave Rectification

The rectification process can be improved by using a full-wave rectifier circuit.

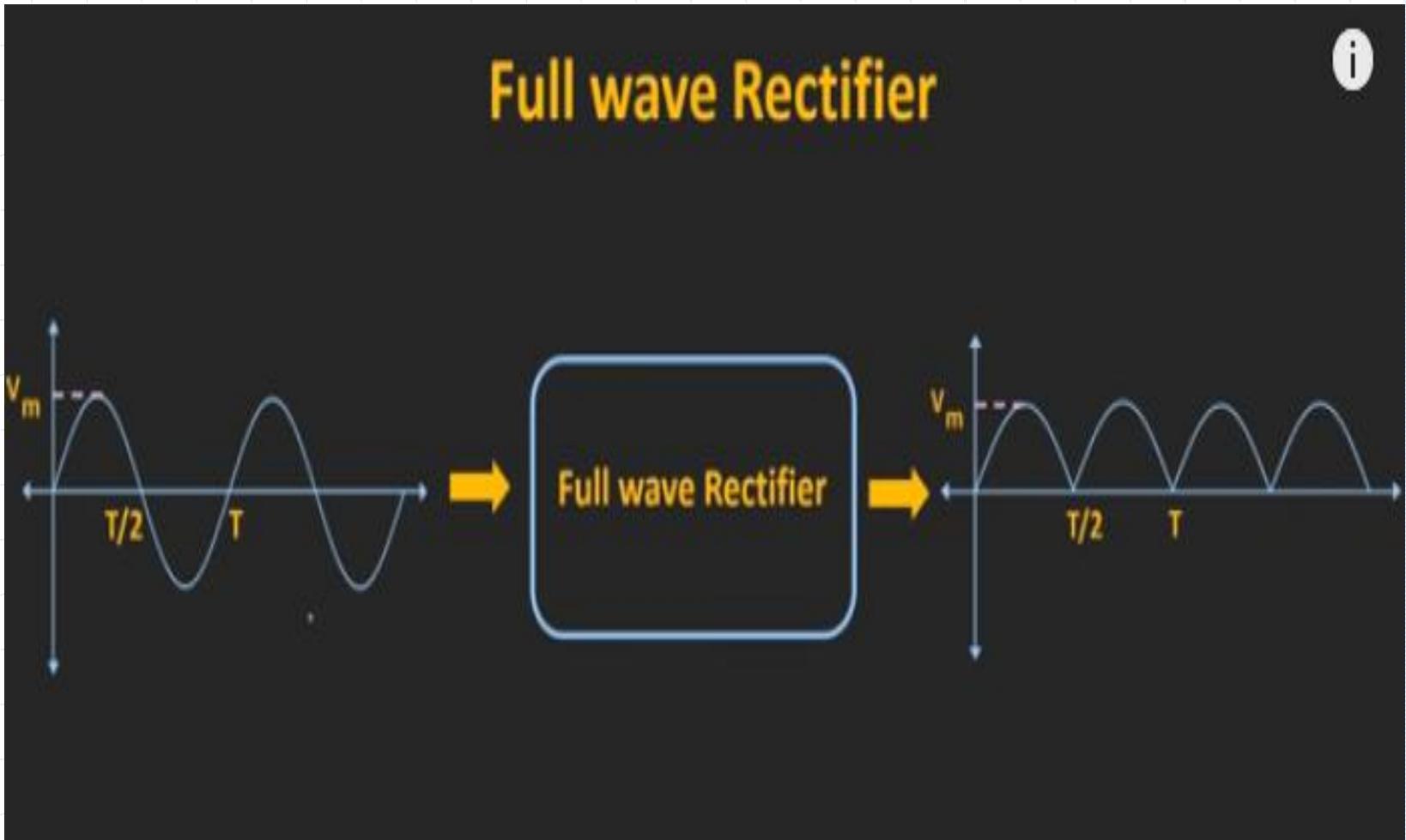
Full-wave rectification produces a greater DC output:

$$\text{Half-wave: } V_{dc} = 0.318 V_m$$

$$\text{Full-wave: } V_{dc} = 0.636 V_m$$



2.7 FULL-WAVE RECTIFICATION



2.7 FULL-WAVE RECTIFICATION

Full wave Rectifier



Center-tapped Transformer

Diode Bridge Circuit

2.7 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. The most familiar network for performing such a function appears in Fig. 2.53 with its four diodes in a bridge configuration.

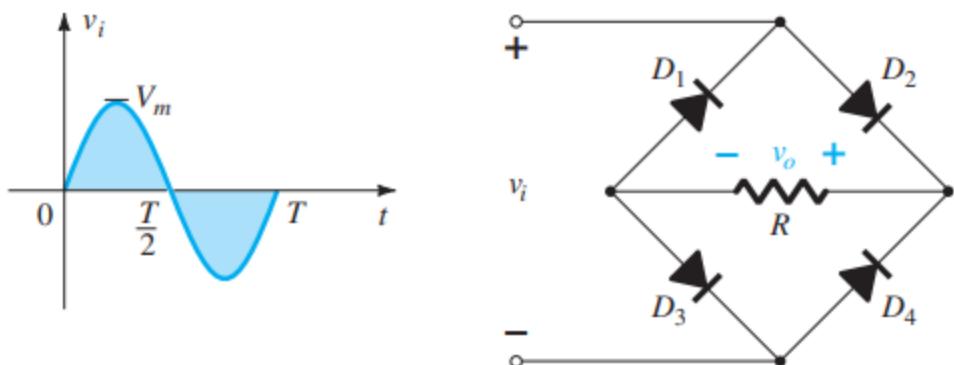


FIG. 2.53

2.7 FULL-WAVE RECTIFICATION

During the period $t=0$ to $T>2$ the polarity of the input is as shown in Fig. 2.54 . The resulting polarities across the ideal diodes are also shown in Fig. 2.54 to reveal that D₂ and D₃ are conducting, whereas D₁ and D₄ are in the “off” state.

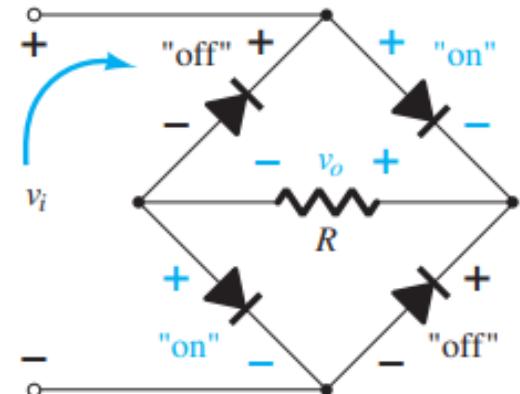


FIG. 2.54

2.7 FULL-WAVE RECTIFICATION

The net result is the configuration of Fig. 2.55 , with its indicated current and polarity across R. Since the diodes are ideal, the load voltage is $v_o = v_i$, as shown in the same figure.

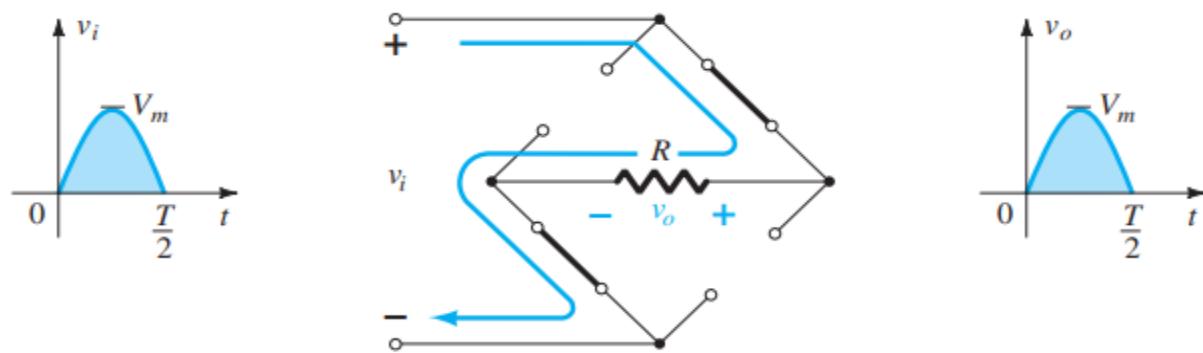


FIG. 2.55

For the negative region of the input the conducting diodes are D1 and D4 , resulting in the configuration of Fig. 2.56 . **The important result is that the polarity across the load resistor R is the same as in Fig. 2.54 , establishing a second positive pulse, as shown in Fig. 2.56 . Over one full cycle the input and output voltages will appear as shown in Fig. 2.57 .**

2.7 FULL-WAVE RECTIFICATION

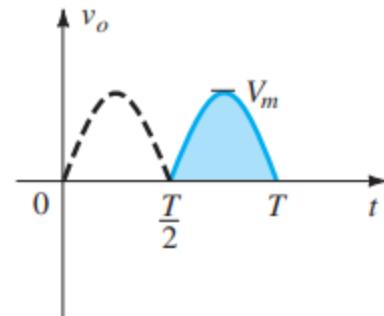
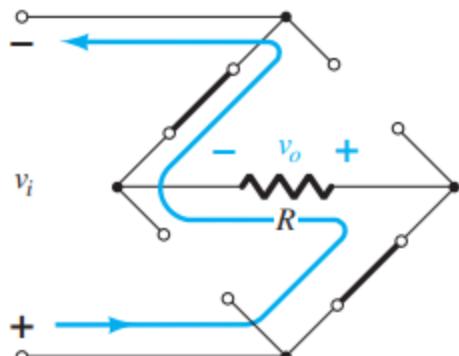
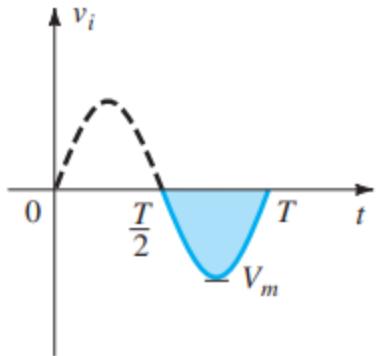


FIG. 2.56

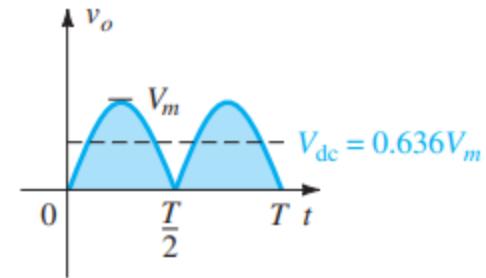
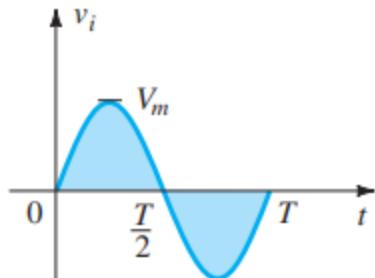


FIG. 2.57

2.7 FULL-WAVE RECTIFICATION

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2[\text{Eq. (2.7)}] = 2(0.318V_m)$$

$$V_{dc} = 0.636 V_m \quad \text{full-wave}$$

(2.10)

If silicon rather than ideal diodes are employed as shown in Fig. 2.58, the application of Kirchhoff's voltage law around the conduction path results in

$$v_i - V_K - v_o - V_K = 0$$

$$v_o = v_i - 2V_K$$

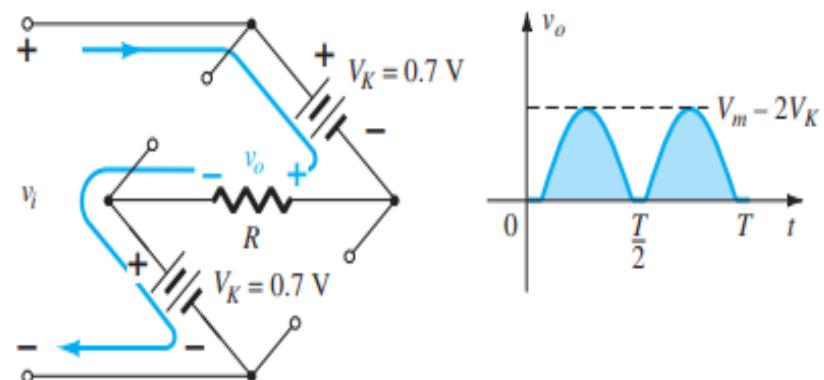


FIG. 2.58

2.7 FULL-WAVE RECTIFICATION

The peak value of the output voltage v_o is therefore

For situations where $V_m \gg 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$V_{dc} \cong 0.636(V_m - 2V_K) \quad (2.11)$$

Then again, if V_m is sufficiently greater than $2V_K$, then Eq. (2.10) is often applied as a first approximation for V_{dc}

2.7 FULL-WAVE RECTIFICATION

PIV The required PIV of each diode (**ideal**) can be determined from Fig. 2.59 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the **PIV** rating is defined by

$$\text{PIV} \geq V_m$$

full-wave bridge rectifier

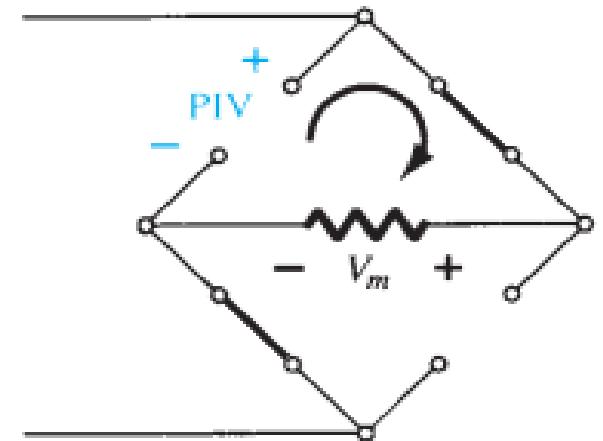
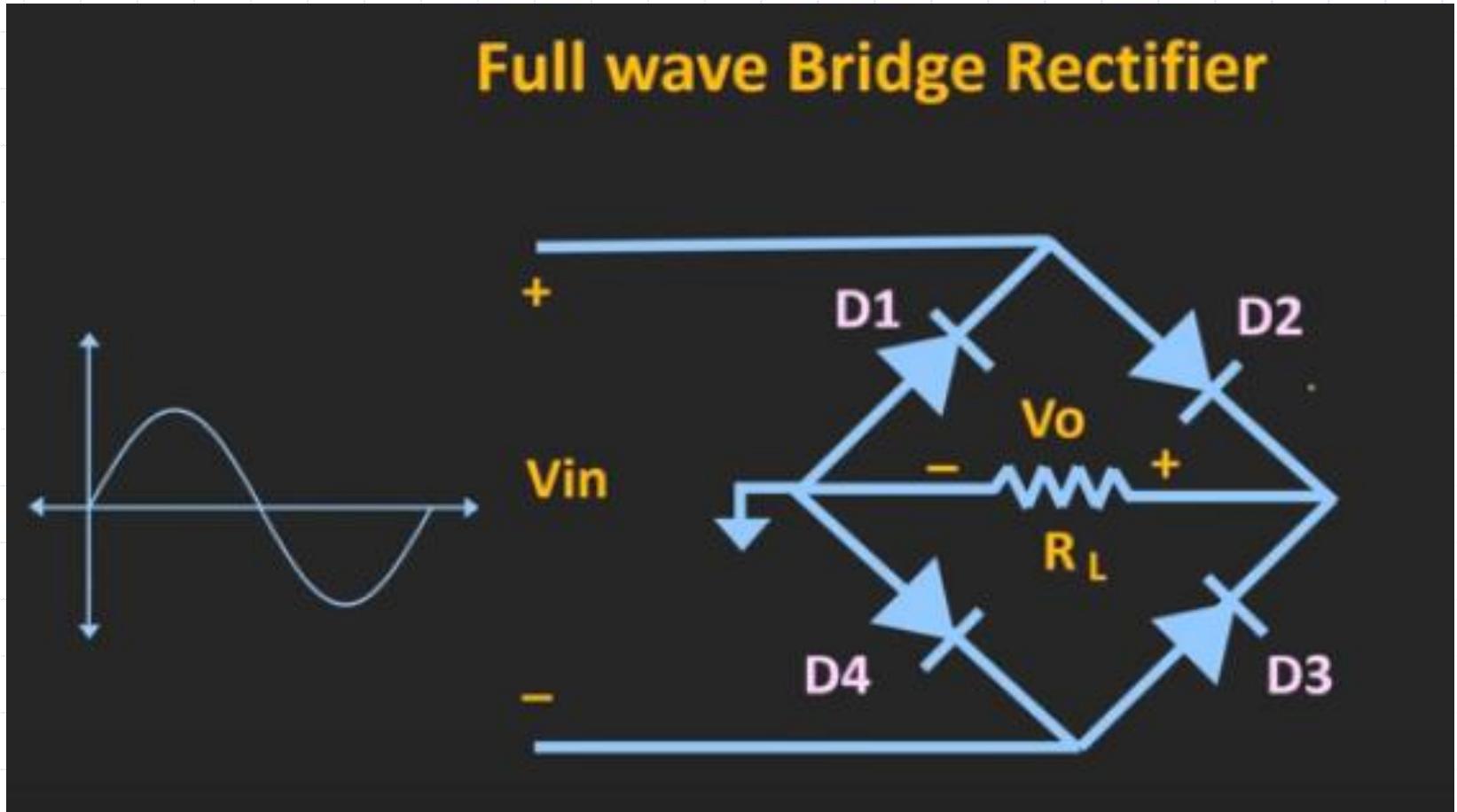
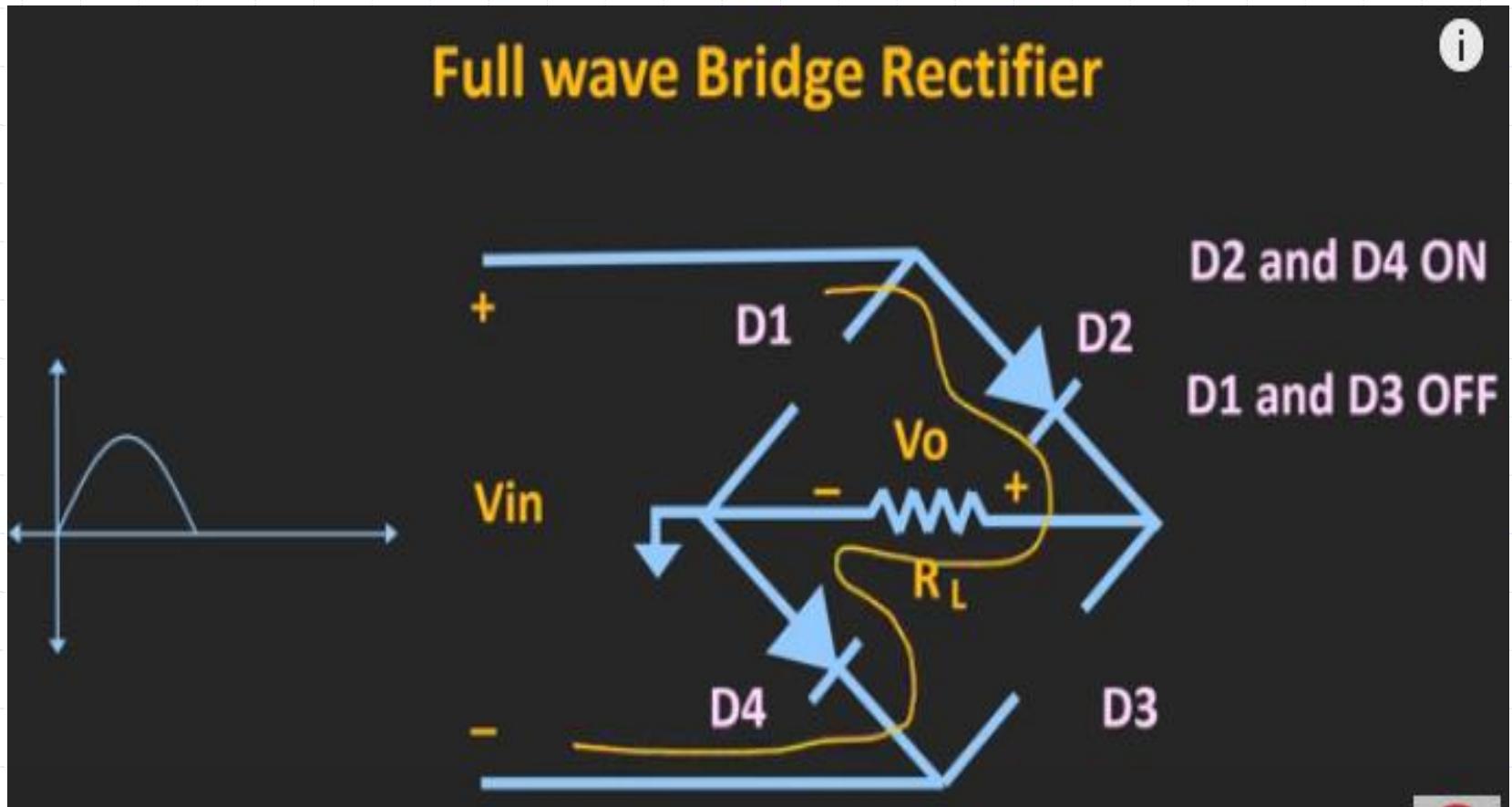


FIG. 2.59

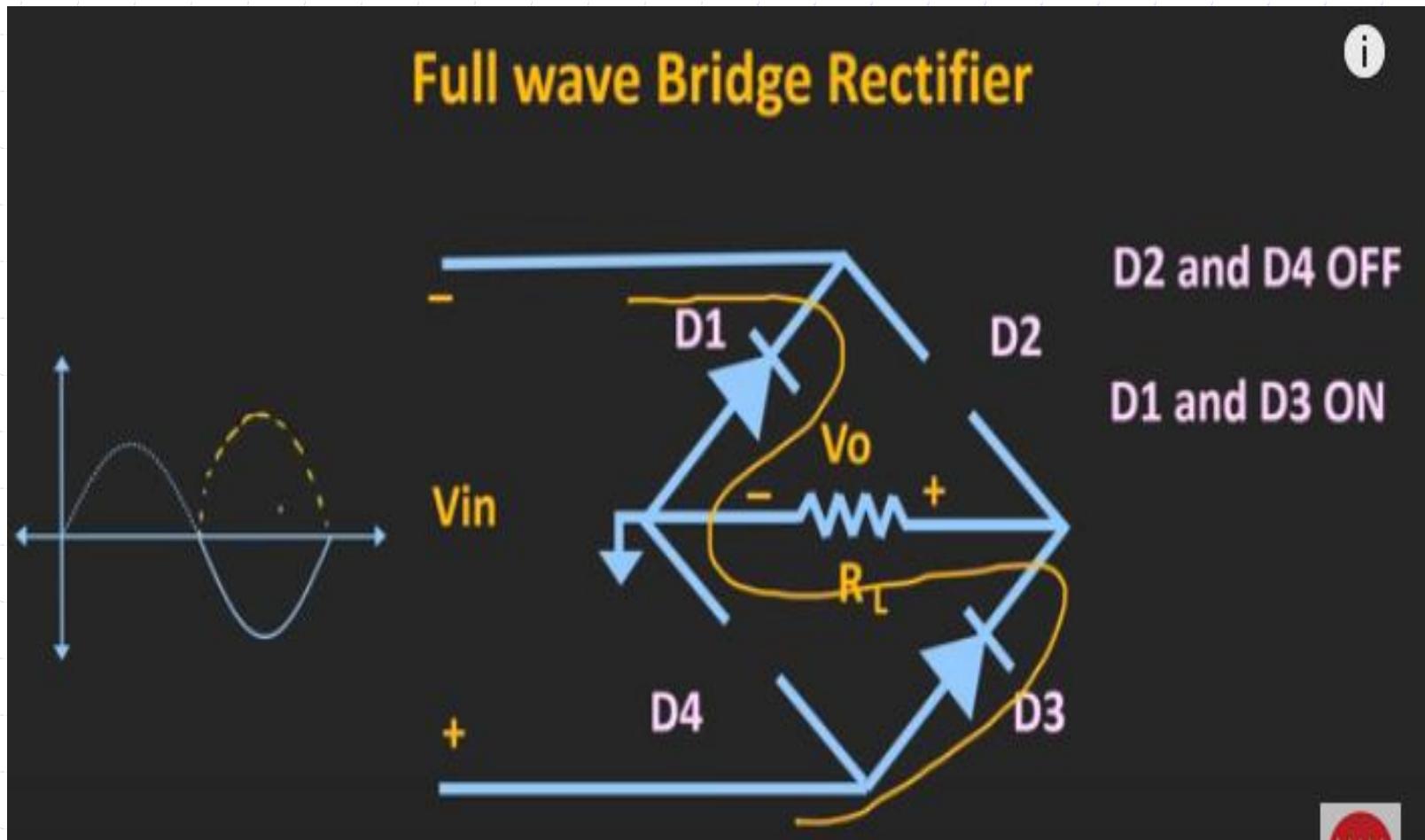
2.7 FULL-WAVE RECTIFICATION



2.7 FULL-WAVE RECTIFICATION

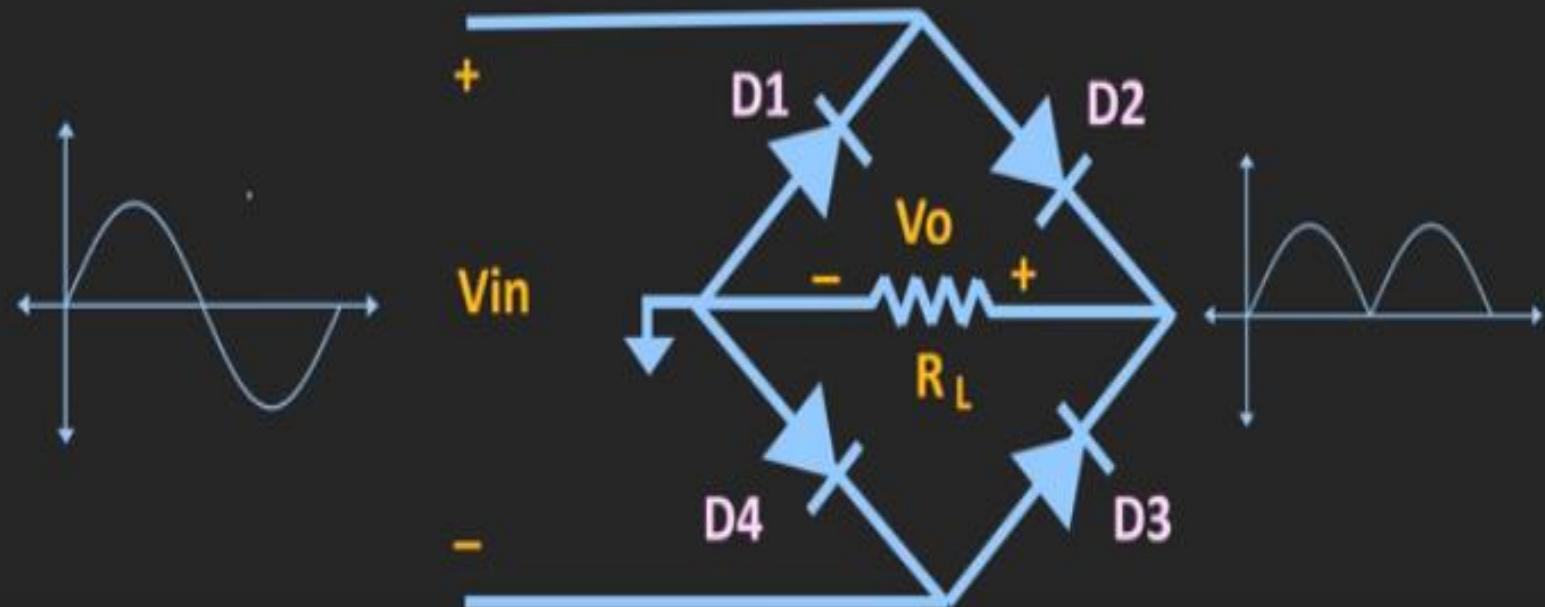


2.7 FULL-WAVE RECTIFICATION

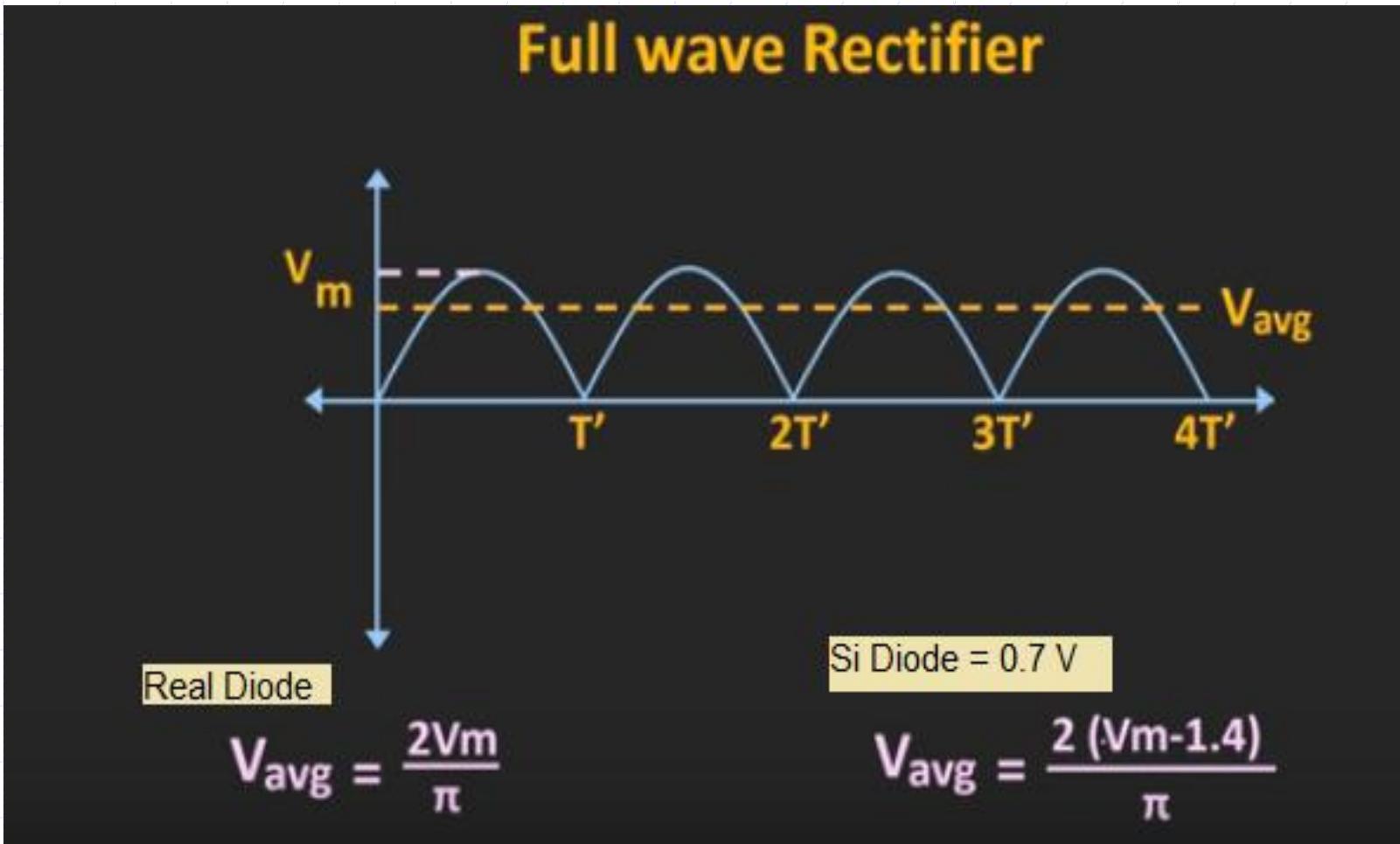


2.7 FULL-WAVE RECTIFICATION

Full wave Bridge Rectifier



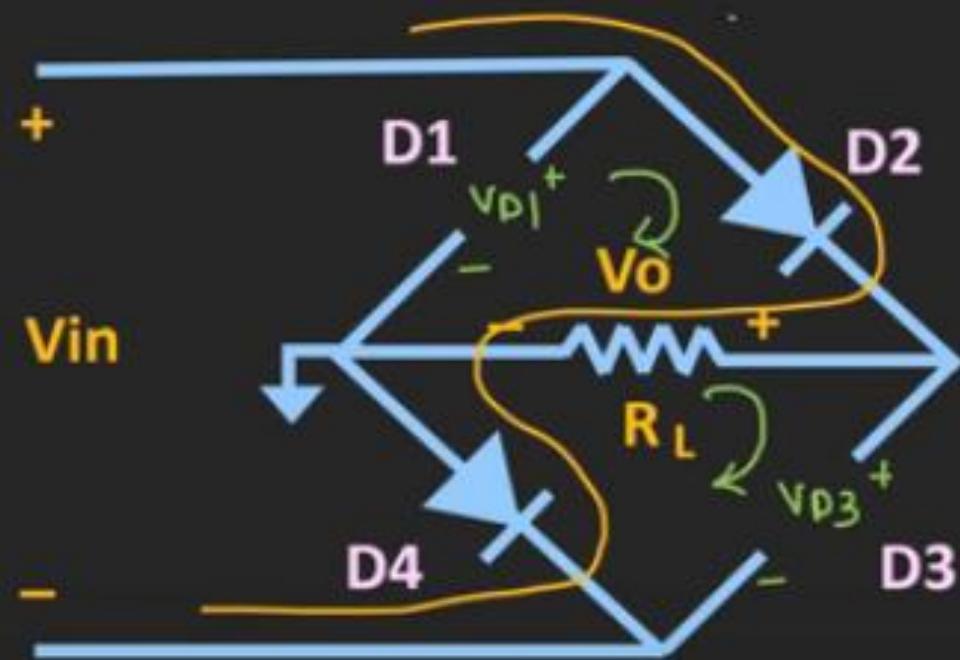
2.7 FULL-WAVE RECTIFICATION



2.7 FULL-WAVE RECTIFICATION

Full wave Bridge Rectifier (PIV)

Peak Inverse Voltage



$$V_{DI} = V_o$$

$$V_{DI} = V_{in}$$

$$\underline{PIV = V_m}$$

2.7 FULL-WAVE RECTIFICATION

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a **center-tapped (CT) transformer** to establish the input signal across each section of the secondary of the transformer

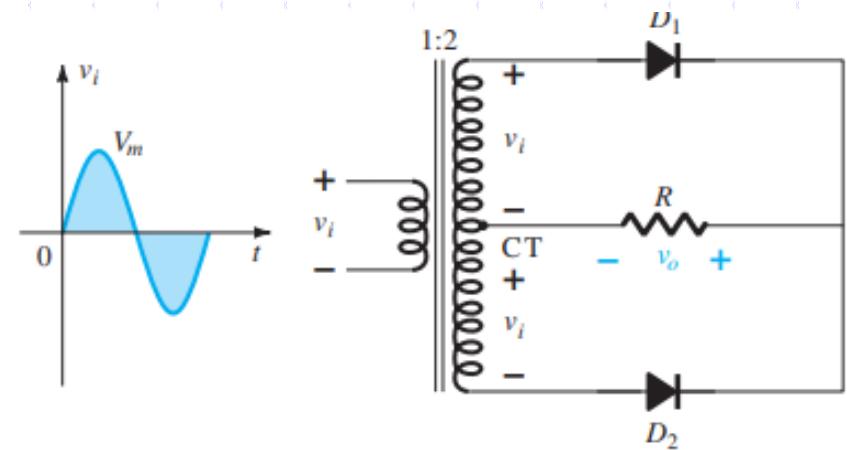


FIG. 2.60

2.7 FULL-WAVE RECTIFICATION

During the **positive portion of v_i** applied to the primary of the transformer, the network will appear as shown in Fig. 2.61 with a positive pulse across each section of the secondary coil. D1 assumes the short-circuit equivalent and D2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.61 .

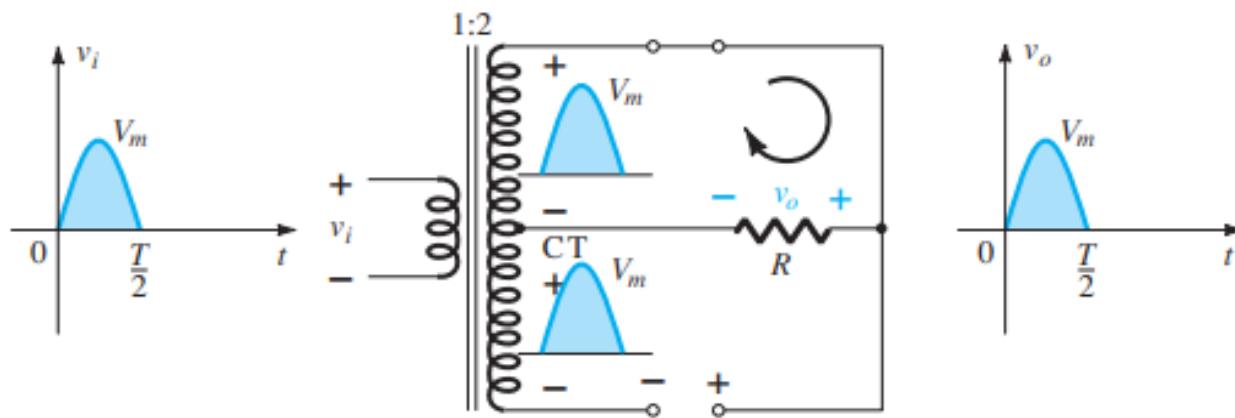


FIG. 2.61

2.7 FULL-WAVE RECTIFICATION

During the **negative portion** of the input the network appears as shown in Fig. 2.62 , reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor R. The net effect is the same output as that appearing in Fig. 2.57 with the same dc levels.

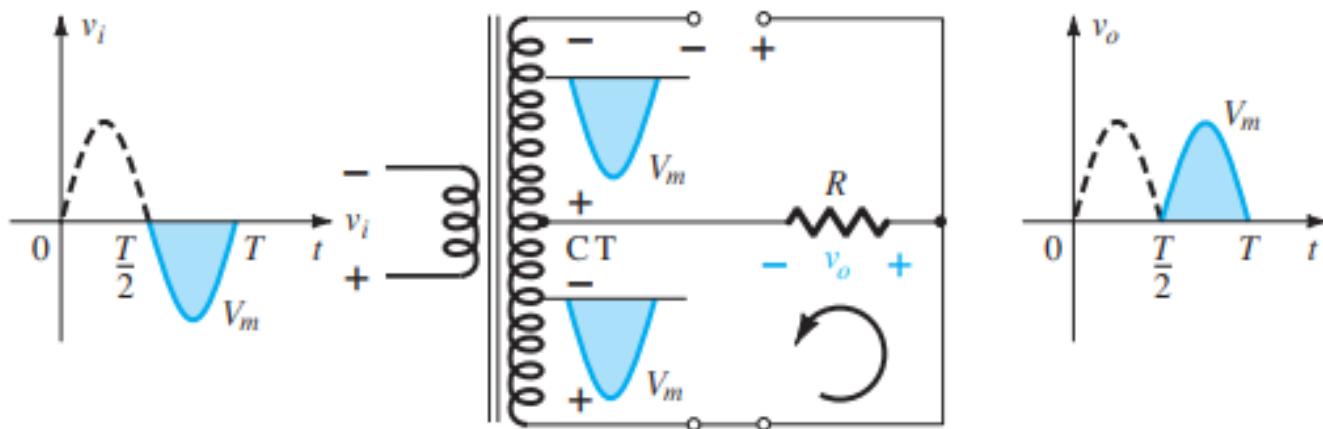


FIG. 2.62

2.7 FULL-WAVE RECTIFICATION

PIV The network of Fig. 2.63 will help us determine the net **PIV** for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

$$\begin{aligned} \text{PIV} &= V_{\text{secondary}} + V_R \\ &= V_m + V_m \end{aligned} \tag{2.13}$$

$$\text{PIV} \geq 2V_m$$

CT transformer, full-wave rectifier

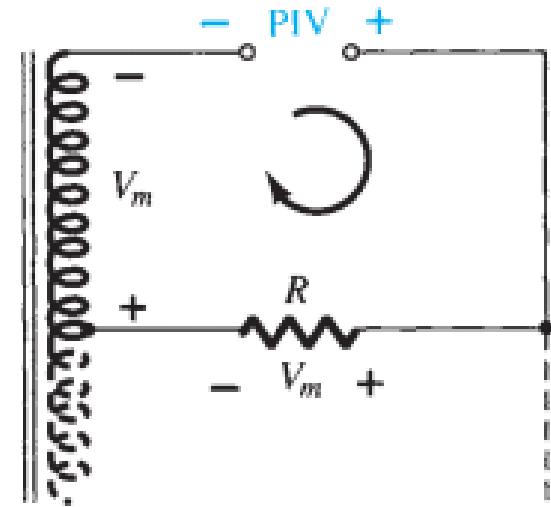
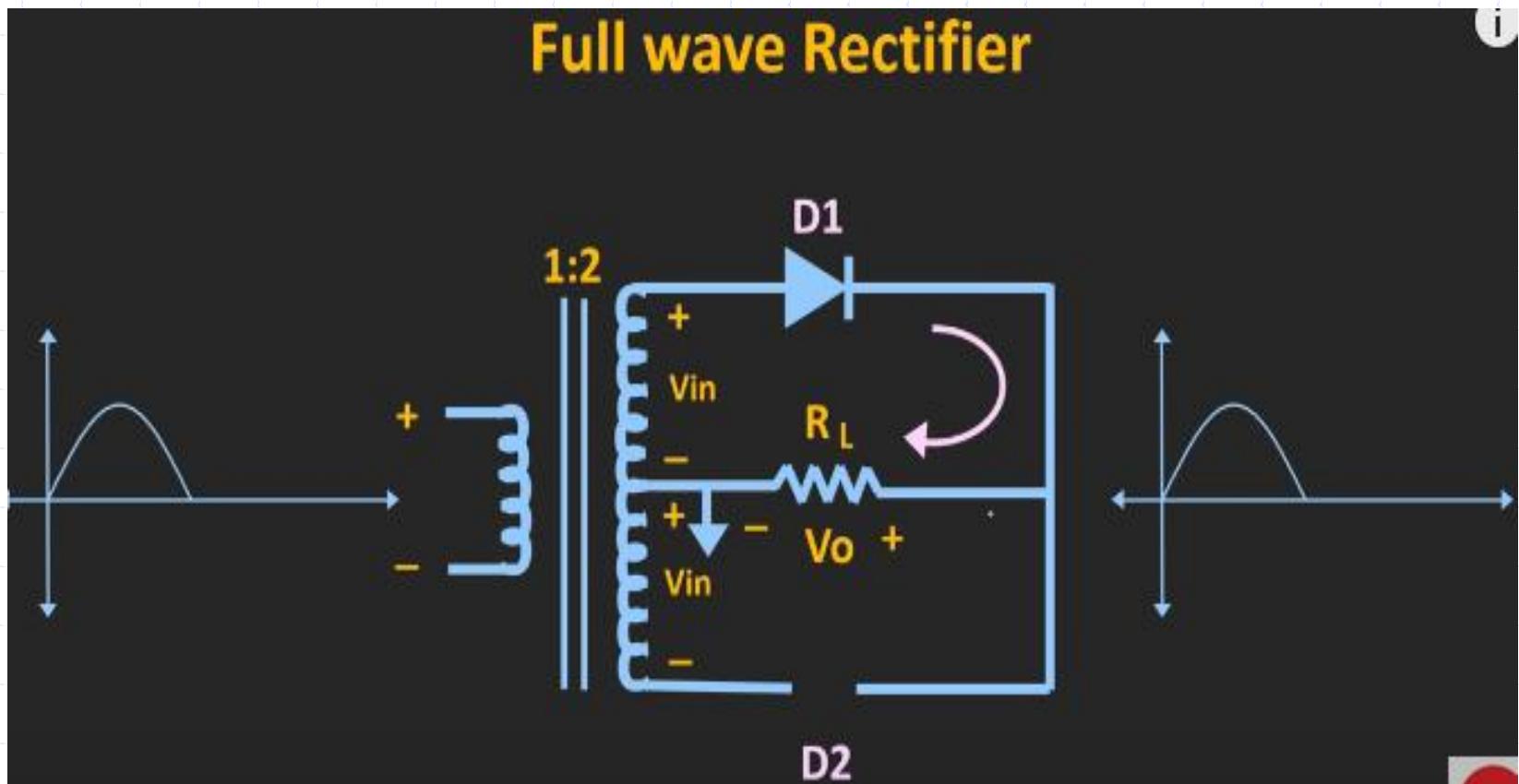
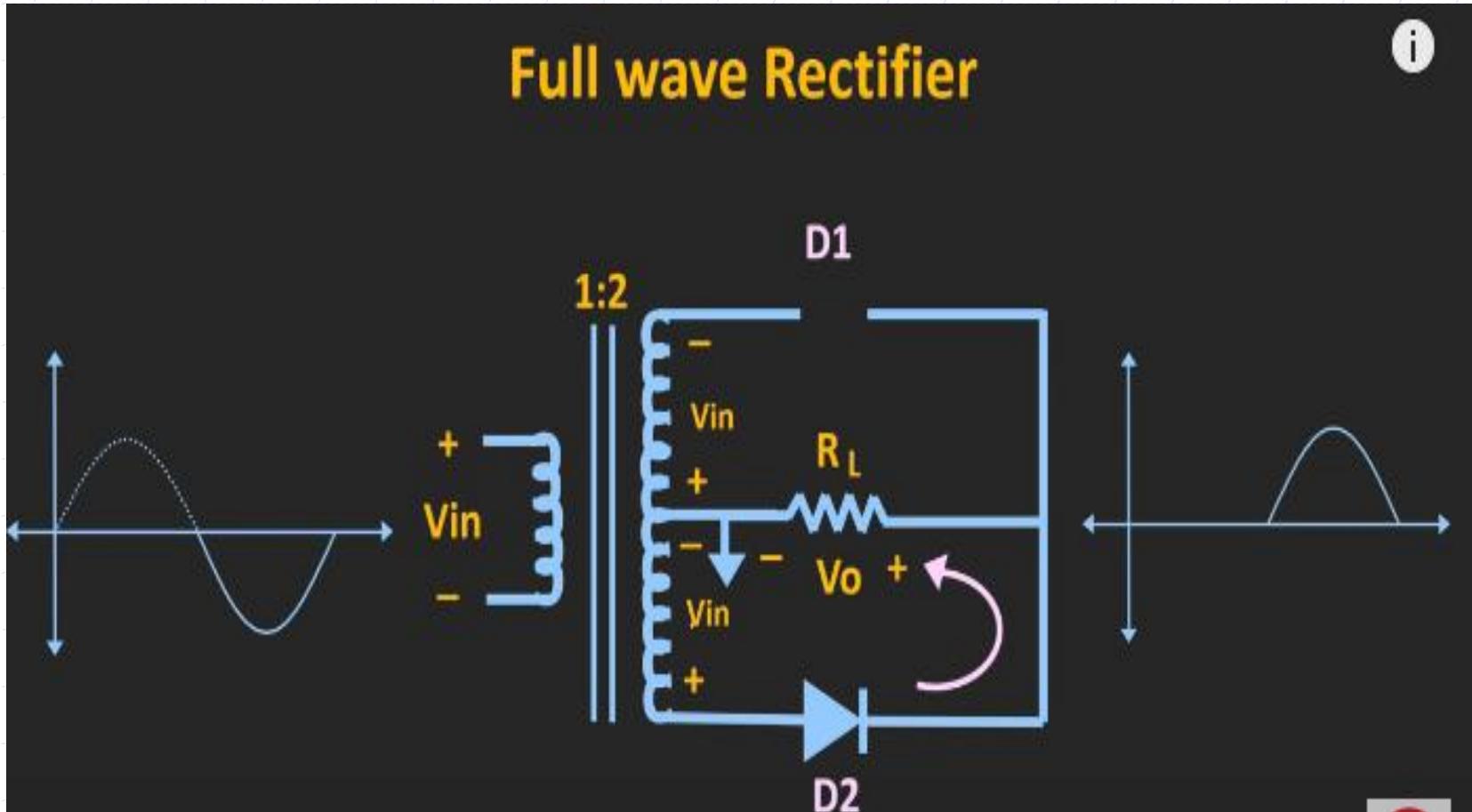


FIG. 2.63

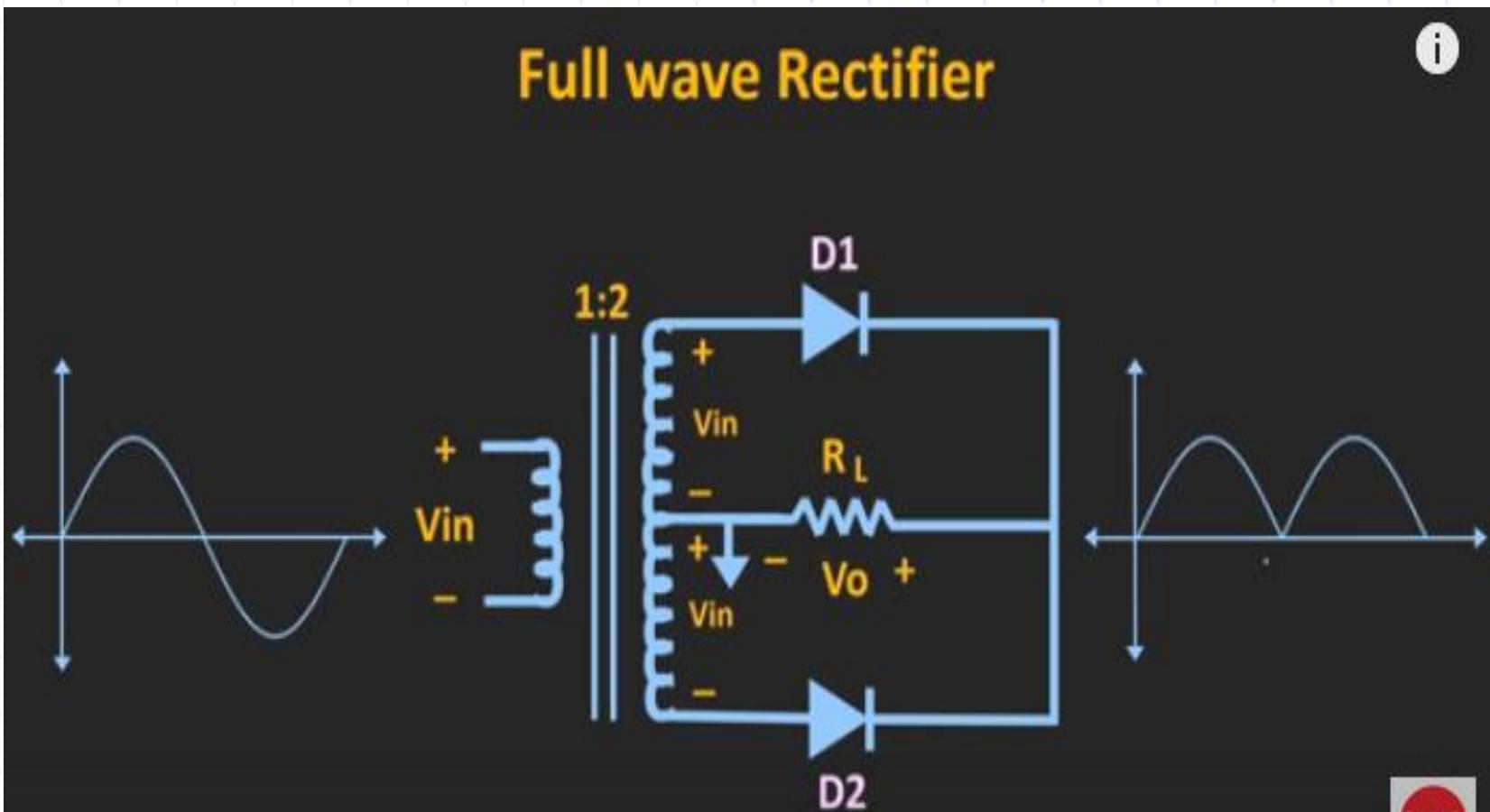
2.7 FULL-WAVE RECTIFICATION



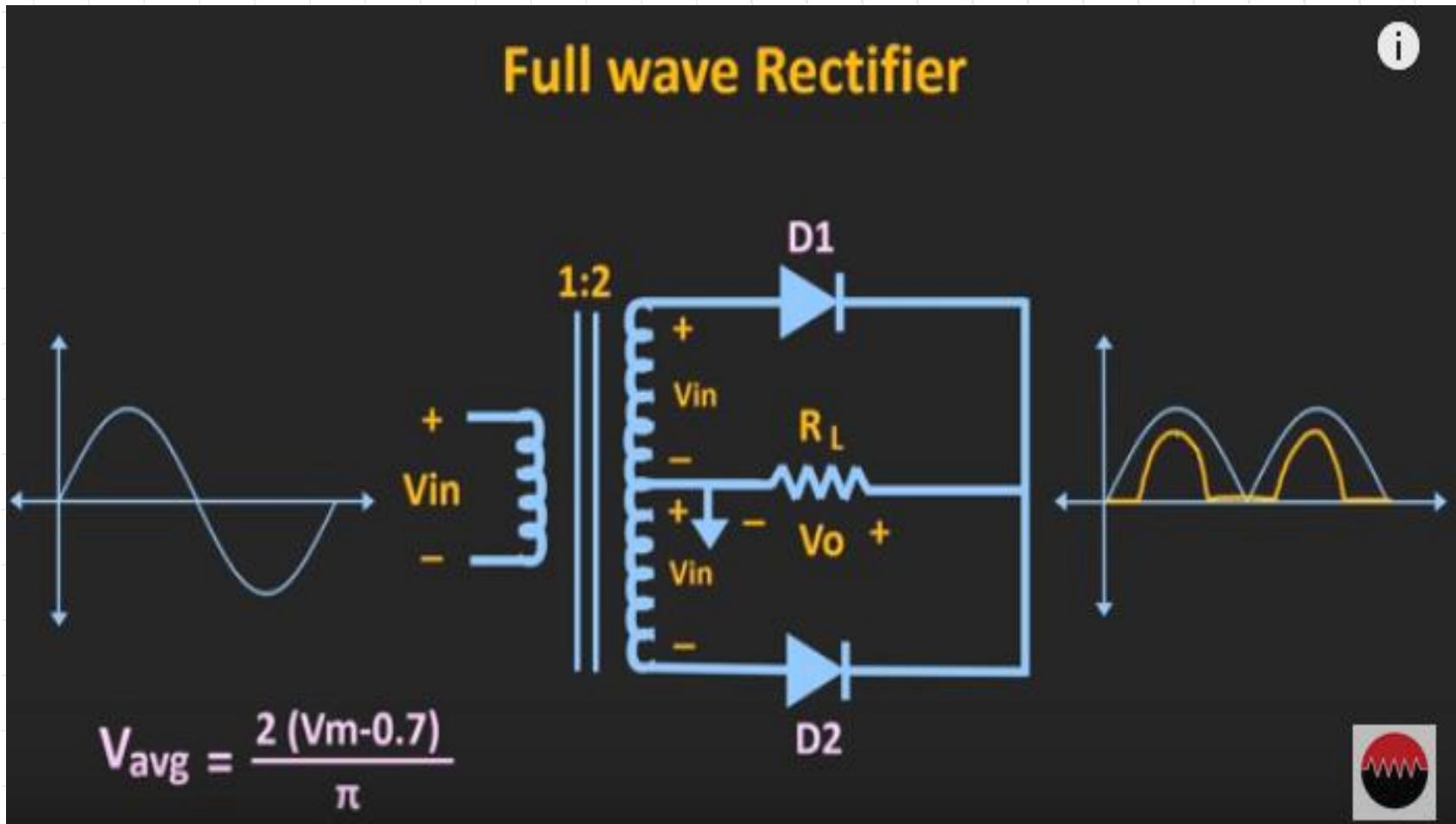
2.7 FULL-WAVE RECTIFICATION



2.7 FULL-WAVE RECTIFICATION



2.7 FULL-WAVE RECTIFICATION



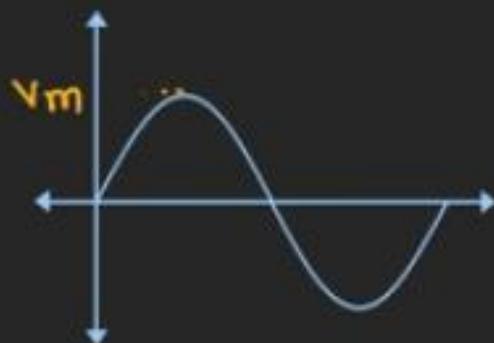
2.7 FULL-WAVE RECTIFICATION

Full wave Rectifier (PIV)

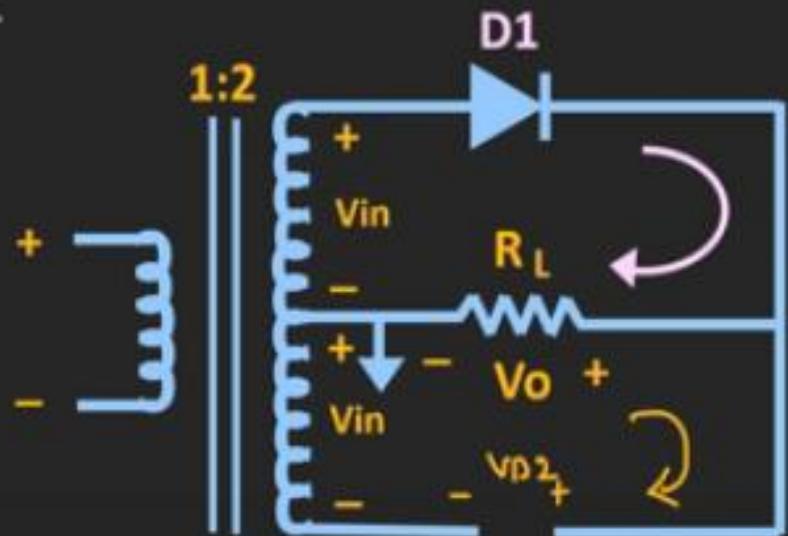
Peak Inverse Voltage

$$V_{in} + V_o = V_{D2}$$

$$\therefore V_{D2} = 2V_{in}$$



$$PIV = 2Vm$$



D2

2.7 FULL-WAVE RECTIFICATION

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where

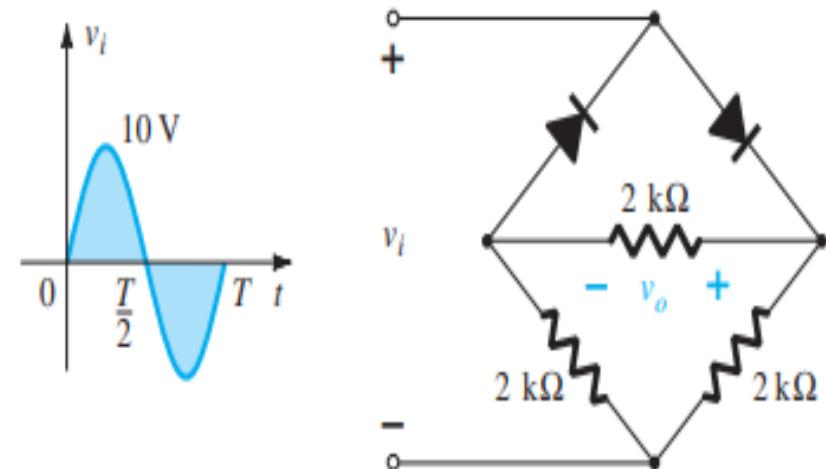


FIG. 2.64

$$V_o = (1/2)V_i \text{ or } V_{o\max} = (1/2)V_{i\max} = 1/2(10 \text{ V}) = 5 \text{ V},$$

2.7 FULL-WAVE RECTIFICATION

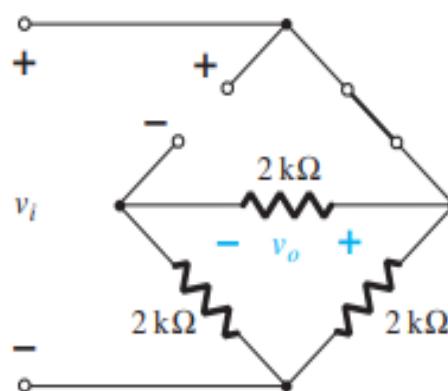
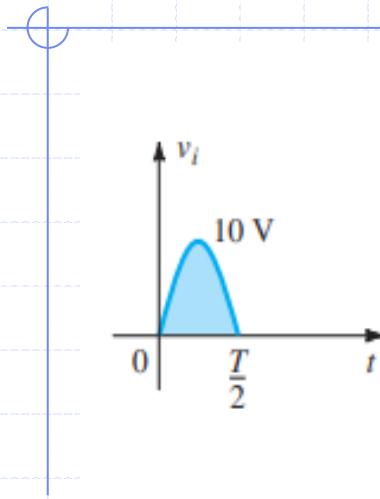


FIG. 2.65

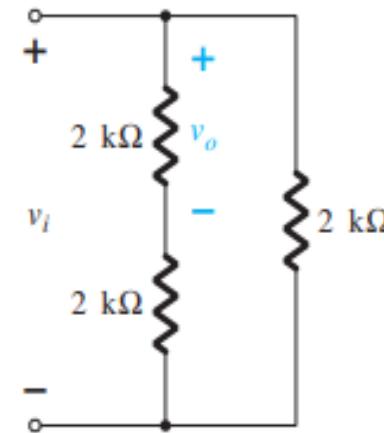
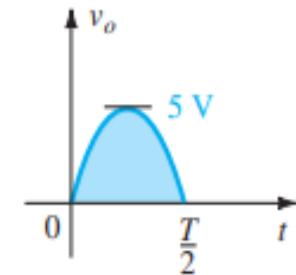


FIG. 2.66



as shown in Fig. 2.66 . For the negative part of the input, the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

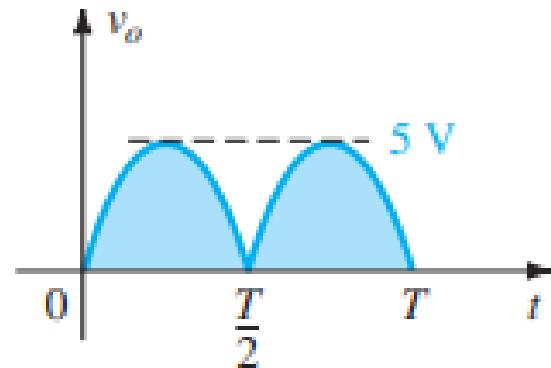


FIG. 2.67

2.7 FULL-WAVE RECTIFICATION

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5 \text{ V}) = 3.18 \text{ V}$$

However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R, which is 5 V, or half of that required for a half-wave rectifier with the same input.

2.11 ZENER DIODES

The analysis of networks employing **Zener diodes** is quite similar to the analysis of **semiconductor diodes** in previous sections. Figure 2.108 reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point.

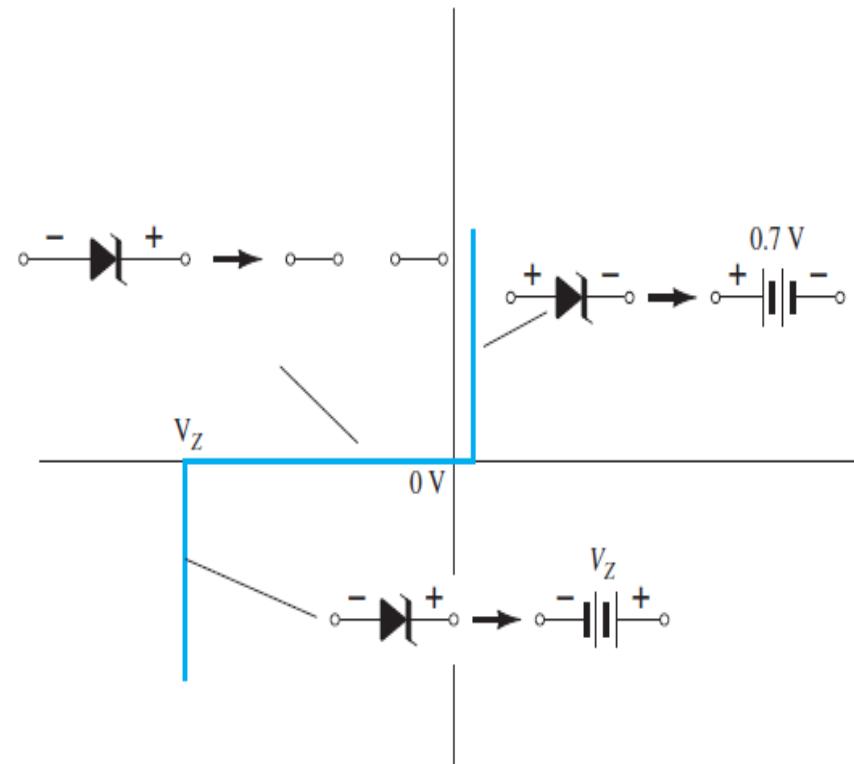


FIG. 2.108

2.11 Zener Diodes

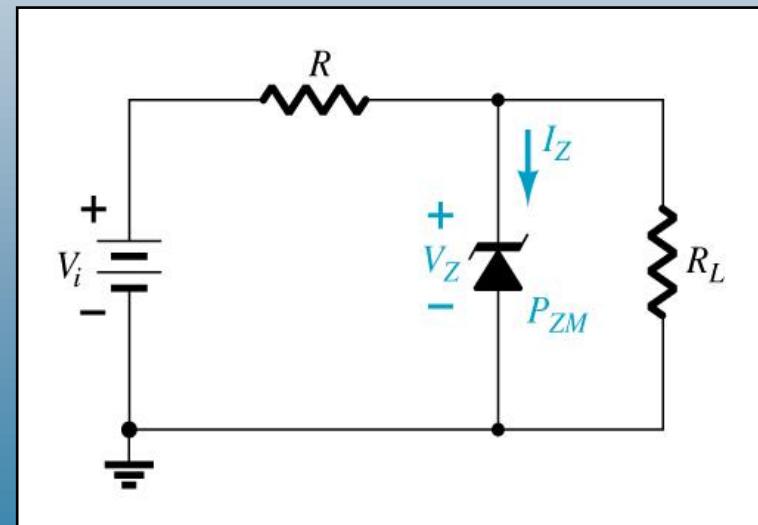
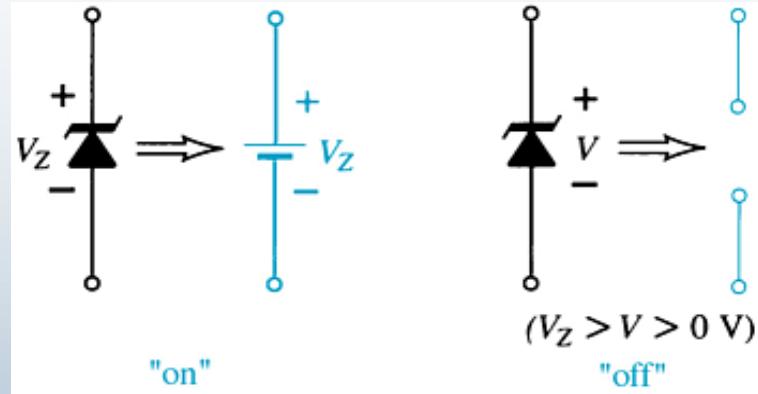
The Zener is a diode that is operated in reverse bias at the Zener Voltage (V_z).

When $V_i \geq V_z$

- The Zener is on
- Voltage across the Zener is V_z
- Zener current: $I_z = I_R - I_{RL}$
- The Zener Power: $P_z = V_z I_z$

When $V_i < V_z$

- The Zener is off
- The Zener acts as an open circuit



2.11 Zener Resistor Values

If R is too large, the Zener diode cannot conduct because $I_Z < I_{ZK}$. The minimum current is given by:

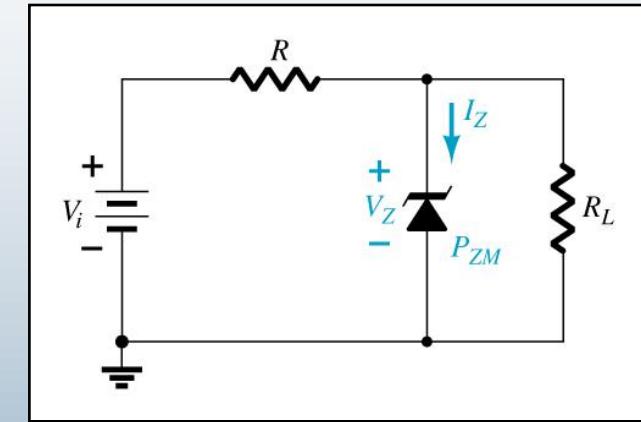
$$I_{Lmin} = I_R - I_{ZK}$$

The *maximum* value of resistance is:

$$R_{Lmax} = \frac{V_z}{I_{Lmin}}$$

If R is too small, $I_Z > I_{ZM}$. The maximum allowable current for the circuit is given by

The *minimum* value of resistance is:

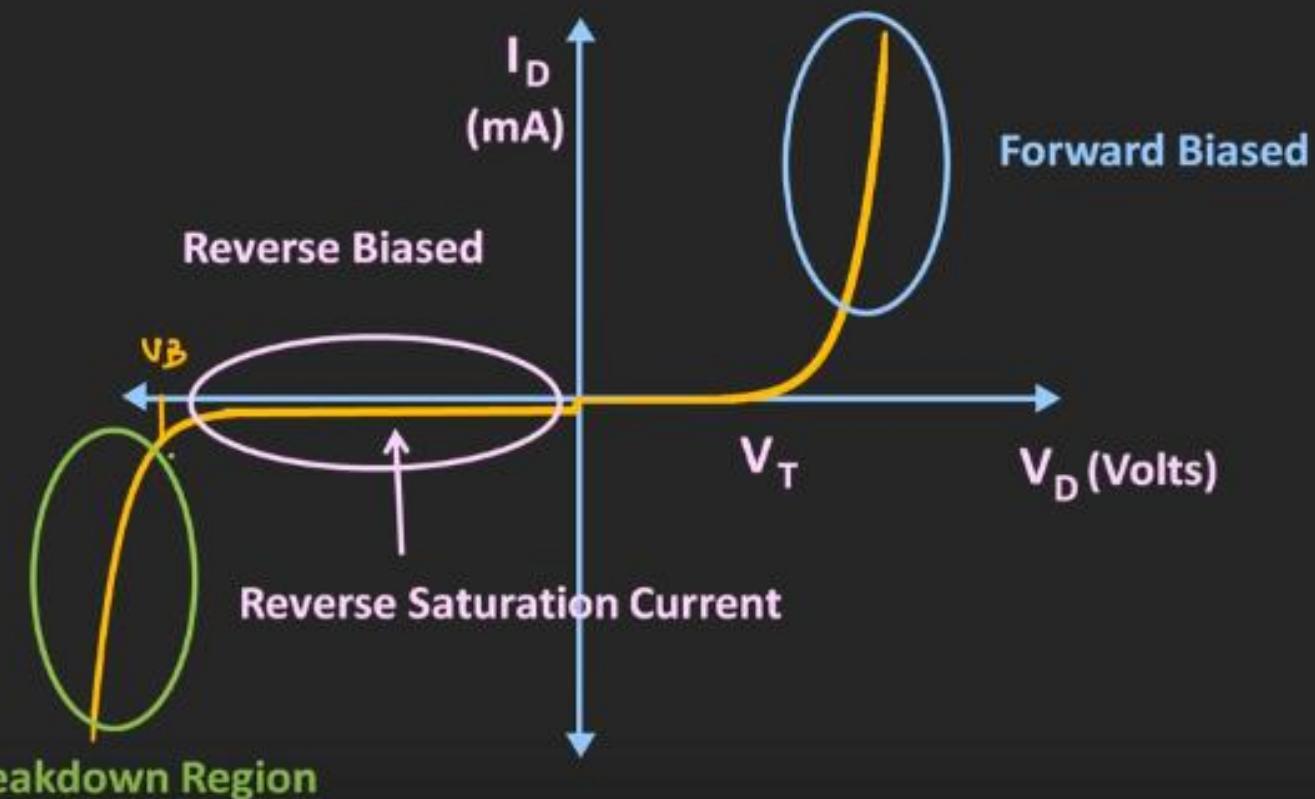


$$I_{Lmax} = \frac{V_L}{R_L} = \frac{V_z}{R_{Lmin}}$$

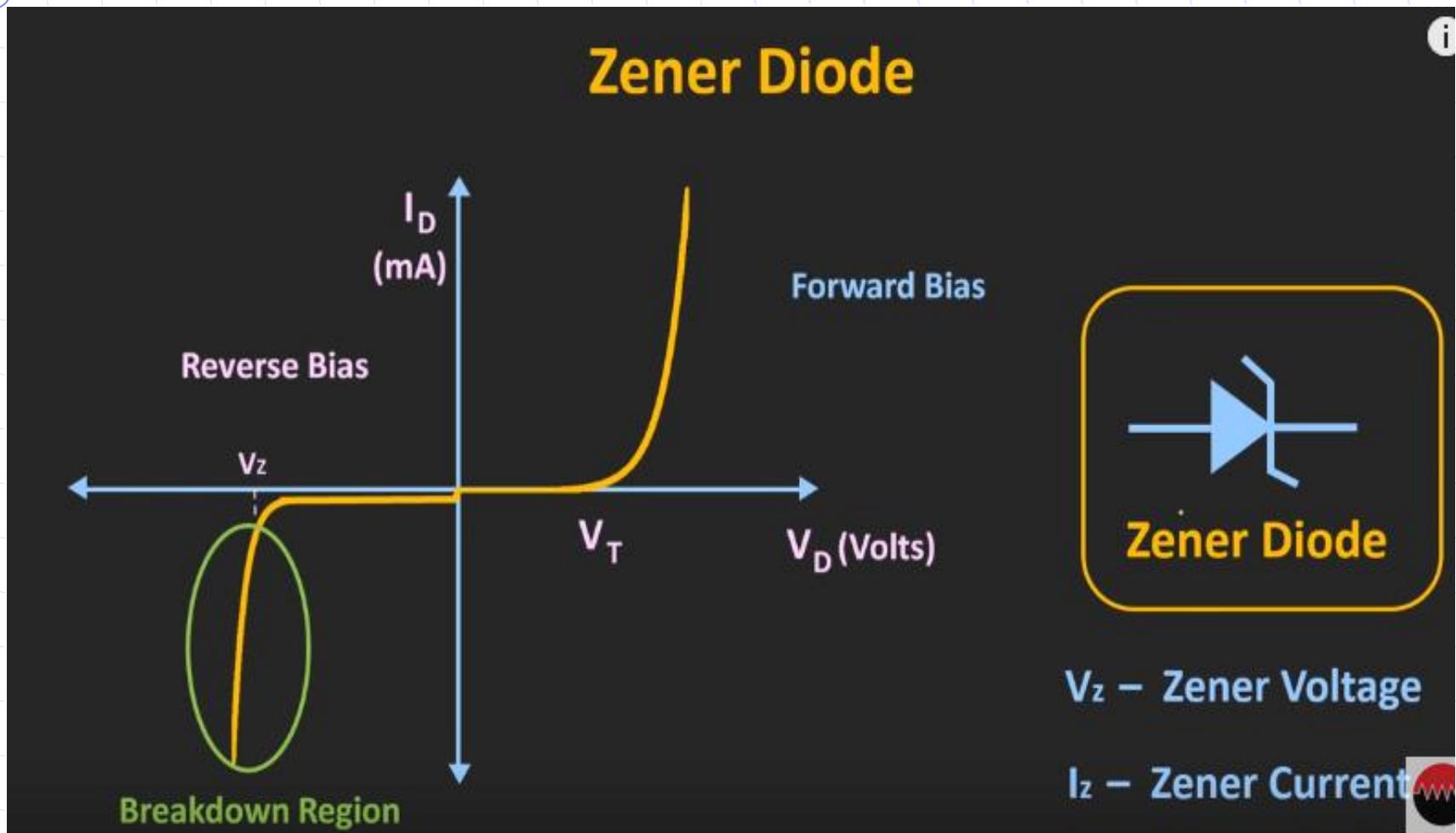
$$R_{Lmin} = \frac{RV_z}{V_i - V_z}$$

2.11 ZENER DIODES

V-I characteristics of PN junction diode

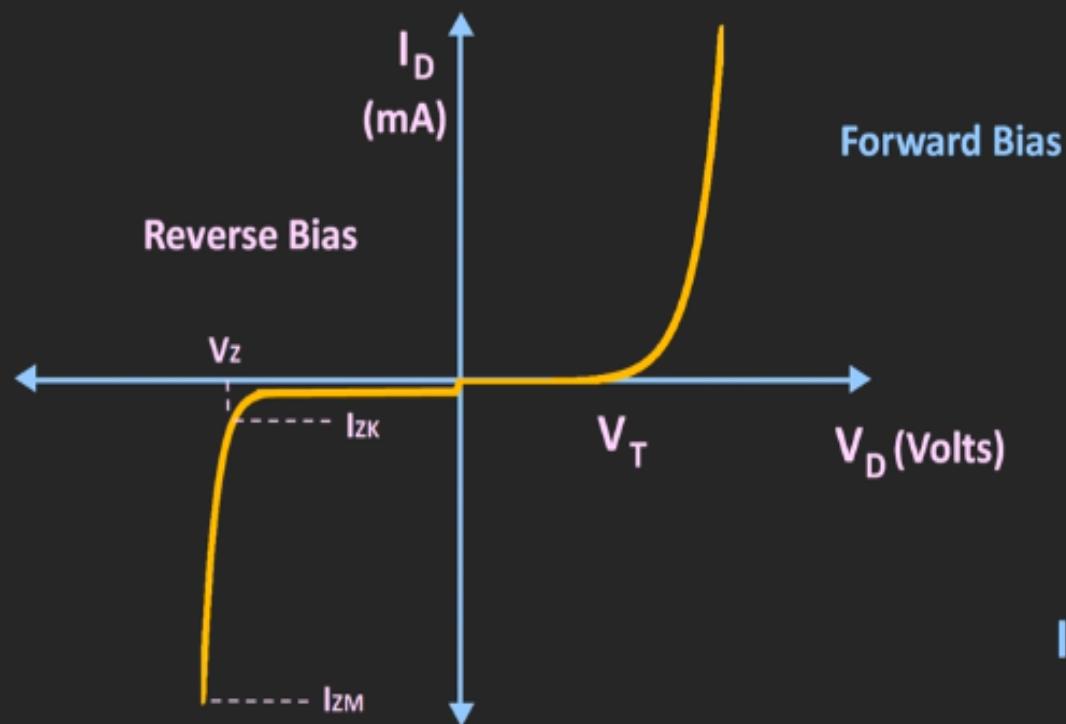


2.11 ZENER DIODES



2.11 ZENER DIODES

Zener Diode



Zener Diode

I_{zK} – Minimum Zener Current

I_{zM} – Maximum Zener Current

2.11 ZENER DIODES

EXAMPLE 2.24 Determine the reference voltages provided by the network of Fig. 2.109 , which uses a white LED to indicate that the power is on. What is the level of current through the LED and the power delivered by the supply? How does the power absorbed by the LED compare to that of the 6-V Zener diode?

Solution: First we have to check that there is sufficient applied voltage to turn on all the series diode elements. The **white LED** will have a drop of about 4 V across it, the **6-V** and **3.3-V Zener diodes** have a total of 9.3 V, and the forward-biased silicon diode has 0.7 V, for a total of 14 V.

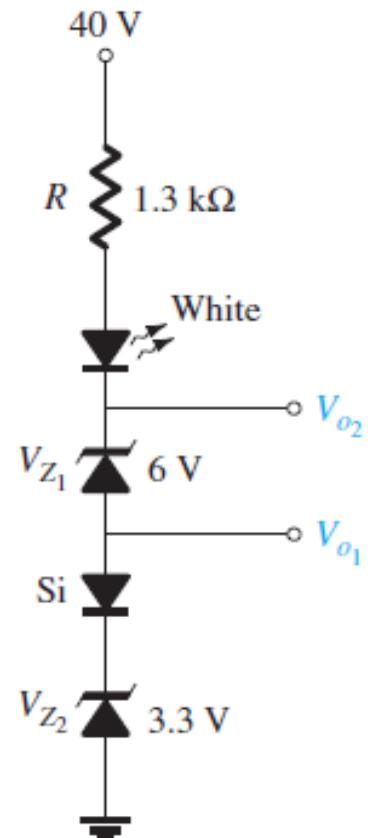


FIG. 2.109

2.11 ZENER DIODES

The applied 40 V is then sufficient to turn on all the elements and, one hopes, establish a proper operating current

Note that the silicon diode was used to create a reference voltage of 4 V because

$$V_{o1} = V_{z2} + V_K = 3.3 \text{ V} + 0.7 \text{ V} = 4.0 \text{ V}$$

Combining the voltage of the 6-V Zener diode with the 4 V results in

$$V_{o2} = V_{o1} + V_{z1} = 4 \text{ V} + 6 \text{ V} = 10 \text{ V}$$

Finally, the 4 V across the white LED will leave a voltage of $40 \text{ V} - 14 \text{ V} = 26 \text{ V}$ across the resistor, and

$$I_R = I_{\text{LED}} = \frac{V_R}{R} = \frac{40 \text{ V} - V_{o2} - V_{\text{LED}}}{1.3 \text{ k}\Omega} = \frac{40 \text{ V} - 10 \text{ V} - 4 \text{ V}}{1.3 \text{ k}\Omega} = \frac{26 \text{ V}}{1.3 \text{ k}\Omega} = 20 \text{ mA}$$

2.11 ZENER DIODES

which should establish the proper brightness for the LED.

The power delivered by the supply is simply the product of the supply voltage and current drain as follows:

$$P_s = EI_s = EI_R = (40 \text{ V})(20 \text{ mA}) = 800 \text{ mW}$$

The power absorbed by the LED is

$$P_{\text{LED}} = V_{\text{LED}}I_{\text{LED}} = (4 \text{ V})(20 \text{ mA}) = 80 \text{ mW}$$

and the power absorbed by the 6-V Zener diode is

$$P_Z = V_ZI_Z = (6 \text{ V})(20 \text{ mA}) = 120 \text{ mW}$$

The power absorbed by the Zener diode exceeds that of the LED by 40 mW.

2.11 ZENER DIODES

EXAMPLE 2.25 The network of Fig. 2.110 is designed to limit the voltage to 20 V during the positive portion of the applied voltage and to 0 V for a negative excursion of the applied voltage. Check its operation and plot the waveform of the voltage across the system for the applied signal. Assume the system has a very high input resistance so it will not affect the behavior of the network

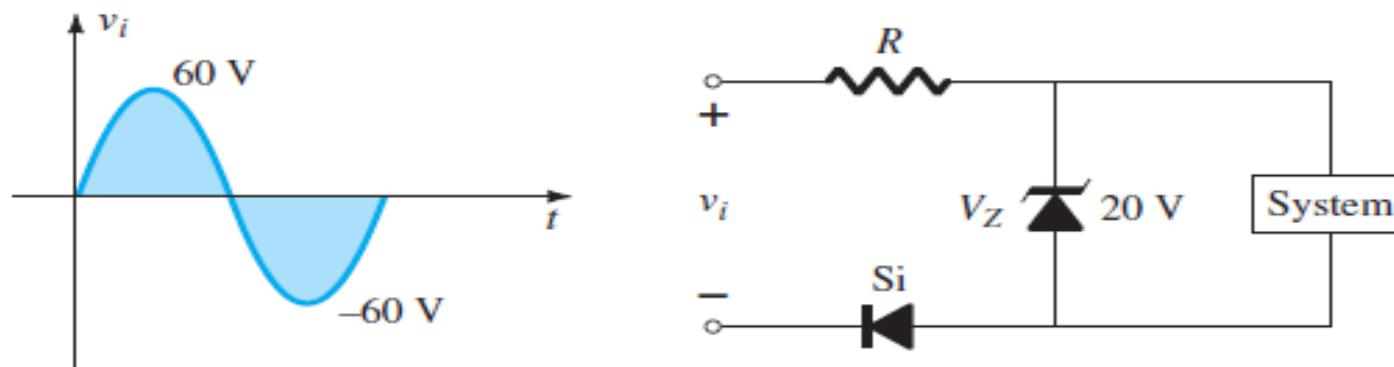


FIG. 2.110

2.11 ZENER DIODES

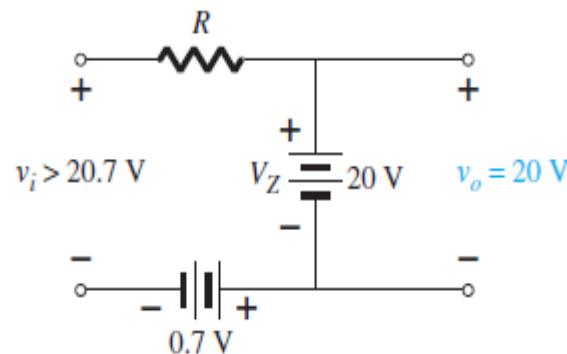
Solution: For positive applied voltages less than the Zener potential of 20 V the **Zener diode** will be in its approximate **open-circuit state**, and the input signal will simply distribute itself across the elements, with the majority going to the system because it has such a high resistance level.

Once the voltage across the Zener diode reaches 20 V the Zener diode will turn on as shown in Fig. 2.111a and the voltage across the system will lock in at 20 V.

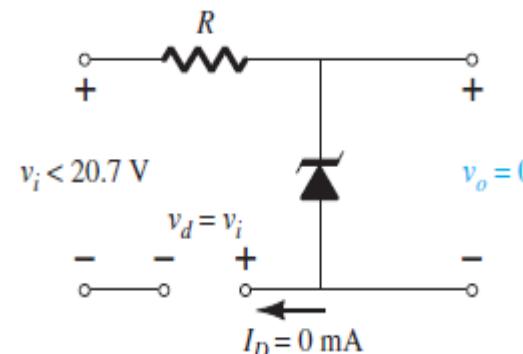
For the negative region of the applied signal the **silicon diode** is reverse biased and presents an open circuit to the series combination of elements. The result is that the full negatively applied signal will appear across the open-circuited diode and the negative voltage across the system locked in at 0 V, as shown in Fig. 2.111b

2.11 ZENER DIODES

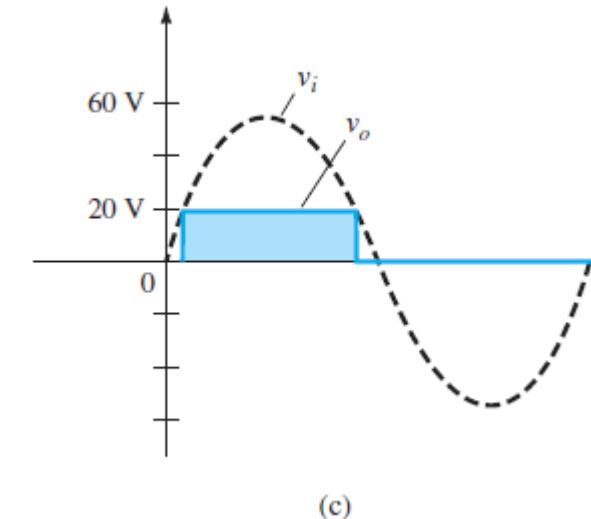
(a)



(a)



(b)



(c)

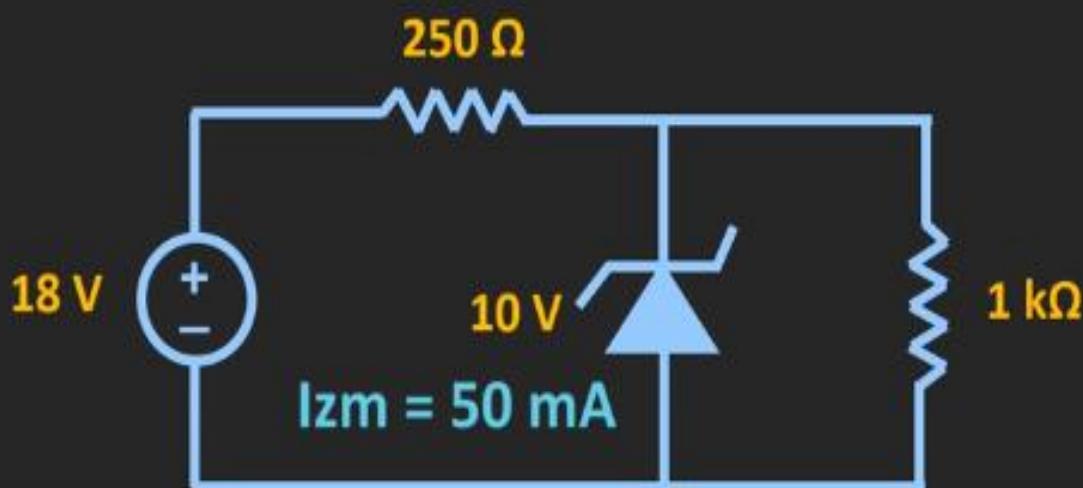
FIG. 2.111

The voltage across the system will therefore appear as shown in Fig. 2.111c .

2.11 ZENER DIODES

Example 1

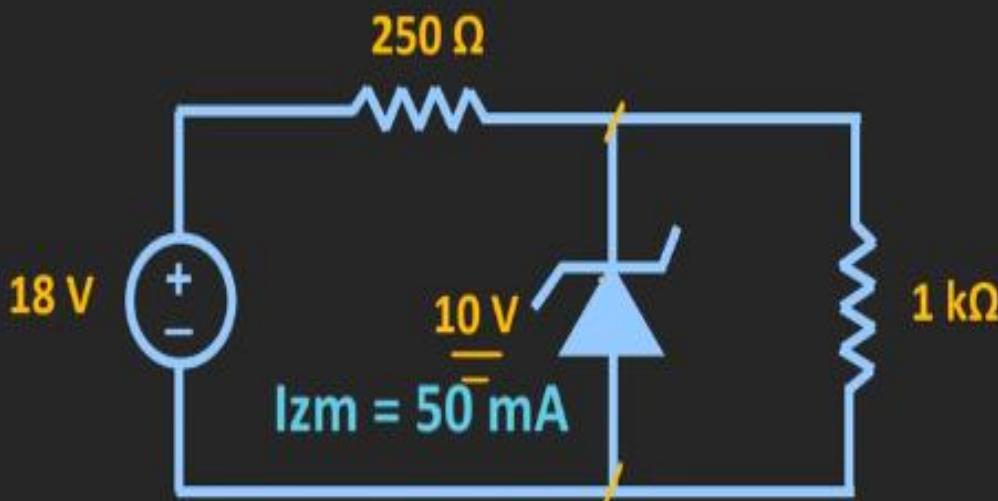
Find the Zener current and power dissipated across Zener diode



2.11 ZENER DIODES

Example 1

Find the Zener current and power dissipated across Zener diode



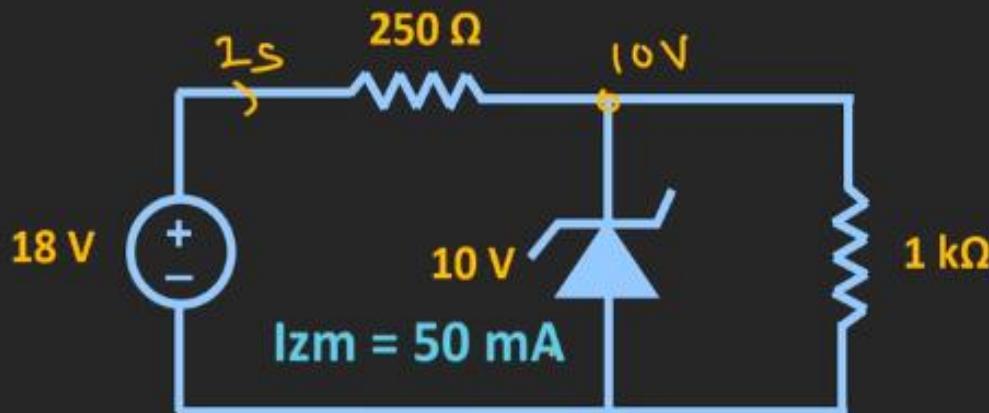
$$V_{th} = \frac{1k\Omega}{1k\Omega + 250\Omega} \times 18V$$

$$V_{th} = 14.4V$$

2.11 ZENER DIODES

Example 1

Find the Zener current and power dissipated across Zener diode



$$I_L = \frac{10\text{V}}{1\text{k}\Omega} = 10\text{mA}$$

$$I_S = \frac{18 - 10\text{V}}{250\Omega}$$

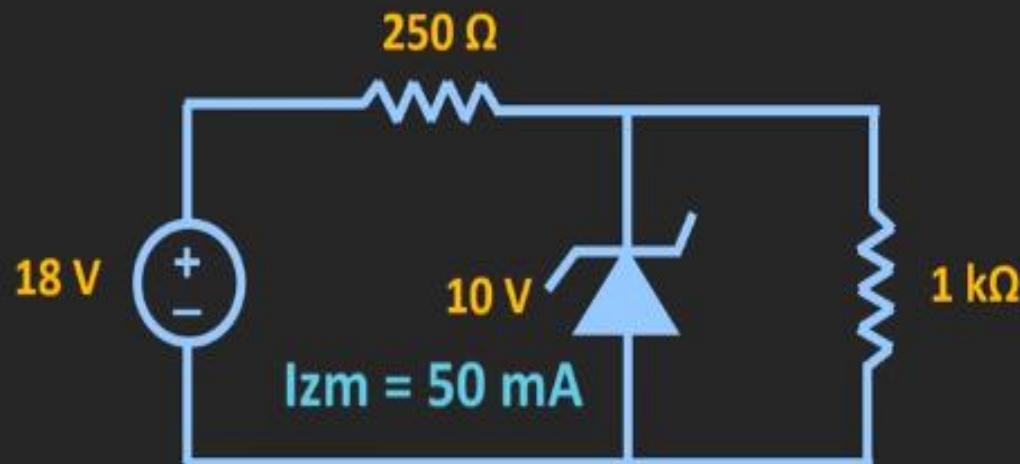
$$\begin{aligned}I_2 &= I_S - I_L \\&= 32 - 10 = 22\text{mA}\end{aligned}$$

$$\underline{I_S = 32\text{mA}}$$

2.11 ZENER DIODES

Example 1

Find the Zener current and power dissipated across Zener diode

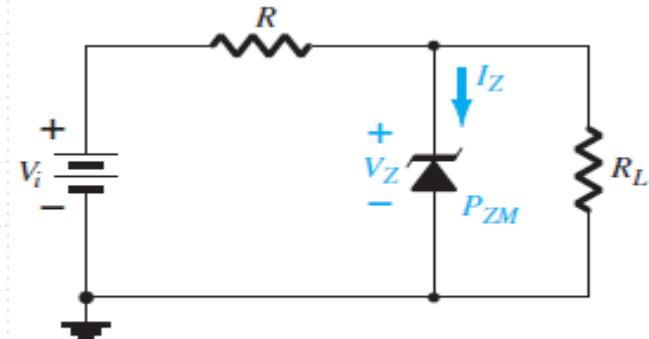


$$\begin{aligned}P_Z &= I_Z \times V_Z \\&= 22 \text{ mA} \times 10 \text{ V}\end{aligned}$$

$$P_Z = 220 \text{ mW}$$

2.11 ZENER DIODES

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered. The analysis provides an excellent opportunity to become better acquainted with the response of the Zener diode to different operating conditions. The basic configuration appears in Fig. 2.112 . The analysis is first for fixed quantities, followed by a fixed supply voltage and a variable load, and finally a fixed load and a variable supply



2.11 ZENER DIODES

Vi and R Fixed

The simplest of **Zener diode regulator** networks appears in Fig. 2.112 . The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps

1. Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.

Applying step 1 to the network of Fig. 2.112 results in the network of Fig. 2.113 , where an application of the voltage divider rule results in

$$V = V_L = \frac{R_L V_i}{R + R_L}$$

(2.16)

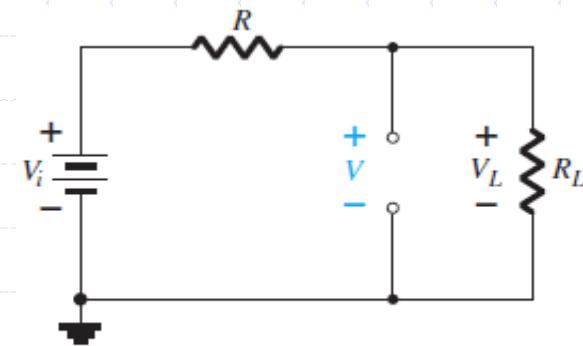


FIG. 2.113

2.11 ZENER DIODES

If $V \geq V_z$, the **Zener diode is on**, and the appropriate equivalent model can be substituted.

If $V < V_z$, the **diode is off**, and the open-circuit equivalence is substituted.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.112 , the “on” state will result in the equivalent network of Fig. 2.114 . Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z$$

(2.17)

2.11 ZENER DIODES

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

$$I_Z = I_R - I_L$$

(2.18)

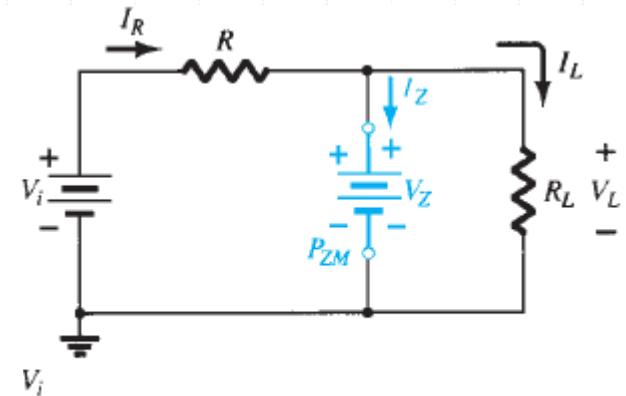


FIG. 2.114

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z$$

(2.19)

that must be less than the P_{ZM} specified for the device

2.11 ZENER DIODES

EXAMPLE 2.26

- For the Zener diode network of Fig. 2.115 , determine V_L , V_R , I_Z , and P_z .
- Repeat part (a) with $R_L = 3 \text{ k}\Omega$

Solution:

a. Following the suggested procedure, we redraw the network as shown in Fig. 2.116
Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2 \text{ k}\Omega(16 \text{ V})}{1 \text{ k}\Omega + 1.2 \text{ k}\Omega} = 8.73 \text{ V}$$

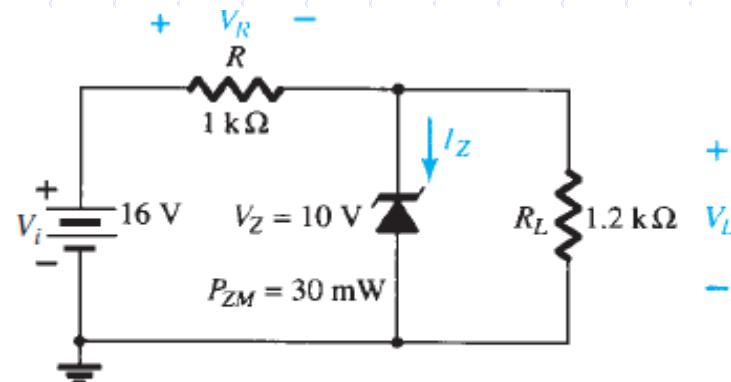


FIG. 2.115

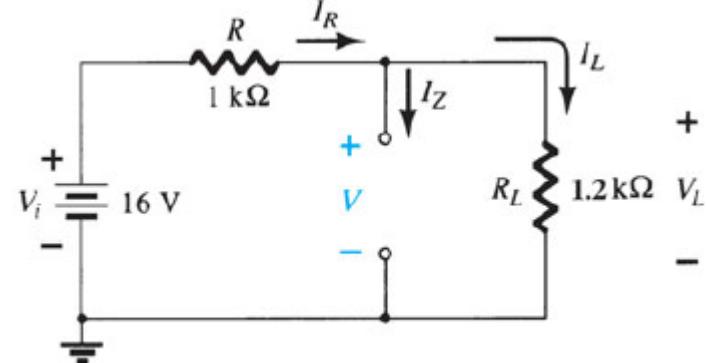


FIG. 2.116

2.11 ZENER DIODES

Since $V = 8.73 \text{ V}$ is less than $V_Z = 10 \text{ V}$, the diode is in the “off” state, as shown on the characteristics of Fig. 2.117. Substituting the open-circuit equivalent results in the same network as in Fig. 2.116, where we find that

$$V_L = V = 8.73 \text{ V}$$

$$V_R = V_i - V_L = 16 \text{ V} - 8.73 \text{ V} = 7.27 \text{ V}$$

$$I_Z = 0 \text{ A}$$

$$P_Z = V_Z I_Z = V_Z(0 \text{ A}) = 0 \text{ W}$$

b. Applying Eq. (2.16) results in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3 \text{ k}\Omega (16 \text{ V})}{1 \text{ k}\Omega + 3 \text{ k}\Omega} = 12 \text{ V}$$

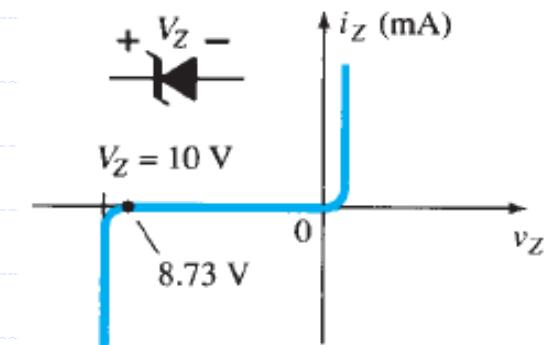


FIG. 2.117

2.11 ZENER DIODES

Since $V=12\text{ V}$ is greater than $V_z=10\text{ V}$, the diode is in the “on” state and the network of Fig. 2.118 results. Applying Eq. (2.17) yields

$$V_L = V_Z = 10\text{ V}$$

$$V_R = V_i - V_L = 16\text{ V} - 10\text{ V} = 6\text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{10\text{ V}}{3\text{ k}\Omega} = 3.33\text{ mA}$$

$$I_R = \frac{V_R}{R} = \frac{6\text{ V}}{1\text{ k}\Omega} = 6\text{ mA}$$

$$\begin{aligned} I_Z &= I_R - I_L [\text{Eq. (2.18)}] \\ &= 6\text{ mA} - 3.33\text{ mA} \\ &= 2.67\text{ mA} \end{aligned}$$

2.11 ZENER DIODES

The power dissipated is

$$P_Z = V_Z I_Z = (10 \text{ V})(2.67 \text{ mA}) = 26.7 \text{ mW}$$

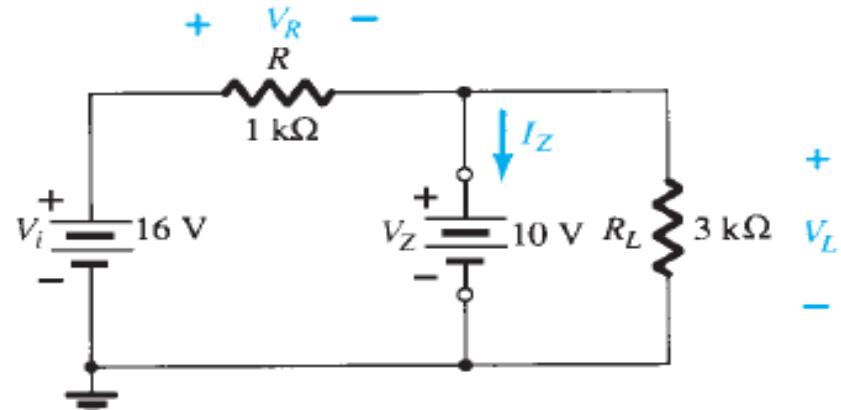


FIG. 2.118

which is less than the specified $P_{ZM} = 30 \text{ mW}$.

2.11 ZENER DIODES

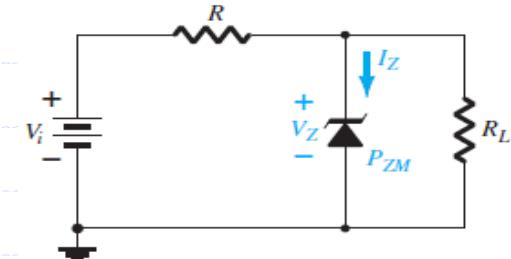


FIG. 2.112

Fixed V_i , Variable R_L

Due to the offset voltage V_Z , there is a specific range of resistor values (and therefore load current) that will ensure that the **Zener** is in the “on” state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z , and the **Zener** device will be in the “off” state.

To determine the minimum load resistance of Fig. 2.112 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

2.11 ZENER DIODES

Solving for R_L , we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z}$$

(2.20)

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the “on” state and the diode can be replaced by its V_Z source equivalent. The condition defined by Eq. (2.20) establishes the minimum R_L , but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}}$$

(2.21)

2.11 ZENER DIODES

Once the diode is in the “on” state, the voltage across R remains fixed at

$$V_R = V_i - V_Z$$

(2.22)

and IR remains fixed at

$$I_R = \frac{V_R}{R}$$

(2.23)

The Zener current

$$I_Z = I_R - I_L$$

(2.24)

2.11 ZENER DIODES

resulting in a minimum I_z when I_L is a maximum and a maximum I_z when I_L is a minimum value, since I_R is constant.

Since I_z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L . Substituting I_{ZM} for I_z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM}$$

(2.25)

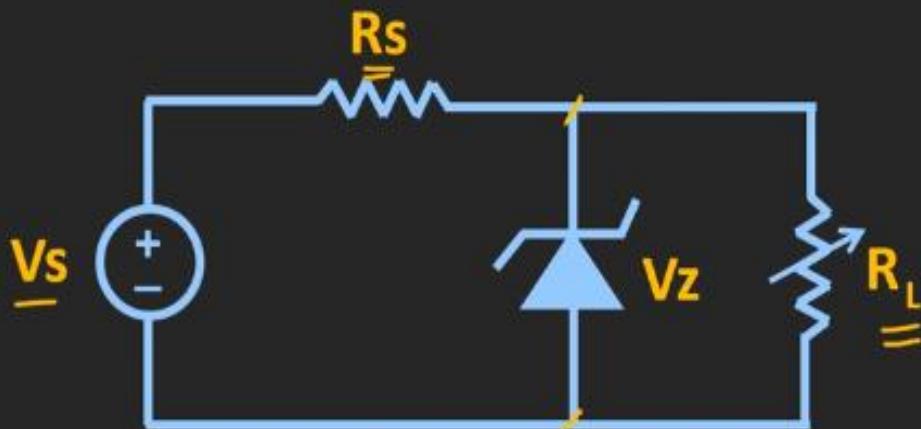
and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}}$$

(2.26)

2.11 ZENER DIODES

Zener Diode as Voltage Regulator



R_L is variable

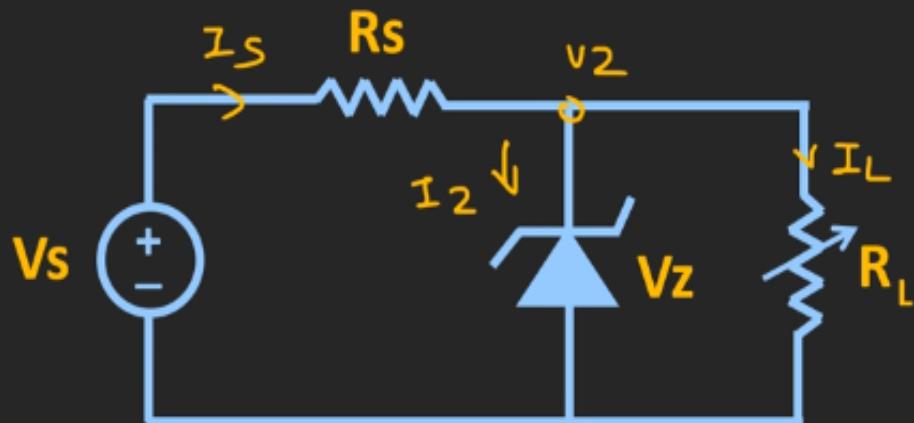
R_{Lcmin})

$$V_{th} = \frac{R_L \times V_s}{R_L + R_s} = V_Z$$

$$R_{Lcmin} = \frac{R_s V_Z}{V_s - V_Z}$$

2.11 ZENER DIODES

Zener Diode as Voltage Regulator



R_L is variable

$$\frac{R_{L(\max)}}{I_{L(\min)} = \frac{V_Z}{R_{L(\max)}}$$

$$I_S = \frac{V_s - V_2}{R_s}$$

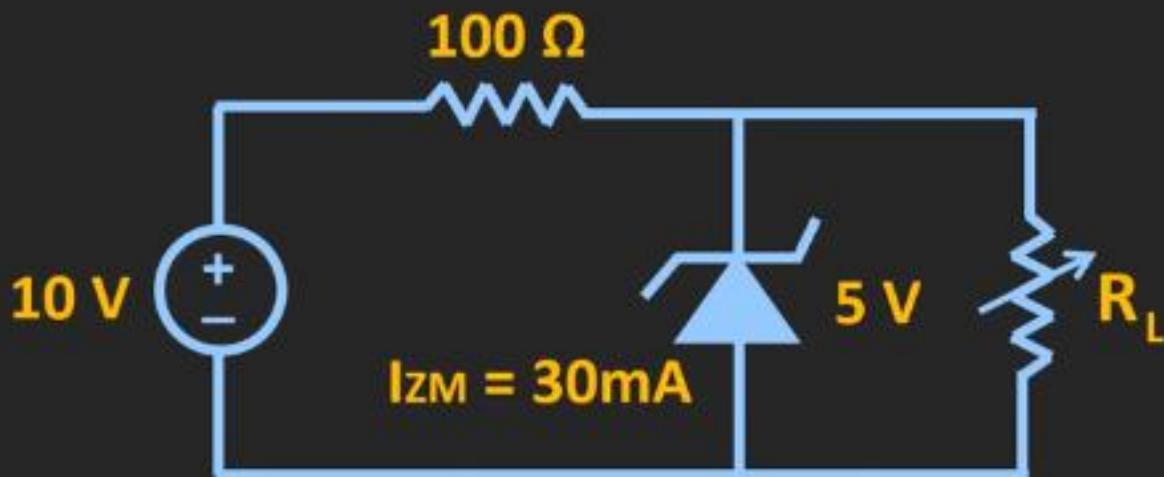
$$I_S = I_{2M} + I_{L(\min)}$$

$$I_{L(\min)} = I_S - I_{2M}$$

2.11 ZENER DIODES

Example 2

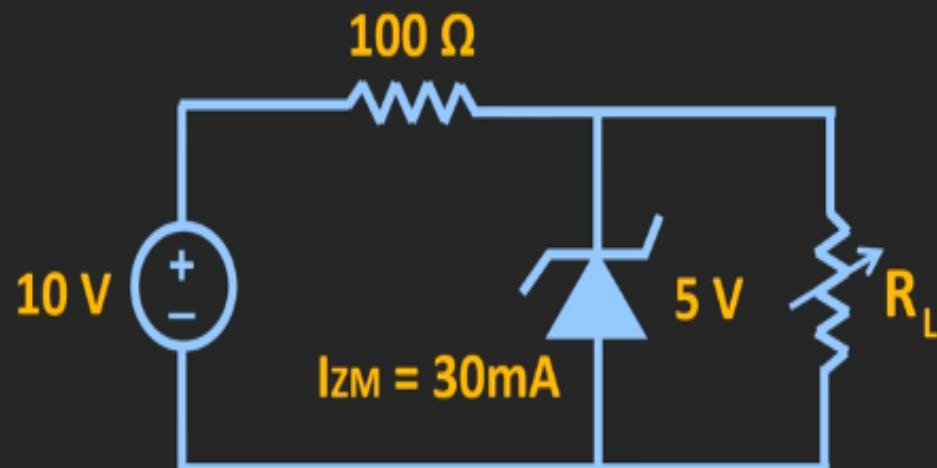
Find the minimum and maximum value of R_L



2.11 ZENER DIODES

Example 2

Find the minimum and maximum value of R_L

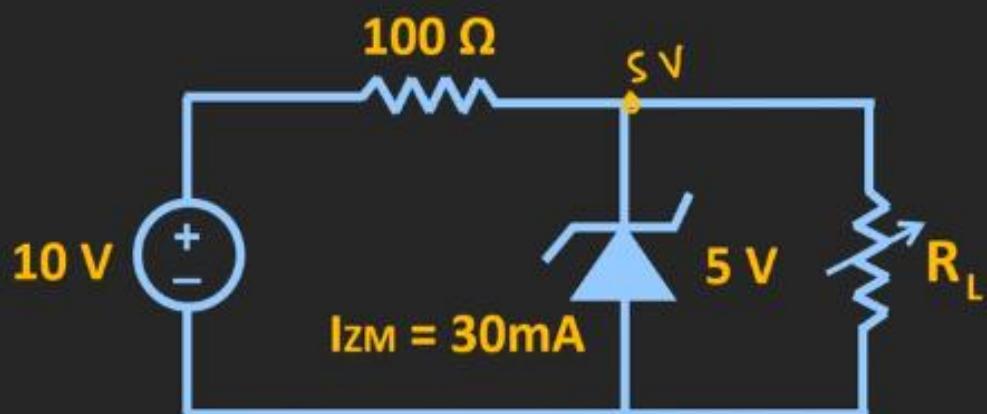


$$\begin{aligned}R_{L(\min)} &= \frac{R_S \times V_Z}{V_S - V_Z} = \frac{100 \times 5}{5 - 5} \\&= 100 \Omega\end{aligned}$$

2.11 ZENER DIODES

Example 2

Find the minimum and maximum value of R_L



$$\underline{R_L(\max)}$$

$$I_S = \frac{10 - 5\text{V}}{100\Omega}$$

$$I_S = 50\text{mA}$$

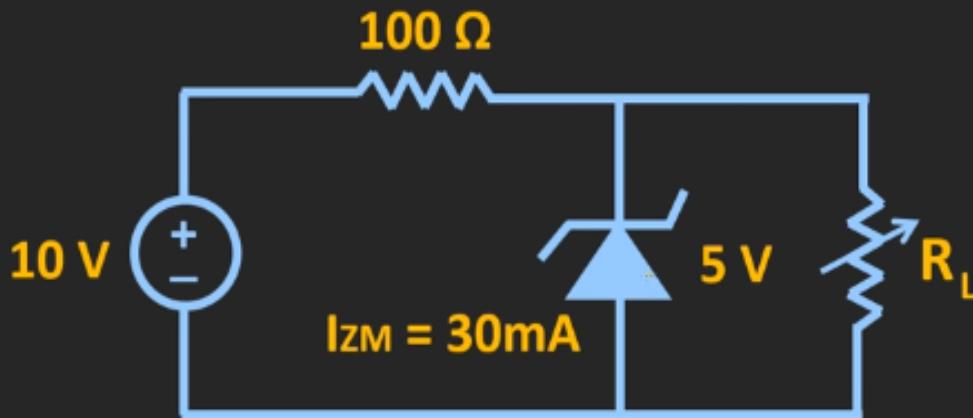
$$I_{2M} = 30\text{mA}$$

$$\begin{aligned} I_{L(\min)} &= I_S - I_{2M} \\ &= 50 - 30 = 20\text{mA} \end{aligned}$$

2.11 ZENER DIODES

Example 2

Find the minimum and maximum value of R_L



$$R_{L(\text{max})} = \frac{V_2}{I_{L(\text{min})}}$$
$$= \frac{5\text{V}}{20\text{mA}}$$

$$\underline{R_{L(\text{max})} = 250\Omega}$$

2.11 ZENER DIODES

EXAMPLE 2.27

- For the network of Fig. 2.119, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10V.
- Determine the maximum wattage rating of the diode.

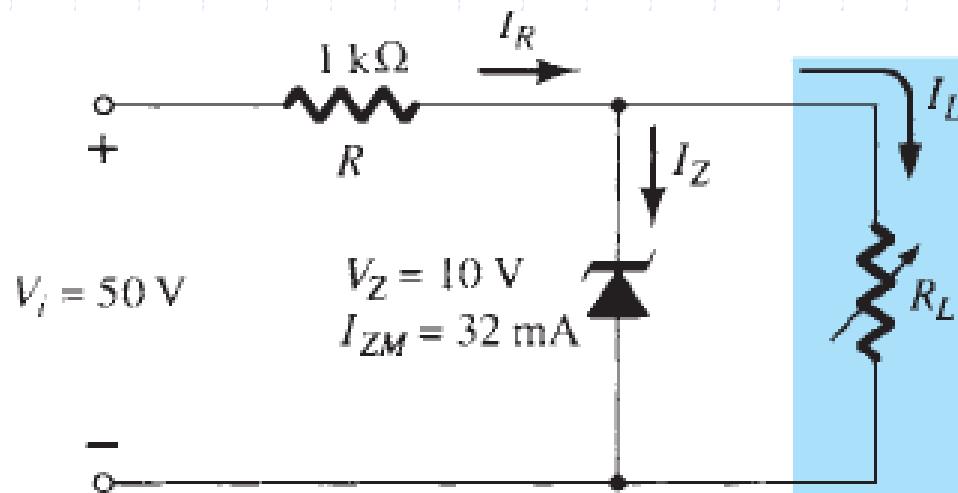


FIG. 2.119

2.11 ZENER DIODES

- a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1 \text{ k}\Omega)(10 \text{ V})}{50 \text{ V} - 10 \text{ V}} = \frac{10 \text{ k}\Omega}{40} = 250 \text{ }\Omega$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50 \text{ V} - 10 \text{ V} = 40 \text{ V}$$

and Eq. (2.23) provides the magnitude of I_R :

$$I_R = \frac{V_R}{R} = \frac{40 \text{ V}}{1 \text{ k}\Omega} = 40 \text{ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

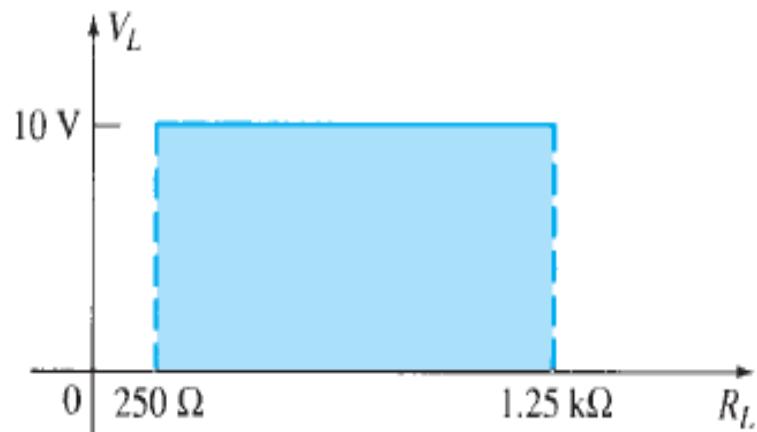
$$I_{L_{\min}} = I_R - I_{ZM} = 40 \text{ mA} - 32 \text{ mA} = 8 \text{ mA}$$

with Eq. (2.26) determining the maximum value of R_L :

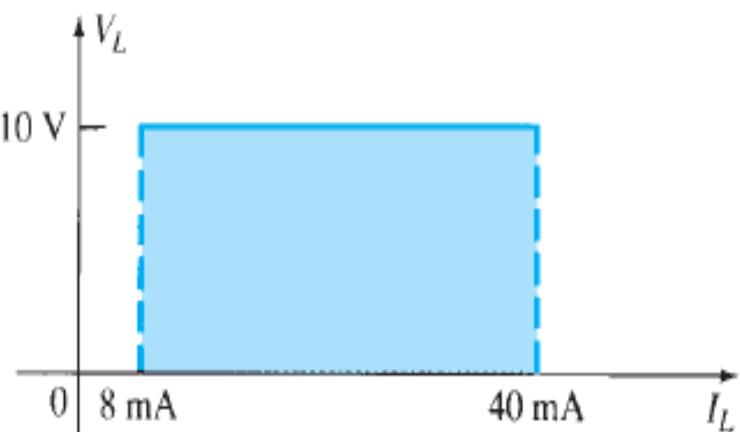
$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10 \text{ V}}{8 \text{ mA}} = 1.25 \text{ k}\Omega$$

A plot of V_L versus R_L appears in Fig. 2.120a and for V_L versus I_L in Fig. 2.120b.

2.11 ZENER DIODES



(a)



(b)

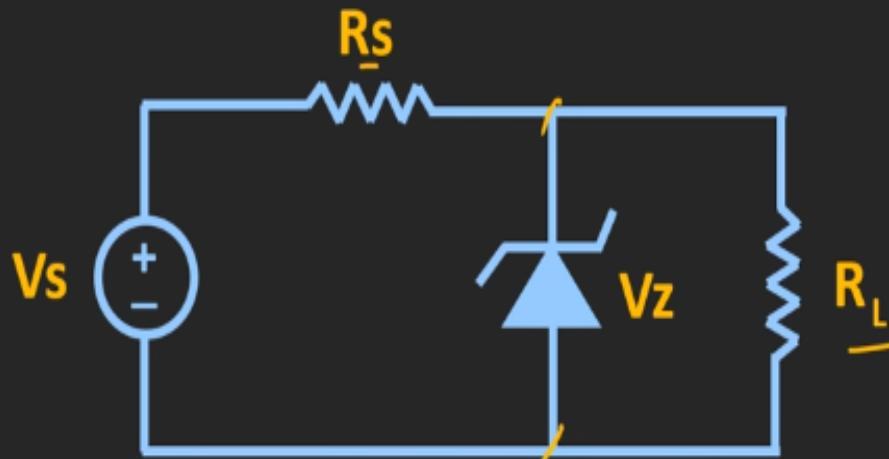
FIG. 2.120

V_L versus R_L and I_L for the regulator of Fig. 2.119.

b. $P_{\max} = V_Z I_{ZM}$
 $= (10 \text{ V})(32 \text{ mA}) = 320 \text{ mW}$

2.11 ZENER DIODES

Zener Diode as Voltage Regulator



V_s is variable

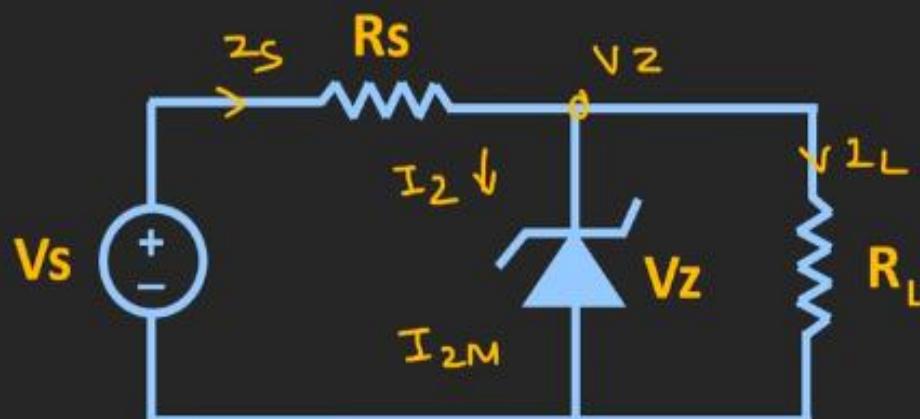
V_{s (min)}

$$V_{th} = \frac{V_s \times R_L}{R_s + R_L} = V_2$$

$$V_{s(min)} = \left(\frac{R_s + R_L}{R_L} \right) \times V_2$$

2.11 ZENER DIODES

Zener Diode as Voltage Regulator



V_s is variable

V_{s(max)}

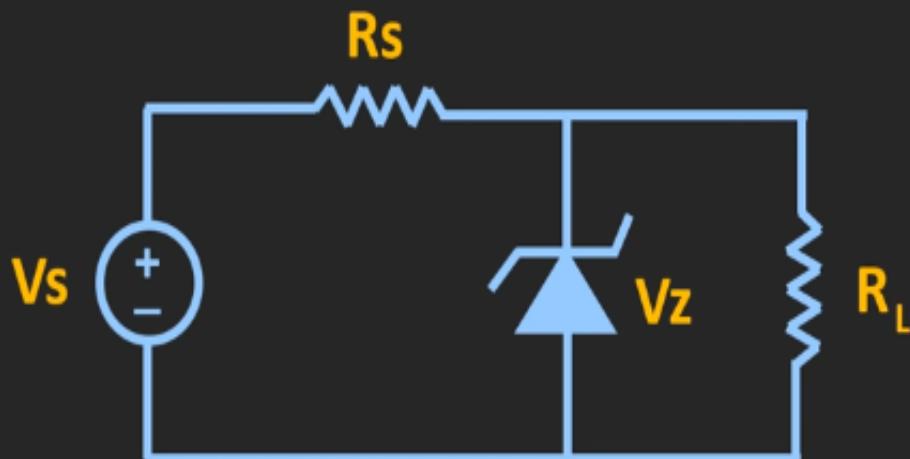
$$I_L = \frac{V_Z}{R_L}$$

$$I_{s(max)} = I_{2M} + I_L$$

$$I_S = \frac{V_s - V_Z}{R_S}$$

2.11 ZENER DIODES

Zener Diode as Voltage Regulator



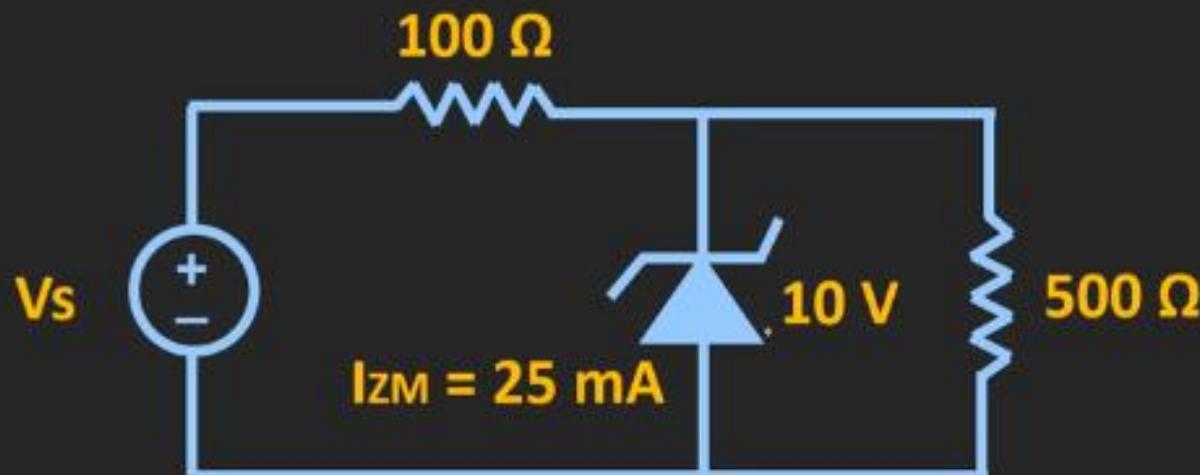
V_s is variable

$$I_{S(max)} = \frac{V_s(max) - V_Z}{R_s}$$

2.11 ZENER DIODES

Example 3

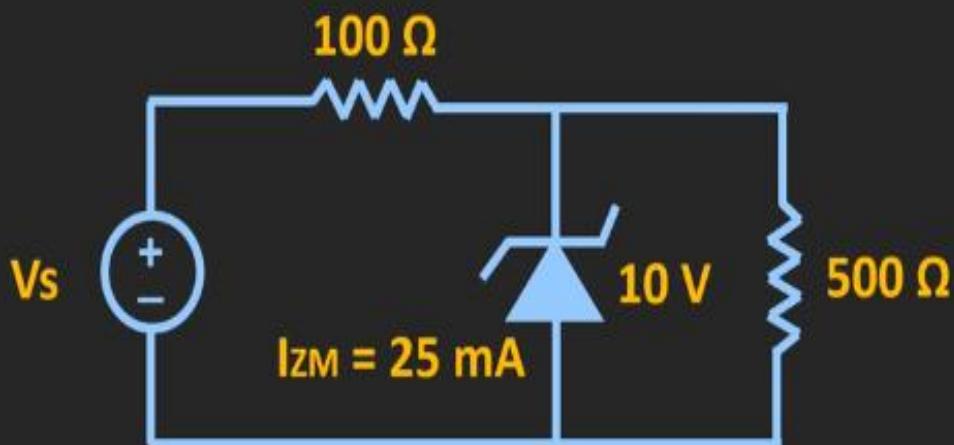
Find the minimum and maximum value of V_s



2.11 ZENER DIODES

Example 3

Find the minimum and maximum value of V_s



$$V_{s(\min)}$$

$$= V_2 \left(\frac{R_S + R_L}{R_L} \right)$$

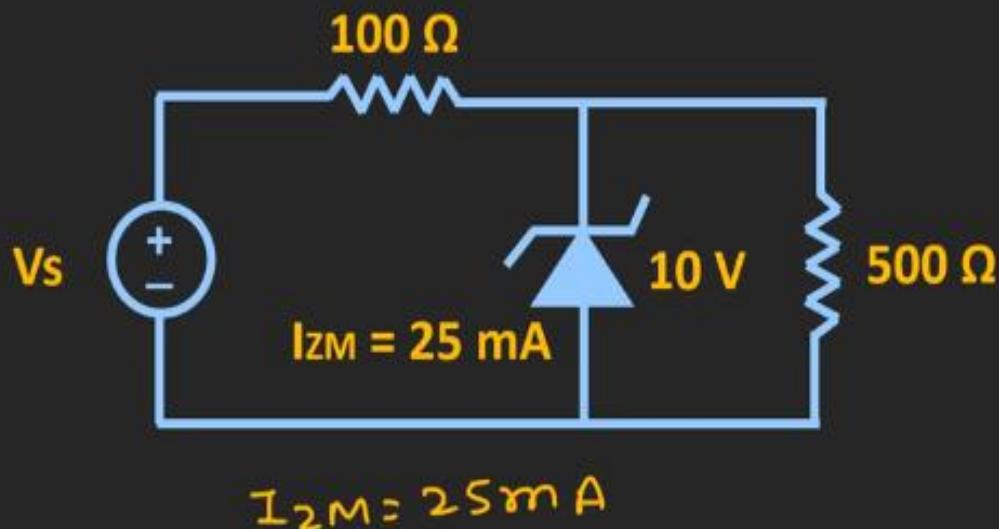
$$= 10 \times \left(\frac{100 + 500}{500} \right)$$

$$\underline{\underline{V_{s(\min)} = 12V}}$$

2.11 ZENER DIODES

Example 3

Find the minimum and maximum value of V_s



$$\underline{\underline{V_{scmax}}})$$

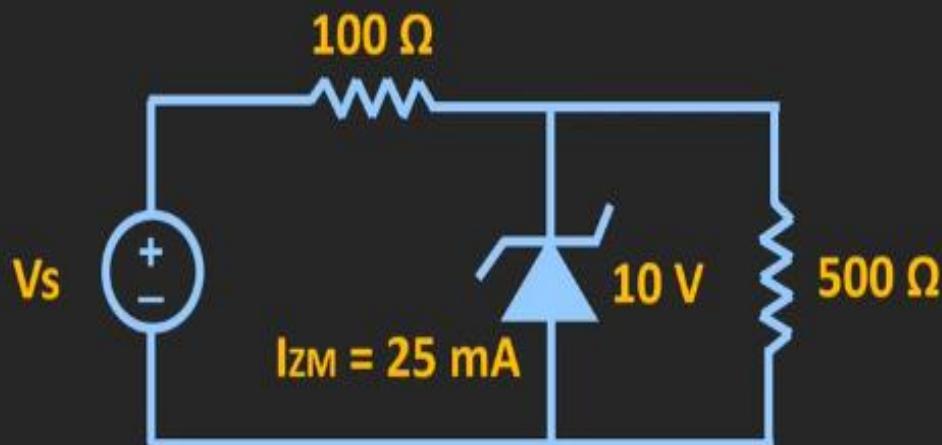
$$I_L = \frac{V_2}{R_L} = \frac{10\text{ V}}{500\ \Omega} = \underline{\underline{20\text{ mA}}}$$

$$I_{scmax}) = I_{ZM} + I_L = 25\text{ mA} + 20\text{ mA} = \underline{\underline{45\text{ mA}}}$$

2.11 ZENER DIODES

Example 3

Find the minimum and maximum value of V_s



$$I_{S(\max)} = \frac{V_{S(\max)} - 10}{100\ \Omega}$$

$$45\text{mA} = \frac{V_{S(\max)} - 10}{100\ \Omega}$$

$$\underline{\underline{V_{S(\max)} = 14.5\text{V}}}$$

2.11 ZENER DIODES

Fixed R_L , Variable V_i

For fixed values of R_L in Fig. 2.112, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i\min}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

$$V_{i\min} = \frac{(R_L + R)V_Z}{R_L}$$

(2.27)

The maximum value of V_i is limited by the maximum Zener current I_{ZM} . Since $I_{ZM} = I_R - I_L$,

$$I_{R_{\max}} = I_{ZM} + I_L$$

(2.28)

2.11 ZENER DIODES

Since I_L is fixed at $V_Z = R_L$ and I_{ZM} is the maximum value of I_Z , the maximum V_i is defined by

$$V_{i_{\max}} = V_{R_{\max}} + V_Z$$

$$V_{i_{\max}} = I_{R_{\max}} R + V_Z$$

(2.29)

EXAMPLE 2.28 Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.121 in the “on” state.

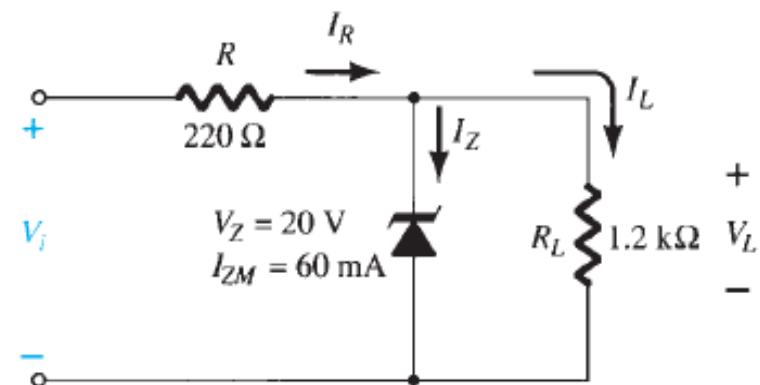


FIG. 2.121

2.11 ZENER DIODES

Solution:

$$\text{Eq. (2.27): } V_{i_{\min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200 \Omega + 220 \Omega)(20 \text{ V})}{1200 \Omega} = 23.67 \text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20 \text{ V}}{1.2 \text{ k}\Omega} = 16.67 \text{ mA}$$

$$\begin{aligned} \text{Eq. (2.28): } I_{R_{\max}} &= I_{ZM} + I_L = 60 \text{ mA} + 16.67 \text{ mA} \\ &= 76.67 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{Eq. (2.29): } V_{i_{\max}} &= I_{R_{\max}}R + V_Z \\ &= (76.67 \text{ mA})(0.22 \text{ k}\Omega) + 20 \text{ V} \\ &= 16.87 \text{ V} + 20 \text{ V} \\ &= 36.87 \text{ V} \end{aligned}$$

A plot of V_L versus V_i is provided in Fig. 2.122.

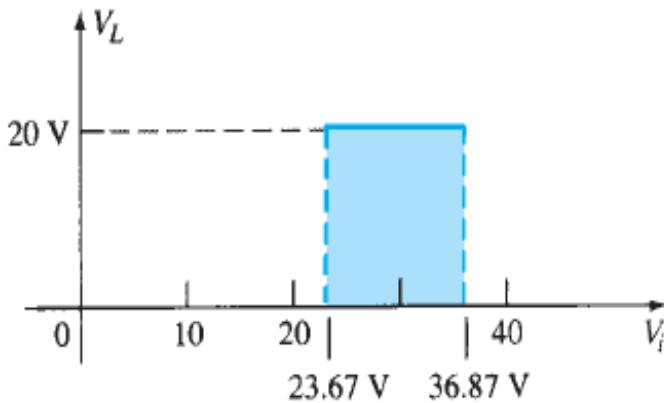


FIG. 2.122