Electronic Devices

Mid Term
Lecture - 04

Faculty Name: Dr. Md. Kabiruzzaman
Email : Kabiruzzaman@aiub.edu

Faculty of Engineering
American International University-Bangladesh

Objectives

- Diodes application : AND/OR gates
- Understand the process of rectification to establish a dc level from a sinusoidal ac input.

Logic OR gates

EXAMPLE 2.14 Determine V_o for the network of Fig. 2.39.

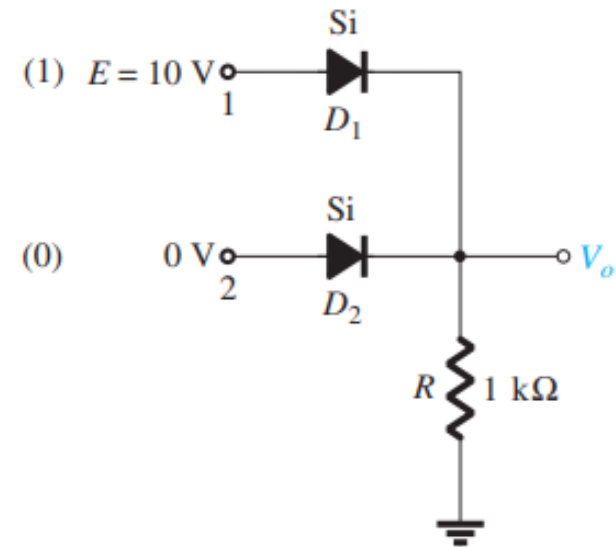Inputs of Diode, D1 and D2 are 1 (10 V) and 0 (0 V), respectively (Fig 2.39)
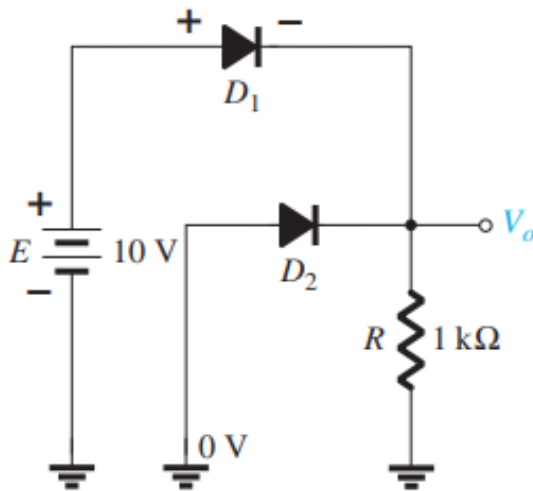

FIG. 2.39
Positive logic OR gate.

$V_o = E - V_K = 9.3$ V (a 1 level)

Output across the resistor is 9.3 V (1 level) Fig. 2.41

FIG. 2.40
Redrawn network of Fig. 2.39.
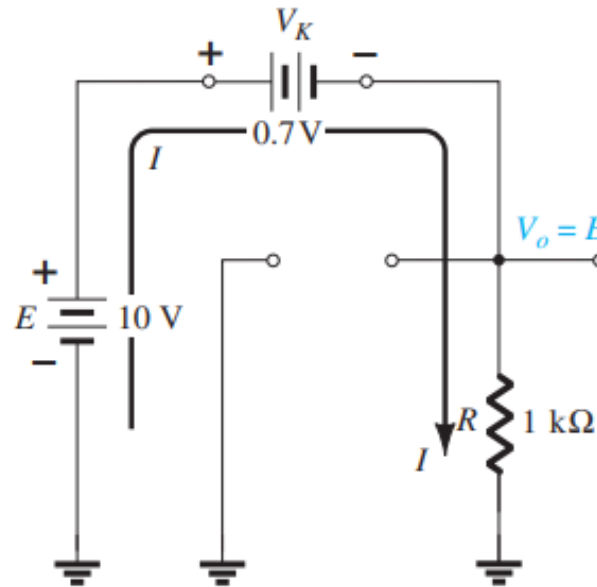
FIG. 2.41
Assumed diode states for Fig. 2.40.

For AND gates see the Example 2.15

SINUSOIDAL INPUTS; HALF-WAVE

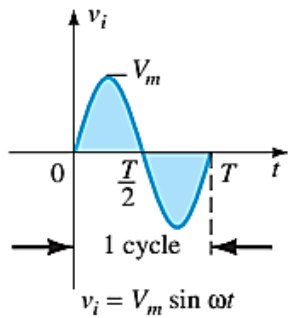$v_i = V_m \sin \omega t$

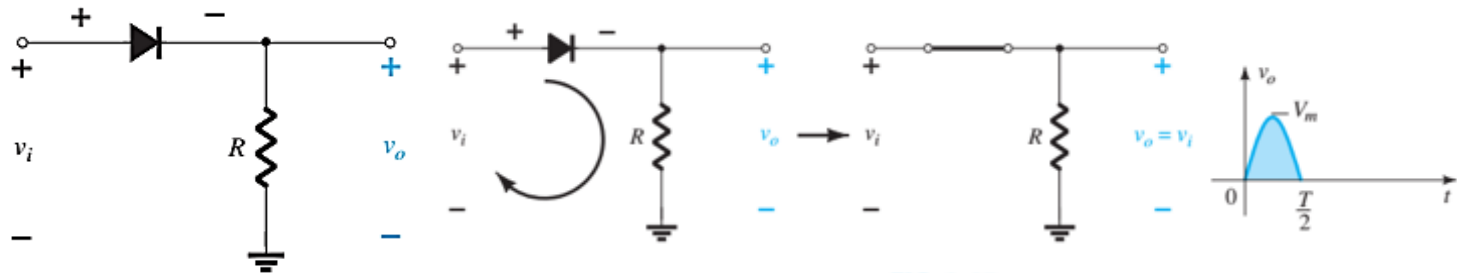**FIG. 2.44**
Half-wave rectifier.

FIG. 2.45
Conduction region $(0 \rightarrow T/2)$.
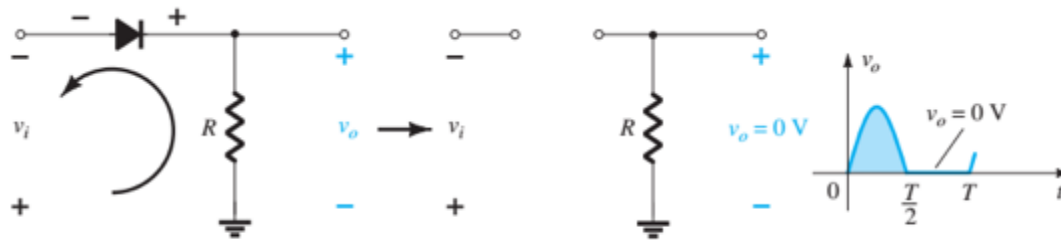
FIG. 2.46
Nonconduction region $(T/2 \rightarrow T)$.
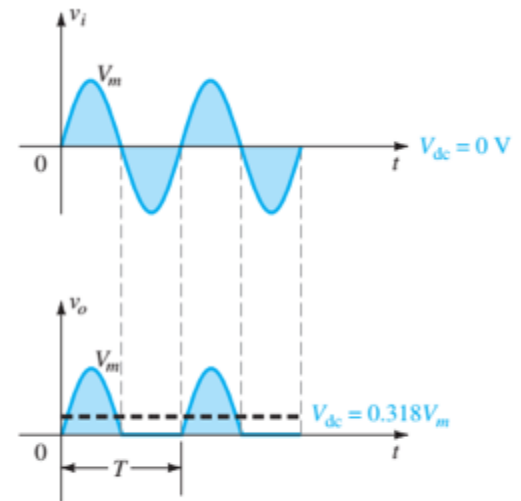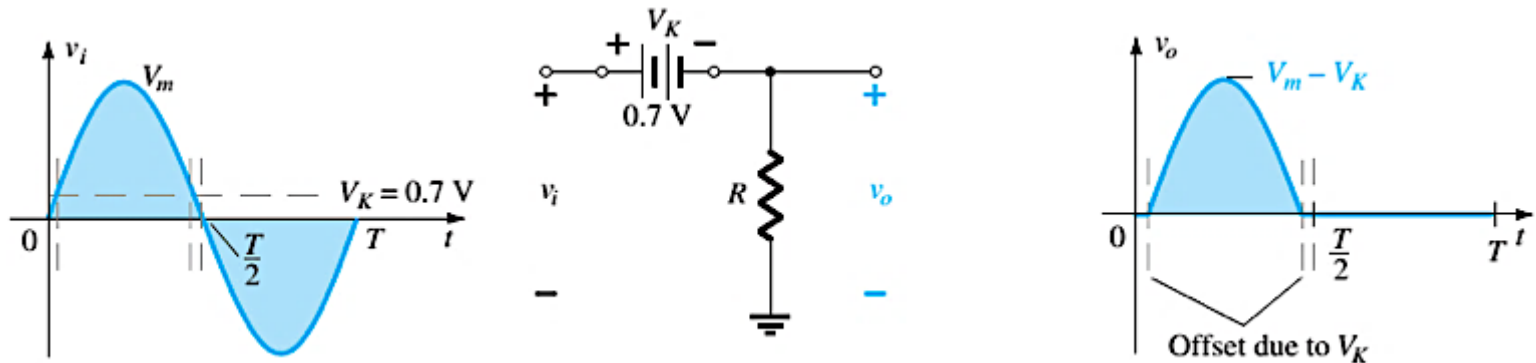
$$V_{dc} = 0.318 \, V_m$$ half-wave

FIG. 2.47
Half-wave rectified signal.

HALF-WAVE RECTIFICATION

- The process of removing one-half the input signal to establish a dc level is called *__halfwave rectification.__*

- The effect of using a silicon diode with $V_K = 0.7$ V is demonstrated in below Figure for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on."

$$V_{dc} \cong 0.318(V_m - V_K)$$

EXAMPLE 2.16

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).
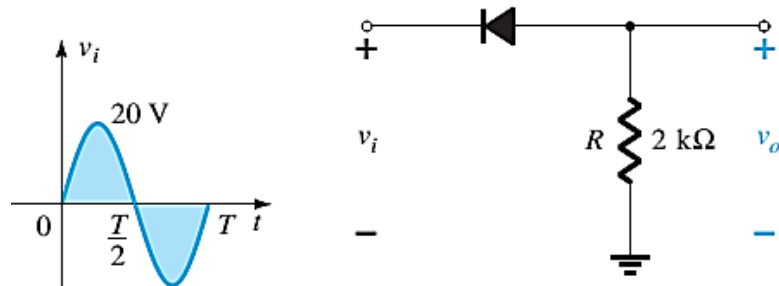
$$V_{dc} = -0.318V_m = -0.318(20\ V) = -6.36\ V$$

FIG. 2.49
Network for Example 2.16.
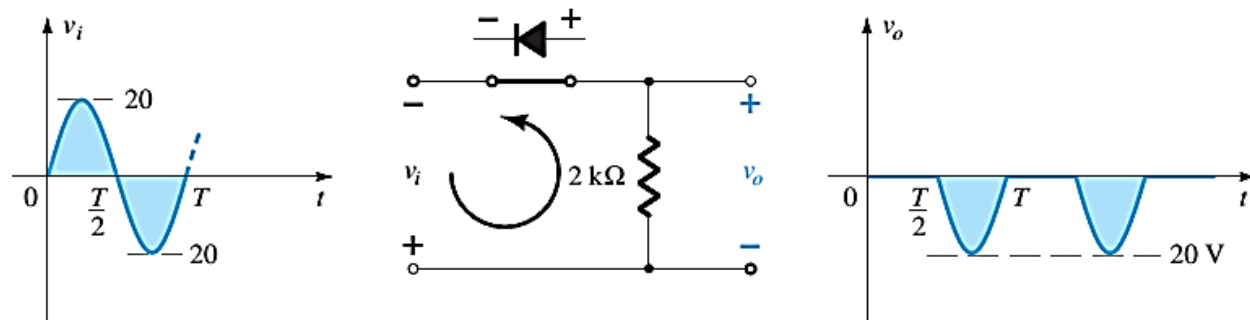
FIG. 2.50
Resulting v_o for the circuit of Example 2.16.

Faculty of Engineering
American International University-Bangladesh

b. For a silicon diode, the output has the appearance of Fig. 2.51, and

$$V_{dc} \cong -0.318(V_m - 0.7 \text{ V}) = -0.318(19.3 \text{ V}) \cong -6.14 \text{ V}$$

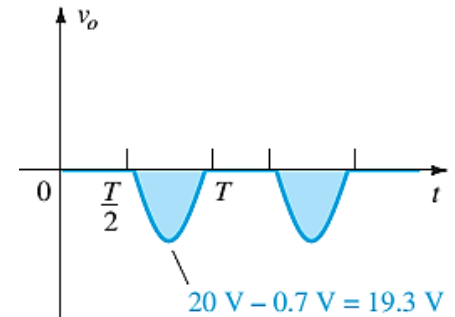The resulting drop in dc level is 0.22 V, or about 3.5%.

20 V – 0.7 V = 19.3 V

FIG. 2.51

Effect of V_K on output of
Fig. 2.50.

c. Eq. (2.7): $V_{dc} = -0.318 \, V_m = -0.318(200 \text{ V}) = -63.6 \text{ V}$

   Eq. (2.8): $V_{dc} = -0.318(V_m - V_K) = -0.318(200 \text{ V} - 0.7 \text{ V})$

   $$= -(0.318)(199.3 \text{ V}) = -63.38 \text{ V}$$

PIV (PRV)

- It is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region.

- Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage.
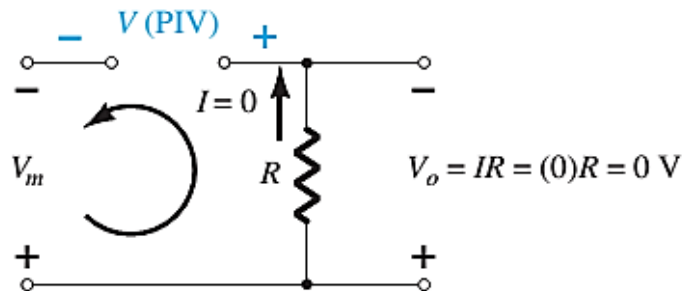

FIG. 2.52

Determining the required PIV rating for the half-wave rectifier.

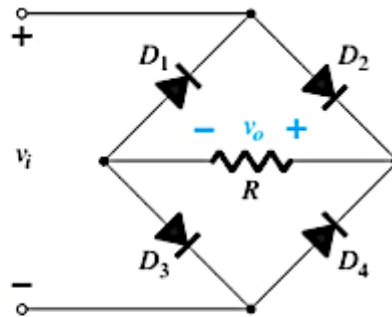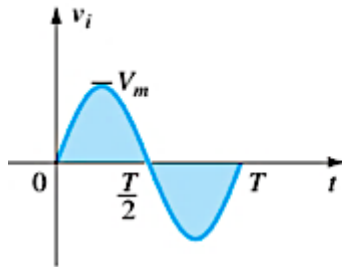$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier}$$

FULL-WAVE RECTIFICATION: BRIDGE NETWORK

FIG. 2.53
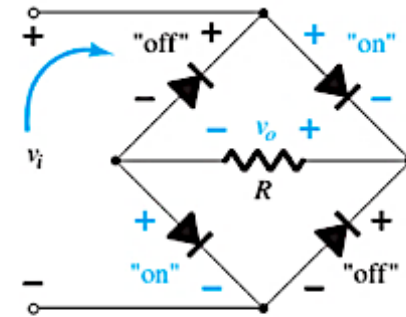Full-wave bridge rectifier.

FIG. 2.54
Network of Fig. 2.53 for the period
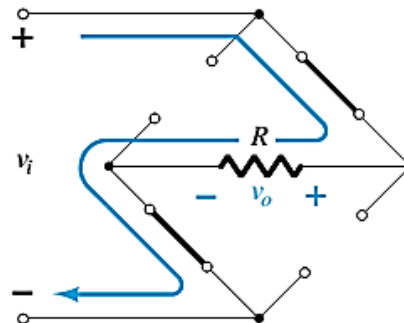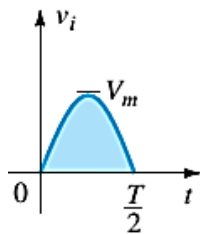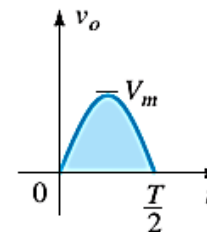$0 \rightarrow T/2$ of the input voltage v_i.

FIG. 2.55
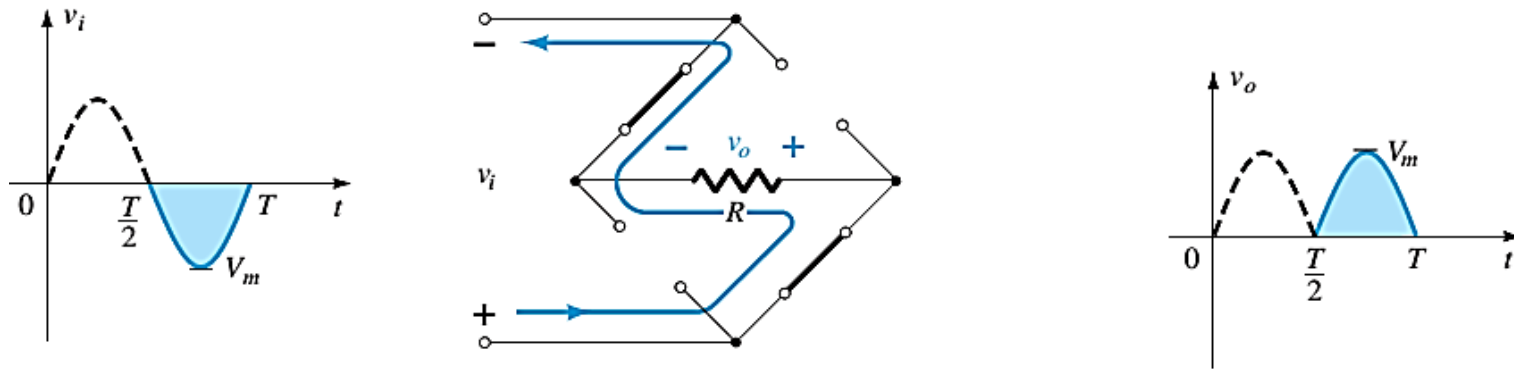Conduction path for the positive region of v_i.

BRIDGE NETWORK

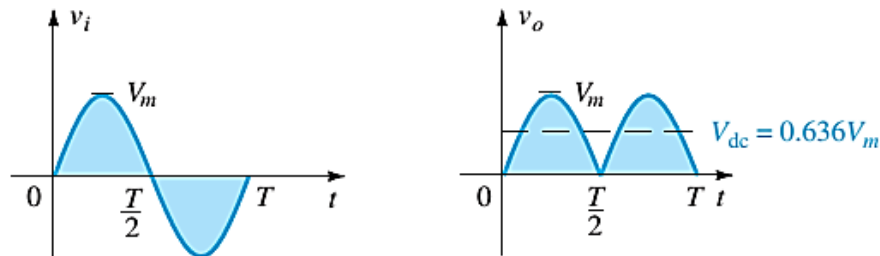**FIG. 2.56**

Conduction path for the negative region of v_i.

FIG. 2.57

Input and output waveforms for a full-wave rectifier.

$V_{dc} = 0.636 V_m$

BRIDGE NETWORK

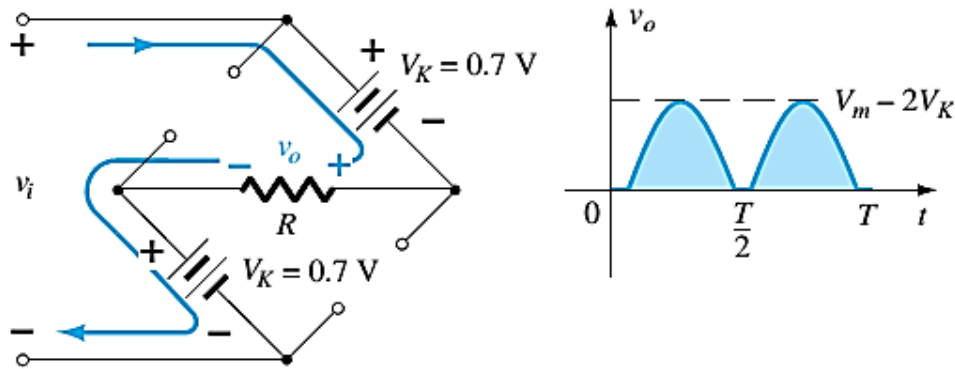**FIG. 2.58**

Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

$$V_{dc} \cong 0.636(V_m - 2V_K)$$
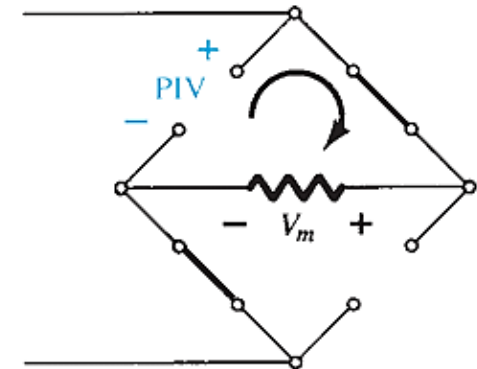
$$PIV \geq V_m$$ full-wave bridge rectifier

FIG. 2.59

Determining the required PIV for the bridge configuration.
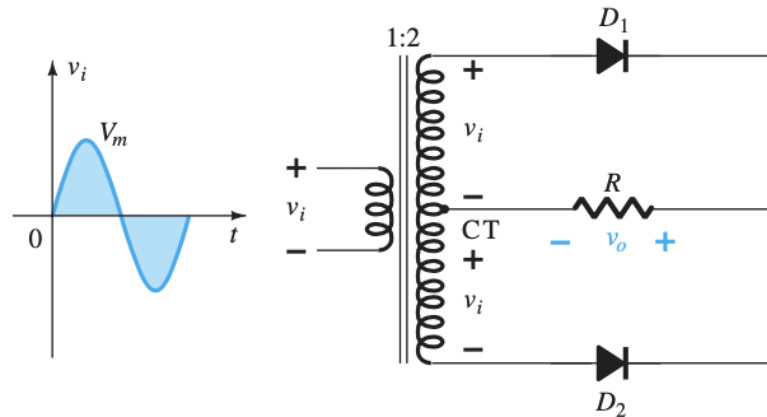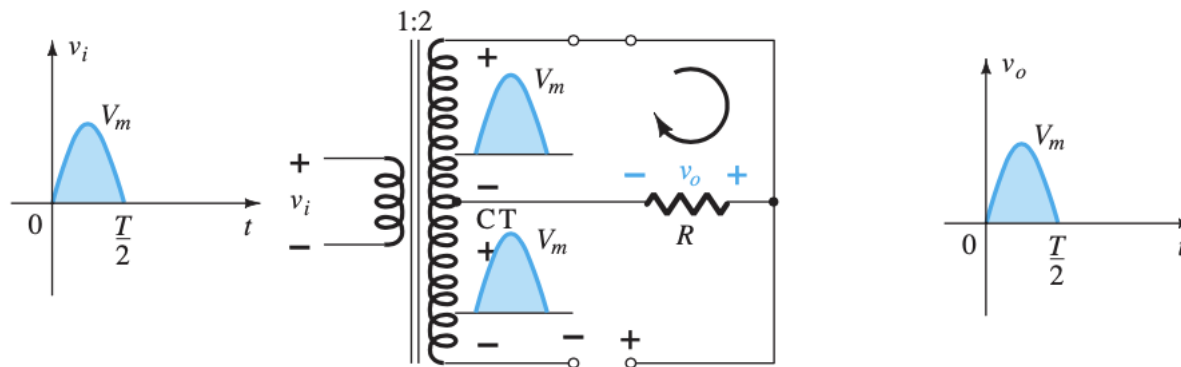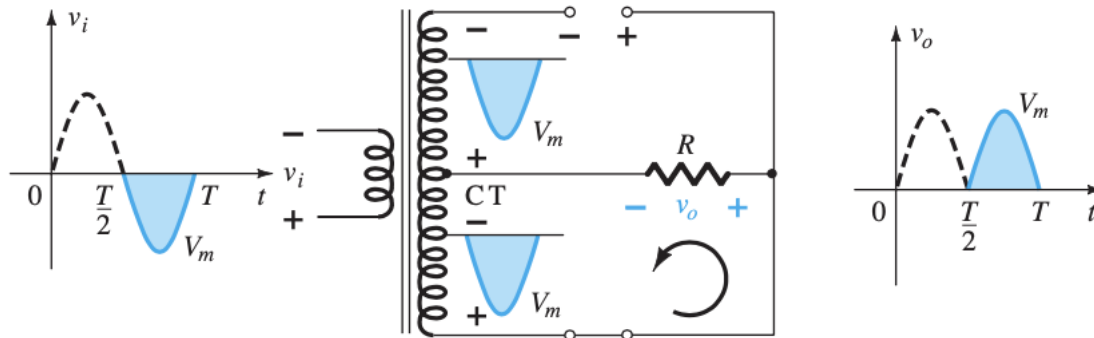
CENTER-TAPPED TRANSFORMER

FIG. 2.60
Center-tapped transformer full-wave rectifier.

Network conditions for the positive region of v_i

CENTER-TAPPED TRANSFORMER

Network conditions for the negative region of v_i

$$PIV = V_{secondary} + V_R$$
$$= V_m + V_m$$

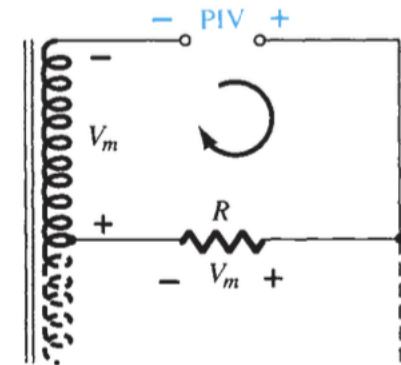$$PIV \geq 2V_m$$ CT transformer, full-wave rectifier

FIG. 2.63
Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.
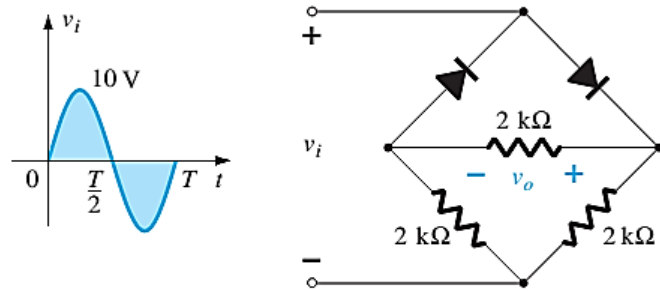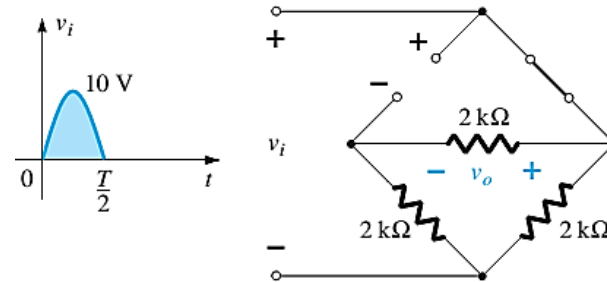

FIG. 2.64

Bridge network for Example 2.17.

FIG. 2.65

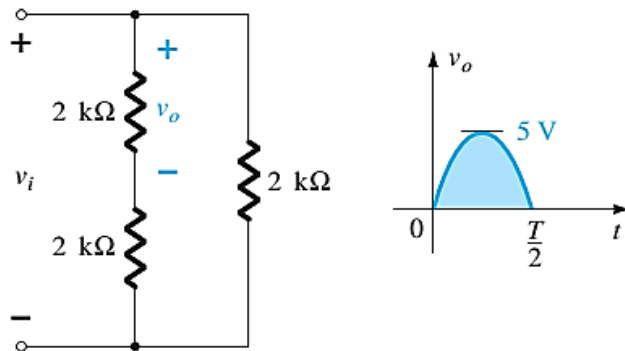*Network of Fig. 2.64 for the positive region of v_i.*
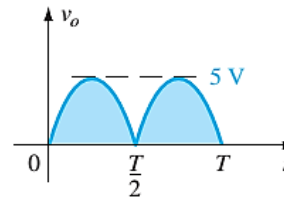

FIG. 2.66

Redrawn network of Fig. 2.65.

FIG. 2.67

Resulting output for Example 2.17.

$$V_{o_{max}} = \tfrac{1}{2}V_{i_{max}} = \tfrac{1}{2}(10 \text{ V}) = 5 \text{ V}$$

$$V_{dc} = 0.636(5 \text{ V}) = \textbf{3.18 V}$$

PIV analysis
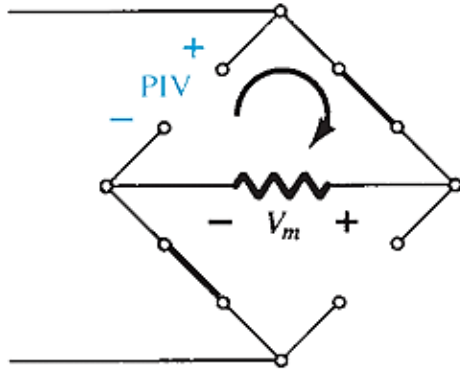

FIG. 2.64
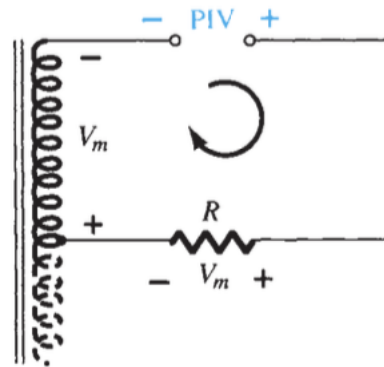
Bridge network for Example 2.17.

FIG. 2.59

Determining the required PIV for
the bridge configuration.

FIG. 2.63

Determining the PIV level for
the diodes of the CT transformer
full-wave rectifier.

FIG. 2.66

Redrawn network of Fig. 2.65.

$$PIV \geq V_m$$ full-wave bridge rectifier

$$PIV = V_{secondary} + V_R$$
$$= V_m + V_m$$

$$PIV \geq 2V_m$$ CT transformer, full-wave rectifier
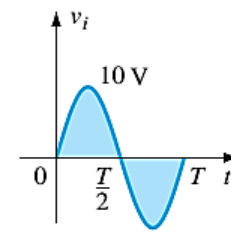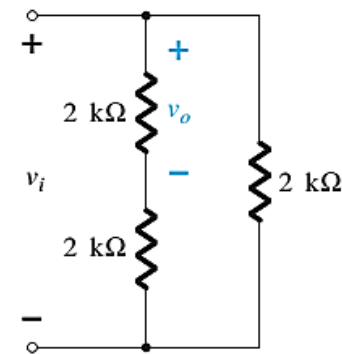
***The PIV as determined from Fig. 2.59 is equal to the maximum voltage across R , which is 5 V, or half of that required for a half-wave rectifier with the same input.

Thank You