PSoC® Creator™
Project Datasheet for VertushkaAnalog

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Table of Contents

1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 4200 family member PSoC 4 device. For details on all the systems listed above, please refer to the PSoC 4 Technical Reference Manual .

Figure 1. PSoC 4200 Device Family Block Diagram

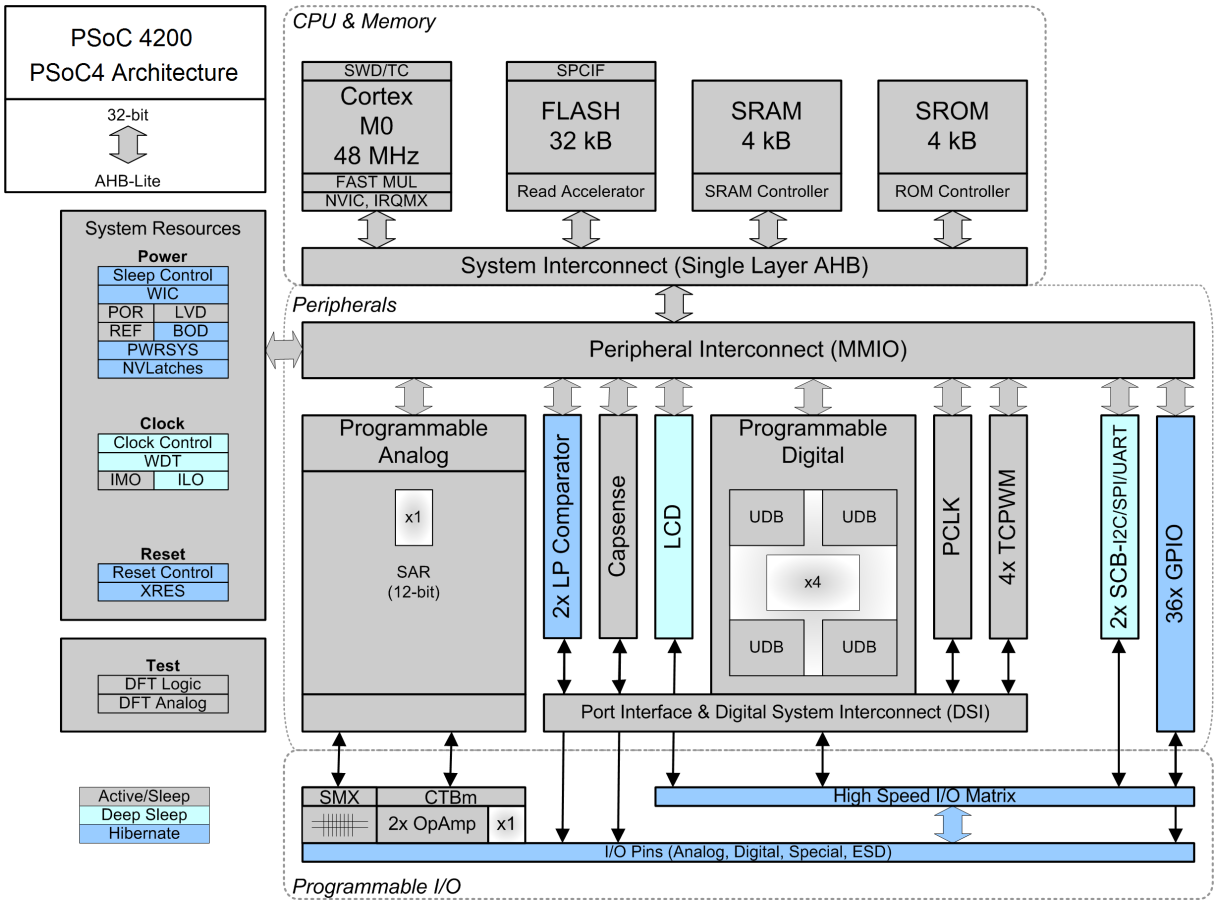


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4245PVI-482
Package Name	28-SSOP
Architecture	PSoC 4
Family	PSoC 4200
CPU speed (MHz)	48
Flash size (kBytes)	32
SRAM size (kBytes)	4
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

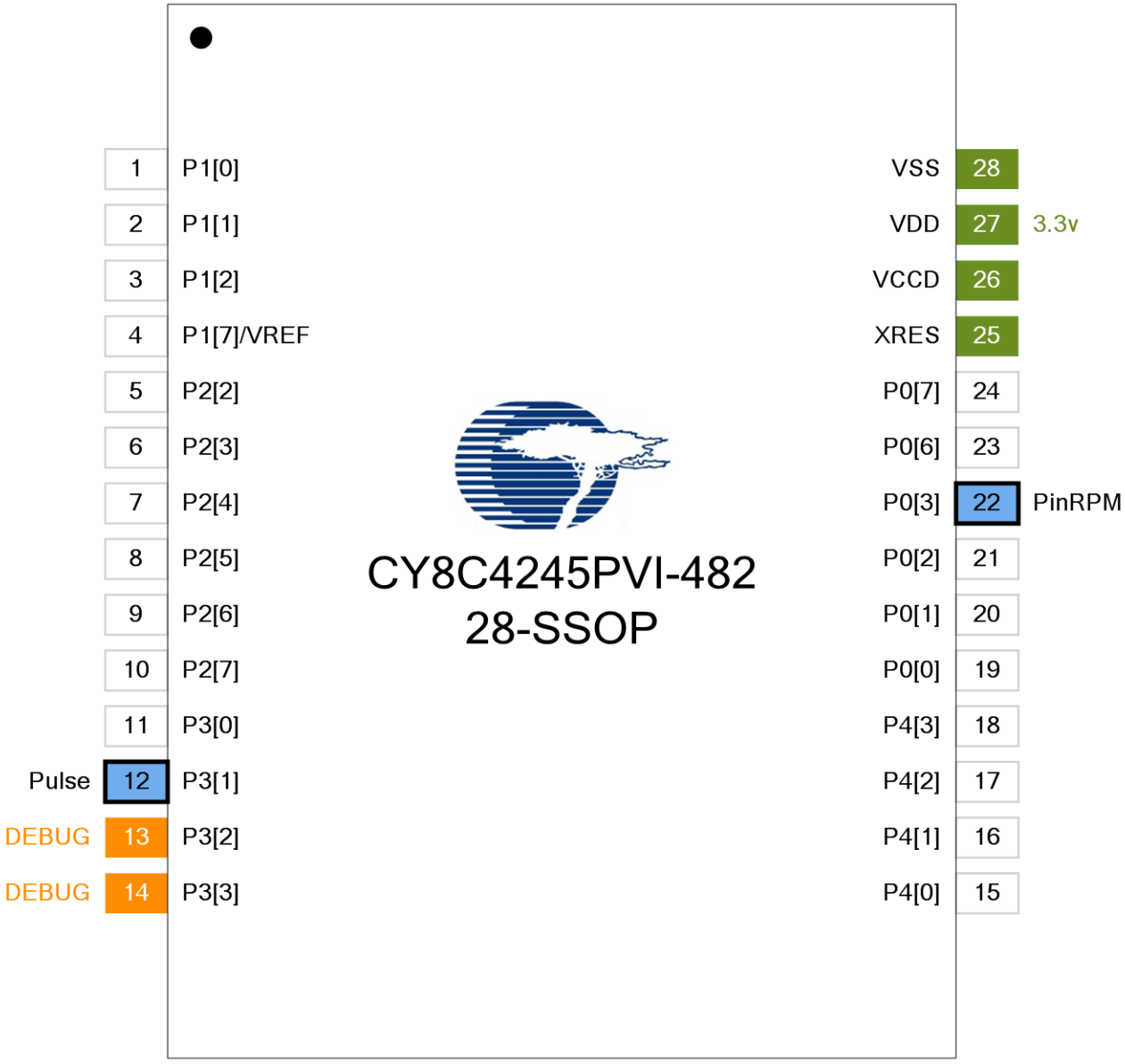
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	2	2	4	50.00 %
Interrupts	2	30	32	6.25 %
IO	4	20	24	16.67 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	0	2	2	0.00 %
Timer/Counter/PWM	0	4	4	0.00 %
UDB				
Macrocells	7	25	32	21.88 %
Unique P-terms	6	58	64	9.38 %
Total P-terms	6			
Datapath Cells	2	2	4	50.00 %
Status Cells	1	3	4	25.00 %
Statusl Registers	1			
Control Cells	1	3	4	25.00 %
Control Registers	1			
Comparator/Opamp	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	1	0	1	100.00 %
DAC				
7-bit IDAC	0	1	1	0.00 %
8-bit IDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	P1[0]	GPIO [unused]		
2	P1[1]	GPIO [unused]		
3	P1[2]	GPIO [unused]		
4	P1[7]/VREF	GPIO [unused]		
5	P2[2]	GPIO [unused]		
6	P2[3]	GPIO [unused]		
7	P2[4]	GPIO [unused]		
8	P2[5]	GPIO [unused]		
9	P2[6]	GPIO [unused]		
10	P2[7]	GPIO [unused]		
11	P3[0]	GPIO [unused]		
12	P3[1]	Pulse	Dgtl Out	Strong drive
13	P3[2]	Debug:SWD_IO	Reserved	
14	P3[3]	Debug:SWD_CK	Reserved	
15	P4[0]	GPIO [unused]		
16	P4[1]	GPIO [unused]		
17	P4[2]	GPIO [unused]		
18	P4[3]	GPIO [unused]		
19	P0[0]	GPIO [unused]		
20	P0[1]	GPIO [unused]		
21	P0[2]	GPIO [unused]		
22	P0[3]	PinRPM	A/D Out	HiZ analog
23	P0[6]	GPIO [unused]		
24	P0[7]	GPIO [unused]		
25	XRES	XRES	Dedicated	
26	VCCD	VCCD	Power	
27	VDD	VDD	Power	
28	VSS	VSS	Power	

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- A/D Out = Analog / Digital Output
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	19	GPIO [unused]		
P0[1]	20	GPIO [unused]		
P0[2]	21	GPIO [unused]		
P0[3]	22	PinRPM	A/D Out	HiZ analog
P0[6]	23	GPIO [unused]		
P0[7]	24	GPIO [unused]		
P1[0]	1	GPIO [unused]		
P1[1]	2	GPIO [unused]		
P1[2]	3	GPIO [unused]		
P1[7]/VREF	4	GPIO [unused]		
P2[2]	5	GPIO [unused]		
P2[3]	6	GPIO [unused]		
P2[4]	7	GPIO [unused]		
P2[5]	8	GPIO [unused]		
P2[6]	9	GPIO [unused]		
P2[7]	10	GPIO [unused]		
P3[0]	11	GPIO [unused]		
P3[1]	12	Pulse	Dgtl Out	Strong drive
P3[2]	13	Debug:SWD_IO	Reserved	
P3[3]	14	Debug:SWD_CK	Reserved	
P4[0]	15	GPIO [unused]		
P4[1]	16	GPIO [unused]		
P4[2]	17	GPIO [unused]		
P4[3]	18	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- A/D Out = Analog / Digital Output
- HiZ analog = High impedance analog
- Dgtl Out = Digital Output

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
GPIO [unused]	P4[1]	
GPIO [unused]	P4[2]	
GPIO [unused]	P0[0]	
GPIO [unused]	P1[0]	
GPIO [unused]	P4[0]	
GPIO [unused]	P0[6]	
GPIO [unused]	P0[7]	
GPIO [unused]	P0[2]	
GPIO [unused]	P4[3]	
GPIO [unused]	P0[1]	
GPIO [unused]	P2[3]	
GPIO [unused]	P2[4]	
GPIO [unused]	P1[7]/VREF	
GPIO [unused]	P1[1]	
GPIO [unused]	P1[2]	
GPIO [unused]	P2[2]	
GPIO [unused]	P2[7]	
GPIO [unused]	P3[0]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[6]	
PinRPM	P0[3]	A/D Out
Pulse	P3[1]	Dgtl Out

Abbreviations used in Table 5 have the following meanings:

- A/D Out = Analog / Digital Output
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0400
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Chip Protection	Open
Debug Select	SWD (serial wire debug)

3.3 System Operating Conditions

Table 8. System Operating Conditions

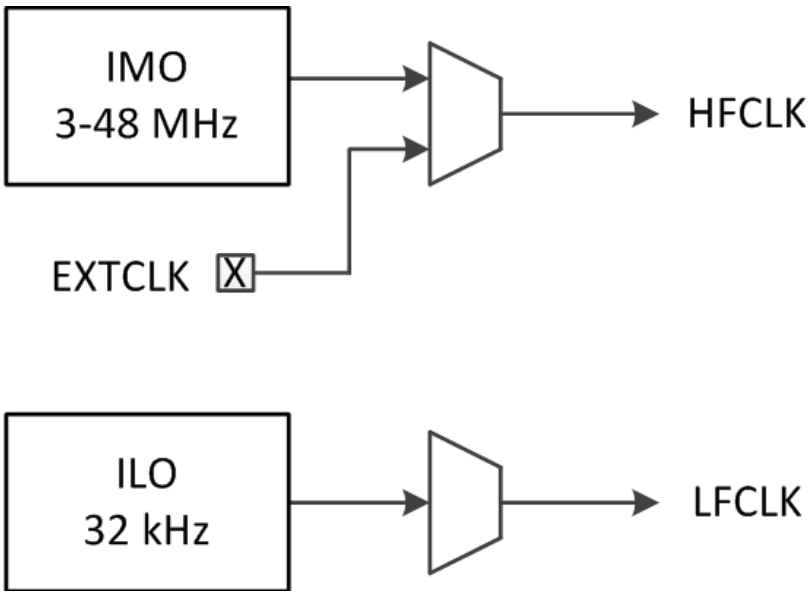
Name	Value
Variable VDDA	True
VDD (V)	3.3

4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±2% at 3 MHz
  - 32 kHz Internal Low Speed Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twelve clock dividers, each with 16-bit divide capability:
  - Eight can be used for fixed-function blocks
  - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
DPLL_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
SYSCLK	NONE	HFCLK	? MHz	24 MHz	±2	True	True
Direct_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
PLL1_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
PLL0_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
HFCLK	NONE	Direct_Sel	24 MHz	24 MHz	±2	True	True
IMO	NONE		24 MHz	24 MHz	±2	True	True
LFCLK	NONE	ILO	? MHz	32 kHz	±60	True	True
ILO	NONE		32 kHz	32 kHz	±60	True	True
Timer2 (WDT2)	NONE	LFCLK	? MHz	? MHz	±0	False	False
EXTCLK	NONE		24 MHz	? MHz	±0	False	False
DigSig3	NONE		? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
DigSig4	NONE		? MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
Timer1 (WDT1)	NONE	LFCLK	? MHz	? MHz	±0	False	False
Timer0 (WDT0)	NONE	LFCLK	? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

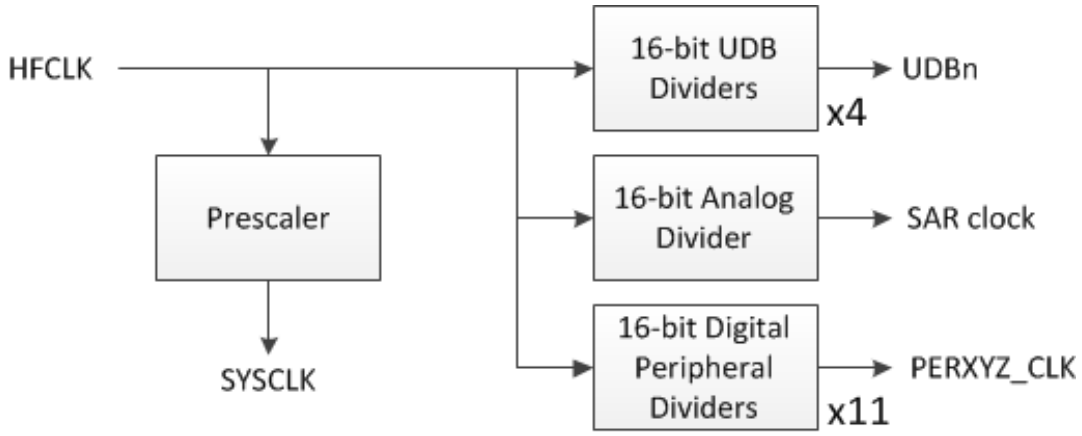


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ADC_intClock	FIXED_-FUNCT-ION	HFCLK	3 MHz	3 MHz	±2	True	True
Clock_100kHz	DIGITAL	HFCLK	500 kHz	500 kHz	±2	True	True
CLK_20Hz	DIGITAL	HFCLK	20 Hz	20 Hz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkWrite API routines

5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
ADC_IRQ	3	14
isr_Timed	3	0

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x7FFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 128 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

For more information on Flash memory and protection, please refer to:

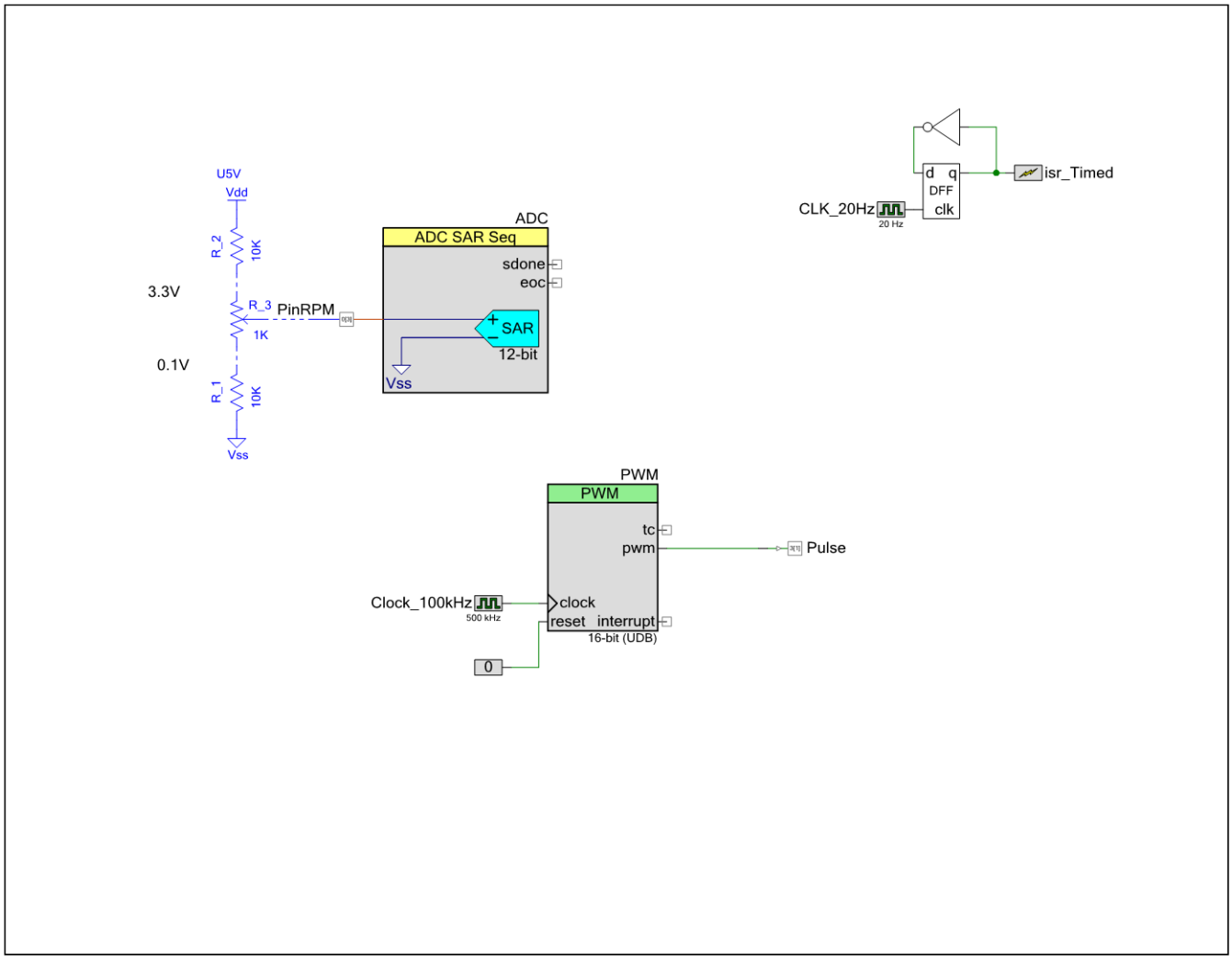
- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance ADC (type: ADC_SAR_SEQ_P4_v2_40)
- Instance PWM (type: PWM_v3_30)

8 Components

8.1 Component type: ADC_SAR_SEQ_P4 [v2.40]

8.1.1 Instance ADC

Description: PSoC 4 Sequencing Successive Approximation ADC
Instance type: ADC_SAR_SEQ_P4 [v2.40]
Datasheet: online component datasheet for ADC_SAR_SEQ_P4

Table 13. Component Parameters for ADC

Parameter Name	Value	Description
AdcAClock	4	Acquisition time in clock cycles for configuration A.
AdcAdjust	ClockFreq	Timing parameter adjustable by the user.
AdcAlternateResolution	8	This parameter sets the alternate ADC resolution to either 8 or 10 bits.
AdcAvgMode	Fixed Resolution	This parameter sets how the averaging mode operates.
AdcAvgSamplesNum	4	This parameter sets the averaging rate for any channel that has its averaging option enabled.
AdcBClock	4	Acquisition time in clock cycles for configuration B.
AdcCClock	4	Acquisition time in clock cycles for configuration C.
AdcChannelsEnConf	1	This bitmask is intended to enable the channels for scanning during runtime.
AdcChannelsModeConf	0	Mode configuration for the channels (0 - Single, 1 - Differential)
AdcClock	Internal	Clock source type.
AdcClockFrequency	3000000	Specifies the internal clock frequency in Hz.
AdcCompareMode	Result < Low_Limit	This parameter sets the condition in which the limit condition will occur.
AdcDataFormatJustification	Right	This parameter sets whether the output data is left or right justified for a 16-bit word. For signed values, the result will be sign extended when configured in right justification mode.
AdcDClock	4	Acquisition time in clock cycles for configuration D.
AdcDifferentialResultFormat	Unsigned	This parameter sets the whether the result from a differential measurement is Signed or Unsigned.
AdcHighLimit	2047	This parameter sets the high limit for a limit compare.

Parameter Name	Value	Description
AdcInjChannelEnabled	false	Determines whether the symbol will display the injection channel.
AdcInputBufGain	Disable	Sets the input buffer gain or disables it.
AdcLowLimit	0	This parameter sets the low limit for a limit compare.
AdcMaxResolution	12	Sets the maximum resolution of the ADC in bits.
AdcSampleMode	FreeRunning	Sampling mode.
AdcSarMuxChannelConfig	0	Channels mode configuration for the multiplexer (0 - Single, 1 - Differential)
AdcSequencedChannels	1	Number of input signals that will be scanned. This excludes the injection channel.
AdcSingleEndedNegativeInput	Vss	Negative input source for single ended operation.
AdcSingleResultFormat	Signed	This parameter sets whether the result from a single ended measurement is Signed or Unsigned.
AdcSymbolHasSingleEn-dedInputChannel	false	Determines whether the configuration contains an external negative input.
AdcVrefSelect	VDDA	The reference voltage that is used for the SAR ADC.
AdcVrefVoltage_mV	1024	The reference voltage value.
rm_int	false	Removes the internal interrupt

8.2 Component type: PWM [v3.30]

8.2.1 Instance PWM

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.30]
Datasheet: online component datasheet for PWM

Table 14. Component Parameters for PWM

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	10	Compares Output 1 to value
CompareValue2	1	Compares Output 2 to value

Parameter Name	Value	Description
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	625	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	16	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 4 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines