**RAM**

Test plan:

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| --- | --- |
| Function | How to test |
| Reset | Make assertions on values after reset |
| Write address | Assert if the din [9:8]==00 the next will be write data which is din[9:8]==01 |
| Read address | Similar constrain input and cover point then make assertions |
| Write data | Similar constrain input and cover point then make assertions |
| Read data | Similar constrain input and cover point then make assertions |

**Run.do file:**

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| --- |
| vlib work  vlog -f src\_files.txt  vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all  add wave -position insertpoint sim:/top/ram\_regif/\*  coverage save ram.ucdb -onexit  run -all |

Constrains randomization to input:

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| --- |
| constraint rst\_n\_c {          rst\_n dist  {1:=99 , 0:=1};      }      constraint rx\_valid\_c {          rx\_valid dist {1:/90 , 0:/10};      }      constraint din\_9\_8\_c {          (old\_value\_9\_8\_din==2'b00) -> din[9:8] == 2'b01 ;          (old\_value\_9\_8\_din==2'b10) -> din[9:8] == 2'b11 ;          (old\_value\_9\_8\_din==2'b01||old\_value\_9\_8\_din==2'b11) -> din[9:8] dist {2'b00:/50 , 2'b10:/50} ;      } |

Constrain din [9:8] if the previous randomization is 00 next to be 10. (Write flow)

Constrain din [9:8] if the previous randomization is 10 next to be 11. (Read flow)

**Code coverage:**

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**Cover groups form Questa:**

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**Assertion’s coverage:**

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| Assertion Coverage:      Assertions                       5         5         0   100.00%  --------------------------------------------------------------------  Name                 File(Line)                   Failure      Pass                                                    Count        Count  --------------------------------------------------------------------  /ram\_top/dut/ram\_sva\_instan/assert\_\_read\_address\_next\_read\_data                       ram\_sva.sv(46)                     0          1  /ram\_top/dut/ram\_sva\_instan/assert\_\_write\_address\_next\_write\_data                       ram\_sva.sv(37)                     0          1  /ram\_top/dut/ram\_sva\_instan/assert\_\_tx\_remain\_low\_to\_nextRead                       ram\_sva.sv(28)                     0          1  /ram\_top/dut/ram\_sva\_instan/assert\_\_check\_tx\_valid\_transition                       ram\_sva.sv(19)                     0          1  /ram\_top/dut/ram\_sva\_instan/assert\_\_check\_reset                       ram\_sva.sv(10)                     0          1  Directive Coverage:      Directives                       5         5         0   100.00% |

**Assertions from Questa sim:**

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**Assertions in code:**

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| --- |
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**Results on wave form:**

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| --- |
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**Bug report:**

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| --- |
|  |

1. **tx\_valid must be low for all cases except read data .**
2. **on reset WRITE\_ADD<=0 ; READ\_ADD <=0 ; should be zero .**
3. **also we should handle the case if rst\_n = 1 and rx\_valid not equal =1 ;**

**code after correctness:**

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| --- |
|  |

**SPI**

**Run.do file:**

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| --- |
| vlib work  vlog -f src\_files.txt  vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all  add wave -position insertpoint sim:/top/ram\_regif/\*  coverage save spi.ucdb -onexit  run -all |

**Cover groups form Questa:**

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| --- |
|  |

**Results on wave form:**

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| --- |
|  |

**Bug report:**

there wasn’t any bugs