Mohammad Farukh Zafar

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Education

- **Indian Institute of Science** — Bangalore, India
  M.Tech in Electronics Systems Engineering; GPA: 8.6 — *2024 - 2026*

- **Jamia Millia Islamia** — New Delhi, India
  B.Tech in Electronics and Communication; GPA: 9.8 — *2020 - 2024*

Experience

- **Stepping Cloud Consulting Pvt Ltd** — New Delhi, India
  Trainee Intern — *Jul 2023 - Sep 2023*
  - Worked with the product development team on developing the software product AlumX-Connecting Alumni
  - Identified and resolved bugs, ensuring improved software reliability and functionality

Projects

- **Quantum Key Distribution (QKD) Receiver System (Ongoing - MTech major project)**: Designing and developing a secure optical receiver system based on the Coherent One-Way (COW) protocol. The project involves interfacing the TDC7200IC with a Basys3 FPGA to achieve high-precision time-of-flight measurements with 55ps resolution. My work has focused on implementing the SPI communication protocol and a Finite State Machine on the FPGA to control the TDC and accurately measure time intervals between start and stop signals. *(Technology: Verilog, FPGA, SPI)*
- **16-bit Multicycle CISC Processor Implementation**: Designed and implemented a 16-bit multicycle CISC processor on Basys3 FPGA platform. Developed comprehensive instruction set including arithmetic operations, memory access, shift/rotate functions, and conditional branching. Implemented unified 32×16-bit memory architecture with distributed RAM and validated design using 8-bit unsigned multiplication algorithm. Achieved 138 MHz maximum operating frequency with efficient resource utilization and robust timing margins. (Technology: Verilog, Processor Design, FPGA)
- **FPGA-Based HDR Image Tone-Mapping System**: Implemented Gaussian filtering component of HDR image tone-mapping algorithm on FPGA for hardware acceleration. Developed efficient line buffer approach for processing high-resolution images with limited on-chip memory and designed UART-based communication interface for host processor integration. Achieved TMQI score of 0.79 indicating high-quality tone-mapping results with minimal visual differences compared to software implementation.

  (Technology: Verilog, FPGA, Image Processing)
- **Embedded Vending Machine System**: Designed and developed a fully functional vending machine prototype using TM4C123G microcontroller with LCD interface, PWM motor control, and IR sensor-based product availability detection. Implemented non-blocking state machine architecture with timer interrupts for responsive operation and integrated payment detection mechanism with audio feedback. Achieved 99% dispensing success rate and 98% IR sensor accuracy through comprehensive testing and optimization. *(Technology: Embedded Systems, TM4C123G, I2C)*
- **16-bit Pipelined Booth Multiplier**: Designed and implemented a 16-bit signed pipelined radix-4 Booth multiplier to enhance multiplication efficiency. Developed 2-stage pipelining approach with Wallace tree reduction and carry-skip adders for optimized performance. Achieved maximum clock frequency of 626 MHz at best PVT corner and demonstrated significant improvement in throughput while maintaining accuracy for both signed and unsigned multiplication operations. *(Technology: Cadence Virtuoso, Digital Design)*

Skills Summary

- **Hardware Description Languages**: Verilog
- **Programming Languages**: C, Python, MATLAB
- **Tools**: Xilinx Vivado, Cadence Virtuoso, Code Composer Studio, Keil uVision, Altium, KiCad
- **Microcontroller/ FPGA boards**: TM4C123G (Arm Cortex-M4), Arduino Uno, ATtiny85, Basys 3 Artix-7, Raspberry Pi 4

Coursework

- Digital VLSI design
- Digital System Design with FPGAs
- Processor System Design
- Fundamentals of MOS Analog Integrated Circuits
- Embedded System Design
- Neuromorphic Analog VLSI Design

Achievements

- GATE Qualified: Qualified the Graduate Aptitude Test in Engineering (GATE) in the 3rd and 4th year of B.Tech with a AIR of 196
- Branch Rank 1: Ranked 1st in the BTech Electronics and Communication Engineering