Ring OSCILLATOR VERIFICATION PLAN

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# Verification Methodology

Simple testbench is developed using SystemVerilog. Since this is a very simple design complex verification methodology like UVM is not used. The testbench computes the expected clock frequency based on parameter values i.e. Inverter stage and Inverter delay using the following equation,

Where, n = number of inverter stage and t= delay value of single inverter.

This frequency value is compared with that of the measured clock frequency and test passes if both are equal.