Ring Oscillator Design Specification

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# Introduction to Ring Oscillator

A **ring oscillator** is a device composed of an odd number of [NOT gates](https://en.wikipedia.org/wiki/Inverter_(logic_gate)) in a ring, whose output [oscillates](https://en.wikipedia.org/wiki/Oscillation) between two voltage levels, representing *true* and *false*. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.



# Proposed Design

The ring oscillator design is parameterized to create a wide range of clock frequency.

The parameters are:

1. NO\_STAGES : Specifies the number of inverter stages. It must be a odd number
2. INV\_DELAY\_ns: Specifies the delay value in ns provided by a single inverter. This value is used for modeling purpose and must be matches with the inverter model in provided technology file or PDK.

Ports:

1. en: Enable signal of ring oscillator.
2. Clk\_out: Output clock signal.

Equation of Frequency generated:

If 't' represents the time-delay for a single Inverter and 'n' represents the number of Inverters in the Inverter chain, then the frequency of oscillation is given by,