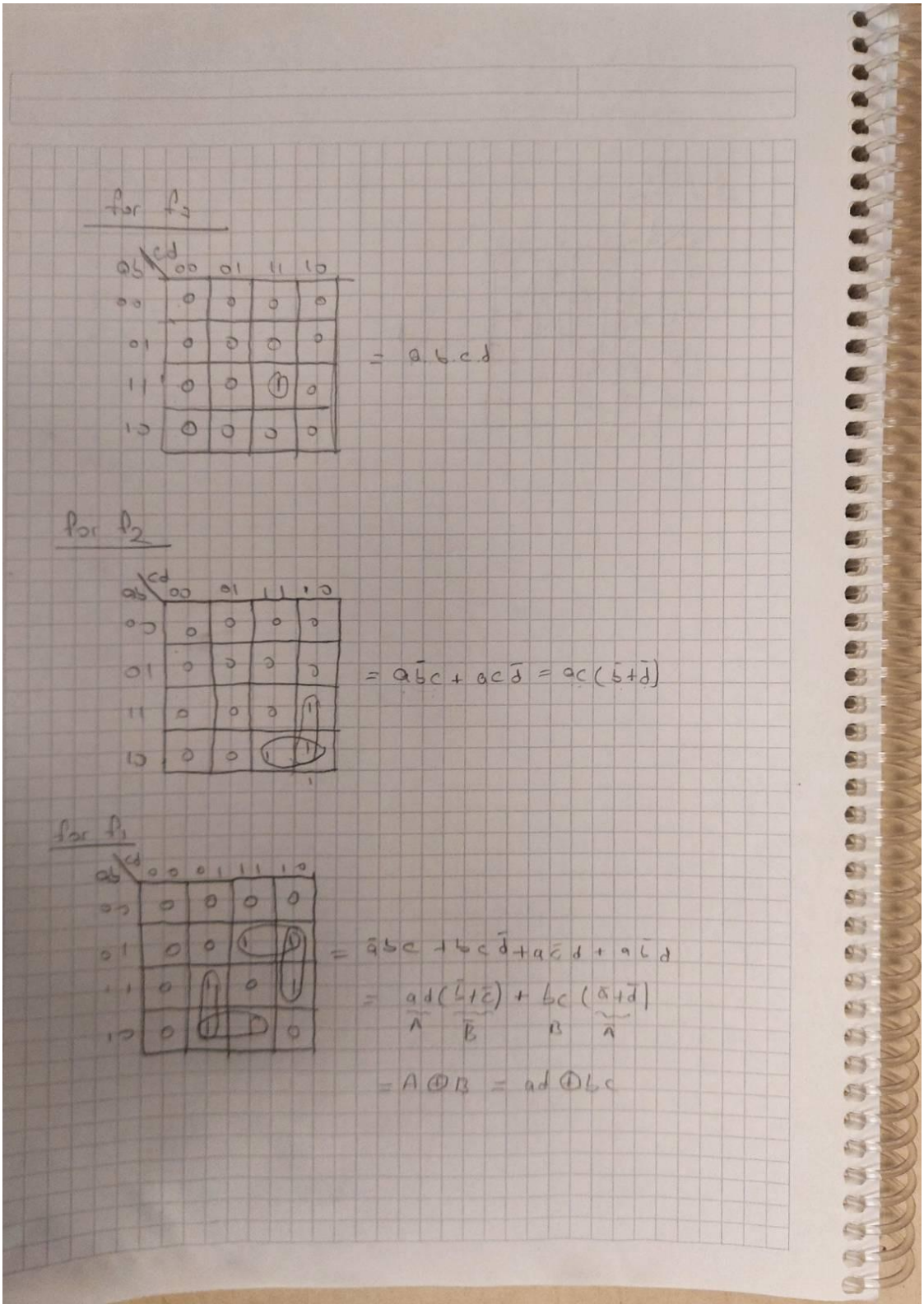
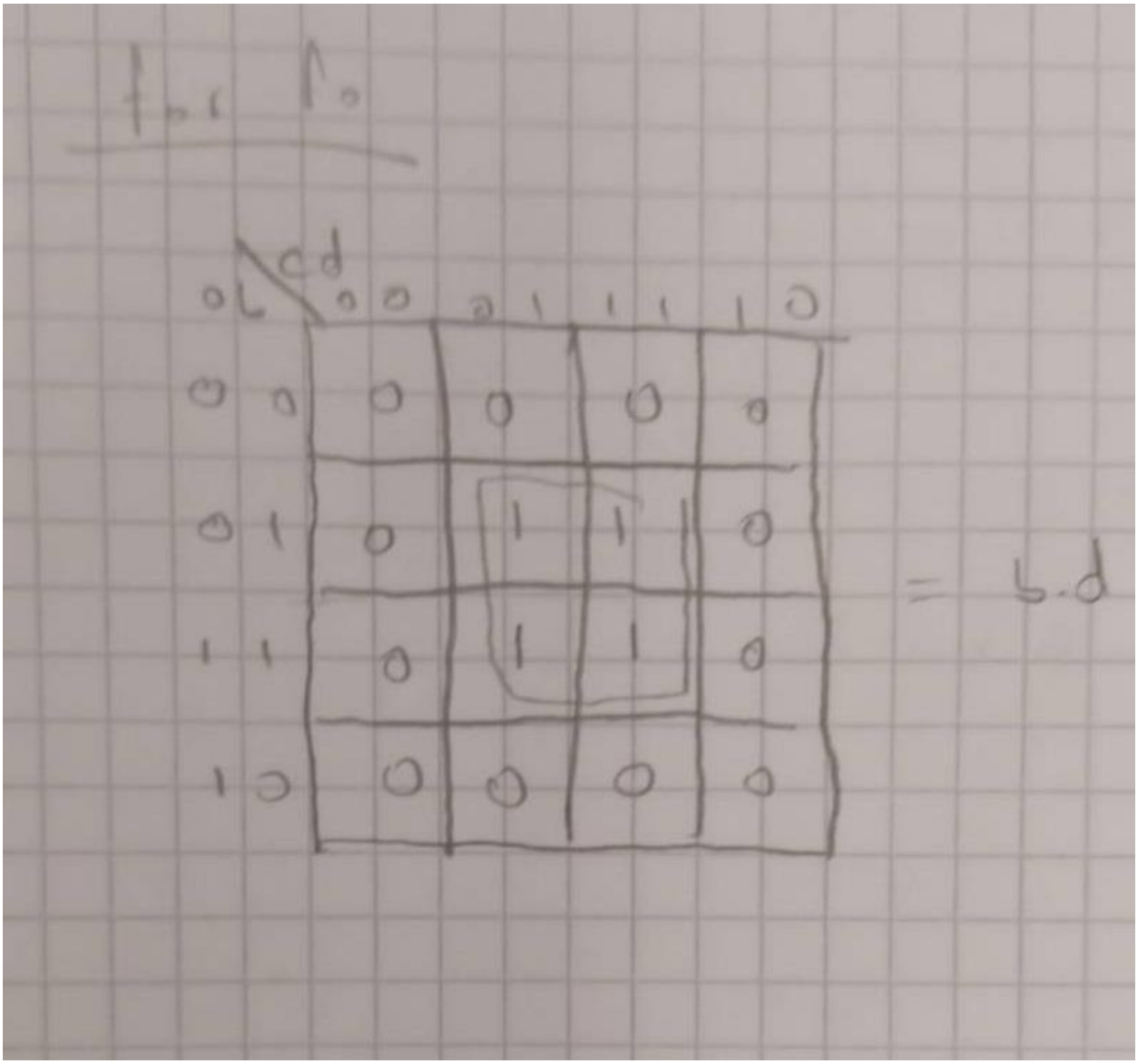
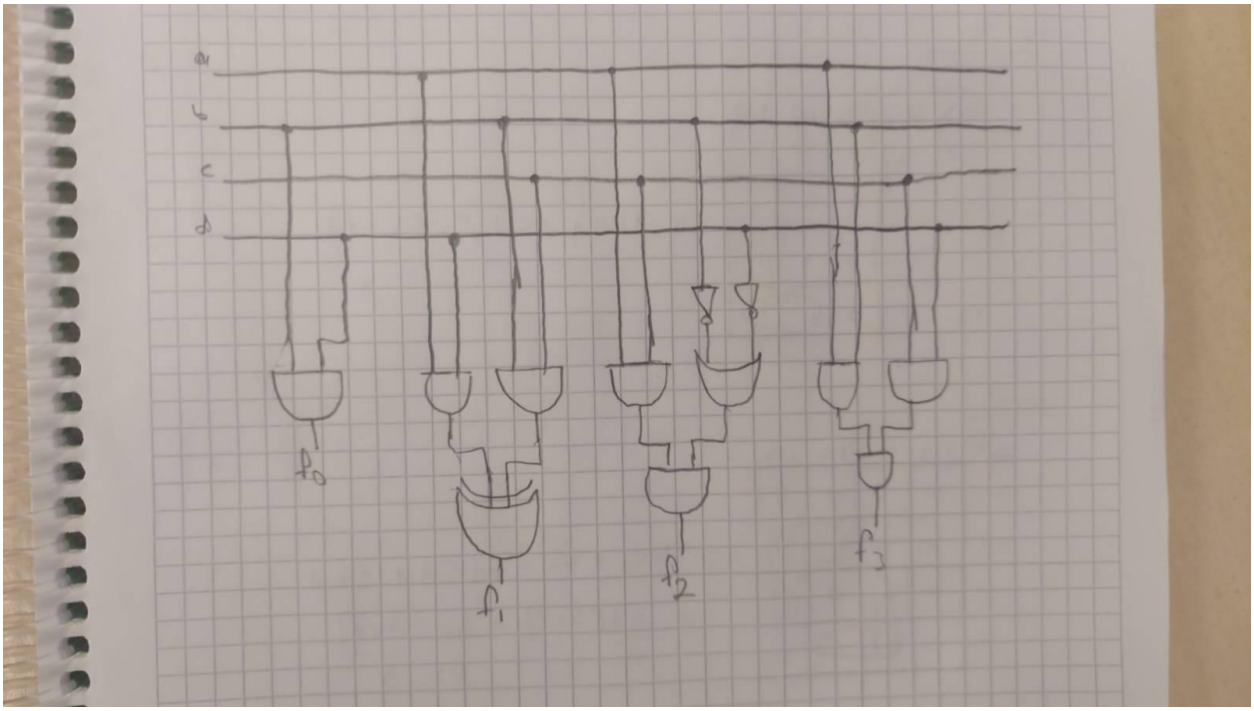
Karnaugh Map




f0,1 f0
cd
ab
00 01 11 10
00 0 0 0 0
01 0 1 1 0
11 0 1 1 0
10 0 0 0 0
= b.d

Hand Drawn Gate Level Circuit



Console Output# run 1000ns

{a,b,c,d}=0000 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=0001 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=0010 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=0011 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=0100 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=0101 => {f3,f2,f1,f0} = 0001 -- TRUE

{a,b,c,d}=0110 => {f3,f2,f1,f0} = 0010 -- TRUE

{a,b,c,d}=0111 => {f3,f2,f1,f0} = 0011 -- TRUE

{a,b,c,d}=1000 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=1001 => {f3,f2,f1,f0} = 0010 -- TRUE

{a,b,c,d}=1010 => {f3,f2,f1,f0} = 0100 -- TRUE

{a,b,c,d}=1011 => {f3,f2,f1,f0} = 0110 -- TRUE

{a,b,c,d}=1100 => {f3,f2,f1,f0} = 0000 -- TRUE

{a,b,c,d}=1101 => {f3,f2,f1,f0} = 0011 -- TRUE

{a,b,c,d}=1110 => {f3,f2,f1,f0} = 0110 -- TRUE

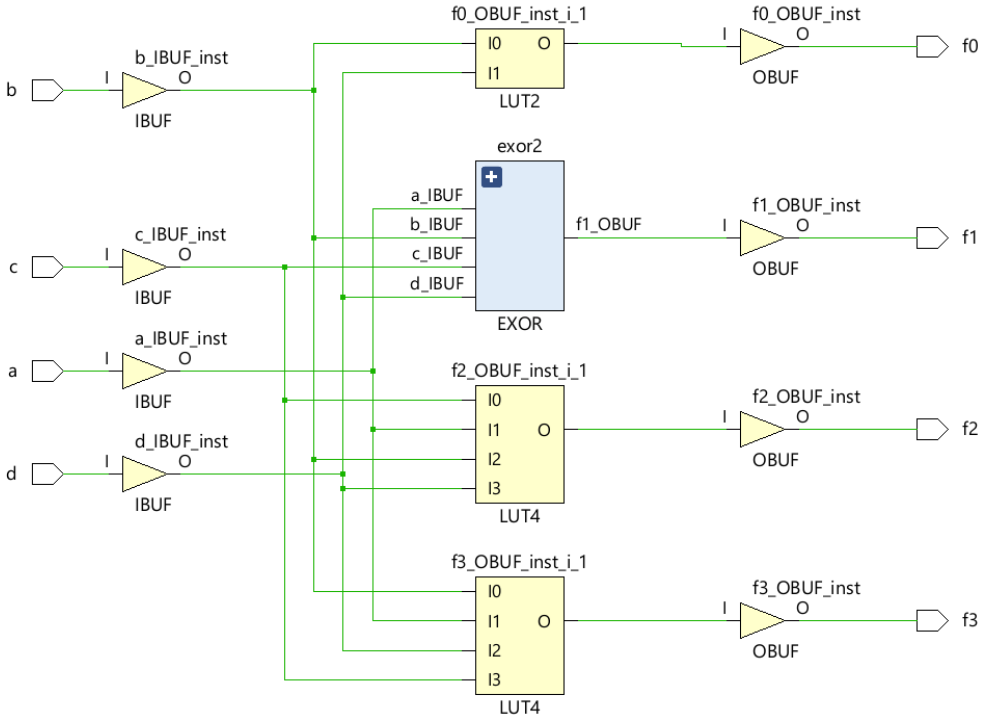
{a,b,c,d}=1111 => {f3,f2,f1,f0} = 1001 -- TRUE

$finish called at time : 800 ns : File "C:/Users/omer/Desktop/Dersler/EHB436E/HW/03/Viv/project_3/project_3.srcs/sim_1/imports/Projectfiles/experiment3_tb.v" Line 52

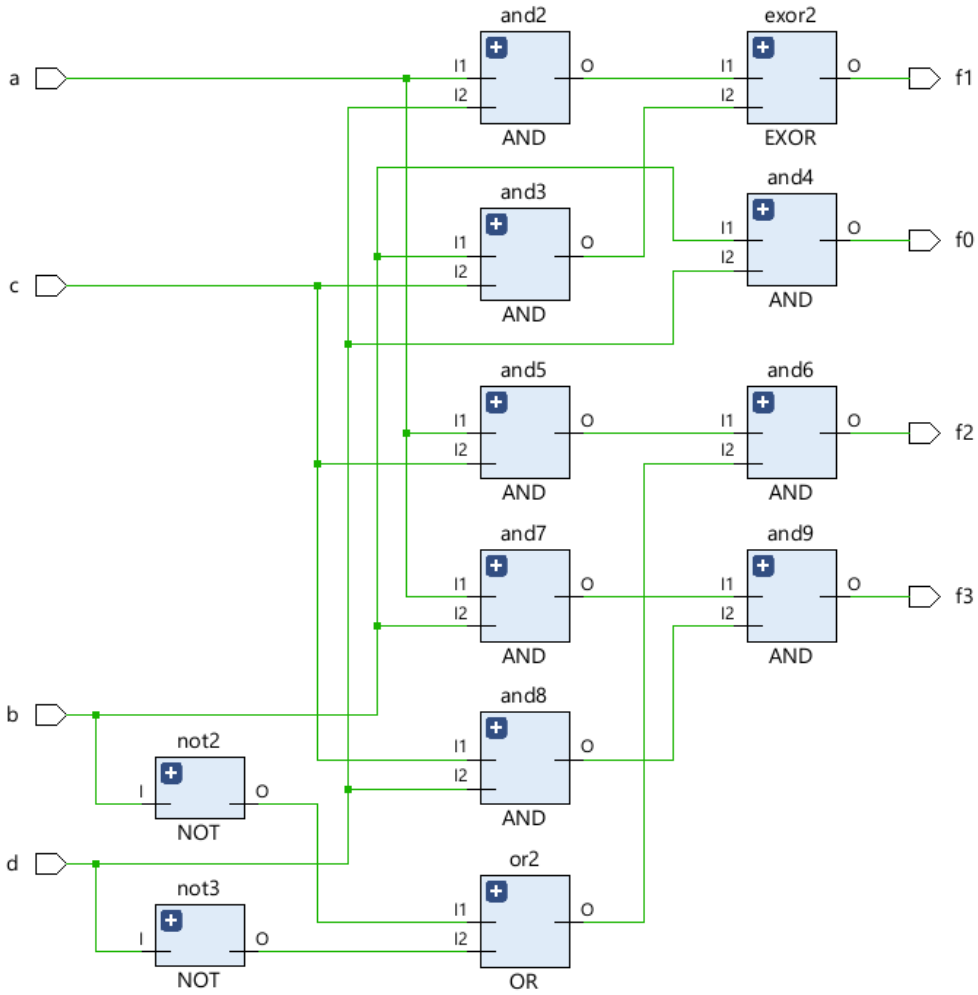
RTL and Technology Schematics

No Timing and LOC Constraints

Technology Schematic



RTL Schematic



Combinational Delay Without Constraints

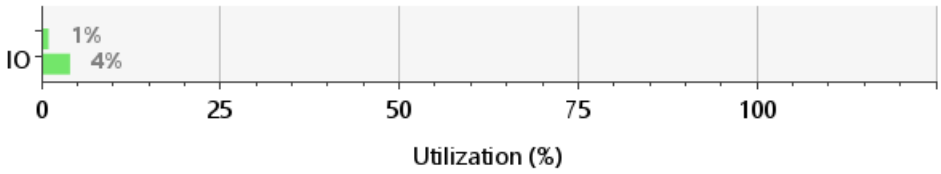
From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f2	9.601	SLOW	2.992	FAST
a	f1	9.524	SLOW	2.9	
d	f2	9.489	SLOW	2.910	FAST
b	f1	9.402	SLOW	2.851	FAST
c	f1	9.199	SLOW	2.728	FAST
a	f3	9.111	SLOW	2.809	FAST
c	f2	9.088	SLOW	2.729	FAST

Select path

Utilization Summary Without Constraints

Summary

Resource	Utilization	Available	Utilization %
LUT	5	63400	0.01
IO	8	210	3.81



With Time Constraint, No LOC Constraint

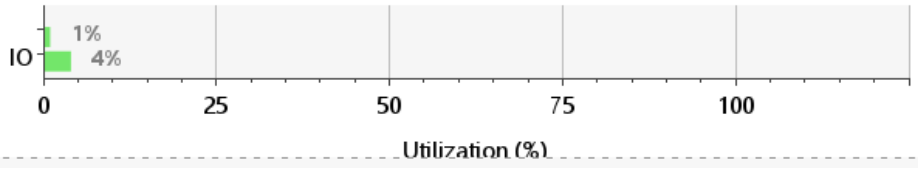
Maximum Combinational Delay with Timing Constraint

From Port	To Port	Max Delay	Max Process Corner
a	f1	8.997	SLOW
c	f2	8.744	SLOW
a	f2	8.720	SLOW
b	f2	8.633	SLOW
d	f1	8.610	SLOW
b	f1	8.562	SLOW

Utilization Summary with Timing Constraint

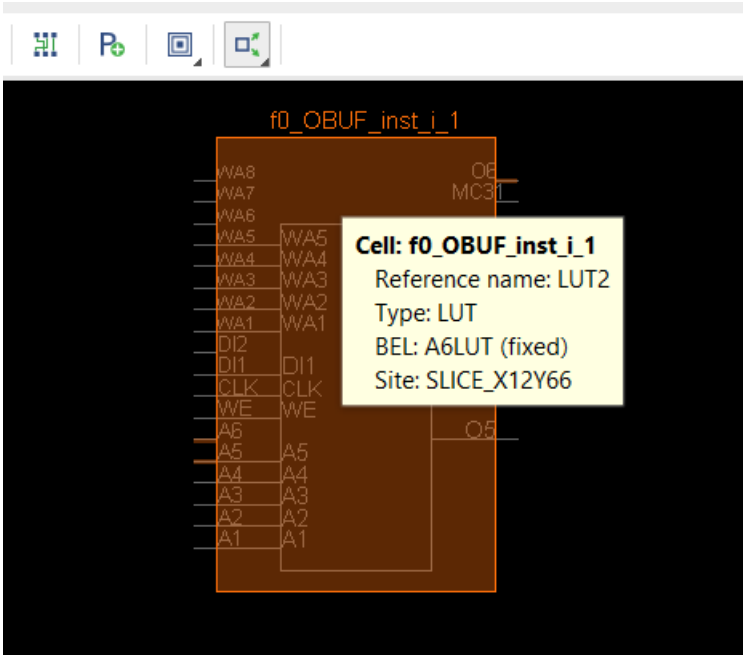
Summary

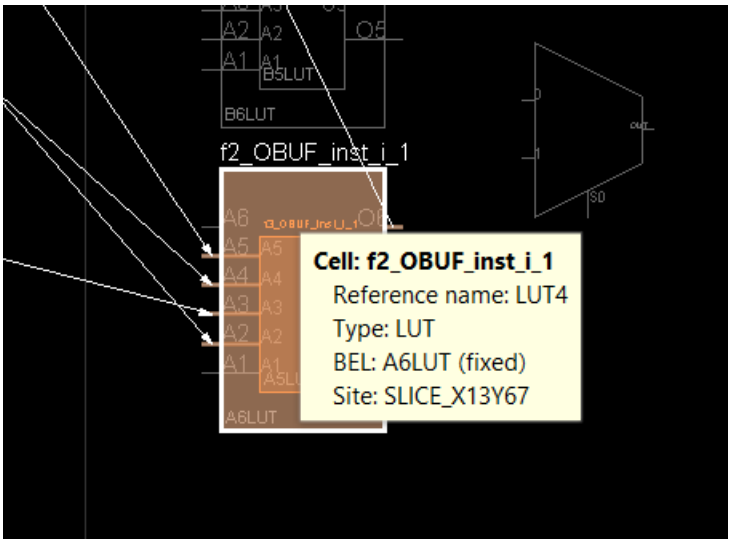
Resource	Utilization	Available	Utilization %
LUT	6	63400	0.01
IO	8	210	3.81



LUT usage is increased and that made circuit faster, using closer LUTs to the relevant port can make circuit faster

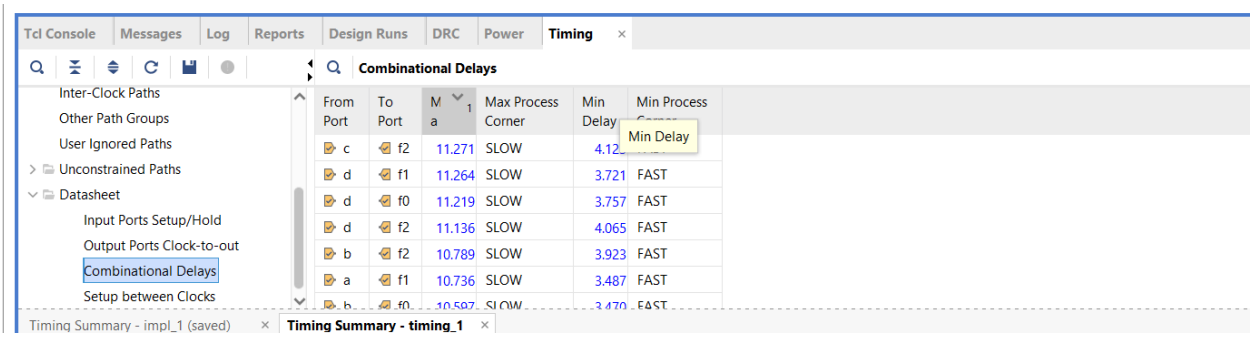
With LOC constraint, No Timing Constraint



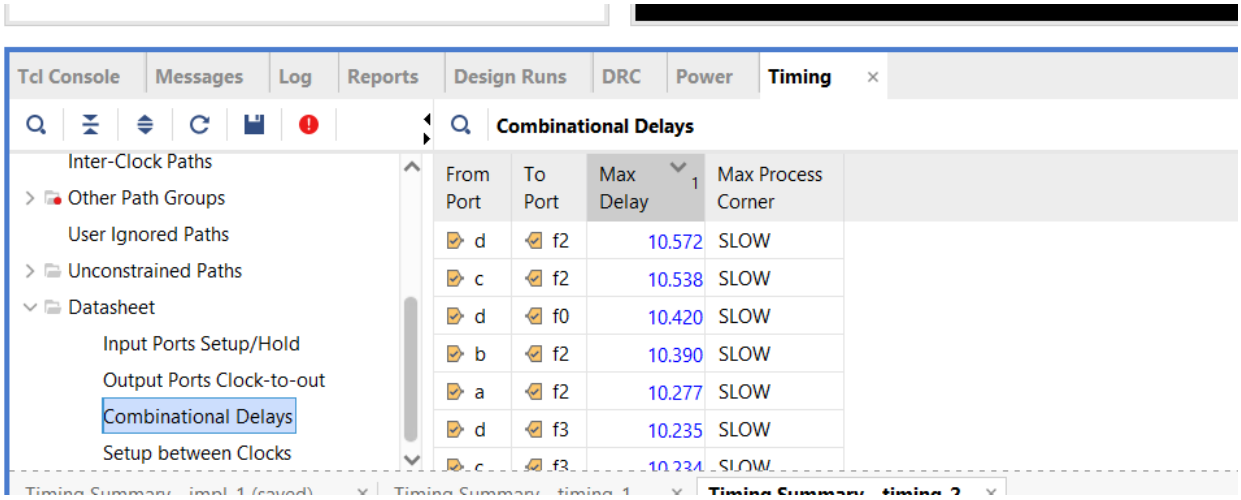



```
set_property LOC SLICE_X13Y67 [get_cells f2_OBUF_inst_i_1]
set_property LOC SLICE_X12Y66 [get_cells f0_OBUF_inst_i_1]
```

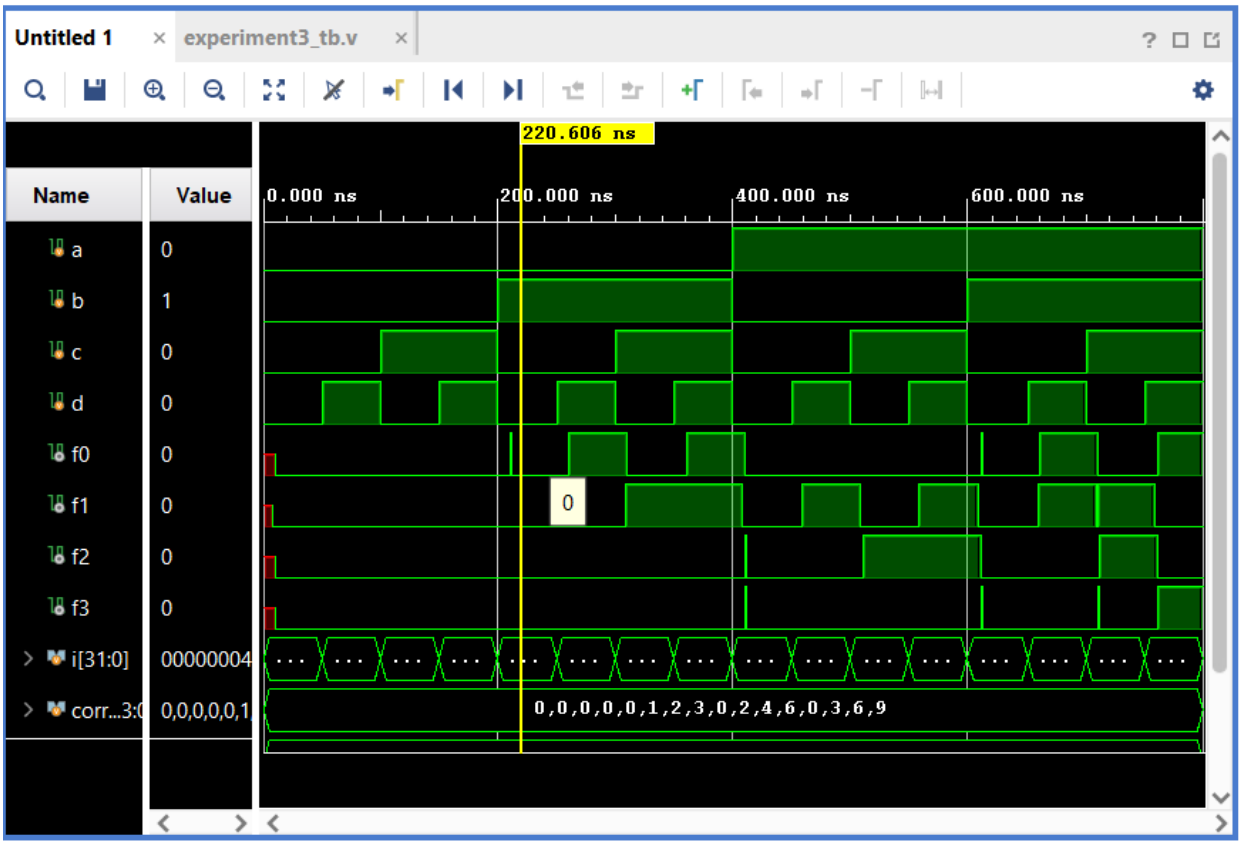
Combinational Delay with LOC constraint



With LOC and Time Constraints



It failed to make circuit delay with desired results because we fixed the locations of the LUTS so it could satisfy the conditions without changing LUTs locations



Difference between behavioural simulation and Post Implementation Timing Simulation

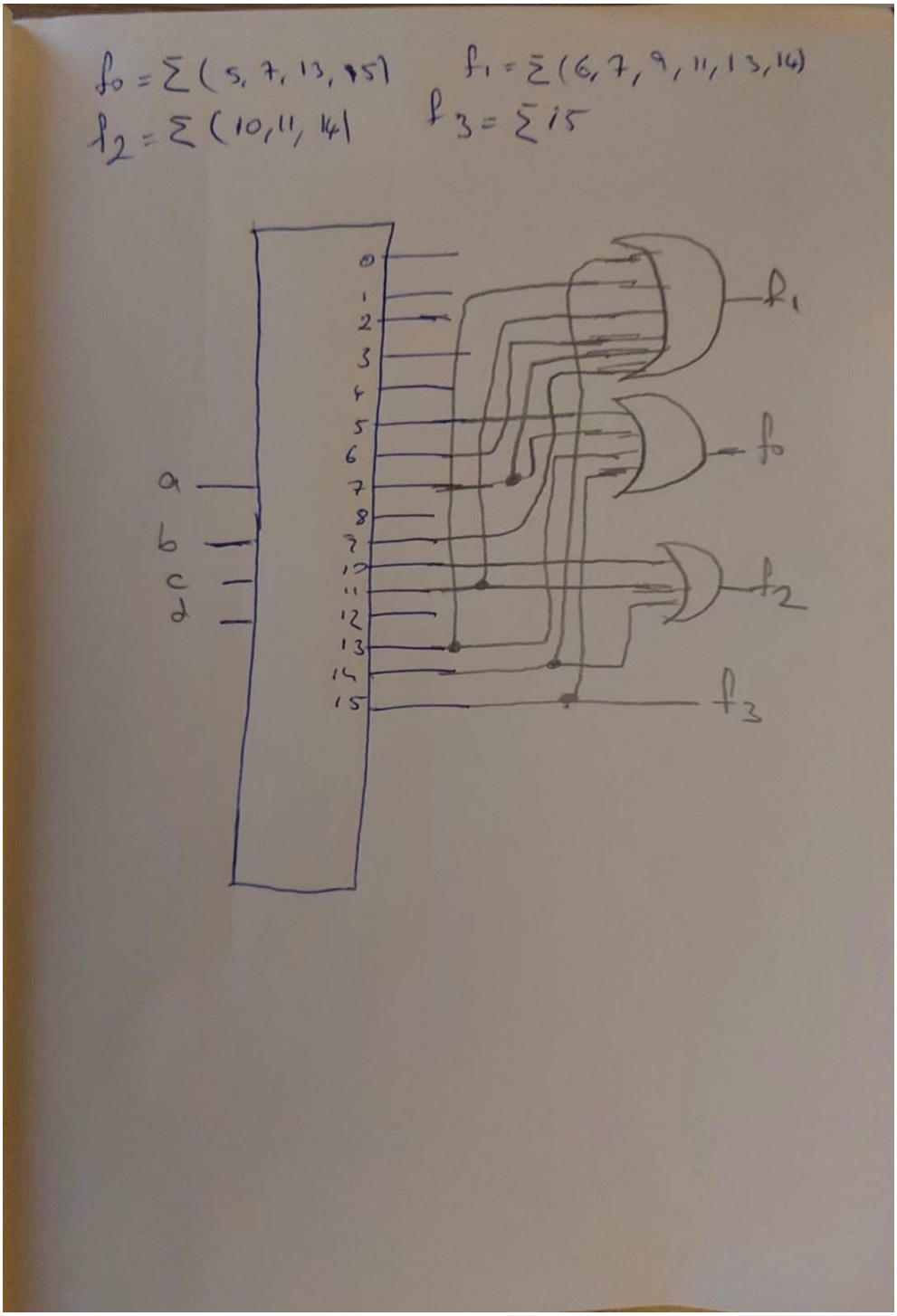
Because of the delays some unwanted results is occurring temporarily like when inputs are 0000 output must be 0000 but we see 1 at f0 for a short time period it is caused by different delay times between ports

Comparison

Each implementation has different delays, fastest one is the one that has only timing constraint because we did not fix any

LUT to a certain point so it changed their locations freely to meet the conditions of constraint file.

2 With Decoder



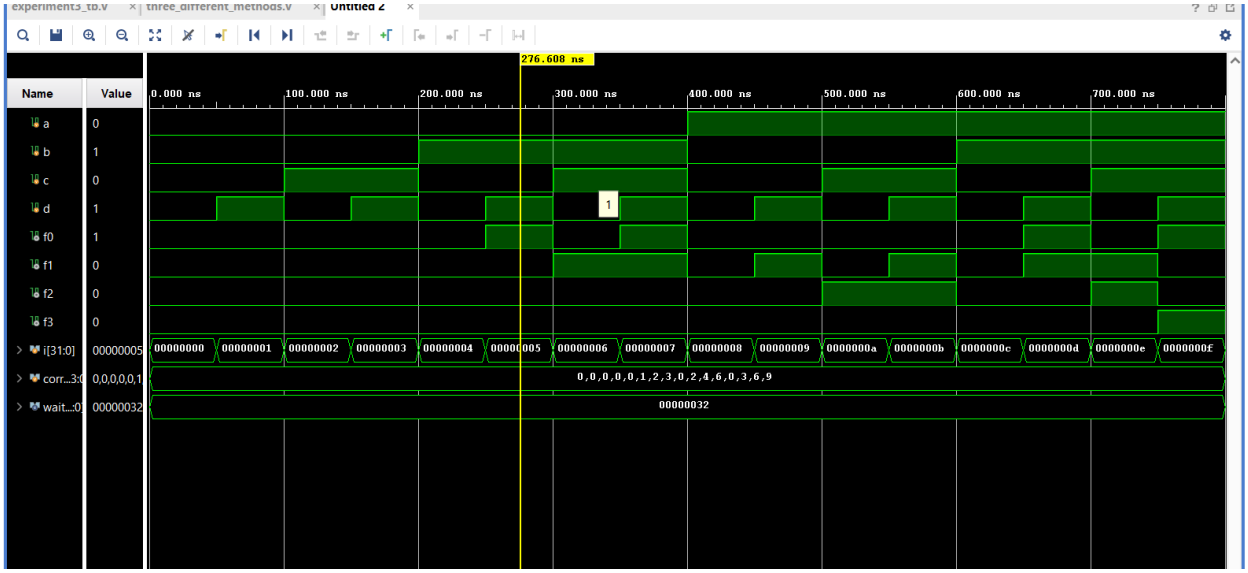
$$f_0 = \bar{a}b\bar{c}d + \bar{a}bcd + ab\bar{c}d + abcd$$

$$f_1 = \bar{a}bc\bar{d} + \bar{a}bcd + a\bar{b}\bar{c}d + a\bar{b}cd + ab\bar{c}d + abc\bar{d}$$

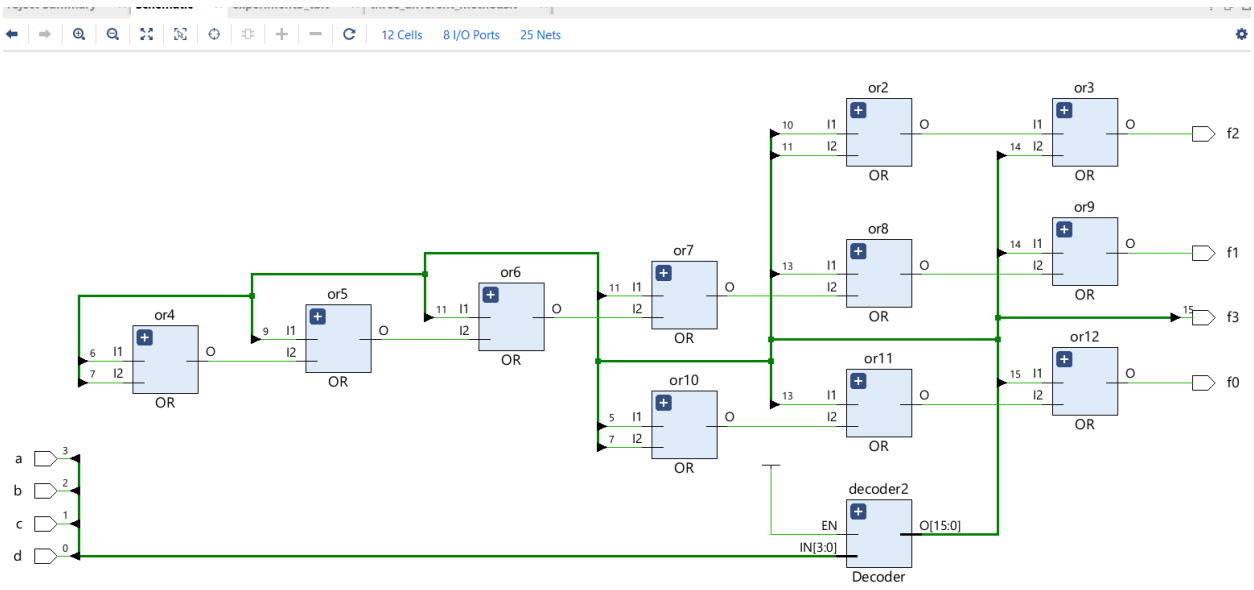
$$f_2 = a\bar{b}c\bar{d} + a\bar{b}cd + abc\bar{d}$$

$$f_3 = abcd$$

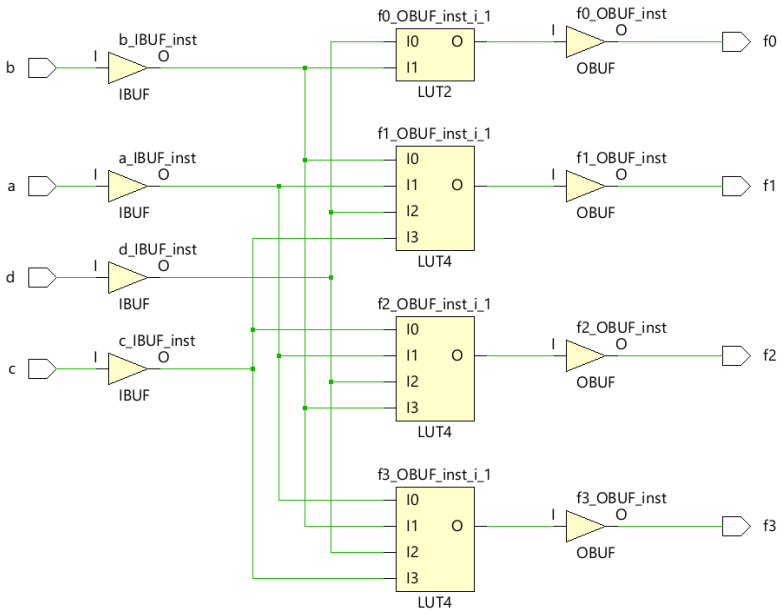
Wave form of behavioral simulation



RTL schematic



Technology Schematic



Combinational Delay

Combinational Delays

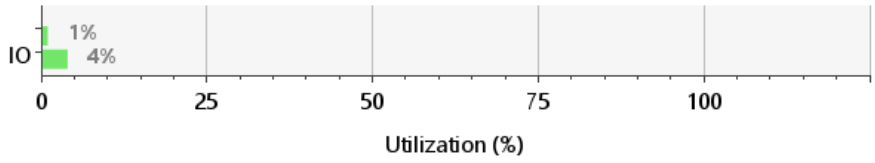
From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
c	f2	14.493	SLOW	7.049	FAST
b	f0	14.143	SLOW	6.210	FAST
b	f2	13.729	SLOW	6.546	FAST
d	f0	12.479	SLOW	5.106	FAST
d	f2	12.051	SLOW	5.429	FAST
c	f1	11.864	SLOW	5.047	FAST
b	f1	11.100	SLOW	4.533	FAST
c	f3	10.942	SLOW	4.613	FAST
a	f2	10.533	SLOW	4.707	FAST
b	f3	10.188	SLOW	4.110	FAST
d	f1	9.425	SLOW	3.427	FAST
d	f3	8.498	SLOW	2.991	FAST
a	f1	7.910	SLOW	2.689	FAST
a	f3	6.998	SLOW	2.264	FAST

There is not different type of cell

Utilization

Summary

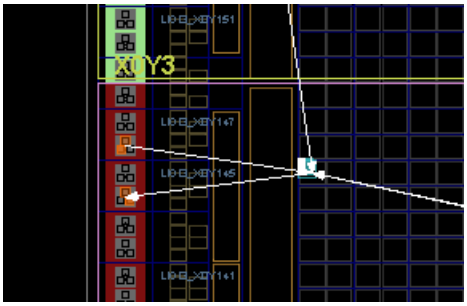
Resource	Utilization	Available	Utilization %
LUT	2	63400	0.00
IO	8	210	3.81



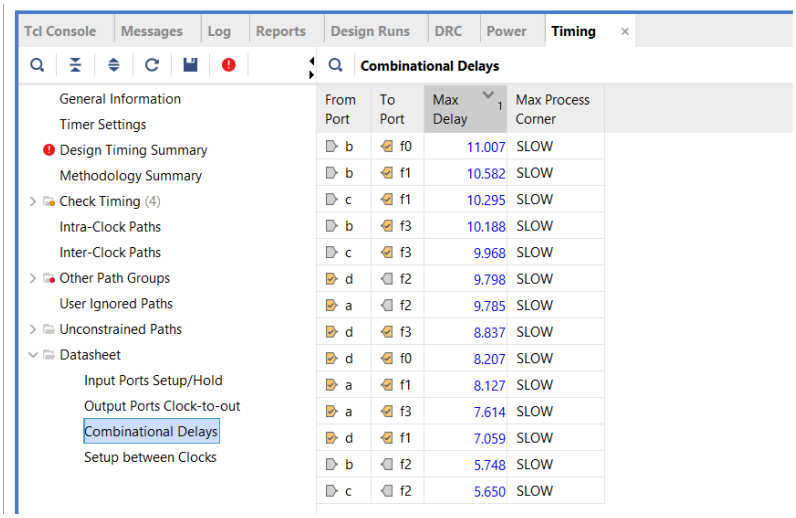
Comparison of Resource Usage Between Decoder and SSI Implementation

Design with decoder needs less process, in decoder part it just gives desired 1 to output, needs less process, that's why designing with decoder needs less resources.

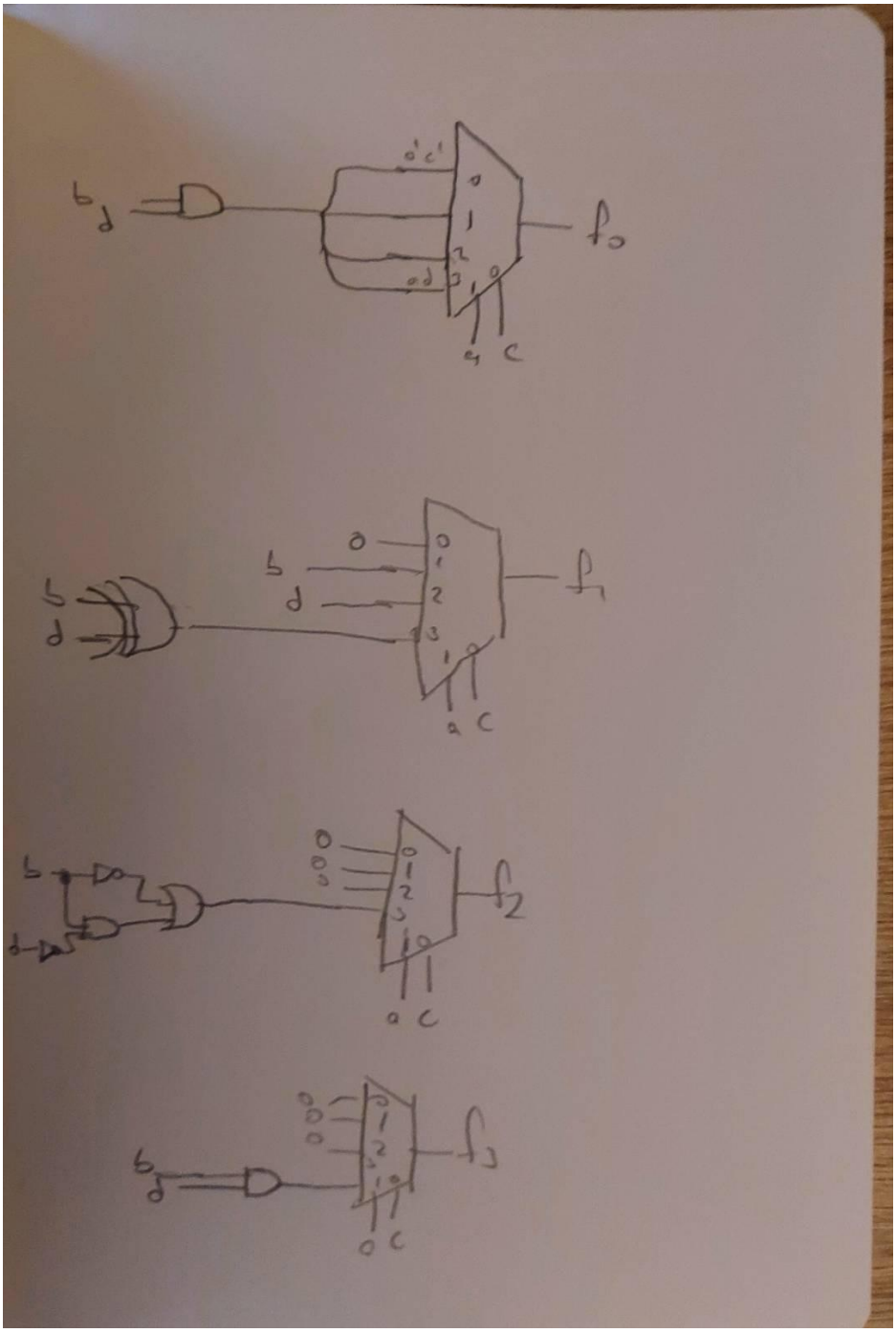
Zoomed Device Layout



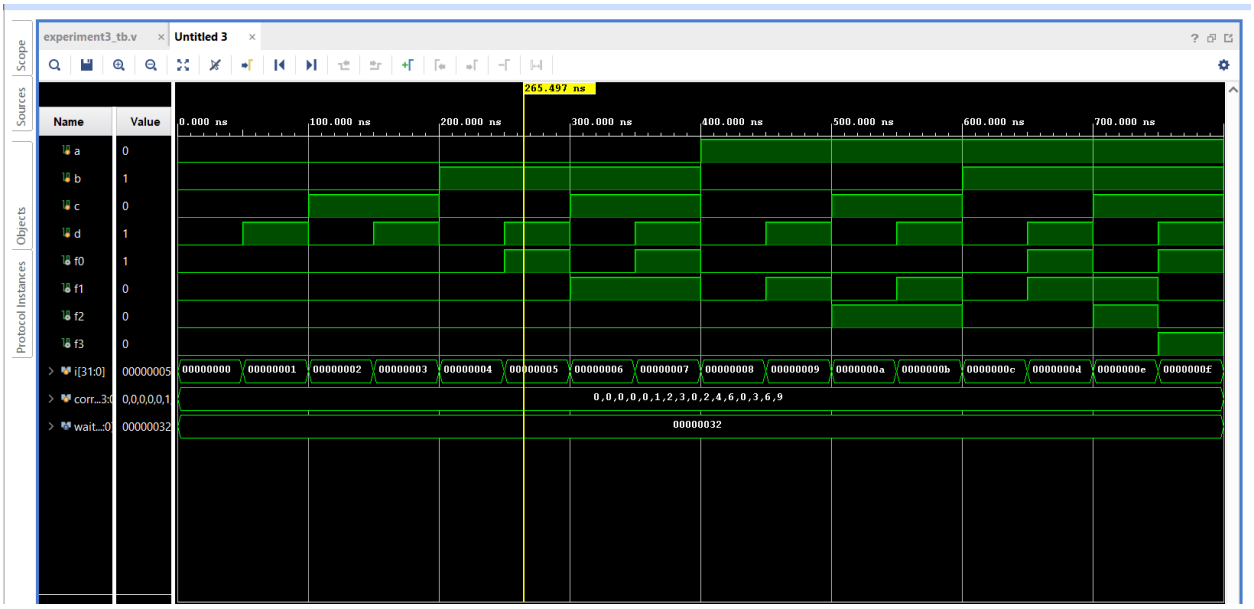
Combinational Delay With Timing Constraint



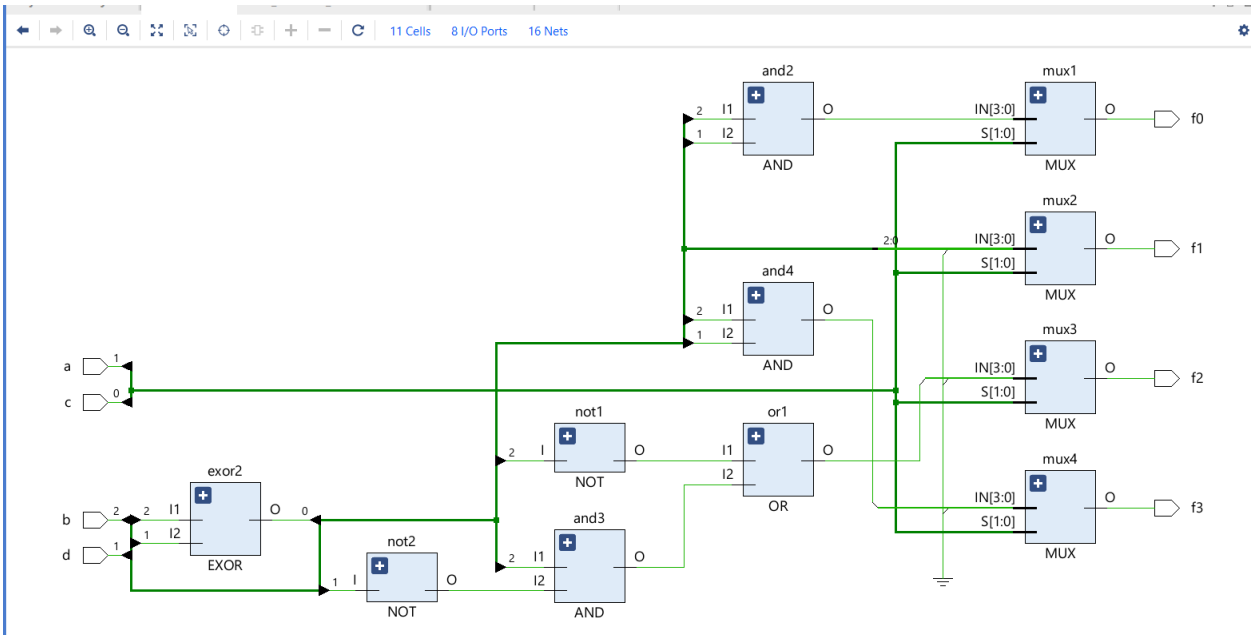
3 Designing With Mux



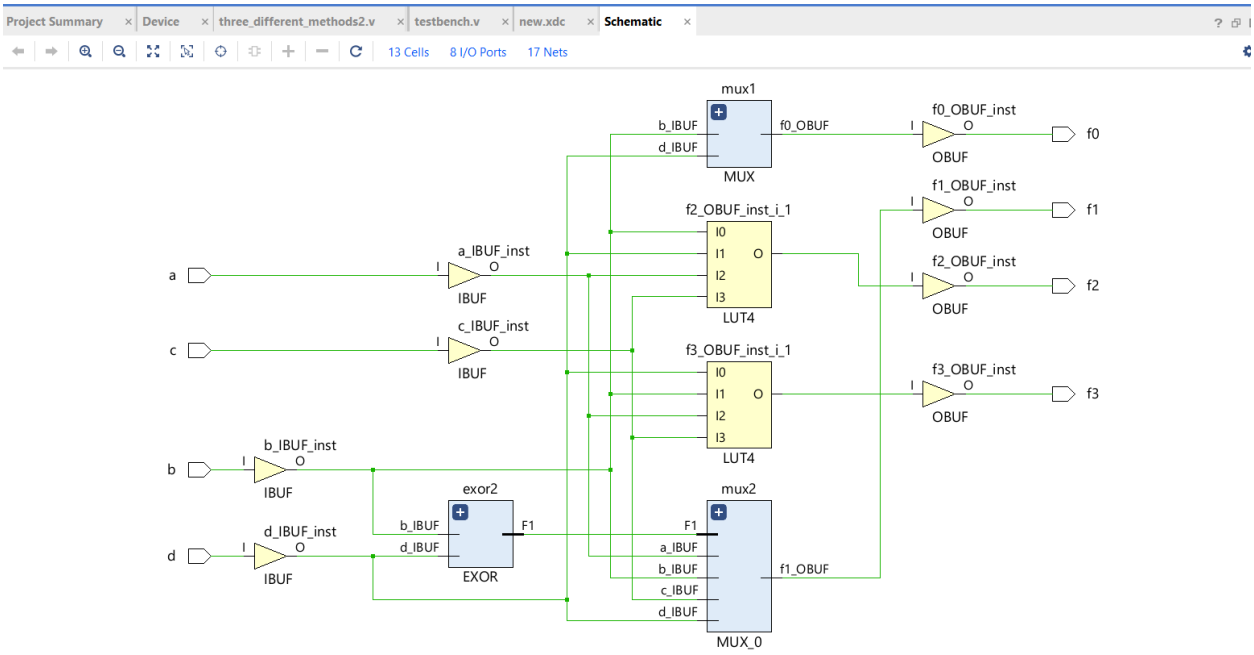
Wave form of Behavioral Simulation



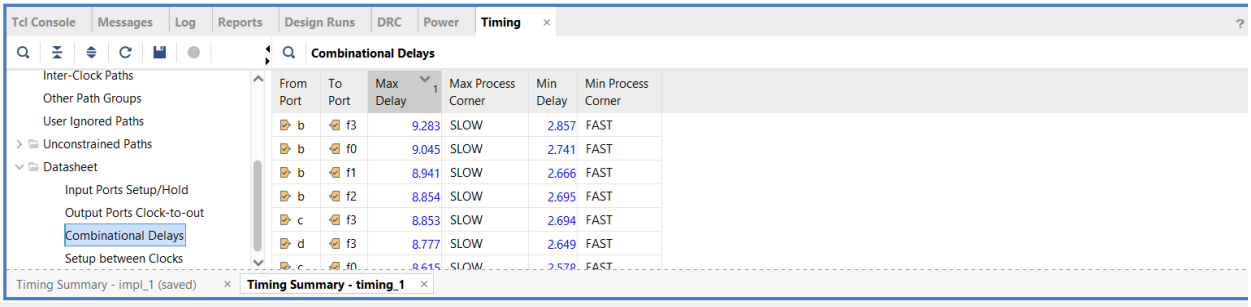
RTL Schematic



Technology Schematic

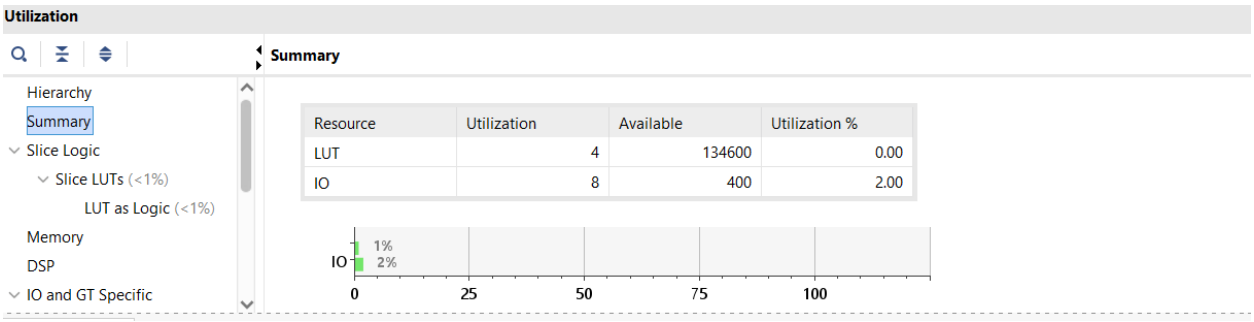


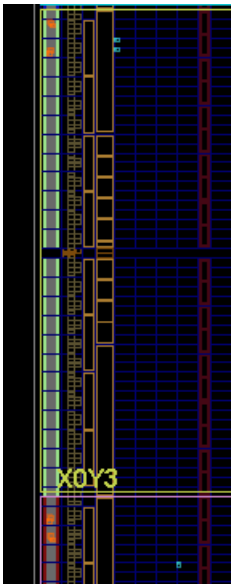
Combinational Delay



There is no difference in used primitive types

Utilization

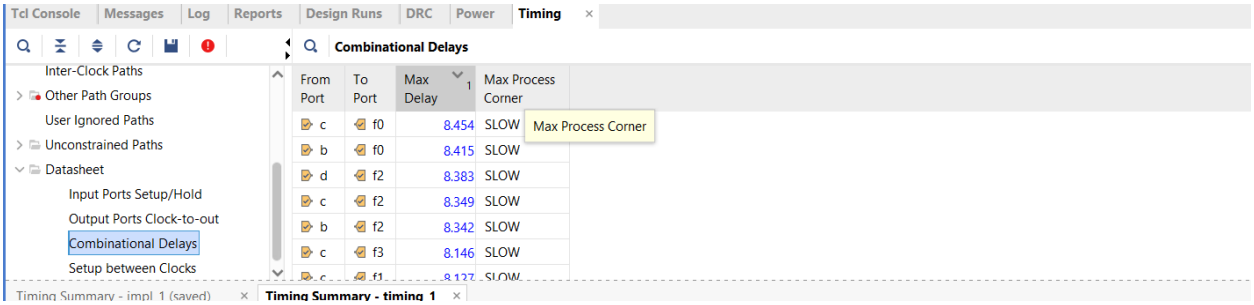




Comparison of three designs

Design with decoder is using least amount of resources because one decoder and 3 or is enough to implement the design, design with mux is in the middle because for every output we have to use one mux and some gates to their inputs, SSI is the worst case because we are using only gates that's why it is using more resources.

Combinational Delay with Time Constraint



4-)

It is 2-bit multiplier

Behavioral simulation is the simulation of our design.

Post Synthesis Functional Simulation is the simulation with synthesized netlists.

Post Implementation Functional Simulation is the simulation with using the elements on the board.

Post Implementation Timing Simulation is showing us that after implementing the design in to board, what happens with delays.

Design difficulty is MUX > Decoder >SSI

Coding difficulty SSI>MUX>Decoder

LUT usage SSI>MUX>Decoder

Path delays Decoder>SSI>MUX