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SSI_library.v

```
`timescale 1ns / 1ps

module AND( output O,
            input I1,I2);

    assign O = I1&I2;
endmodule

module OR (output O,
            input I1,I2);

    assign O = I1|I2;
endmodule

module NOT( output O,
            input I);

    assign O = ~I;
endmodule

module NAND(output reg O,
            input I1,I2);

    always @(I1,I2) begin
        O = ~(I1&I2);
    end
endmodule

module NOR(output reg O,
            input I1,I2);

    always @(I1,I2) begin
        O = ~(I1|I2);
    end
endmodule

module EXOR(output O,
            input I1,I2);
    LUT2 #(
        .INIT ( 4'b0110 )
    ) EXOR
    (
```

```
.I0( I1 ),  
.I1( I2 ),  
.O ( O )  
);  
endmodule  
  
module EXNOR(output O,  
             input I1,I2);  
    LUT2 #(  
        .INIT ( 4'b1001 )  
    ) EXNOR  
    (  
        .I0( I1 ),  
        .I1( I2 ),  
        .O ( O )  
    );  
endmodule  
  
module TRI(input I,E,  
           output O);  
    assign O = (E==1) ? (I) : (1'bz);  
endmodule
```

Top_module.v

```

`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
/
// Company:
// Engineer:
//
// Create Date: 10/13/2022 01:10:23 PM
// Design Name:
// Module Name: Top_module
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
/

module Top_module(O,IN

    );
    output [7:0]O;
    input [15:0]IN;

    AND GATE1(.O(O[0]),.I1(IN[0]),.I2(IN[1]));
    OR GATE2(.O(O[1]),.I1(IN[2]),.I2(IN[3]));

    NAND GATE4(.O(O[2]),.I1(IN[4]),.I2(IN[5]));
    NOR GATE5(.O(O[3]),.I1(IN[6]),.I2(IN[7]));
    EXOR GATE6(.O(O[4]),.I1(IN[8]),.I2(IN[9]));
    EXNOR GATE7(.O(O[5]),.I1(IN[10]),.I2(IN[11]));
    TRI GATE8(.O(O[6]),.I(IN[12]),.E(IN[13]));

    NOT GATE3(.O(O[7]),.I(IN[14]));

endmodule

```

Top_module_tb.v

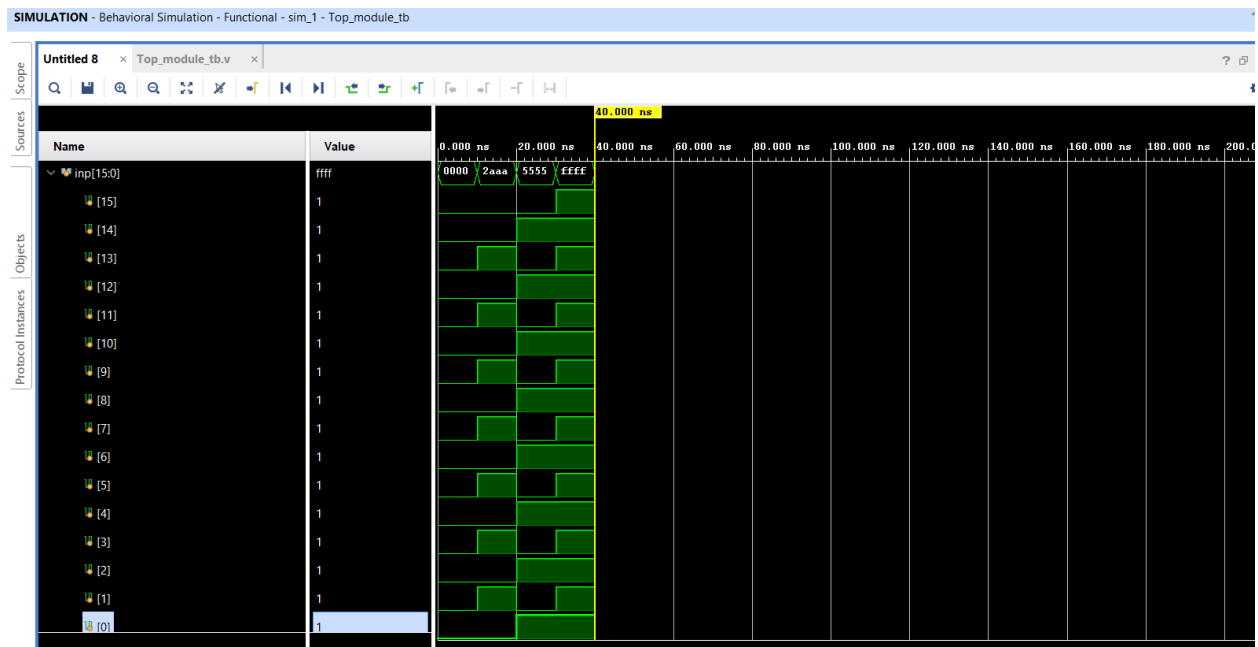
```
`timescale 1ns / 1ps

module Top_module_tb;
    reg [15:0] inp;
    wire [7:0] out;
    integer i;

    Top_module uut(.O(out), .IN(inp));

    initial
    begin
        // inp1 =0 inp2=0
        inp=16'h00;
        #10
        // inp1=0 inp2=1
        for (i=0 ; i<14 ; i=i+2 ) begin
            inp[i]=0;inp[i+1]=1;
        end
        #10
        // inp1=1; inp2=0; also changing not input from 0 to 1
        for (i=0 ; i<14 ; i=i+2 ) begin
            inp[i]=1;inp[i+1]=0;
        end
        inp[14]=1;
        #10
        inp=16'b1111111111111111;
        #10
        $finish;

    end
endmodule
```



Input 0,1 and

Input 2,3 or

Input 4,5 nand

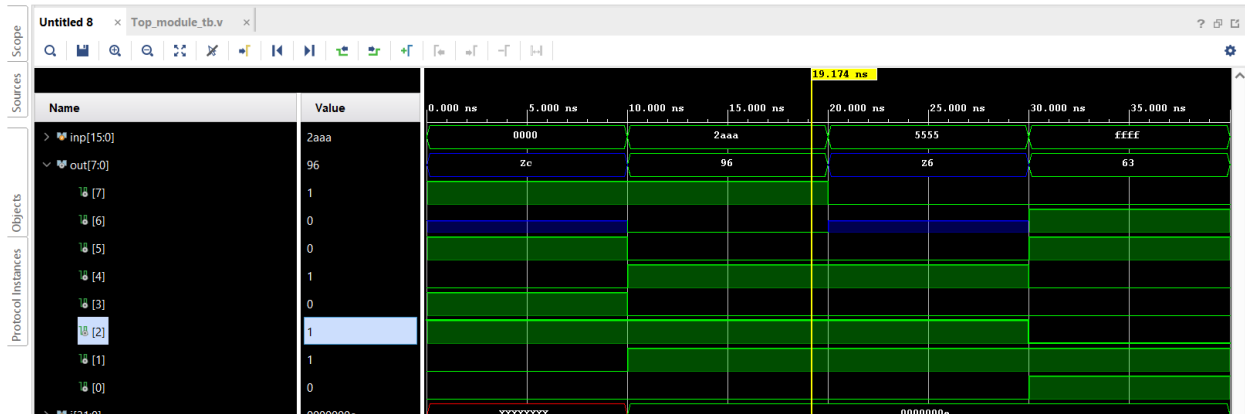
Input 6,7 nor

Input 8,9 exor

Input 10,11 exnor

Input 12,13 tri 13 is E port

Input 14 not



Output 0 and

Output 1 or

Output 2 nand

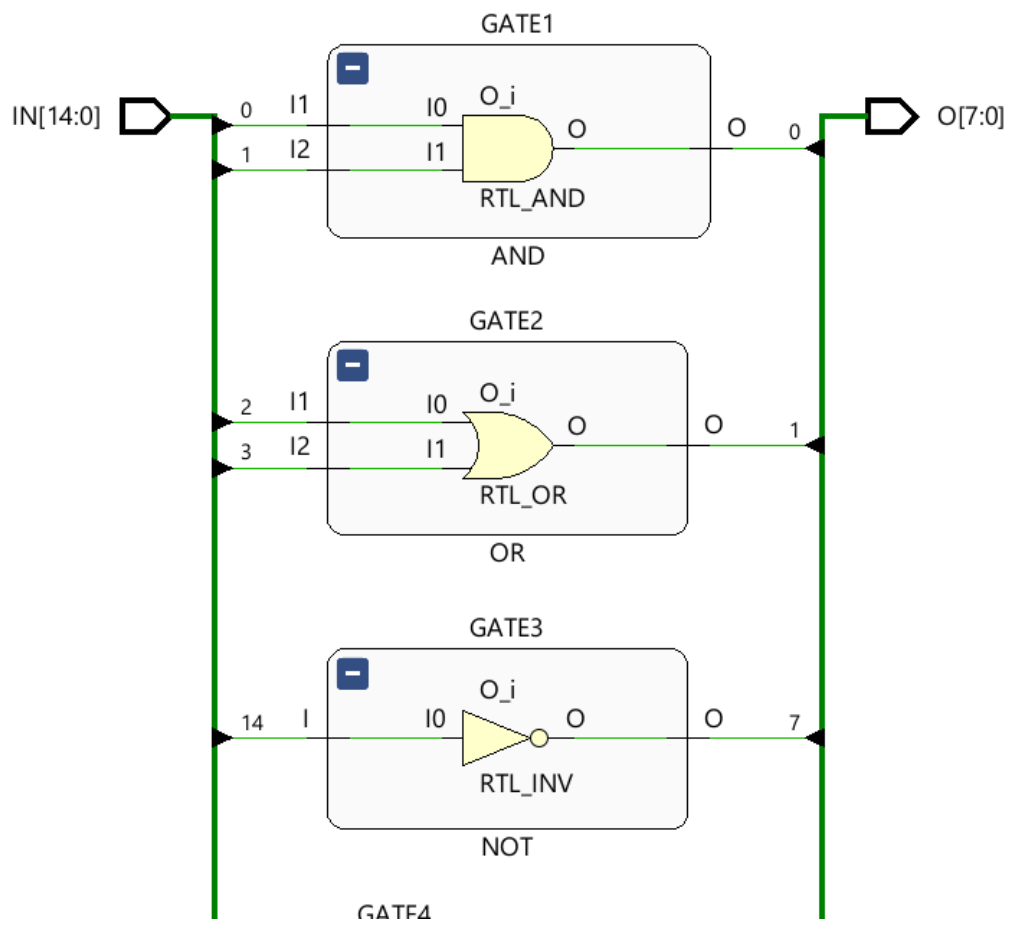
Output 3 nor

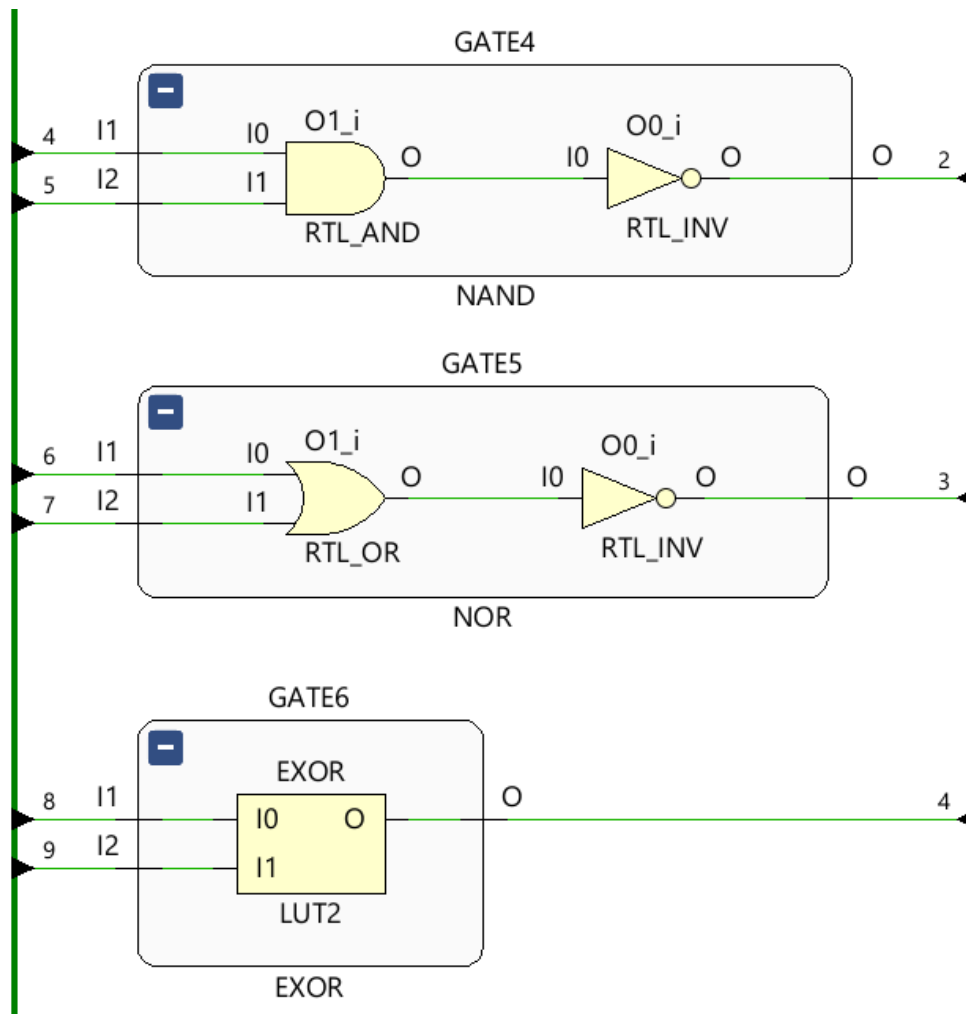
Output 4 exor

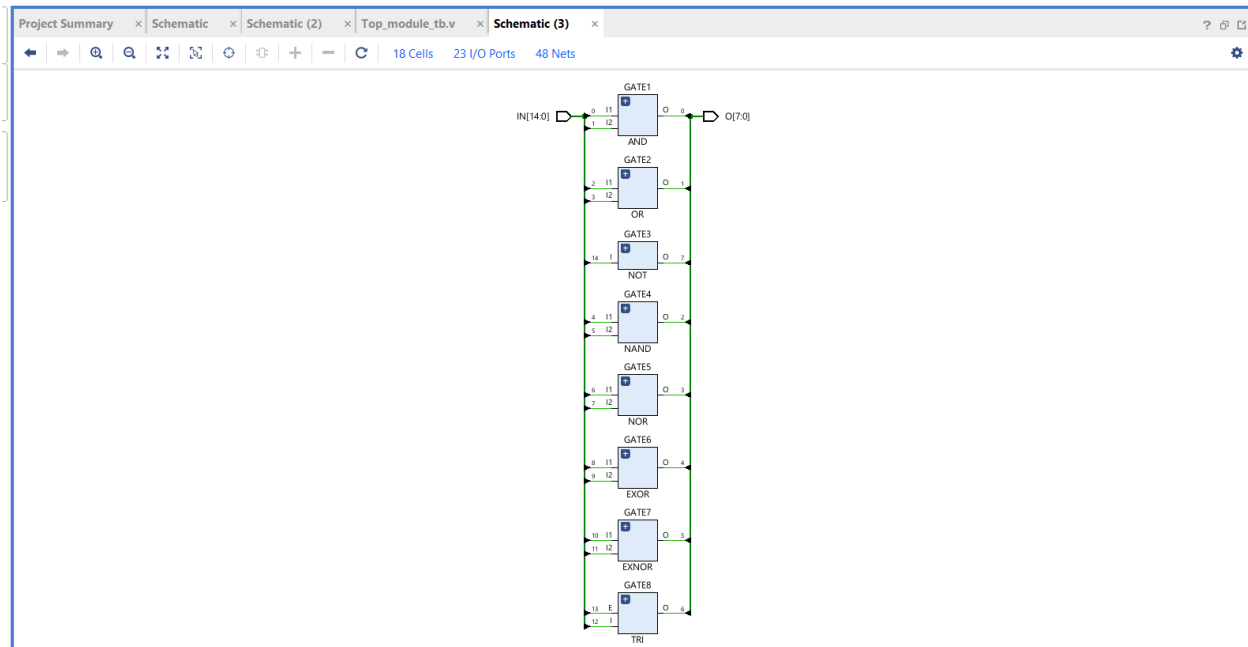
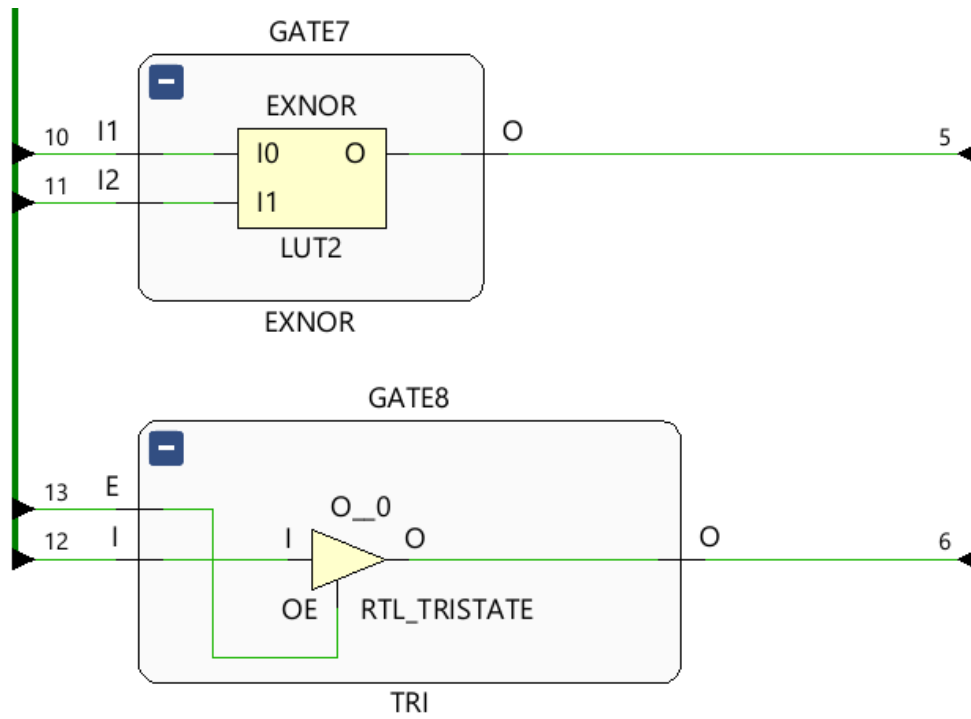
Output 5 exnor

Output 6 tri

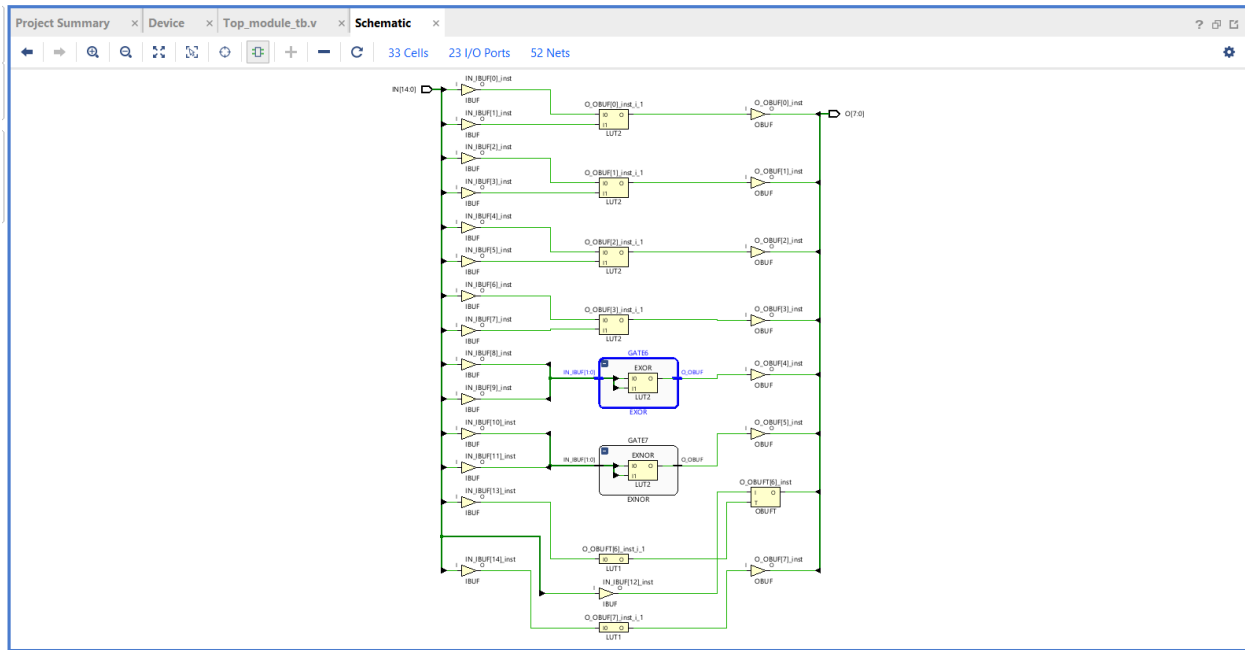
Output 7 not //after 20ns I changed the input of the not gate







TECHNOLOGY SCHEMATIC



AND

Cell Properties			
O_OBUF[0]_inst_i_1			
I1	I0	O=I0 ...	
0	0	0	
0	1	0	
1	0	0	
1	1	1	

OR

Cell Properties			
O_OBUF[1]_inst_i_1			
I1	I0	O=I0 + I1	
0	0	0	
0	1	1	
1	0	1	
1	1	1	

NAND

Cell Properties			
O_OBUF[2]_inst_i_1			
I1	I0	O=!I0 + !I1	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

NOR

Cell Properties			
O_OBUF[3]_inst_i_1			
I1	I0	O=!!I0 & !!I1	
0	0	1	
0	1	0	
1	0	0	
1	1	0	

EXOR

Cell Properties			
EXOR			
I1	I0	O=I0 & !I1 + !I0 & I1	
0	0	0	
0	1	1	
1	0	1	
1	1	0	

EXNOR

Cell Properties			
EXNOR			
I1	I0	O=!I0 & !I1 + I0 & I1	
0	0	1	
0	1	0	
1	0	0	
1	1	1	

NOT

SYNTHESIZED DESIGN - xc/a100tcsg324-1		
Cell Properties		
■ O_OBUF[7]_inst_i_1		
I0	O=!!I0	
0	1	
1	0	

Post-synthesis simulation model

INFO: [VRFC 10-2263] Analyzing Verilog file

"C:/Users/omer/Desktop/Dersler/EHB436E/SSTU-01/deney-01/deney-01.sim/sim_1/synth/timing/xsim/top_module_tb_time_synth.v" into library xil_defaultlib

INFO: [VRFC 10-311] analyzing module Top_module

INFO: [VRFC 10-311] analyzing module glbl

INFO: [VRFC 10-2263] Analyzing Verilog file

"C:/Users/omer/Desktop/Dersler/EHB436E/SSTU-01/deney-01/deney-01.srcs/sim_1/new/top_module_tb.v" into library xil_defaultlib

INFO: [VRFC 10-311] analyzing module top_module_tb

UTILIZATION SUMMARY IMPLEMENTATION

The top screenshot displays the 'Utilization Summary' report in the Vivado IDE. The report is organized into a table with columns for Resource, Utilization, Available, and Utilization %.

Resource	Utilization	Available	Utilization %
LUT	8	63400	0.01
IO	23	210	10.95

Below the table, a bar chart shows the utilization percentage for LUT (0.01%) and IO (10.95%).

The bottom screenshot displays the 'Hierarchy' tab of the Utilization report. It shows a detailed breakdown of resource utilization across the design hierarchy.

Name	Slice LUTs (63400)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)
Top_module	8	8	8	23
GATE6 (EXOR)	1	1	1	0
GATE7 (EXNOR)	1	1	1	0

UTILIZATION SUMMARY SYNTHESIS

The screenshot displays the Xilinx Vivado IDE interface during the synthesis phase. The left sidebar shows the project navigation tree with sections for SYNTHESIS and IMPLEMENTATION. The central area shows the schematic of the design, which includes several input buffers (IBUF), an EXNOR gate (GATE7), and output buffers (OBUF). The bottom panel shows the Utilization report, which is currently selected. This report provides a summary of resource usage, including LUTs, IOs, Memory, and DSPs.

Utilization Summary Table:

Resource	Utilization	Available	Utilization %
LUT	8	63400	0.01
IO	23	210	10.95

The bar chart below the table shows the utilization percentage for each resource type: LUT (0.01%) and IO (10.95%). The x-axis represents the Utilization (%) from 0 to 100.

SYNTHESIS TIMING REPORTS

SYNTHESIZED DESIGN - xc7a100tcs9324-1

Tcl Console | Messages | Log | Reports | Design Runs | **Timing** ×

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
IN[0]	O[0]	6.728	SLOW	2.189	FAST
IN[1]	O[0]	6.730	SLOW	2.191	FAST
IN[2]	O[1]	6.750	SLOW	2.211	FAST
IN[3]	O[1]	6.742	SLOW	2.203	FAST
IN[4]	O[2]	6.775	SLOW	2.235	FAST
IN[5]	O[2]	6.780	SLOW	2.240	FAST
IN[6]	O[3]	6.774	SLOW	2.235	FAST
IN[7]	O[3]	6.788	SLOW	2.249	FAST
IN[8]	O[4]	6.263	SLOW	2.185	FAST
IN[9]	O[4]	6.248	SLOW	2.170	FAST
IN[10]	O[5]	6.764	SLOW	2.224	FAST
IN[11]	O[5]	6.784	SLOW	2.244	FAST
IN[12]	O[6]	9.835	SLOW	3.519	FAST
IN[13]	O[6]	6.823	SLOW	1.837	FAST
IN[14]	O[7]	6.795	SLOW	2.255	FAST

Maximum combinational path delay is 9.835ns

IMPLEMENTATION TIMING REPORT

Flow Navigator

Report DRC
Report Noise
Report Utilization
Report Power
Schematic

IMPLEMENTATION

Run Implementation

Open Implemented Design

Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

IMPLEMENTED DESIGN - xc7a100tcs9324-1

Tcl Console Messages Log Reports Design Runs DRC Power Timing

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
IN[0]	O[0]	8.251	SLOW	2.403	FAST
IN[1]	O[0]	8.370	SLOW	2.454	FAST
IN[2]	O[1]	8.320	SLOW	2.466	FAST
IN[3]	O[1]	8.645	SLOW	2.641	FAST
IN[4]	O[2]	9.377	SLOW	2.889	FAST
IN[5]	O[2]	8.679	SLOW	2.608	FAST
IN[6]	O[3]	8.522	SLOW	2.561	FAST
IN[7]	O[3]	8.261	SLOW	2.429	FAST
IN[8]	O[4]	11.002	SLOW	4.006	FAST
IN[9]	O[4]	11.356	SLOW	4.119	FAST
IN[10]	O[5]	8.102	SLOW	2.376	FAST
IN[11]	O[5]	8.311	SLOW	2.466	FAST
IN[12]	O[6]	10.946	SLOW	3.885	FAST
IN[13]	O[6]	8.245	SLOW	2.262	FAST
IN[14]	O[7]	8.072	SLOW	2.384	FAST

General Information
Timer Settings
Design Timing Summary
Methodology Summary

Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths

Unconstrained Paths

Datasheet

Input Ports Setup/Hold
Output Ports Clock-to-out
Combinational Delays
Setup between Clocks

Maximum combinational path delay is 11.356ns

In synthesis part using ideal components but in implementation part it uses the actual components.

My design does meet the expected results and works properly but maximum combinational path delay is too high.

Fan-in – Fan-out

Fan-in is the maximum input signal that logic cell can be fed and Fan-out is the maximum output signal that logic cell can feed.

LUT

Lookup Table is an array that can store truth tables. Using LUT can be faster compared the computation.

Set-up and Hold-time

Setup-time is the minimum stable input signal time required before the rising edge of the clock for it to be latched

Hold time is the minimum stable input time after clock's active edge.