Implementing Boolean Functions by Using Zipper Logic

ELE504E - Homework 10, Spring 2025

1 Procedure

In this session, you are going to implement a Boolean function using Zipper Logic Gates.

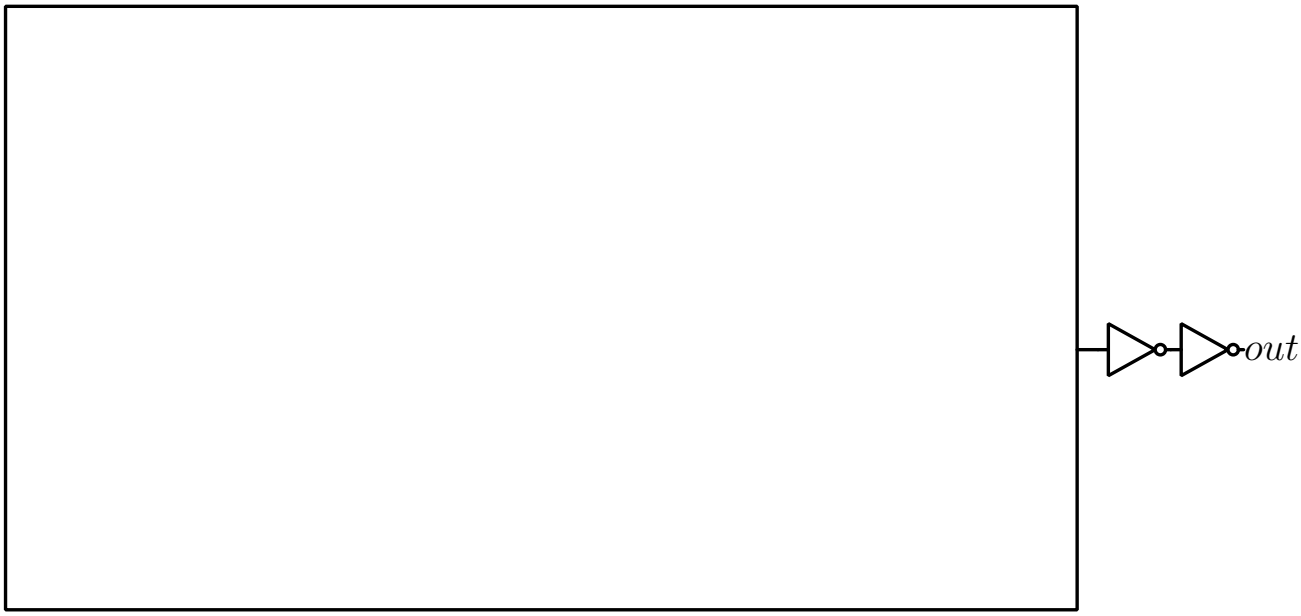
- Fill in the truth table of Boolean Function :.....

A	B	C	D	Y

- Beginning with the Pull-down Network, draw the complete electrical schematic of 3-stage zipper gate whose stages are indicated as:

.....

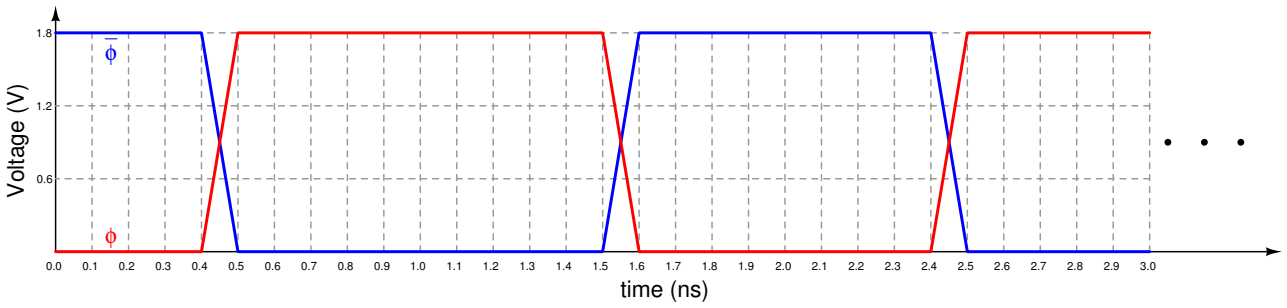
3-stage Zipper Gate



- Write the spice netlist of your circuit above (including the inverters), with minimum-geometry devices (calculate `ad,as,pd,ps` of each device) and carefully indicate all variables at appropriate nodes.
- Define input signals A, B, C and C by using the following lines:

```
va <input_node_a> 0 pulse 0 1.8 16.1n 100p 100p 15.9n 32n
vb <input_node_b> 0 pulse 0 1.8 8.1n 100p 100p 7.9n 16n
vc <input_node_c> 0 pulse 0 1.8 4.1n 100p 100p 3.9n 8n
vd <input_node_d> 0 pulse 0 1.8 2n 100p 100p 2n 4n
```

- Define the clock signals ϕ and $\overline{\phi}$ from the timing diagram given below:



- Perform a transient analysis up to 31.5 ns with 10 ps timestep. Plot ϕ, $\overline{\phi}$, D, C, B, A and *out* with the following command:

```
plot v(<input_node_phi>) v(<input_node_phin>) v(<input_node_d>)+2
v(<input_node_c>)+4 v(<input_node_b>)+6 v(<input_node_a>)+8
v(<output_node_out>)+10
```