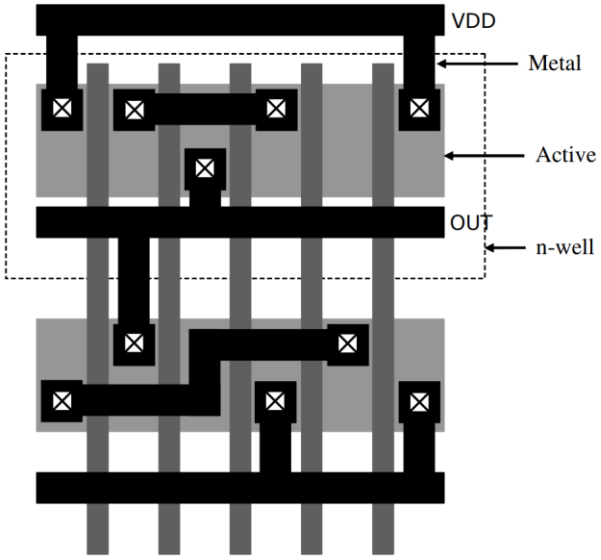
ELE504E MIDTERM EXAM

Name:
Number:

Q1) The Layout of a complex gate is shown. The gate has five inputs (from left to right: X1, X2, X3, X4, X5), an output (OUT) and VDD and GND connections.



a) Draw the electrical schematic of the gate.
b) Find the Boolean expression realized by the gate.
c) Write the netlist of the circuit assuming the gate is to be realized in TSMC 0.18 technology.

Q2) A chain of three inverters fabricated in TSMC 0.18 is to drive a capacitive load of 5pF.

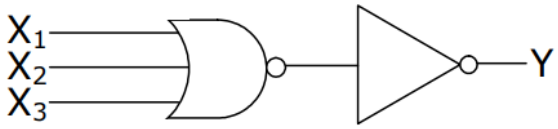
a) Determine all device widths in the chain in such a way that total latency is minimized.

Inverter #	Wn	Wp
1	**0.5u**	
2		
3		

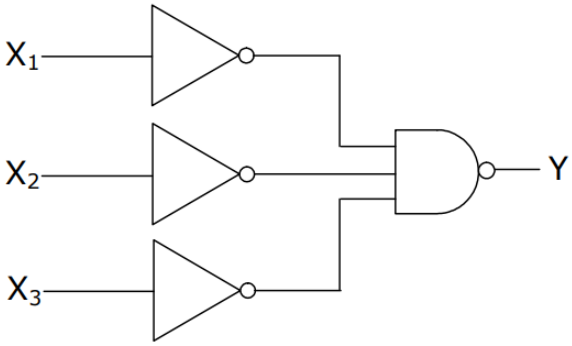
b) Calculate the total chain latency.

c) Verify the results using a SPICE simulation.

Q3) You are supposed to implement the Boolean function Y = X1 + X2 + X3 with CMOS static gates. Since such gates inevitably invert, you have two options:



or



a) Assuming that all devices in all options are built with minimum geometry devices, which option will yield a shorter latency? Explain.

b) Verify the results found in (a) with a SPICE simulation. Write your input netlist and provide your simulation results.