Determining Delay Times and Setup Time of a Typical D-Latch Circuit

ELE504E - Homework 8, Spring 2025

1 Procedure

In this session, we are going to study a "Clocked D-latch circuit." D-Latch is an improved version of SR latch in the sense that the problem in the case S=R=1 is eliminated by simply connecting S and R together with an inverter in between. Therefore, D latch has only one input instead of two R and S inputs. This input is called D or data input. The logic schematic of a NOR-based D latch is given in Figure 1.1.

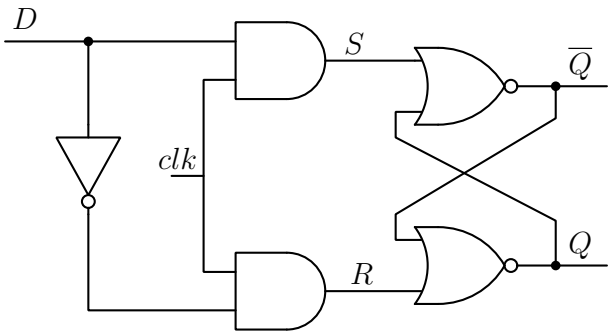

Figure 1.1. A typical D Latch

The clock signal plays an important role in D Latch. This signal is used gate the input D and $\overline{D}$ to the latch. When the *clk* is logic-1, both AND gates act as buffers and thus D and $\overline{D}$ appears at the input of the NOR gates, and D latch is thus placed in set mode ($D = 1$) or reset mode ($D = 0$). When *clk* is logic-0, both S and R are driven low. The D latch goes into a hold state in which it retains the very last value of D prior to the high-to-low transition of the *clk*.

During this session, you will be examining the effect of *clk* on D-latch operation. The electrical schematic of the circuit involved is shown in Figure 1.2. Notice that the output drives capacitive loads C_{L1} and C_{L2} each being 20fF.

Write the SPICE netlist of D-Latch given in Figure 1.2. In your input file, use minimum geometry dimensions for NMOS and PMOS. You also have to include following lines for defining clock and data signals:

```
vclk clk 0 pulse 1.8 0 10n 10p
vd d 0 pulse 0 1.8 1n 10p 10p 2n 4.2n
```

Perform a transient analysis up to 20 ns with 5 ps timesteps. Plot the nodes "clk","d","q" by following command:

```
plot v(clk) v(d)+2 v(q)+4
```

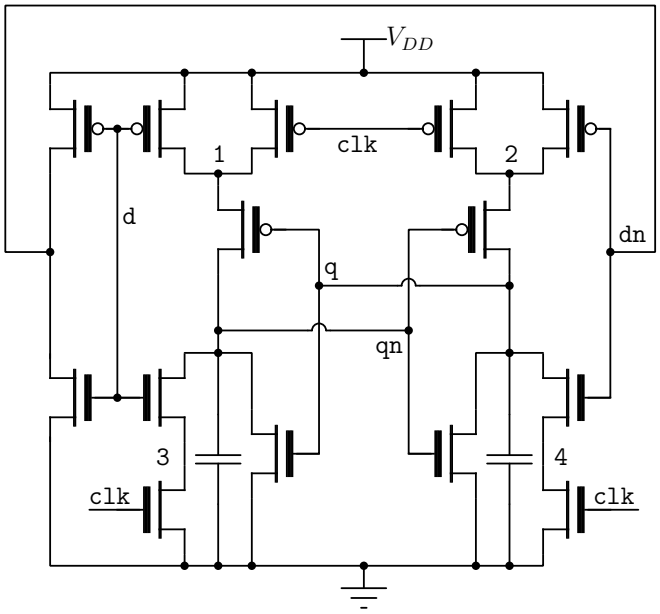

Figure 1.2. Electrical Schematic of D-Latch

Modify the clock signal as:

```
vclk clk 0 pulse 1.8 0 12n 10p
```

Repeat the simulation. Take a screenshot of two graphs in a single file.

Using the simulation results, you are going to calculate the propagation delays of the output Q in response to the applied data input D. The delays are calculated for the transition of Q from high-to-low and low-to-high levels. These delays are the summation of delay contributions (T_{PHL} or T_{PLH}) of devices that are playing part in the transition of output Q from one level to the other. First, you have to theoretically determine the high-to-low and low-to-high transition delays of Q and compare if they are equal to each other or not. If not, you have to answer why. Afterwards, you must experimentally evaluate the transition delays and check whether they are approximately matching with your theoretical values.

Theoretical High-to-Low Delay:

Theoretical Low-to-High Delay:

Are theoretical high-to-low and low-to-high delays same? Why?

Experimental High-to-Low Delay:

Experimental Low-to-High Delay:

Are experimental values and theoretical values matching? Why?

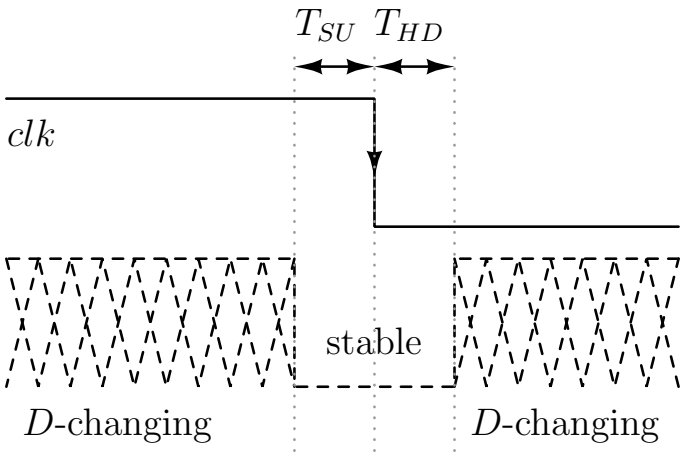

Figure 1.3. Setup Time Illustration

At the last step of our session you will learn about the set-up time "T_{SU}". It is the minimum time period for which the data should have been stable before the clock makes a valid transition. Therefore, you are supposed to determine the setup time of the latch via manipulating the delay time of the clock. You have to reduce the delay time of the clock to the minimum time as possible for the output to be still interpreted correctly.

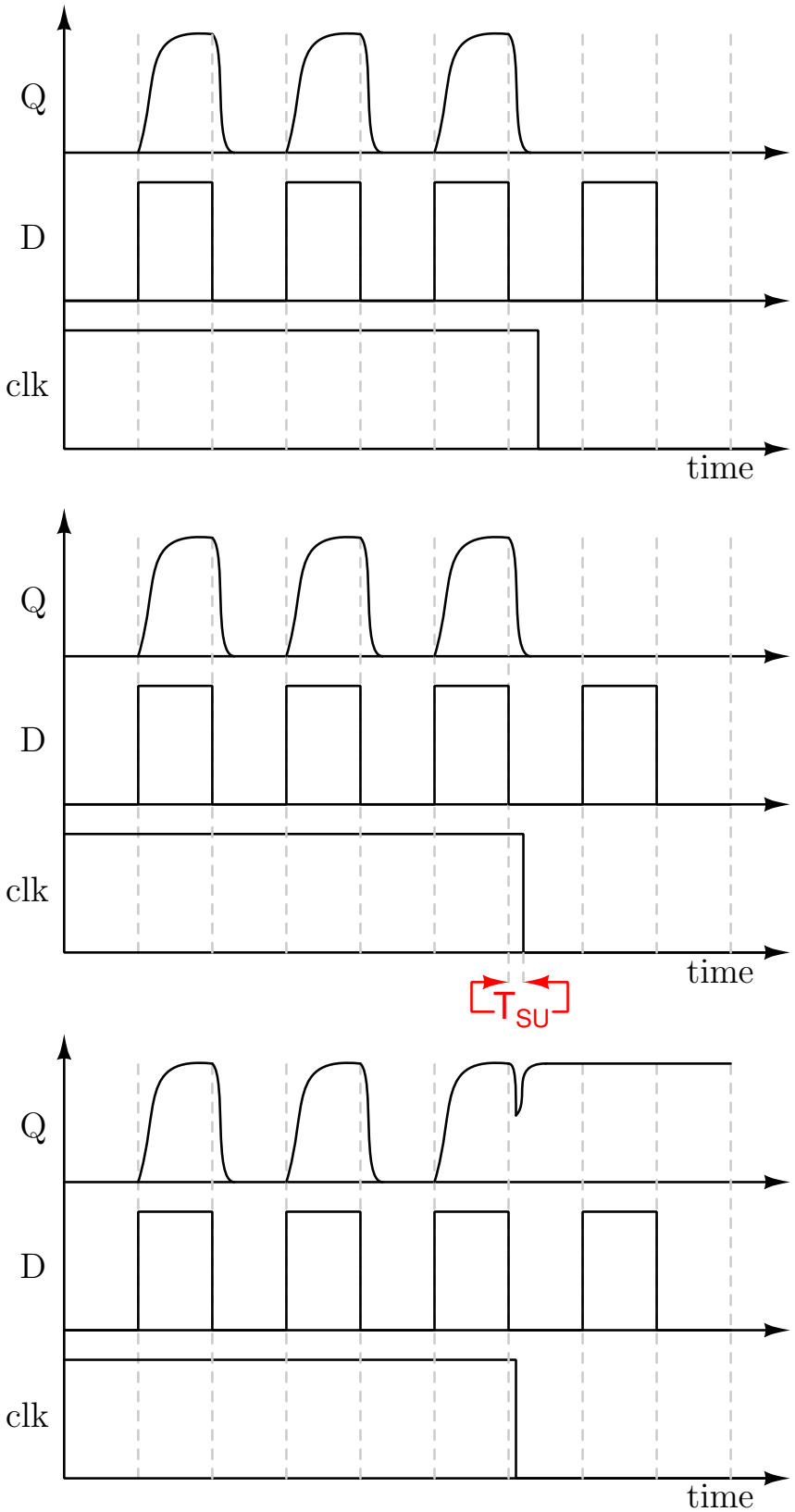

Figure 1.4. Setup Time Example