

Homework 7

Realizing a Given Boolean Function and Constructing the Optimum Layout

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May 19, 2025

1 Schematic

Figure 1 shows schematic of the circuit and nodes are marked to use them to generate Euler's Path

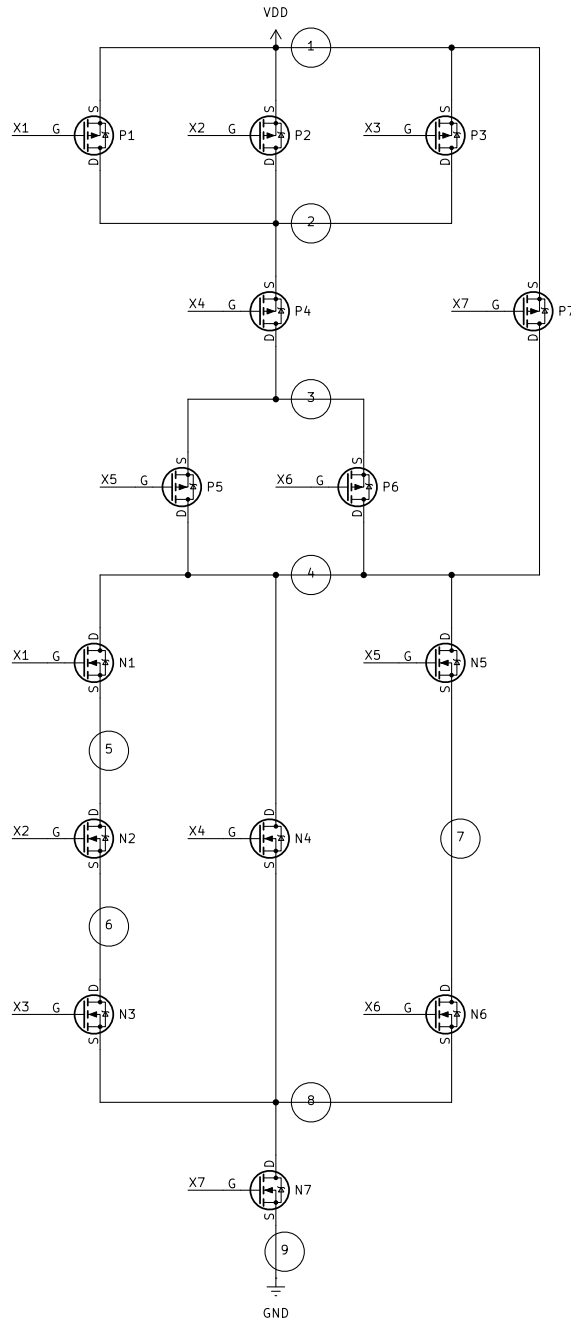


Figure 1: Circuit schematic with marked nodes.

2 Euler's Path

Figure 2 shows PMOS part of the network and Figure 3 shows NMOS part of the network. In both graphs, (*start*) shows start node, and (*stop*) shows stop node. And arrows shows to path for following. When we follow paths, it gives X5-X6-X4-X1-X2-X3-X7. This is our common Euler Path.

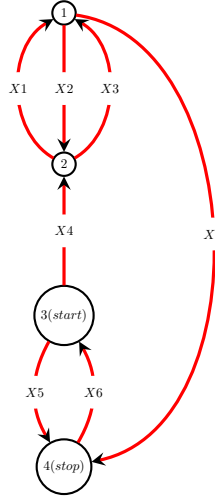


Figure 2: pMOS Network Graph

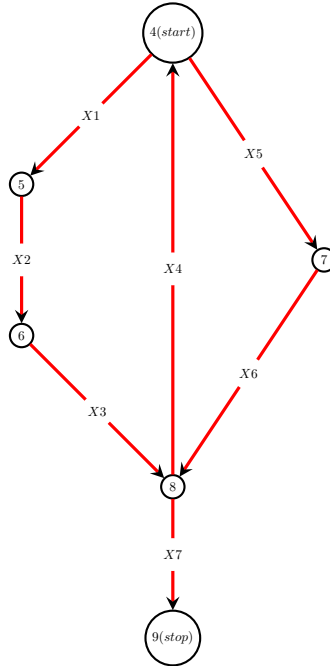


Figure 3: nMOS Network Graph

3 Stick Diagram

When I use Euler's Path in stick diagram, I get Figure 4 as stick diagram.

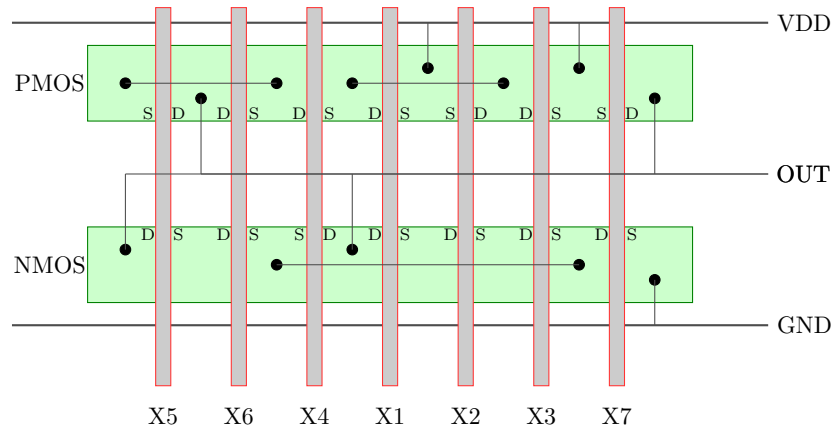


Figure 4: Stick diagram according to Euler's Path.

4 Electric Drawing

Figure 5 shows drawing of the circuit by using Electric, *.jelib* file is also attached to this homework.

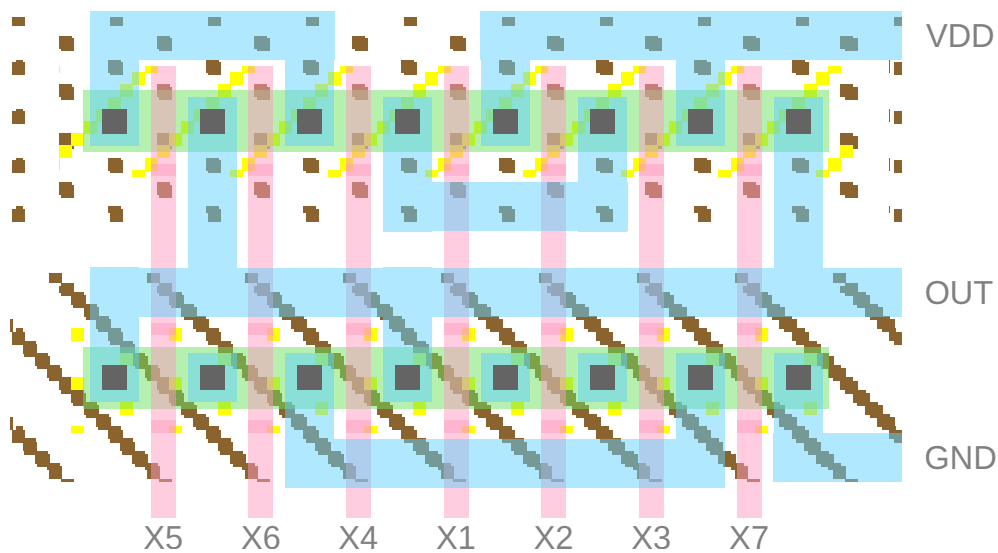


Figure 5: Drawing output from Electric