Implementing Full-Adder Circuits with Pass Logic Gates

ELE504E - Homework 7, Spring 2025

1 Introduction

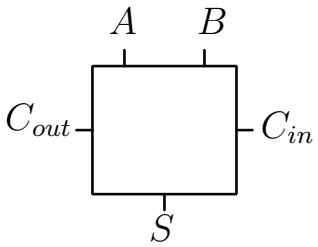

Figure 1.1. 1-bit Full Adder.

The truth table of a 1-bit Full-Adder is shown in Table 1.1.

Table 1.1. Full-Adder Truth Table

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Using the table given above, the Boolean Function of S and C_{out} is derived as follows:

$$S = \overline{A} \cdot \overline{B} \cdot C_{in} + \overline{A} \cdot B \cdot \overline{C_{in}} + A \cdot B \cdot C_{in} + A \cdot \overline{B} \cdot \overline{C_{in}} \quad (1)$$

$$C_{out} = \overline{A} \cdot B \cdot C_{in} + A \cdot B \cdot C_{in} + A \cdot B \cdot \overline{C_{in}} + A \cdot \overline{B} \cdot C_{in} \quad (2)$$

2 Procedure

- Select C_{in} as the control variable closest to the output and A as the control variable closest to the input.
- Apply Shannon decomposition in (1) and (2) to modify S and C_{out}.

S=

C_{out}=

- Realize the switch tree of 1-bit Full-Adder with CMOS transmission gates and mark any redundant transistor.

- Write a spice netlist of your circuit with minimum geometry devices. (Calculate `ad,as,pd,ps` of each device)
  - Define 3 voltage sources for supplying logic signals to the inputs A, B and C_{in} by writing the following lines:
    ```
    va A 0 pulse 0 1.8 8n 50p 50p 8n 16n
    vb B 0 pulse 0 1.8 4.05n 50p 50p 4n 8.0n
    vcin Cin 0 pulse 0 1.8 2n 50p 50p 2n 4n
    ```
  - Perform a transient analysis with 1 ps timestep up to 16 ns. Plot the outputs with the following command:
    ```
    plot v(Cin) v(B)+2 v(A)+4 v(S)+6 v(Cout)+8
    ```