Effects of Device Parameters on Performance Metrics of a CMOS Inverter

ELE504E - Homework 4b, Spring 2025

1 Introduction

In this session, you will examine the concept of propagation delay which is a dynamic property of the inverter. You will calculate "high-to-low propagation delay" T_{PHL} and "low-to-high propagation delay" T_{PLH} for various different values of device parameters.

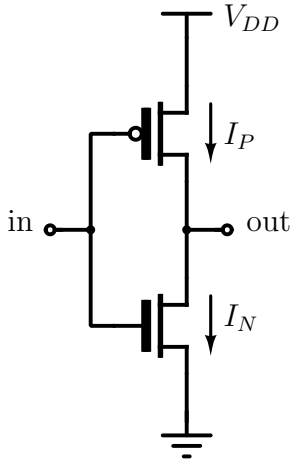

Figure 1.1. Electrical Schematic of CMOS Inverter.

2 Propagation Delay

As you know from past lectures, "propagation delay" T_P is a key property to be minimized to enhance system dynamic performance. In this part of our session, you will study, experimentally, to find out how T_P is related to the technological variables and design parameters in a CMOS inverter. In order to do so, you will use an ideal pulse as an input to your inverter. Due to the finite MOSFET current available for discharging or charging the capacitive loading of the output of the inverter a delay will be observed. This delay is quantified with high-to-low propagation delay T_{PHL} for output falling transition, and with low-to-high propagation delay T_{PLH} for output rising transition.

These are defined as the time difference between the two waveforms at the voltage level $(V_H+V_L)/2$, which is $V_{DD}/2$for the CMOS family of logic gates including the inverter. However, note that when we talk about the "propagation delay" of a logic gate, we usually mean the average of T_{PLH} and T_{PHL} that is:

$$T_P = \frac{T_{PLH} + T_{PHL}}{2} \tag{1}$$

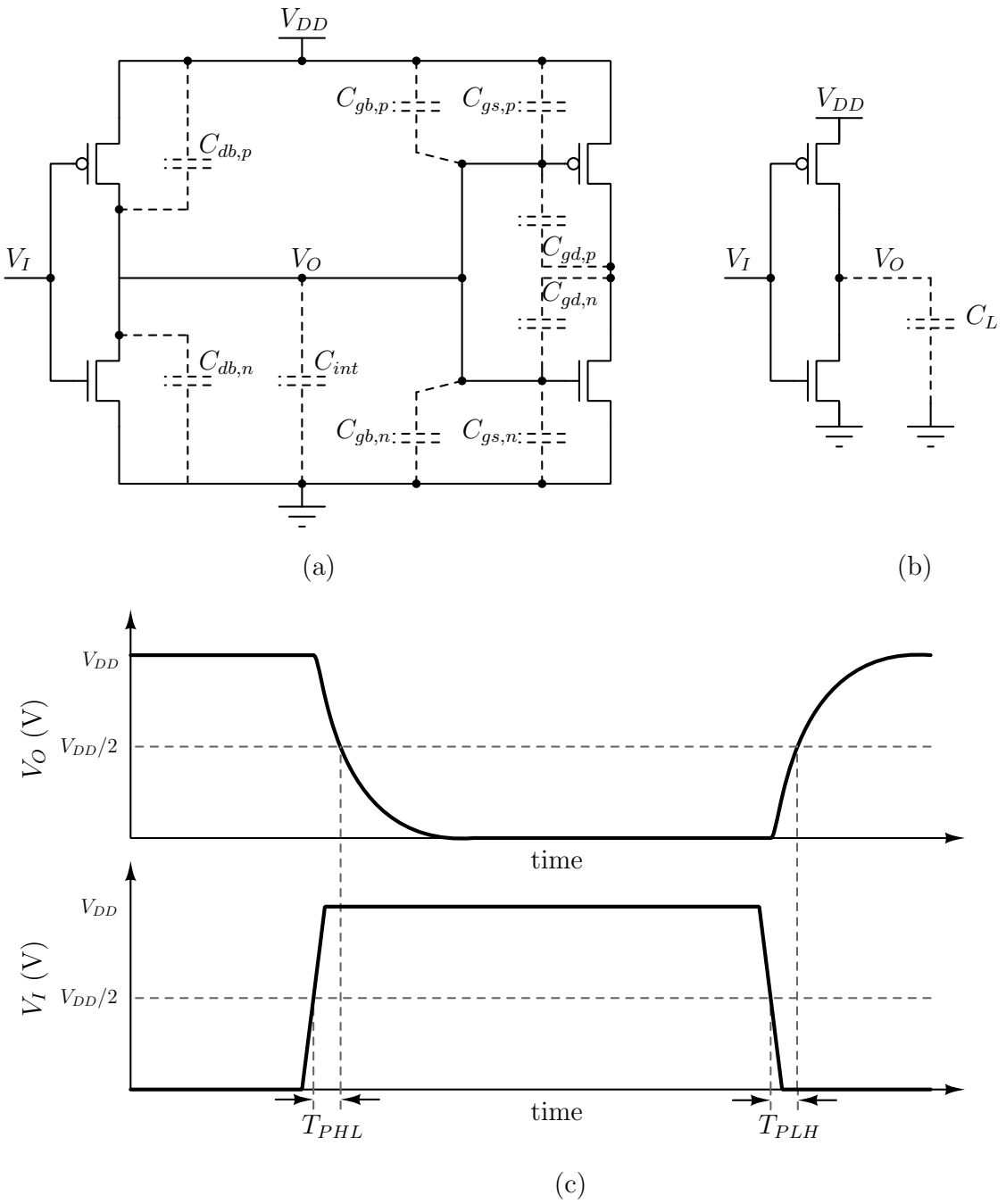

Figure 2.1. (a) Load capacitance components (b) Simplified model of load capacitance c) Output Response to an abrubtly changing input.

As mentioned before, the main parameter affecting these delays is the capacitive loading of the output of the inverter. The most influential components of this capacitance are given in the following formula but, again, be keep in mind that Ngspice does not take the interconnection capacitances into account.

$$C_L = C_{out} + C_{int} + \sum C_{in} \tag{2}$$

You will be asked to simulate our simple inverter with respect to different loading capacitances and also investigate the affects of change of other device parameters in order to reduce this delay. You may need the following expressions to see what parameters are affecting the propagation delay of a CMOS inverter.

$$T_{PHL} = \frac{C_L \cdot A_N \cdot T_{ox} \cdot L_N \cdot V_{DD}}{\mu_n \cdot \epsilon_{OX} \cdot W_N \cdot (V_{DD} - V_{TN})^2} \tag{3}$$

$$T_{PLH} = \frac{C_L \cdot A_P \cdot T_{ox} \cdot L_P \cdot V_{DD}}{\mu_p \cdot \epsilon_{OX} \cdot W_P \cdot (-V_{DD} - V_{TP})^2} \tag{4}$$

3 Procedure

- Write the netlist of the circuit given in Figure 3.1 to obtain the transient response of a CMOS inverter.
- Set device size dimensions W_P, L_P, W_N, L_N and load capacitance C_L as given in Table 3.1 (2^{nd} column). Calculate `ad, as, pd, ps` of each device.

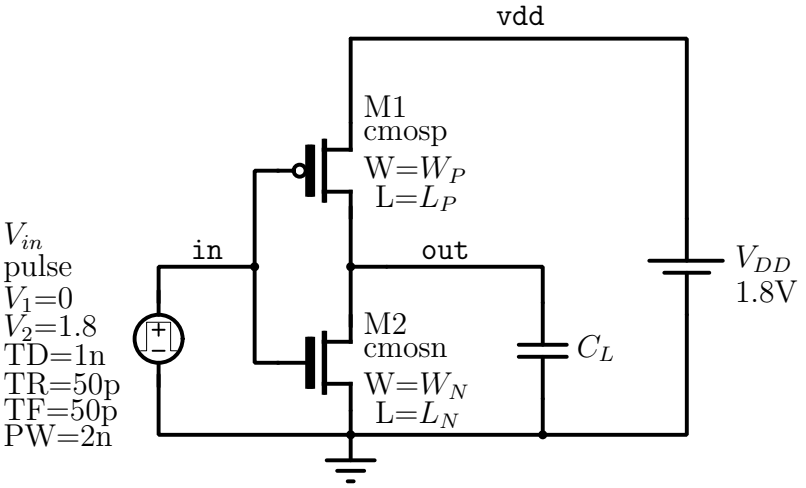

Figure 3.1. Electrical schematic for obtaining transient response of a CMOS inverter.

- Perform a transient analysis with 0.1 picosecond time steps up to 7 nanoseconds .
- Measure T_{PHL} and T_{PLH} to fill the Table 3.1.
- Repeat the previous steps for the rest of the columns and fill in Table 3.1.
- Explain the difference in your measurements due to different capacitances and device dimensions. Finally, make a conclusion.

Conclusion:

Table 3.1. Inverter Comparison Table

C_L	100fF	100fF	10fF	10fF	1fF	1fF
$L_P = L_N$	0.2μm	0.2μm	0.2μm	0.2μm	0.2μm	0.2μm
W_P	0.3μm	0.9μm	0.3μm	0.9μm	0.3μm	0.9μm
W_N	0.3μm	0.3μm	0.3μm	0.3μm	0.3μm	0.3μm
T_{PHL}						
T_{PLH}						