HW1: Layout of a 5-Stage Ring Oscillator

ELE504E, Spring 2025

1 Introduction

Ring Oscillators find widespread use in PLLs to provide a clock signal for digital and RF circuits. It is built with odd number of inverters whose outputs oscillate between supply voltage levels. An example electrical schematic of a ring oscillator built with 5 inverters is shown in Figure 1.1.

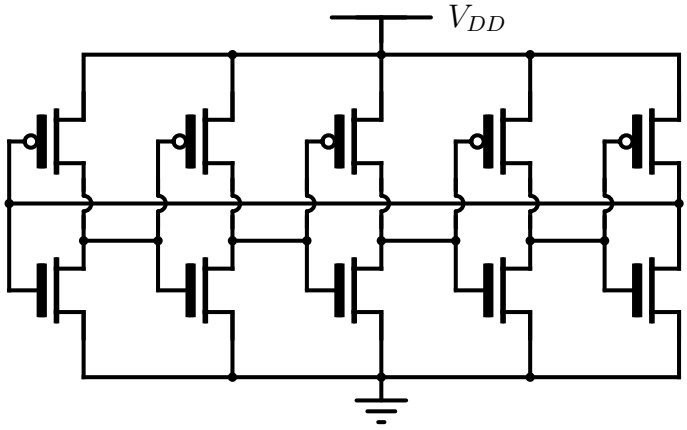

Figure 1.1. Electrical Schematic of a 5-Stage Ring Oscillator.

2 Procedure

Draw the layout of the Ring Oscillator whose schematic is given in Figure 1.1. In your layout, obey the following rules:

- Select 5λ for channel width, 2λ for channel length of each device.
- Only Metal-1 and Poly are allowed for routing.
- Make sure that all PMOS devices share a common bulk. (Same is also valid for NMOS devices.)
- Add proper bulk contacts and label as appropriate power level.
- Layout must be DRC-clean in a minimum area.

You can see the example layout in Figure 2.1.

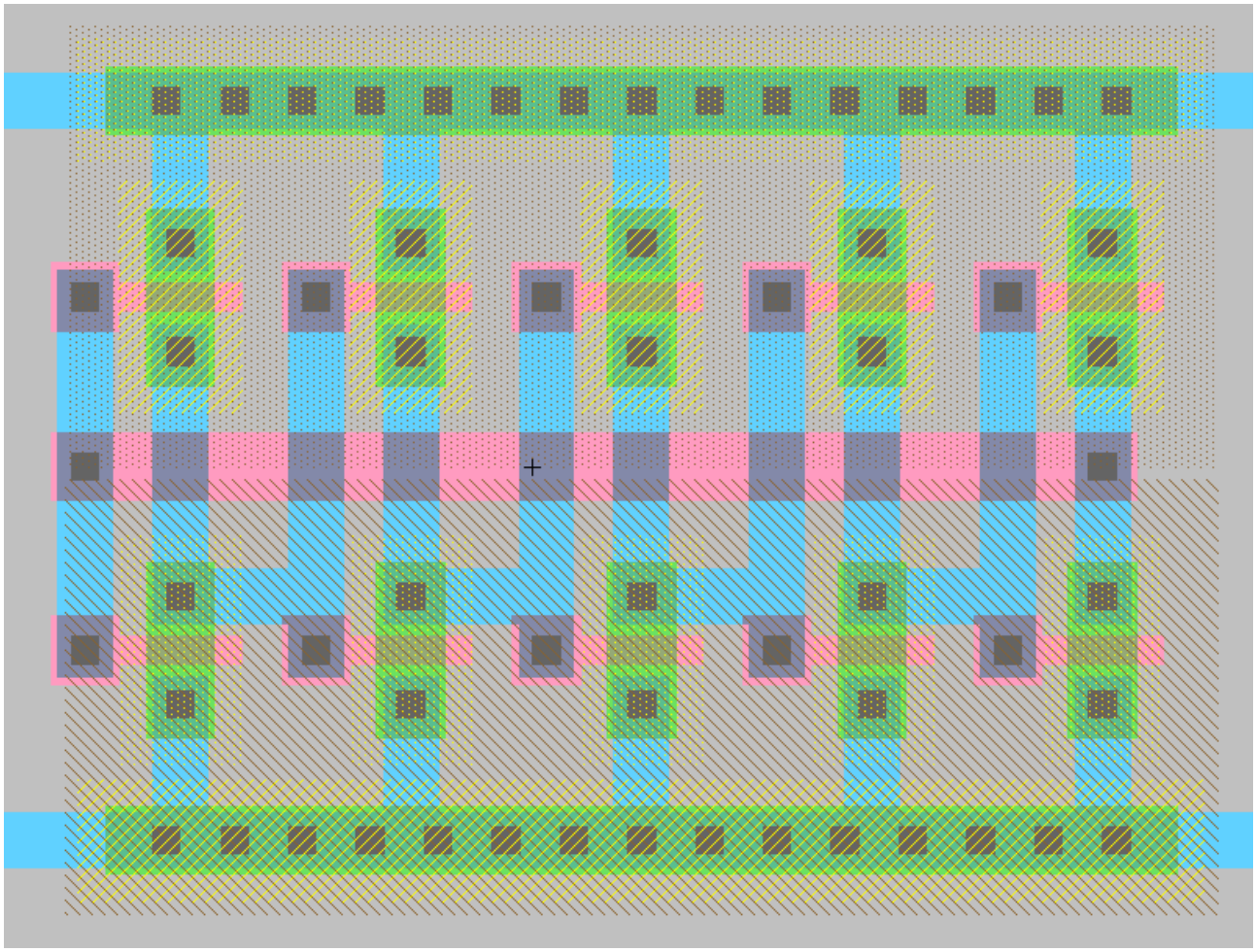

Figure 2.1. Example Layout of a 5-Stage Ring Oscillator.