Design of a Staged (Tapered) Buffered Circuit

ELE504E - Homework 5, Spring 2025

1 Introduction

In this homework, you are supposed to design a typical staged (tapered) buffer circuit which is the most useful application of the optimization procedure in order to minimize the latency of a chain of inverters. A staged buffer is used for coupling the last inverter of a core digital processor to a large capacitive load. Had there been no buffer stage between the last inverter and the capacitive load, a long delay would be observed since the device widths in the core are small. Therefore, in order to avoid this, you must place a properly designed chain of inverters between the two by optimizing the number of inverters in the chain, as well. How you will perform such a design is explained in section 2 via including a reference figure (Figure 2.1) illustrating the regarding inverter chain.

2 Designing the Tapered Buffered Circuit

As mentioned above, the number of inverters n has to be optimized in the circuit. Designating the last inverter of the core block as the first inverter of the staged buffer, the design starts with $W_{N(1)}$ and C_L as two known parameters. In this session, these parameter values are given as:

$W_{N(1)} = 0.2\mu$m and $C_L = 10$ pF.

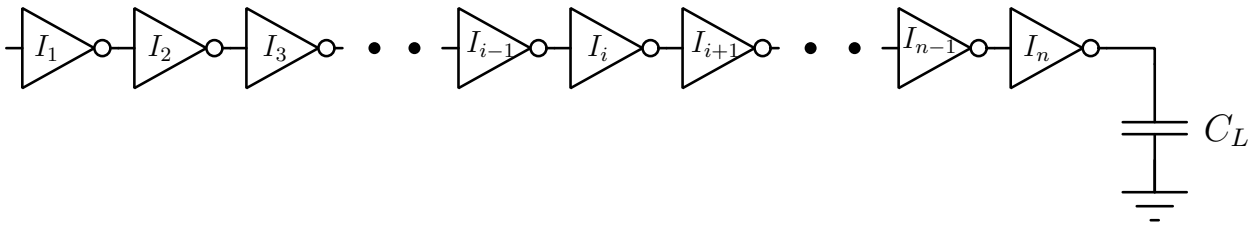

Figure 2.1. Chain of n inverters.

The first step is to determine the optimum value of n via using the following expression:

$$n = \ln\left[\frac{C_L}{\left(1+\sqrt{\frac{J_{N(max)}}{J_{P(max)}}}\right)\cdot(L_{min}\cdot C_{OX}+2\cdot \texttt{CGSO})\cdot W_{N(1)}}\right] \tag{1}$$

where $J_{N(max)}$ and $J_{P(max)}$ are saturation drive current density per unit device width for NMOS and PMOS devices, respectively. They are fixed by technological parameters and supply voltage. The values of $J_{N(max)}$ and $J_{P(max)}$ for our technology are 508A/m and 224A/m, respectively. The equation for n yields a real number, however, you must select the closest even or odd integer for.

Since we designated the last inverter of the core block as the first inverter of the staged buffer, n must be odd in order for the added inverters of the buffer not to invert the signal

generated by the core. Afterwards, you need to calculate tapering factor m via using the following expression:

$$m = \left[\frac{C_L}{\left(1 + \sqrt{\frac{J_{N(max)}}{J_{P(max)}}}\right) \cdot (L_{min} \cdot C_{OX} + 2 \cdot \texttt{CGSO}) \cdot W_{N(1)}} \right]^{\frac{1}{n}} \tag{2}$$

Also you can calculate the minimized latency from the equation given as:

$$\mathcal{L} = \frac{1}{4} \cdot \left(\frac{1}{\sqrt{J_{N(max)}}} + \frac{1}{\sqrt{J_{P(max)}}} \right)^2 \cdot (L_{min} \cdot C_{OX} + 2 \cdot \texttt{CGSO} \ ) \cdot V_{DD} \cdot m \cdot n \tag{3}$$

Once you have calculated n , m and $\mathcal{L}$, fill in Table 5.1.

Then proceed with the sizing of NMOS and PMOS devices using the equation (4) & (5) and fill in Table 5.2.

$$m = \frac{W_{N(i)}}{W_{N(i-1)}} = \frac{W_{N(i+1)}}{W_{N(i)}}, i = 2, ..., n-1 \tag{4}$$

$$\frac{W_{P(i)}}{W_{N(i)}} = \sqrt{\frac{J_{N(max)}}{J_{P(max)}}} \tag{5}$$

In order to understand the importance of using a staged buffer circuit, it will be useful to calculate the delay time in the case that no stage buffer is placed between the last inverter of the core block and the capacitive load. In the next step of our session, you will be dealing with determining the delay time of such a case.

3 Determining the Latency Without Using Staged Buffered Circuit

First step is to calculate high-to-low,T_{PHL}, and low-to-high, T_{PLH} propagation delays of the first inverter of the chain using the following expressions for delay times.

$$T_{PHL} = \frac{C_L}{W_{N(1)}} \cdot \frac{V_{DD}}{2 \cdot J_{N(max)}} \tag{6}$$

$$T_{PLH} = \frac{C_L}{W_{P(1)}} \cdot \frac{V_{DD}}{2 \cdot J_{P(max)}} \tag{7}$$

Then you will calculate the latency of the inverter by simply taking the average of these two delays as follows.

$$\mathcal{L} = \frac{T_{PHL} + T_{PLH}}{2} \tag{8}$$

Once you have calculated T_{PHL} , T_{PLH} and $\mathcal{L}_{inv}$, fill in Table 5.3.

So far, manual calculations of latencies for either cases are completed. In the final step of the session, you are supposed to perform a SPICE simulation to support your calculations in a more accurate way.

4 Procedure

- Calculate n , m and $\mathcal{L}$, using (1), (2), (3) and record the values in Table 5.1.
- Calculate channel width W of each device in the staged buffer using (4) and (5). Record the values in Table 5.2
- Calculate theoretical latency of a single inverter using (6), (7) and (8). Fill in the results into Table 5.3.
- Write the netlist of the circuit given in Figure 4.1 to inspect the transient response of the staged buffer circuit designed in the previous step.
- Note that the whole circuit is not given because the number of inverters depend on parameter n which is to be calculated in the beginning of the experiment.
- Set each device size $W_{N(1)}$, $W_{P(1)}$, ... ,$W_{N(n)}$, $W_{P(n)}$ using Table 5.2. Calculate `ad, as, pd, ps` of each device.
- Select L=0.2μ for all devices. Use same C_L as in your calculation.

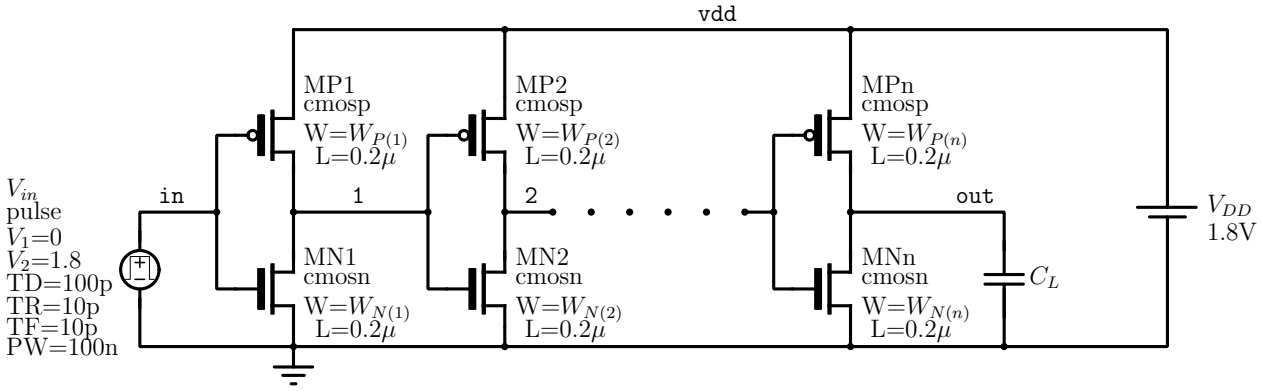

Figure 4.1. Electrical Schematic for Procedure (a).

- Perform a transient analysis with 5ps timesteps up to 200ns.
- Plot V_{in} and V_{out} with the following command: `plot v(in) v(out)`
- Measure T_{PHL} and T_{PLH} of staged buffer and calculate the latency $\mathcal{L}$ using (8). Record the result in Table 5.4 (1^{st} column)

- Write the netlist of the circuit given in Figure 4.2 to inspect the transient response of single inverter circuit.
- Set device sizes $W_{N(1)}$, $W_{P(1)}$ using Table 5.2. Calculate `ad, as, pd, ps` of each device.
- Select L=0.2μ for all devices. Use same C_L as in your calculation.

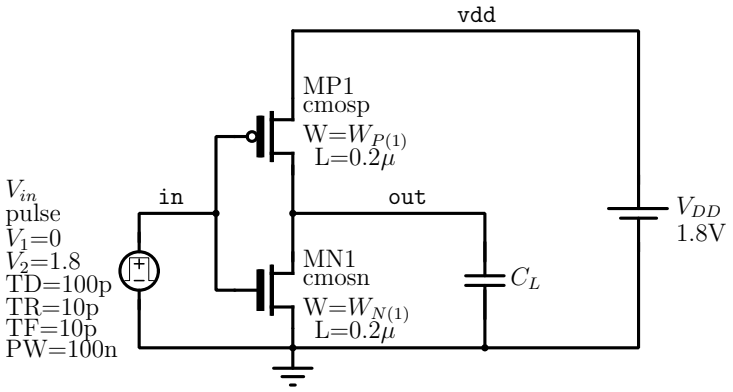

Figure 4.2. Electrical Schematic for Procedure (b).

- Perform a transient analysis with 5ps timesteps up to 200ns.
- Plot V_{in} and V_{out} with the following command: `plot v(in) v(out)`
- Measure T_{PHL} and T_{PLH} of the inverter and calculate the latency $\mathcal{L}$ using (8). Record the result in Table 5.4 (2^{nd} column)
- Answer the questions given in result sheet.

5 Result Sheet

Table 5.1. Chain Number, Tapering Factor and Minimized Latency (Analytical)

n	
m	
$\mathcal{L}$	

Table 5.2. Staged Buffer Device Sizes

Inverter	W_N	W_P
1^{st}		
2^{nd}		
.		
.		
.		
.		
.		
.		
.		
.		

Table 5.3. Single Inverter Delays and Latency. (Analytical)

T_{PHL}	T_{PLH}	$\mathcal{L}_{inv}$

Table 5.4. Simulation Results.

Simulated $\mathcal{L}$ for Tapered Buffer	Simulated $\mathcal{L}_{inv}$ for single inverter.

Why did the latencies calculated manually and simulation differ?

Make a brief conclusion.