Effects of Device Parameters on Performance Metrics of a CMOS Inverter

ELE504E - Homework 4, Spring 2025

1 Introduction

In this homework, we will analyze the CMOS inverter as shown in Figure 1.1. Your focus will be on determining the threshold voltage V_{TH} for a given VTC. You will also investigate the effect of device parameters on the logic threshold voltage. By doing so, you will learn how to adjust these parameters in order to maximize the noise immunity of the inverter at hand.

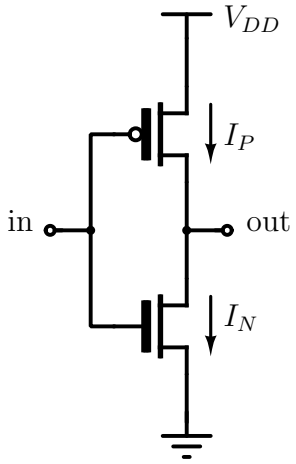

Figure 1.1. Electrical Schematic of CMOS Inverter.

2 Voltage Transfer Curve (VTC) of the CMOS Inverter

Unlike the ideal inverter, CMOS inverter has a finite negative gain in between points C and D as can be shown in Figure 2. This is because the MOSFETs do not perfectly saturate. The unity-slope line passing through the origin intersects the VTC in between these points.

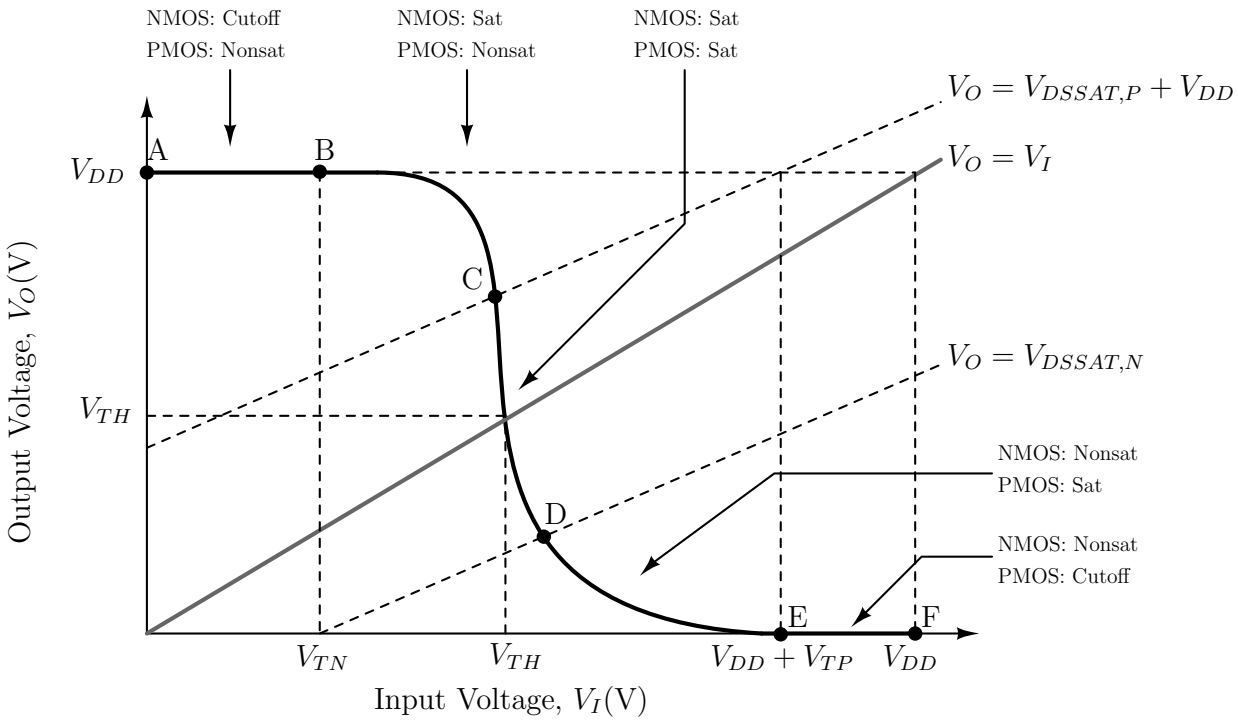

Figure 2.1. VTC of CMOS inverter.

Therefore, the logic threshold voltage, V_{TH}, is defined on this nearly vertical segment. Solving the equation which was based upon $I_P = I_N$ at static conditions for V_I gives the following expression for V_{TH} :

$$V_{TH} = \frac{V_{DD} + V_{TP} + V_{TN} \cdot \sqrt{\frac{W_N}{W_P} \cdot \frac{L_P}{L_N} \cdot \frac{\mu_N}{\mu_P} \cdot \frac{A_P}{A_N}}}{1 + \sqrt{\frac{W_N}{W_P} \cdot \frac{L_P}{L_N} \cdot \frac{\mu_N}{\mu_P} \cdot \frac{A_P}{A_N}}} \tag{1}$$

Noise immunity of the CMOS inverter can be globally maximized by setting V_{TH} in the middle of the logic swing of the inverter. Among the device parameters appearing in the above equation for V_{TH}, only device dimensions W_N, L_N, W_P, L_P can be set by a device designer. In terms of these, equation (1) can be expressed as :

$$\frac{W_P/L_P}{W_N/L_N} = \frac{\mu_N}{\mu_P} \cdot \frac{A_P}{A_N} \cdot \left(\frac{V_{TH} - V_{TN}}{V_{DD} + V_{TP} - V_{TH}} \right)^2 \tag{2}$$

For the specific value $V_{TH} = V_{DD}/2$ of logic threshold and by assuming $V_{TN} \approx V_{TP}$ & $A_N \approx A_P$ and being aware of the need for selecting device channel lengths at minimum in order to speed-up the inverter, equation (2) can be simplified as:

$$\frac{W_P}{W_N} = \frac{\mu_N}{\mu_P} \tag{3}$$

According to (3), W_N and W_P are the only two variables at designer's disposal for setting V_{TH} to $V_{DD}/2$. After setting the logic threshold of your inverter, you must specify the noise margins NM_H and NM_L which guarantee proper interpretation of input level only when the input voltage stays within these margins. These margins are determined via the use of VTC, as well. Calculation of NM_H and NM_L is illustrated in Figure 2.2.

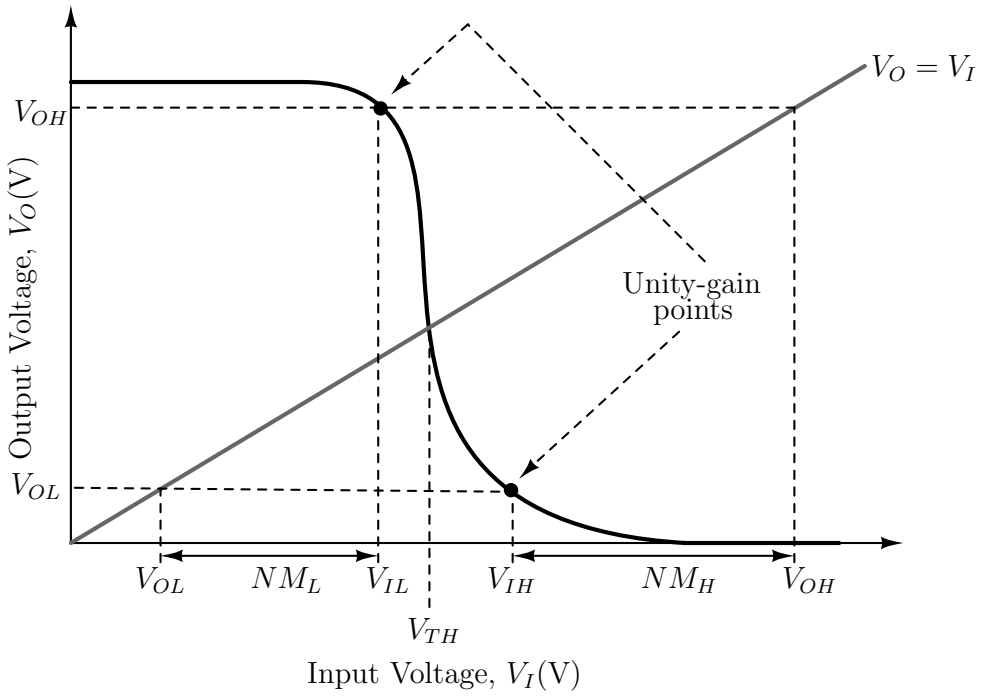

Figure 2.2. Noise Margins of a CMOS Inverter.

$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

In these expressions, V_{IL} is the maximum input-voltage low-level and V_{IH} is the minimum input-voltage high-level which define the uppermost and lowermost permissible input levels for logic-0 and logic-1, respectively. The greater the width of these noise margins the better the noise immunity of your inverter. Therefore, it is important to set V_{IL} and V_{IH} in such a way that the noise margins are maximized. As you may recall from class work, the optimum values of V_{IL} and V_{IH} are set to unity-gain points of the VTC.

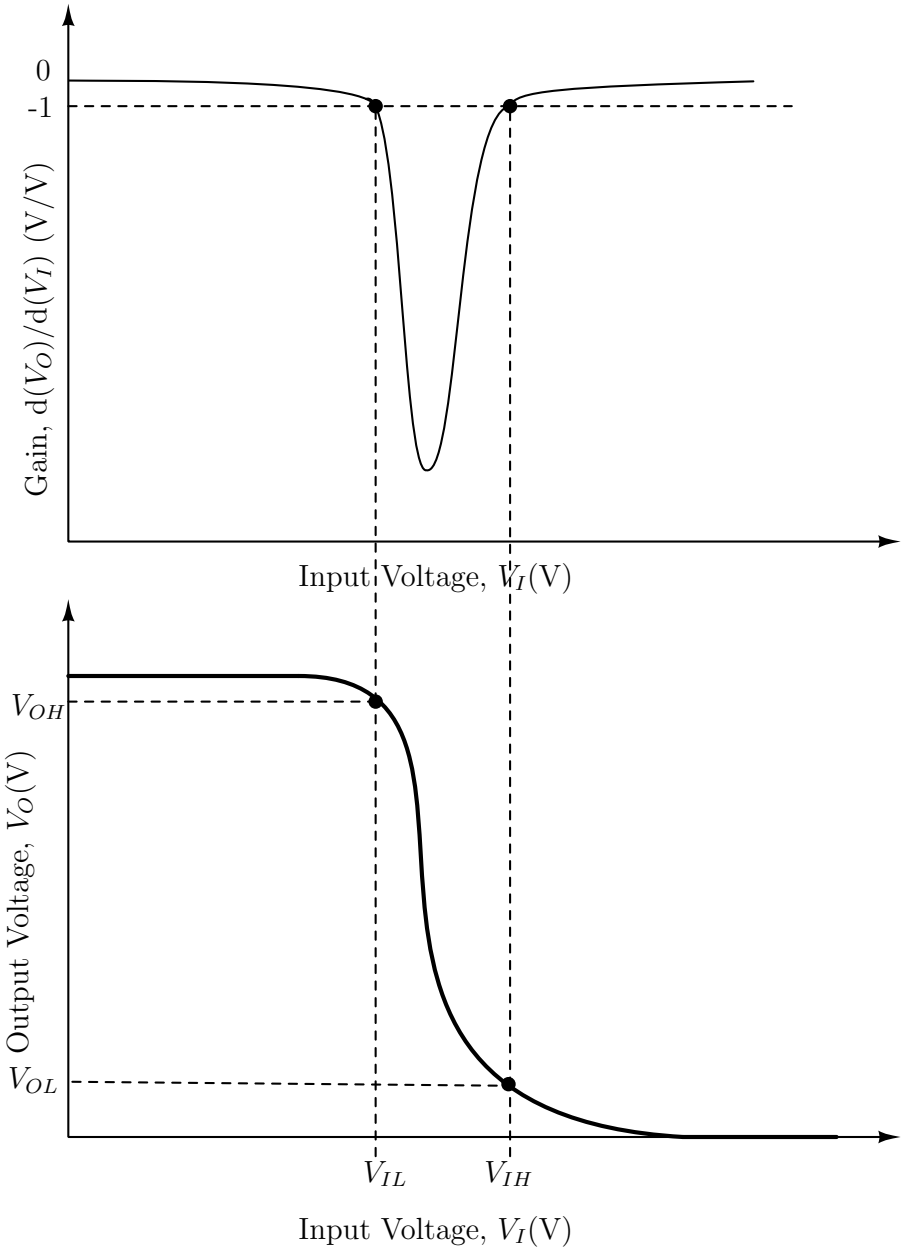

Figure 2.3. Gain plot of an inverter for finding Unity-Gain Points.

3 Procedure

- Write the netlist of the circuit given in Figure 3.1 for obtaining VTC of a CMOS inverter.
- Set device size dimensions W_P, L_P, W_N, L_N as given in Table 3.1 (1^{st} column).
- Perform a dc sweep with the voltage source V_{IN} from 0V to 1.8V with 1mV increments.
- Plot V_{OUT} to obtain the voltage transfer curve with the command: `plot v(out)`.
- Plot $\frac{\partial V_{OUT}}{\partial V_{IN}}$ to find the unity-gain points with the command: `plot deriv(v(out))`
- Measure $V_{IL}, V_{OH}, V_{IH}, V_{OL}, V_{TH}, NM_L, NM_H$ and fill in Table 3.1 (1^{st} column).
- Repeat the same procedure with the device sizes given in Table 3.1 (2^{nd} column).

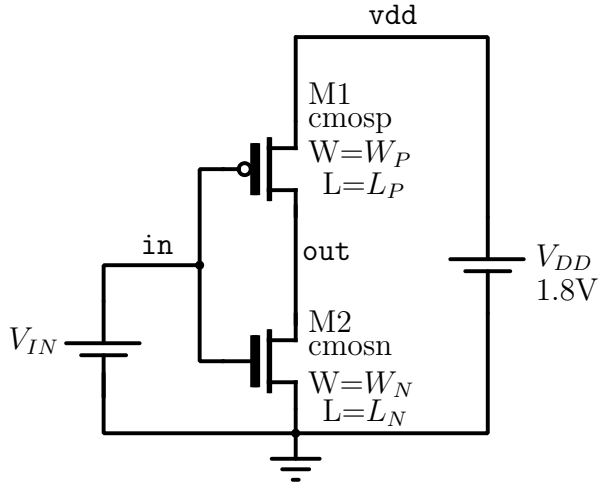

Figure 3.1. Electrical schematic for obtaining VTC of a CMOS inverter.

- Measure $V_{IL}, V_{OH}, V_{IH}, V_{OL}, V_{TH}, NM_L, NM_H$ and fill in Table 3.1 (2^{nd} column).
- Compare your results, explain the differences and their reasons.

Table 3.1. Inverter Comparison

Property	**Inverter-1**	**Inverter-2**
$L_P = L_N$	0.2μm	0.2μm
W_P	0.3μm	0.9μm
W_N	0.3μm	0.3μm
V_{IL}	0.58v	0.72v
V_{OH}	1.72v	1.69v
V_{IH}	0.81v	0.96v
V_{OL}	0.1v	0.1v
NM_L	0.48v	0.62v
NM_H	0.91v	0.73v
V_{TH}	0.75v	0.85v

Comparison:

Vth get closer to middle point 0.9V because mobiliy of PMOS is lower then NMOS so whe we make pmos Width higher it makes PMOS to have similar drive current compared to NMOS. NML is higher because we made the threshold closer to the middle, it was lower because VIL was lower. NMH is lower because Vth was lower in inverter 1 but in inverter 2 it is higher so there are less region that it stay low on the output high on the input. VIH is higher because Vth is moved forward on the line so minimum input voltage for high input is moved forward because of the same reason VIL is moved forward.