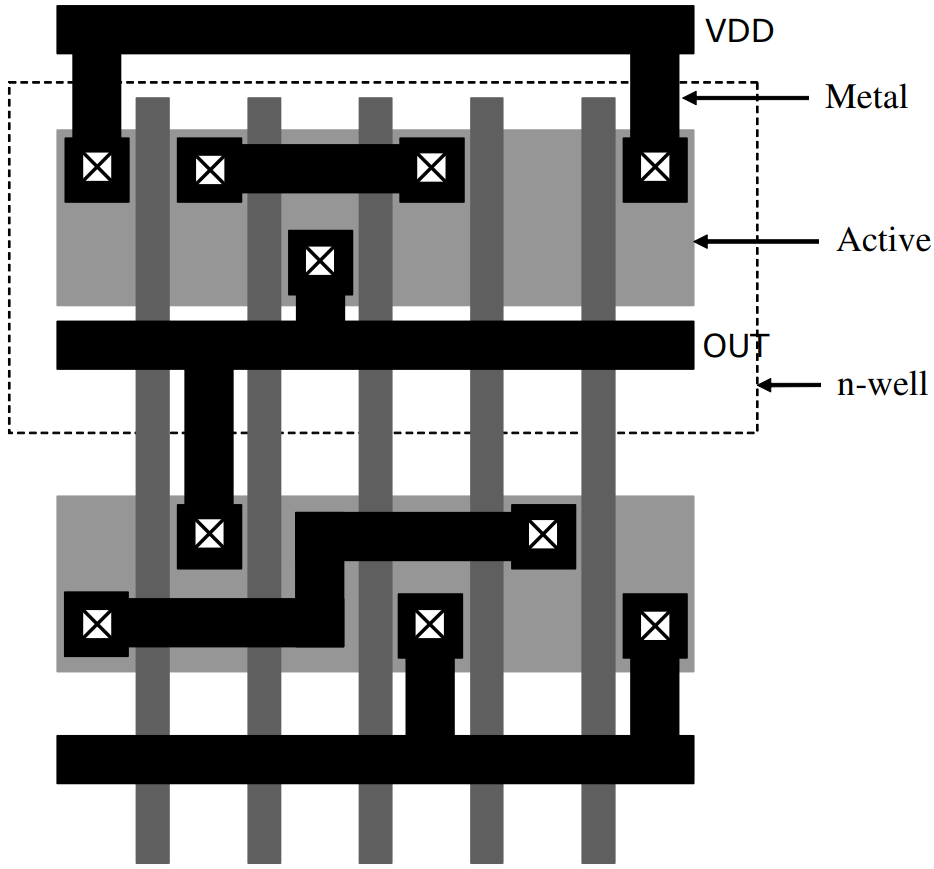
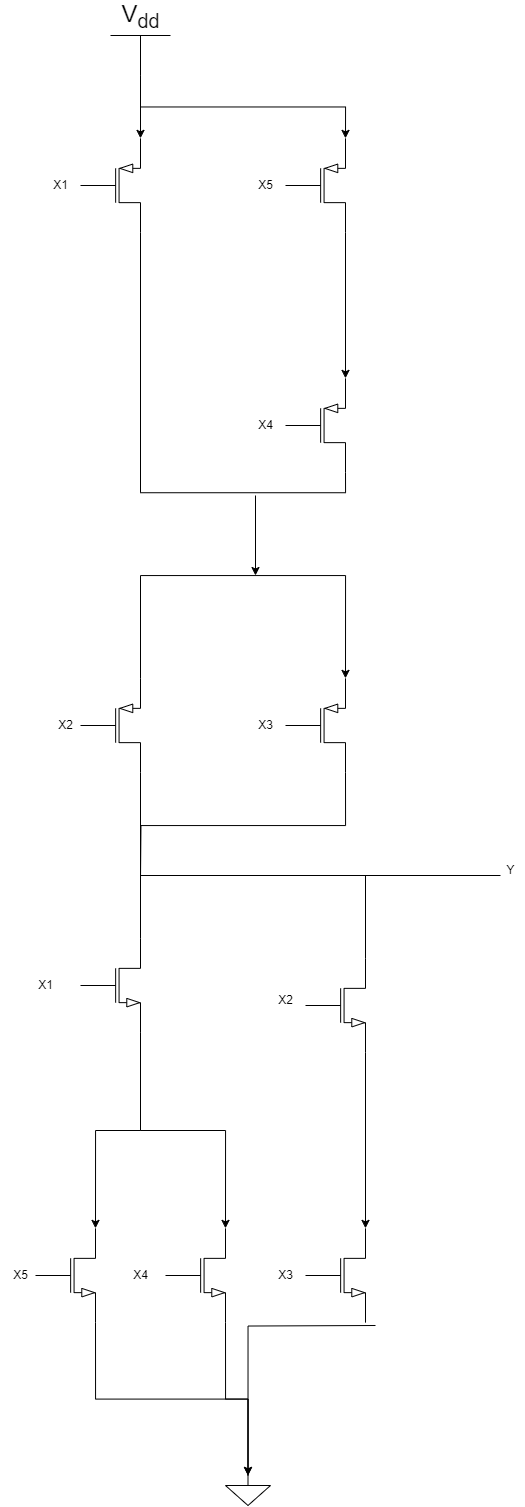
**ELE504E MIDTERM EXAM**

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**Q1)** The Layout of a complex gate is shown. The gate has five inputs (from left to right: X1, X2, X3, X4, X5), an output (OUT) and VDD and GND connections.



1. Draw the electrical schematic of the gate.



1. Find the Boolean expression realized by the gate.

Y

1. Write the netlist of the circuit assuming the gate is to be realized in TSMC 0.18 technology.

midterm q1c

.incl tsmc18.sp

.param wp=0.3u

.param wn=0.3u

vdd vdd 0 dc 1.8

Vx1 x1 0 PULSE(0 1.8 0n 1n 1n 5n 10n)

Vx2 x2 0 PULSE(0 1.8 0n 1n 1n 10n 20n)

Vx3 x3 0 PULSE(0 1.8 0n 1n 1n 20n 40n)

Vx4 x4 0 PULSE(0 1.8 0n 1n 1n 40n 80n)

Vx5 x5 0 PULSE(0 1.8 0n 1n 1n 80n 160n)

mp1 p1 x1 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp2 y x2 p1 p1 cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp3 y x3 p1 p1 cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp4 p1 x4 p2 p2 cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp5 p2 x5 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mn1 y x1 n1 n1 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn2 y x2 n2 n2 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn3 n2 x3 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn4 n1 x4 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn5 n1 x5 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

.control

tran 0.5n 160n

plot v(x1) v(x2)+2 v(x3)+4 v(x4)+6 v(x5)+8 v(y)+10

.endc

**Q2)** A chain of three inverters fabricated in TSMC 0.18 is to drive a capacitive load of 5pF.

1. Determine all device widths in the chain in such a way that total latency is minimized.

|  |  |  |
| --- | --- | --- |
| **Inverter #** | **Wn** | **Wp** |
| **1** | **0.5u** | **0.75u** |
| **2** | **5.42u** | **8.13u** |
| **3** | **58.86u** | **88.3u** |

For this calculations

Cl=5pF Jn(Max)=508A/m Jp(max)=224A/m Lmin=0.2um Cox=8.41 10^-3 F/m^2

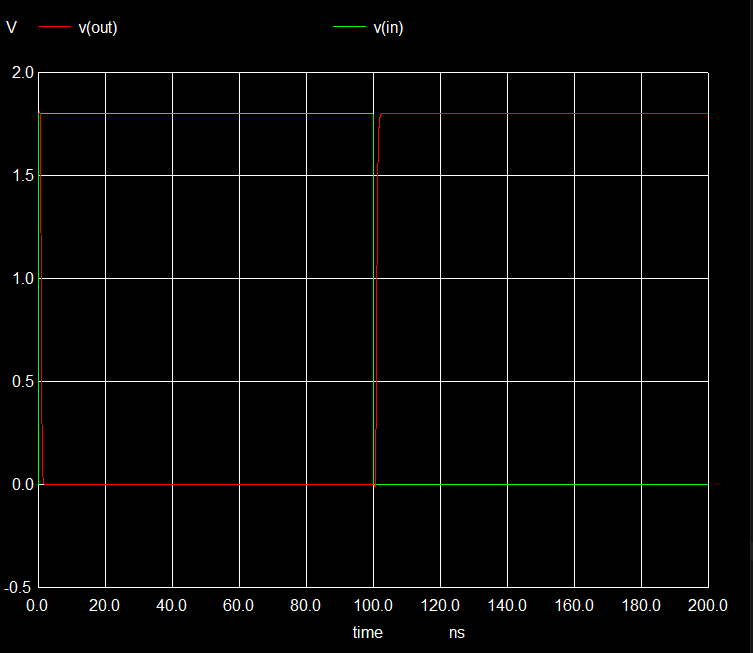
CGSO=7.19 10^-10 F/m Wn(1) = 0.5um

1. Calculate the total chain latency.   
   L = 5.64 10^-10 s , for the calculations equations in stage buffer homework are used.
2. Verify the results using a SPICE simulation.

Tplh from simulation = 8.64 10^-10 s

Tphl simulaton = 7.33 10^-10 s

L = 7.98 10^10s



\* 3-Stage Cascaded CMOS Inverter Chain

.incl tsmc18.sp

\* Parameters

.param Wp=0.75u

.param Lp=0.2u

.param Wn=0.5u

.param Lnch=0.2u

.param Cl=5pf

\* Power supply

VDD vdd 0 1.8

\* Input pulse

Vin in 0 PULSE(0 1.8 100p 10p 10p 100n 200n)

\* Inverter 1

M1\_1 n1 in vdd vdd cmosp W={Wp} L={Lp} ad='Wp\*0.55u' as='Wp\*0.55u' pd='2\*(Wp+0.55u)' ps='2\*(Wp+0.55u)'

M2\_1 n1 in 0 0 cmosn W={Wn} L={Lnch} ad='Wn\*0.55u' as='Wn\*0.55u' pd='2\*(Wn+0.55u)' ps='2\*(Wn+0.55u)'

.param wp2=8.13u

.param wn2=5.42u

\* Inverter 2

M1\_2 n2 n1 vdd vdd cmosp W={wp2} L={Lp} ad='wp2\*0.55u' as='wp2\*0.55u' pd='2\*(wp2+0.55u)' ps='2\*(wp2+0.55u)'

M2\_2 n2 n1 0 0 cmosn W={wn2} L={Lnch} ad='wn2\*0.55u' as='wn2\*0.55u' pd='2\*(wn2+0.55u)' ps='2\*(wn2+0.55u)'

.param wp3=88.3u

.param wn3=58.86u

\* Inverter 3

M1\_3 out n2 vdd vdd cmosp W={wp3} L={Lp} ad='wp3\*0.55u' as='wp3\*0.55u' pd='2\*(wp3+0.55u)' ps='2\*(wp3+0.55u)'

M2\_3 out n2 0 0 cmosn W={wn3} L={Lnch} ad='wn3\*0.55u' as='wn3\*0.55u' pd='2\*(wn3+0.55u)' ps='2\*(wn3+0.55u)'

\* Load Capacitance

Cload out 0 {Cl}

\* Simulation control

\*.tran 5p 200n

\* Propagation delay measurements (optional)

\*.measure tran tplh TRIG V(in) VAL=0.9 RISE=1 TARG V(out) VAL=0.9 RISE=1

\*.measure tran tphl TRIG V(in) VAL=0.9 FALL=1 TARG V(out) VAL=0.9 FALL=1

.control

tran 5p 200n

plot v(in) v(out)

meas tran tphl TRIG v(in) VAL=0.9 RISE=1 TARG v(out) VAL=0.9 FALL=1

meas tran tplh TRIG v(in) VAL=0.9 FALL=1 TARG v(out) VAL=0.9 RISE=1

.endc

.end

**Q3)** You are supposed to implement the Boolean function Y = X1 + X2 + X3 with CMOS static gates. Since such gates inevitably invert, you have two options:

A black line drawing of a plug

Description automatically generated

or

A diagram of a network

Description automatically generated

1. Assuming that all devices in all options are built with minimum geometry devices, which option will yield a shorter latency? Explain.

Delay of Inverter

Lets say Rp=2Rn and Cload = C

Tplh = 0.7 Rp Cload = 1.4 R C

Tphl = 0.7 Rn Cload = 0.7 R C

L = (Tplh + Tphl ) /2 = 1.05 R C

Delay of 3 Input Nand

N = 3

Tplh = 0.7 (Rp/N) Cload = 0.7 (2R/3) C = 0.47 R C

Tphl = 0.7 N Rn Cload = 0.7 3 R C = 2.1 R C

L = (Tplh+Tphl)/2 = ( 0.47 R C + 2.1 R C ) / 2 = 1.285 R C

Delay of NOR

Tplh = 0.7 N Rp Cload = 0.7 3 2 R C = 4.2 R C

Tphl = 0.7 (Rn/N) Cload = ( 0.7 / 3 ) R C = 0.23 R C

L = 2.21 R C

Nor and Inverter delay

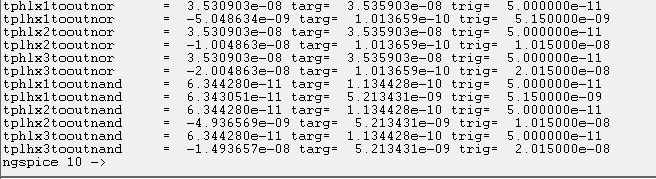
L= (2.21+1.05) R C = 3.26 R C

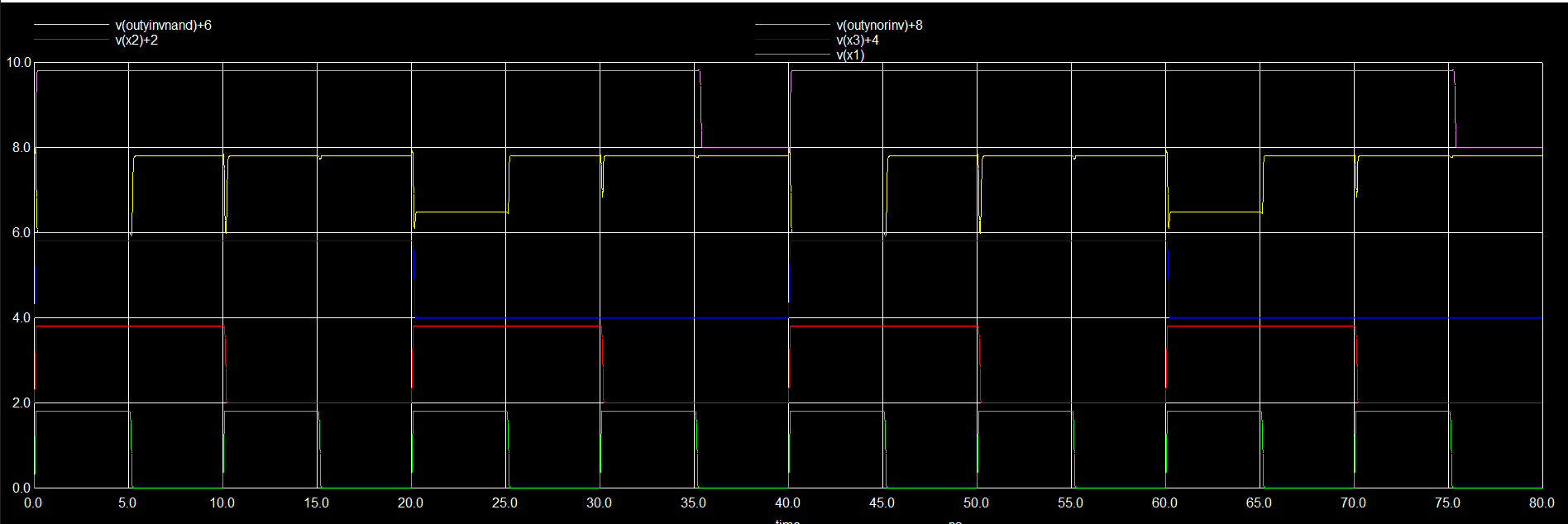
Inverters and Nand delay

L = (1.285 + 1.05 ) R C = 2.335 R C

**Inverters and Nand yields to shorter latency**

1. Verify the results found in (a) with a SPICE simulation. Write your input netlist and provide your simulation results.





\* Midterm q3c

.include tsmc18.sp

.global vdd

\* Power supply

VDD vdd 0 1.8

\*Signals

Vx1 x1 0 PULSE(0 1.8 0n 0.1n 0.1n 5n 10n)

Vx2 x2 0 PULSE(0 1.8 0n 0.1n 0.1n 10n 20n)

Vx3 x3 0 PULSE(0 1.8 0n 0.1n 0.1n 20n 40n)

\* NOR and Inverter

xnor x1 x2 x3 outnor nor

xinvnor outnor outynorinv inv

\* 3 Inv and NAND

xinvnand1 x1 x1n inv

xinvnand2 x2 x2n inv

xinvnand3 x3 x3n inv

xnand x1 x2 x3 outyinvnand nand

.control

tran 10p 80n

\* Delay from x1 to out nor

meas tran tphlx1tooutnor TRIG v(x1) VAL=0.9 RISE=1 TARG v(outynorinv) VAL=0.9 FALL=1

meas tran tplhx1tooutnor TRIG v(x1) VAL=0.9 FALL=1 TARG v(outynorinv) VAL=0.9 RISE=1

\* Delay from x2 to out nor

meas tran tphlx2tooutnor TRIG v(x2) VAL=0.9 RISE=1 TARG v(outynorinv) VAL=0.9 FALL=1

meas tran tplhx2tooutnor TRIG v(x2) VAL=0.9 FALL=1 TARG v(outynorinv) VAL=0.9 RISE=1

\* Delay from x3 to out nor

meas tran tphlx3tooutnor TRIG v(x3) VAL=0.9 RISE=1 TARG v(outynorinv) VAL=0.9 FALL=1

meas tran tplhx3tooutnor TRIG v(x3) VAL=0.9 FALL=1 TARG v(outynorinv) VAL=0.9 RISE=1

\* Delay from x1 to out nand

meas tran tphlx1tooutnand TRIG v(x1) VAL=0.9 RISE=1 TARG v(outyinvnand) VAL=0.9 FALL=1

meas tran tplhx1tooutnand TRIG v(x1) VAL=0.9 FALL=1 TARG v(outyinvnand) VAL=0.9 RISE=1

\* Delay from x2 to out nand

meas tran tphlx2tooutnand TRIG v(x2) VAL=0.9 RISE=1 TARG v(outyinvnand) VAL=0.9 FALL=1

meas tran tplhx2tooutnand TRIG v(x2) VAL=0.9 FALL=1 TARG v(outyinvnand) VAL=0.9 RISE=1

\* Delay from x3 to out nand

meas tran tphlx3tooutnand TRIG v(x3) VAL=0.9 RISE=1 TARG v(outyinvnand) VAL=0.9 FALL=1

meas tran tplhx3tooutnand TRIG v(x3) VAL=0.9 FALL=1 TARG v(outyinvnand) VAL=0.9 RISE=1

plot v(x1) v(x2)+2 v(x3)+4 v(outyinvnand)+6 v(outynorinv)+8

.endc

.subckt inv in out wp=0.3u wn=0.3u

m1 out in vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

m2 out in 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

.ends

.subckt nand x1 x2 x3 out wp=0.3u wn=0.3u

mp1 out x1 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp2 out x2 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp3 out x3 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mn1 out x1 n1 n1 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn2 n1 x2 n2 n2 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn3 n2 x2 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

.ends

.subckt nor x1 x2 x3 out wp=0.3u wn=0.3u

mp1 p1 x1 vdd vdd cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp2 p2 x2 p1 p1 cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mp3 out x3 p2 p2 cmosp w='wp' l=0.2u ad='wp\*0.55u' as='wp\*0.55u' pd='2\*(wp+0.55u)' ps='2\*(wp+0.55u)'

mn1 out x1 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn2 out x2 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

mn3 out x3 0 0 cmosn w='wn' l=0.2u ad='wn\*0.55u' as='wn\*0.55u' pd='2\*(wn+0.55u)' ps='2\*(wn+0.55u)'

.ends

.end