Course name: Digital Design

Number: CS 223

Section: 3

Number of the lab: 2

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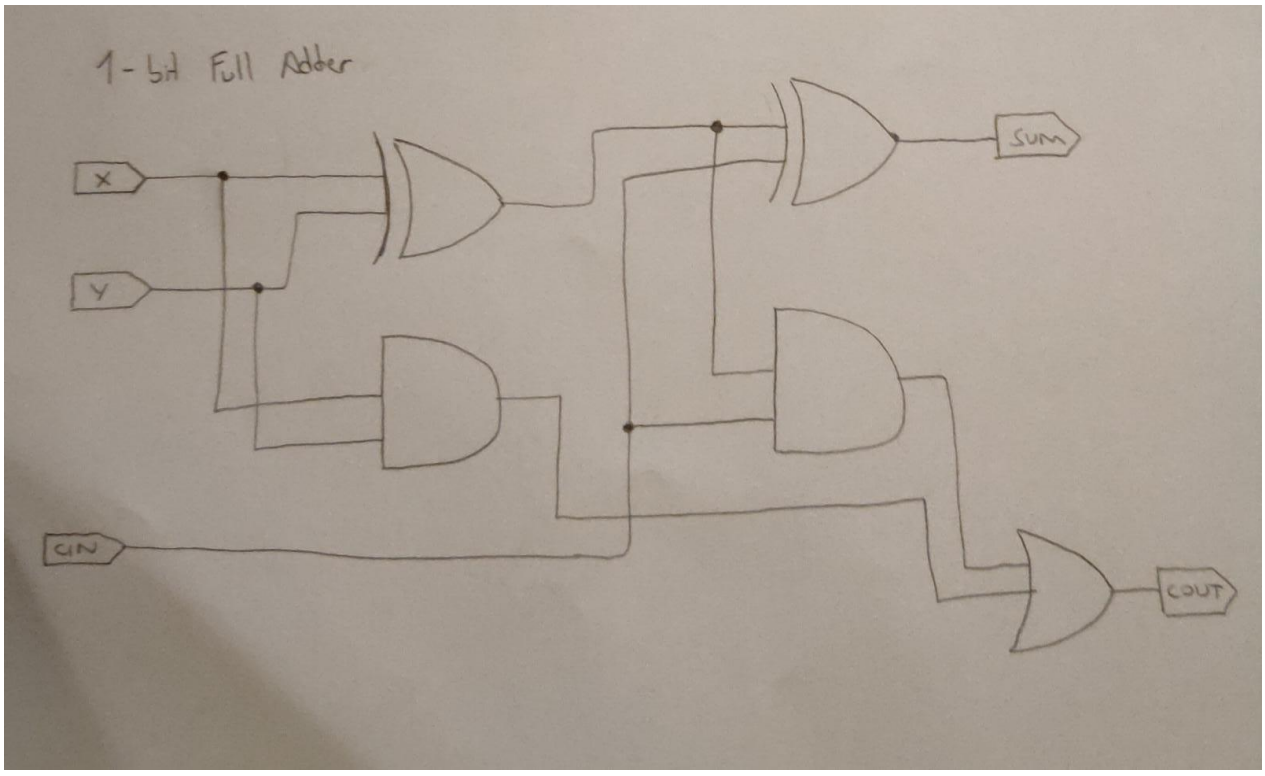
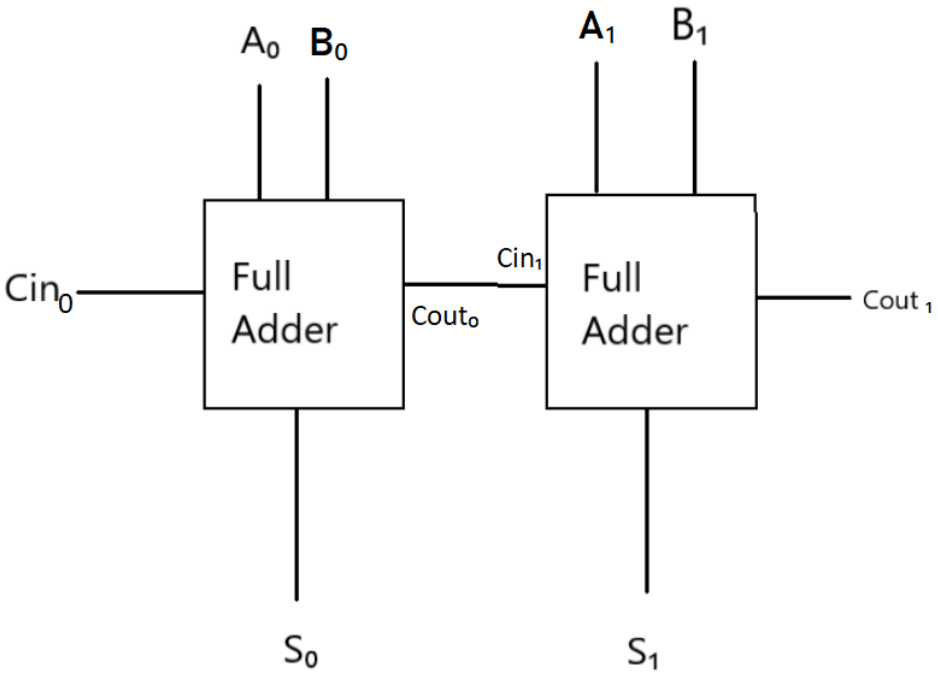
B) Schematic for a 1-bit fulladder



C) Schematic for a 2-bit adder made from two 1-bit fulladders



D) Dataflow Systemverilog module for the 1-bit fulladder

```
module dataflow( input logic x, y, cin, output logic sum, cout);

assign sum = (x ^ y) ^ cin;
assign cout = (x & y) | ((x ^ y) & cin);

endmodule
```

E) Structural Systemverilog module for the 1-bit fulladder

```
module structuralOneBitFullAdder( input x, y, cin, output sum, cout );

logic out0, out1, out2;

xor0 xor0(x, y, out0);
xor0 xor1(out0, cin, sum);
and0 and0(x, y, out1);
and0 and1(out0, cin, out2);
or0 or0(out2, out1, cout);

endmodule

module xor0( input a, b, output out);
assign out = a ^ b;
endmodule
module and0( input a, b, output out);
assign out = a & b;
endmodule
module or0( input a, b, output out);
assign out = a | b;
endmodule
```

TESTBENCH

```
module testbenchOneBitFullAdder();

logic x, y, cin, sum, cout;
structuralOneBitFullAdder dut( x, y, cin, sum, cout);
```

```
initial begin
    x = 0; y = 0; cin = 0; #10;
    cin = 1; #10;
    y = 1; cin = 0; #10;
    cin = 1; #10;
    x = 1; y = 0; cin = 0; #10;
    cin = 1; #10;
    y = 1; cin = 0; #10;
    cin = 1; #10;
end

endmodule
```

F) Structural Systemverilog module for the 2-bit adder

```
module structuralTwoBitAdder( input logic a0, b0, cin, a1, b1, output logic s0, s1, cout1);

    logic cout0;

    fullAdder fullAdder0( a0, b0, cin, s0, cout0);
    fullAdder fullAdder1( a1, b1, cout0, s1, cout1);

endmodule

module fullAdder( input logic a, b, cin, output logic s, cout);

    logic out0, out1, out2;

    assign out0 = a ^ b;
    assign s = out0 ^ cin;
    assign out1 = a & b;
```

```
    assign out2 = out0 & cin;
    assign cout = out2 | out1;

Endmodule
```

TESTBENCH

```
module testbenchTwoBitAdder();

    logic a0, b0, cin, a1, b1, s0, s1, cout1;

    structuralTwoBitAdder dut( a0, b0, cin, a1, b1, s0, s1, cout1);

    initial begin
        a0 = 0; b0 = 0; cin = 0; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        cin = 1; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        b0 = 1; cin = 0; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        cin = 1; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        a0 = 1; b0 = 0; cin = 0; a1 = 0; b1 = 0; #10;
```

```
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        cin = 1; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        b0 = 1; cin = 0; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
        cin = 1; a1 = 0; b1 = 0; #10;
        b1 = 1; #10;
        a1 = 1; b1 = 0; #10;
        b1 = 1; #10;
    end

endmodule
```