CS 224 – Computer Organization

Bilkent University

CS

Preliminary Report

Lab 6

Section 1

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1-

| No. | Cache Size KB | N way cache | Word Size in bits | Block size (no. of words) | No. of Sets | Tag Size in bits | Index Size (Set No.) in bits | Word Block Offset Size in bits[1] | Byte Offset Size in bits[2] | Block Replacement Policy Needed (Yes/No) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 128 | 1 | 32 | 4 | $2^{13}$ | 15 | 13 | 2 | 2 | no |
| 2 | 128 | 2 | 32 | 4 | $2^{12}$ | 16 | 12 | 2 | 2 | yes |
| 3 | 128 | 4 | 32 | 8 | $2^{10}$ | 17 | 10 | 3 | 2 | yes |
| 4 | 128 | Full | 32 | 8 | $2^{0}$ | 27 | 0 | 3 | 2 | yes |
| 9 | 256 | 1 | 16 | 4 | $2^{15}$ | 14 | 15 | 2 | 1 | no |
| 10 | 256 | 2 | 16 | 4 | $2^{14}$ | 15 | 14 | 2 | 1 | yes |
| 11 | 256 | 4 | 16 | 16 | $2^{11}$ | 16 | 11 | 4 | 1 | yes |
| 12 | 256 | Full | 16 | 16 | $2^{0}$ | 27 | 0 | 4 | 1 | yes |

2-

| Memory Address Accessed (hex) | Set No. | Hit (yes/no) |
|---|---|---|
| 00 00 00 24 | 0 | no |
| 00 00 00 42 | 0 | no |
| 00 00 00 68 | 1 | no |
| 00 00 00 04 | 0 | no |
| 00 00 00 0C | 1 | no |
| 00 00 00 4C | 1 | no |

3-

| Memory Address Accessed (hex) | Set No. | Hit (yes/no) |
|---|---|---|
| 00 00 00 2C | 1 | no |
| 00 00 00 48 | 1 | no |
| 00 00 00 44 | 0 | no |
| 00 00 00 0C | 1 | no |
| 00 00 00 04 | 0 | no |
| 00 00 00 0C | 1 | yes |

4-

T(L1) = 1 clk cycle, T(L2) = 2 clk cycles, T(MM) = 20 clk cycles, M(rL1) = 20%, M(rL2) = 5%

AMAT = T(L1) + M(rL1) x (T(L2) M(rL2) x T(MM))

AMAT = 1 + 0.2 ( 2 + 0.05 x 20 ) = 1.6 clk cycles

1 GHz processor has a cycle time of 1.0 ns and a 4 GHz processor has a cycle time of 0.25 ns.

Time for $10^{12}$ instructions = $10^{12}$ x 0.25 ns x 1.60 = 400 s