`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 19:37:09 06/18/2023

// Design Name: Vending\_Machine

// Module Name: C:/Users/Faseeh/Desktop/Vending\_Machine/VendingMachine/Vending\_Machine\_tb.v

// Project Name: VendingMachine

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: Vending\_Machine

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module Vending\_Machine\_tb;

// Inputs

reg clk;

reg reset;

reg [1:0] I0;

// Outputs

wire out;

wire [1:0] change;

// Instantiate the Unit Under Test (UUT)

Vending\_Machine uut (

.clk(clk),

.reset(reset),

.I0(I0),

.out(out),

.change(change)

);

initial begin

// Initialize Inputs

clk = 0;

reset = 1;

I0 = 0;

#100 reset = 0;

I0 = 1;

// Wait 100 ns for global reset to finish

#100 I0 = 2'b01;

#100 I0 = 2'b10;

#100 I0 = 2'b01;

// Add stimulus here

end

always #10 clk = ~clk;

endmodule