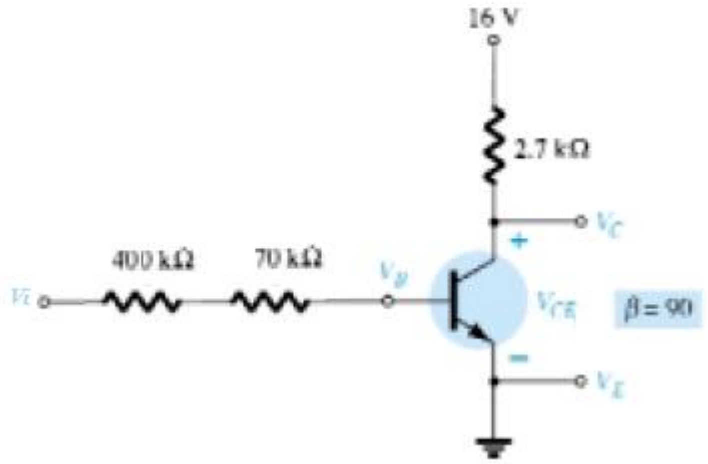
National University of Computer & Emerging Sciences, Lahore
Department of Computer Science

Basic Electronics (Spring 2015)
Assignment-5
Due Date for Sections A, B: 28 May 2015
Due Date for Sections C, D, E, and F: 27 May 2015

Topics:

- Transistor circuit with DC source as input
  - Active Region
  - Saturation Region
- Transistor as a switch
  - Logic gates

1. Find I_B, I_C, V_{CE}, V_C, V_B, V_E in the circuit given below, if $V_i = 5V$.



$$V_E = 0$$

$$V_{BE} = V_B = 0.7V$$

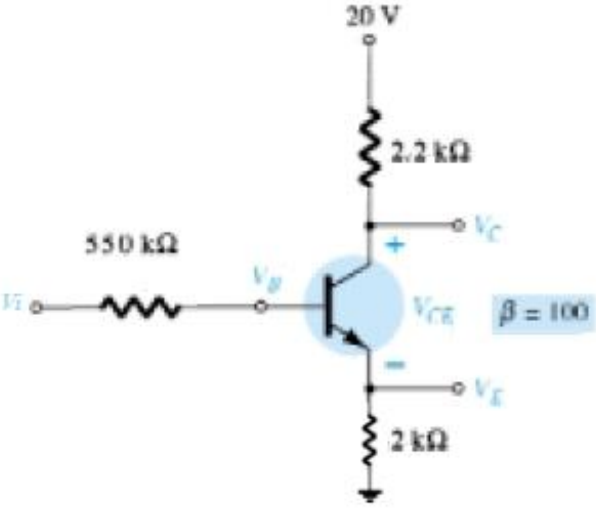
$$I_B = \frac{5 - 0.7}{470K} = 9.15uA$$

Assuming Active mode:

$$I_C = \beta I_B = 0.824mA$$

$V_C = 16 - 2.7KI_C = \mathbf{13.78V}$ > V_B *so active mode assumption is correct*

2. Find I_B, I_C, V_C, V_E, V_{CE}, V_B in the circuit given below, if V_i =10V.



Assuming Active Mode

$V_E = I_E \times 2K$

$I_E = (1+\beta)I_B$

$$I_B = \frac{Vi - VBE - VE}{550K}$$

$$I_B = \frac{10 - 0.7 - VE}{550K}$$

$$I_B = \frac{10 - 0.7 - (I_E \times 2K\ )}{550K}$$

$$I_B = \frac{10 - 0.7 - ((1+\beta)I_B \times 2K\ )}{550K} = 12.37uA$$

$I_E = (1+\beta)I_B = 1.24mA$

$V_E = I_E \times 2K = 2.5\text{V}$

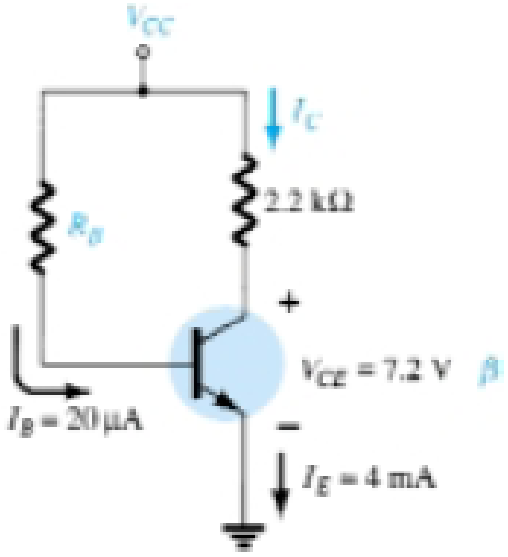
$V_B = VBE + VE = 0.7 + 2.5 = 3.2V$

$I_C = (\beta)I_B = 1.23mA$

$V_C = \ 20 - 2.2KI_C = \mathbf{17.294V} > V_B$ *so active mode assumption is correct*

$V_{CE} = V_C - V_E = 14.794V$

3. Find I_C, Vcc, β, R_B, V_E, V_B, V_C in the circuit given below.

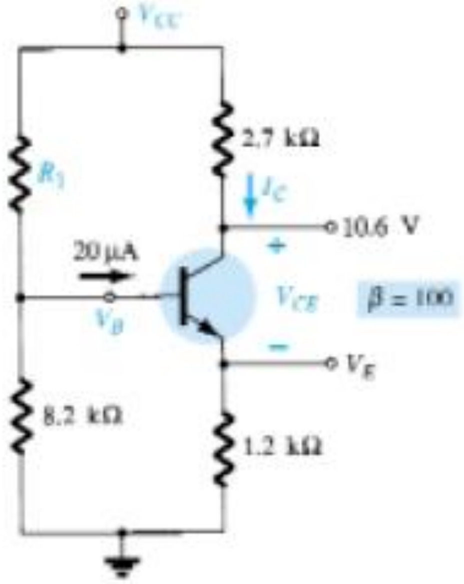


$I_E = (1 + \beta)I_B$

$\beta = 199$
$I_C = (\beta)I_B = 3.98mA$
$V_{BE} = V_B = 0.7V$
$V_{CE} = V_C = 7.2V$

Since, $V_C > V_B$ so active mode
$V_{CC} = I_C Rc + V_{CE} = 15.96$
$V_{CC} = I_B R_B + V_{BE}$ => $R_B = 763K$

4. Find I_C, V_E, V_{CC}, V_{CE}, V_B, R_1 in the circuit given below:



$I_B = 20uA$

Assuming active mode

$I_C = (\beta)I_B = 2mA$

$I_E = 2.02mA$

$V_E = I_E \times 1.2K = 2.42\text{V}$

$V_B = VBE + VE = 0.7 + 2.42 = 3.12V$

$V_C = 10.6 > V_B$ *so active mode assumption is correct*

$V_{CE} = V_C - V_E = 8.18V$

$V_{CC} = I_C Rc + V_C = 16$

$$\frac{VB - Vcc}{R1} + 20u + \frac{VB - 0}{8.2K} = 0 => R1 = 32.16K$$

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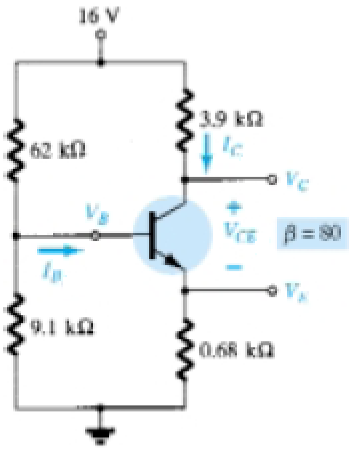
5. Find I_B, I_C, V_C, V_E, V_{CE},V_B in the circuit given below:



$$\frac{VB-16}{62K}+I_B+\frac{VB-0}{9.1K}=0$$

$V_B = VBE + VE = 0.7 + (1+\beta)I_B \times 0.68K$

Solving above two equations

$I_B = 21.4uA$

$V_B = 1.878V$

$I_C = 1.712mA$

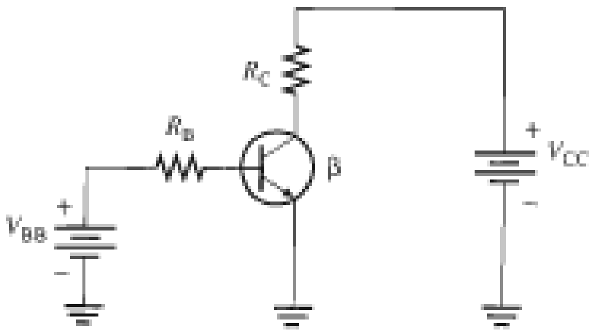
$I_E = 1.7334mA$

V_E =1.179V

$V_{CC} - \ I_C Rc = V_C$ = 9.32

$V_{CE} = 8.14V$

6. Determine whether or not the transistor is saturated for the following values: β = 125, V_{BB} =1.5V, R_B = 6.8kΩ, R_C = 180Ω and V_{CC} =12V and V_{CE} = 0.2V.



$$I_B = \frac{1.5 - 0.7}{6.8K} = 117.64uA$$

Assuming Active mode

$$I_C = (\beta)I_B = 14.71mA$$

$$V_{CC} - I_C Rc = V_C = 14.6478 > VB \; so \; no \; saturation$$

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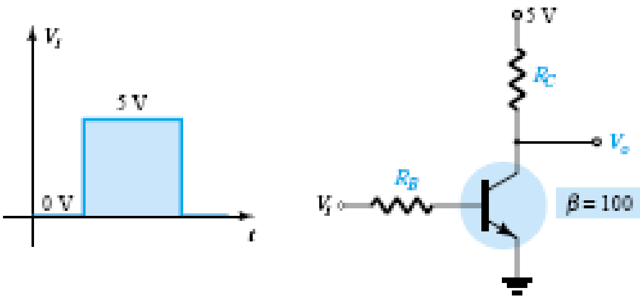
7. Design the transistor inverter of figure given below to operate with a saturation current of 8mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of I_{Bmax} and find the resistor values. $V_{CE(sat)}$=0.2volts.



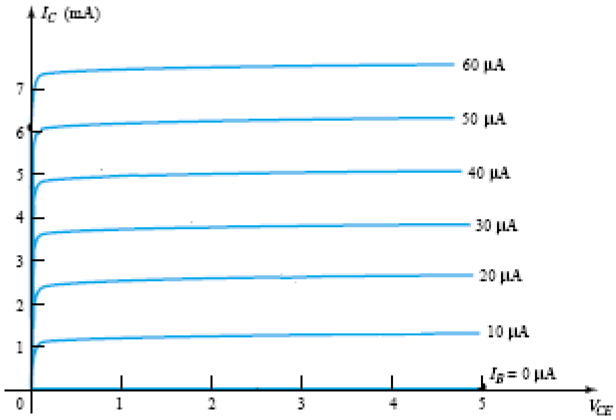
If in saturation, VCE(sat) = 0.2
IC(sat) = (Vcc – 0.2)/R_C = 8mA => **Rc = 600**

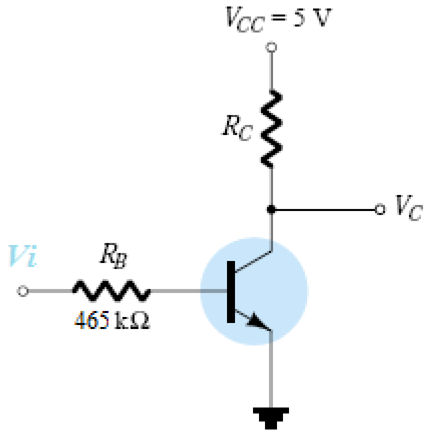
$$I_{B(\max)} = \frac{Ic(sat)}{\beta} = 80uA$$

$$I_B = 120\% \; I_{B(\max)} = 96uA$$

R_B = (5-0.7)/I_B = 44.8K

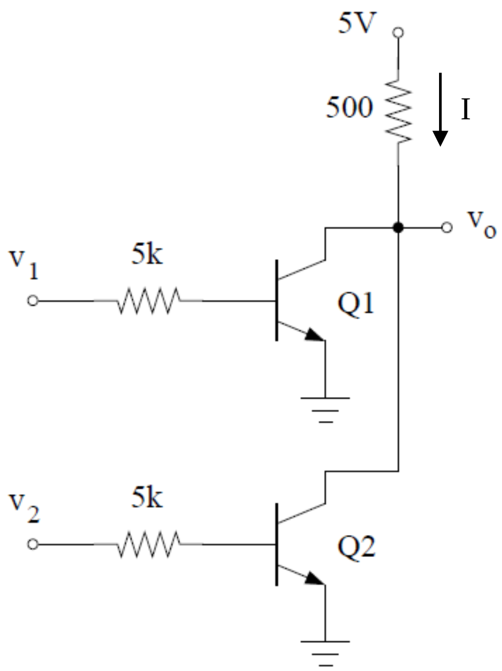
8. Find value of β and R_c in the circuit given below, if $V_{CE} = 1V$ and $V_i = 10V$.





Vc = 1V ,
I_B= (10-0.7)/465K = 20uA
From graph, Ic = 2.5mA, β = 125
Ic = (5-1)/Rc => Rc = 1.6K

9. If β =100 and $V_{CE(sat)}$=0.2V for each transistor, then find out which 2-input logic gate is shown below.
<u>Note:</u> Use high logic H = 5V and for low logic L = 0V



$I = I_{c1} + I_{c2}$

1) If V1 = 0, and V2 = 0, I_{c1} =0, I_{c2} = 0, I =0, so **Vo = 5V**
2) If V1 = 0, and V2 = 5, I_{c1}=0, => $I = I_{c2}$
If Q2 is active, I_{B2} = (5-0.7) / 5K = 860uA => Ic2 = 86mA => I = 86mA
=> Vo = (5-86mx500) = -38<V_{B2} so Q2 is not in active mode but in saturation => **Vo = 0.2**
3) If V1 = 5, and V2 = 0, I_{c2}=0, => $I = I_{c1}$
If Q1 is active, I_{B1} = (5-0.7) / 5K = 860uA => Ic1 = 86mA => I = 86mA

=> $V_o = (5\text{-}86m\times500) = -38 < V_{B1}$ so Q1is not in active mode but in saturation => **Vo = 0.2**

4) If V1 = 5, and V2 = 5,

If Q1 is active, $I_{B1} = (5-0.7) / 5K = 860uA$ => Ic1 = 86mA

If Q2 is active, $I_{B2} = (5-0.7) / 5K = 860uA$ => Ic2 = 86mA

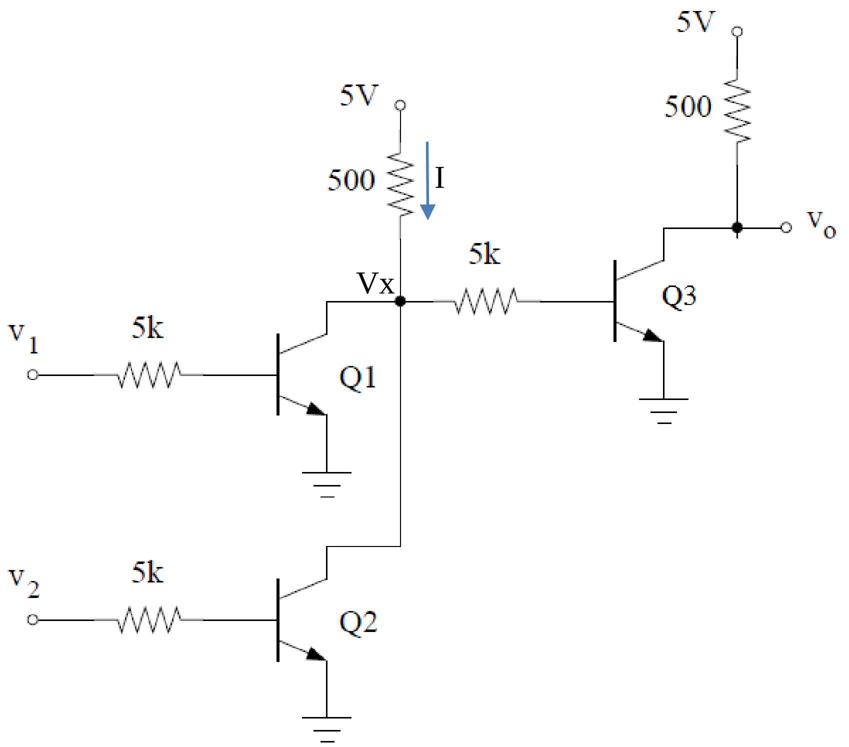
I = Ic1+Ic2 = 172mA

=> $V_o = (5\text{-}172m\times500) = -81 < V_{B1}$ so Q1 and Q2 both are in saturation => **Vo =0.2**

V1	**V2**	**Vo**
0	0	5
0	5	0.2
5	0	0.2
5	5	0.2

So this is a NOR gate

10. If β =100 and $V_{CE(sat)}$=0.2V for each transistor, then find out which 2-input logic gate is shown below.
<u>Note:</u> Use high logic H = 5V and for low logic L = 0V



$I = I_{c1} + I_{c2} + I_{B3}$

1) If V1 = 0, and V2 = 0, I_{c1} =0, I_{c2} = 0, I = I_{B3}
I_{B3} = (5 – 0.7)/5500 = 0.78mA , assuming Q3 is in active mode, Ic = 78.18mA => Vc = -34.1 < 0.7
So Q3 is in saturation => **Vo = 0.2**

2) If V1 = 0, and V2 = 5, I_{c1} =0, I = I_{c2} + I_{B3}

Assuming Q2 in saturation,
V_x = 0.2 => Q3 is in cut off => I_{B3} = 0 & I_{c3} = 0, => Vo = 5
I = $I_{c2(sat)}$
$I_{c2\ (sat)}$ = (5-0.2)/500 = 9.6mA

I_{B2} = (5 – 0.7)/5000 = 860uA
$I_{c2\ (active)}$ = 86mA
For saturation $I_{c2(sat)} < I_{c2(active)}$ TRUE so Q2 is surely in saturation

3) If V1 = 5, and V2 = 0, I_{c2} =0, I = I_{c1} + I_{B3}

Assuming Q1 in saturation,
V_x = 0.2 => Q3 is in cut off => I_{B3} = 0 & I_{c3} = 0, => Vo = 5
I = $I_{c1(sat)}$
$I_{c1\ (sat)}$ = (5-0.2)/500 = 9.6mA

I_{B1} = (5 – 0.7)/5000 = 860uA
$I_{c1\ (active)}$ = 86mA

For saturation $I_{c1(sat)} < I_{c1(active)}$ TRUE so Q1 is surely in saturation

4) If V1 = 5, and V2 = 5, $I = I_{c1} + I_{c2} + I_{B3}$

Assuming Q1 and Q2 both in saturation,
$V_x = 0.2$ => Q3 is in cut off => $I_{B3} = 0$ & $I_{c3} = 0$, => Vo = 5
$I = I_{c1(sat)} + I_{c2(sat)} = 9.6mA$

$I_{B1} = (5 – 0.7)/5000 = 860uA$ => $I_{c1\ (active)} = 86mA$
$I_{B2} = (5 – 0.7)/5000 = 860uA$ => $I_{c2\ (active)} = 86mA$
If both are in active then I = 172mA
$I_{sat} < I$ so Q1 and Q2 both are in saturation