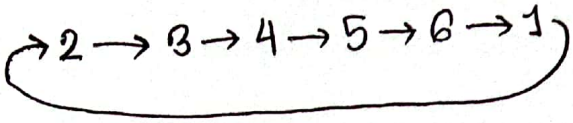
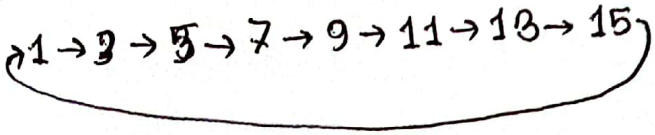
Experiment No. : 08

Experiment Name: i) Design a synchronous sequential circuit with the sequence given below using JK FFs:



ii) Design a 4-bit odd counter:

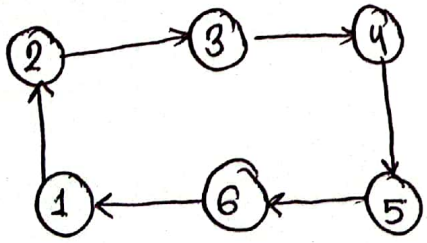


Objective:

The objective of this experiment is to implement two synchronous sequential circuit. In the first experiment we will implement a random synchronous sequential clock counter and in the second experiment we will implement a 4-bit odd counter. In the first experiment we will use 3 JK flip-flops and in the second we will use 4 D flip-flops.

For (i),

State Diagram:



State Table:

Present State			Next State		
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
0	0	1	0	1	0

∴ There will be 3 JK Flip-Flops

and, $d = \Sigma(0, 7)$

Excitation Table:

Present State			Next State			Flip - Flop					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	0	0	1	x	1	x	1	1	x
0	0	1	0	1	0	0	x	1	x	x	1

Function Simplification:

For 3rd Flip-Flop:

For J_3,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
Q_3'	X		1	
Q_3	X	X	X	X

$\therefore J_3 = Q_2Q_1$

For K_3,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
Q_3'	X		X	X
Q_3			X	1

$\therefore K_3 = Q_2$

For 2nd Flip-Flop:

For J_2,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	$Q_2'Q_1'$
Q_3'	X	1	X	X
Q_3		1	X	

$\therefore J_2 = Q_1$

For K_2,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
Q_3'	x	x	1	
Q_3	x	x	x	1

$\therefore K_2 = Q_3 + Q_1$

For 1st Flip-Flop:

For J_1,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
Q_3'	x	x	x	1
Q_3	1	x	x	1

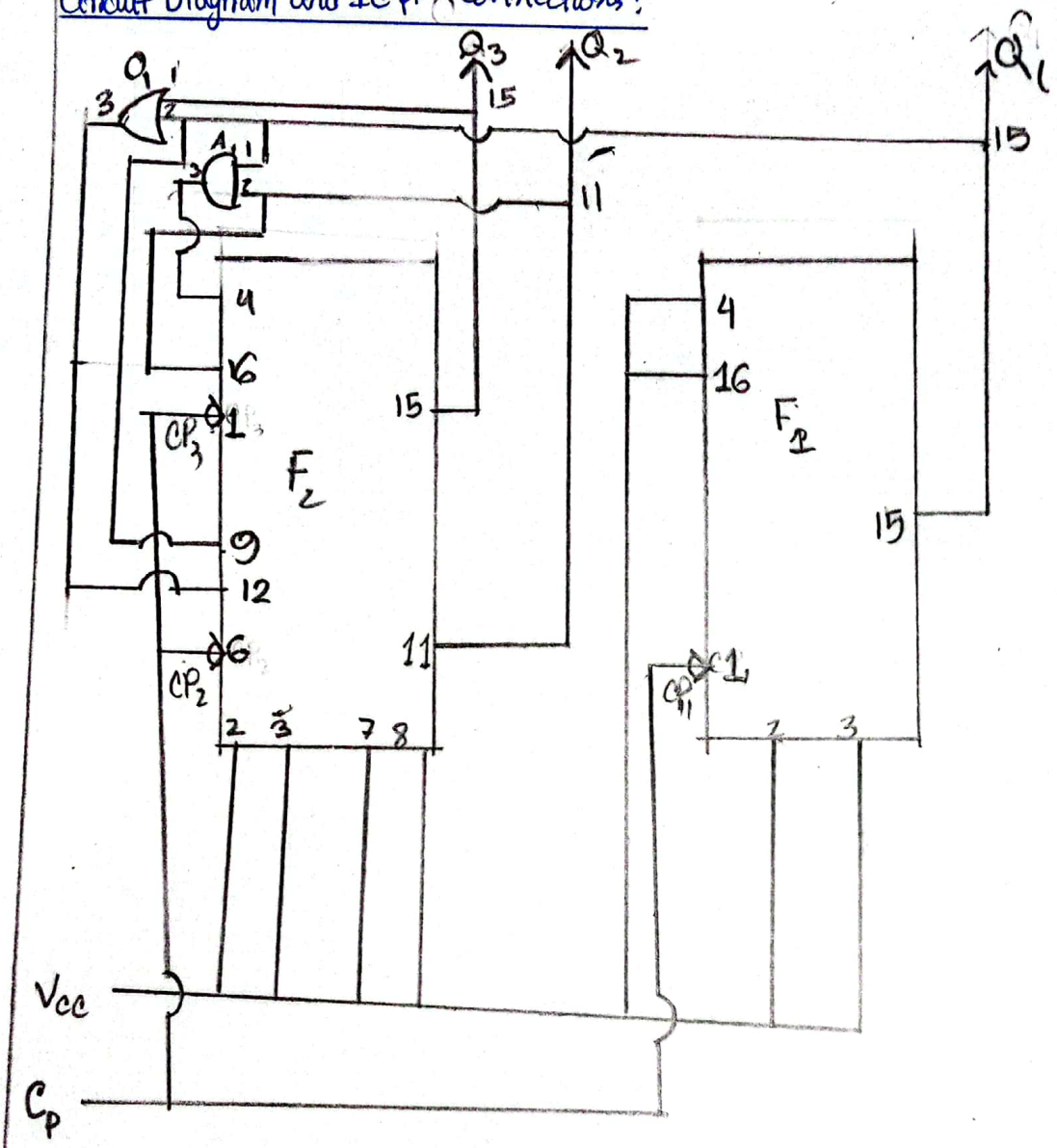
$\therefore J_1 = 1$

For K_1,

Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
Q_3'	x	1	1	x
Q_3	x	1	x	x

$\therefore K_1 = 1$

Circuit Diagram and IC pin Connections:



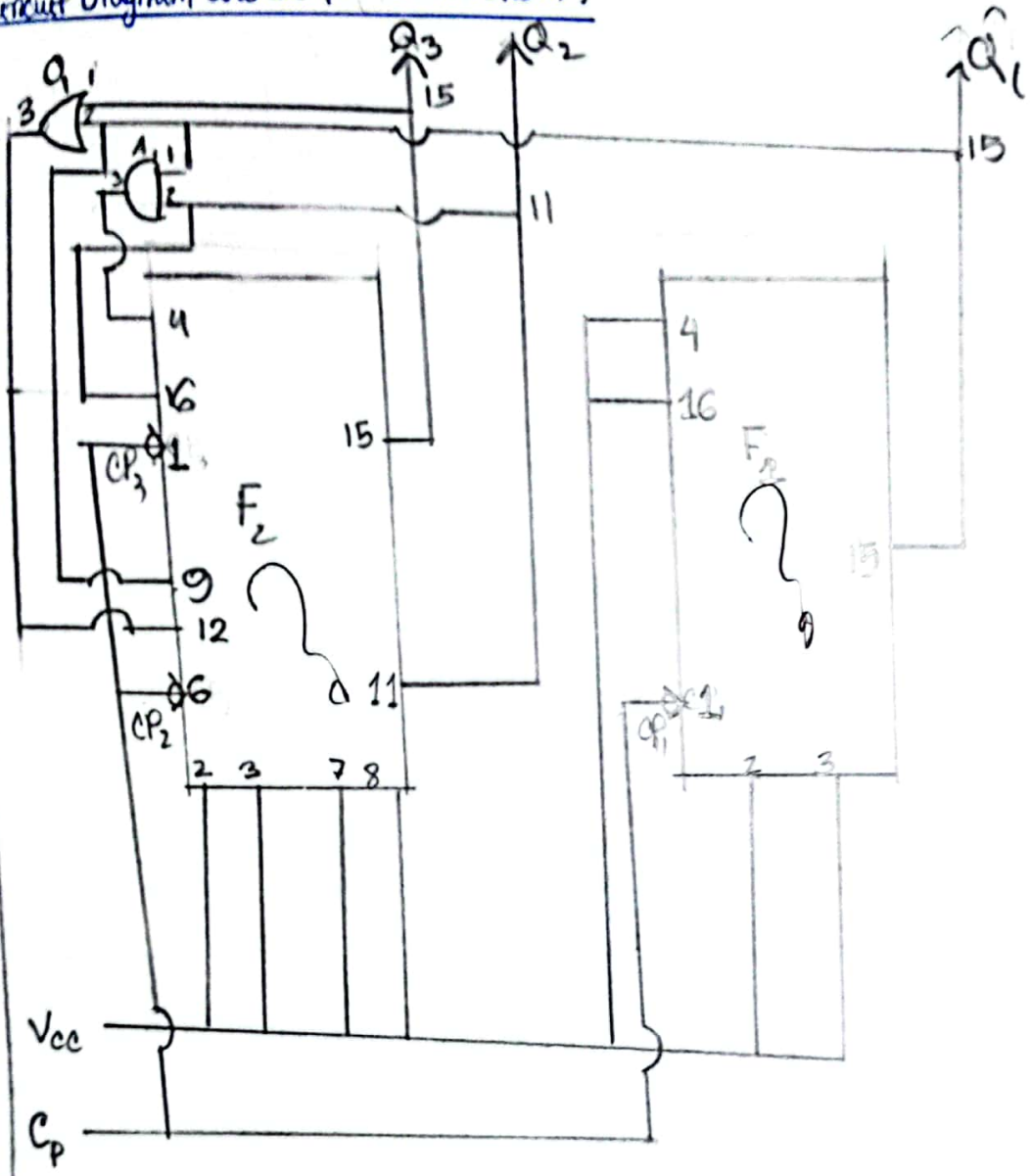
Required ICs:

i) A_1 — AND Gate (7408); Quantity: 1

ii) O_1 — OR Gate (7432); Quantity: 1

iii) F_1, F_2 — JK Flipflop (7476); Quantity: 2

Circuit Diagram and IC pin Connections:



Required ICs:

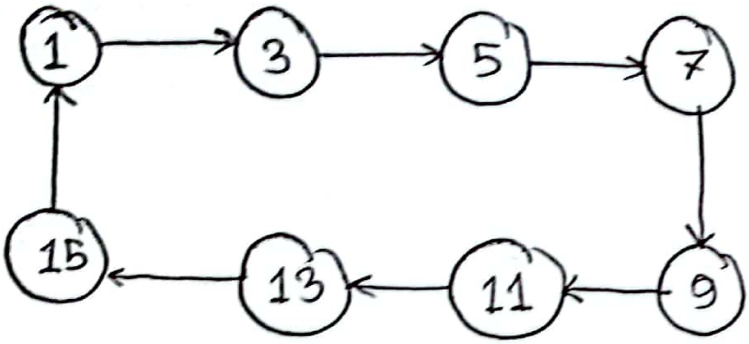
i) A_1 — AND Gate (7408); Quantity: 1

ii) O_1 — OR Gate (7432); Quantity: 1

iii) F_1, F_2 — JK Flipflop (7476); Quantity: 2

For (ii),

State Diagram:



State Table:

Present State				Next State			
Q_4	Q_3	Q_2	Q_1	G_4	Q_3	Q_2	G_1
0	0	0	1	0	0	1	1
0	0	1	1	0	1	0	1
0	1	0	1	0	1	1	1
0	1	1	1	1	0	0	1
1	0	0	1	1	0	1	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	1	0	0	0	1

∴ There will be 4 D Flip-Flops

and, $d = \Sigma(0, 2, 4, 6, 8, 10, 12, 14)$

Excitation Table:

Present State				Next State				Flip-Flops			
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	D_4	D_3	D_2	D_1
0	0	0	1	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	1	0	0	0	1

Function Simplification:

For D_4,

Q_4Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
$Q_4'Q_3'$	X			X
$Q_4'Q_3$	X		1	X
Q_4Q_3	X	1		X
Q_4Q_3'	X	1	1	X

$\therefore D_4 = Q_4Q_3' + Q_4Q_2' + Q_4'Q_3Q_2$

$= Q_4(Q_3' + Q_2') + Q_4'Q_3Q_2$; [Distributive Law]

For D_3,

Q_4Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
$Q_4'Q_3'$	X		1	X
$Q_4'Q_3$	X	1		X
Q_4Q_3	X	1		X
Q_4Q_3'	X		1	X

$\therefore D_3 = Q_3Q_2' + Q_3'Q_2$

$= Q_3 \oplus Q_2$

For D_2,

Q_4Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
$Q_4'Q_3'$	X	1		X
$Q_4'Q_3$	X	1		X
Q_4Q_3	X	1		X
Q_4Q_3'	X	1		X

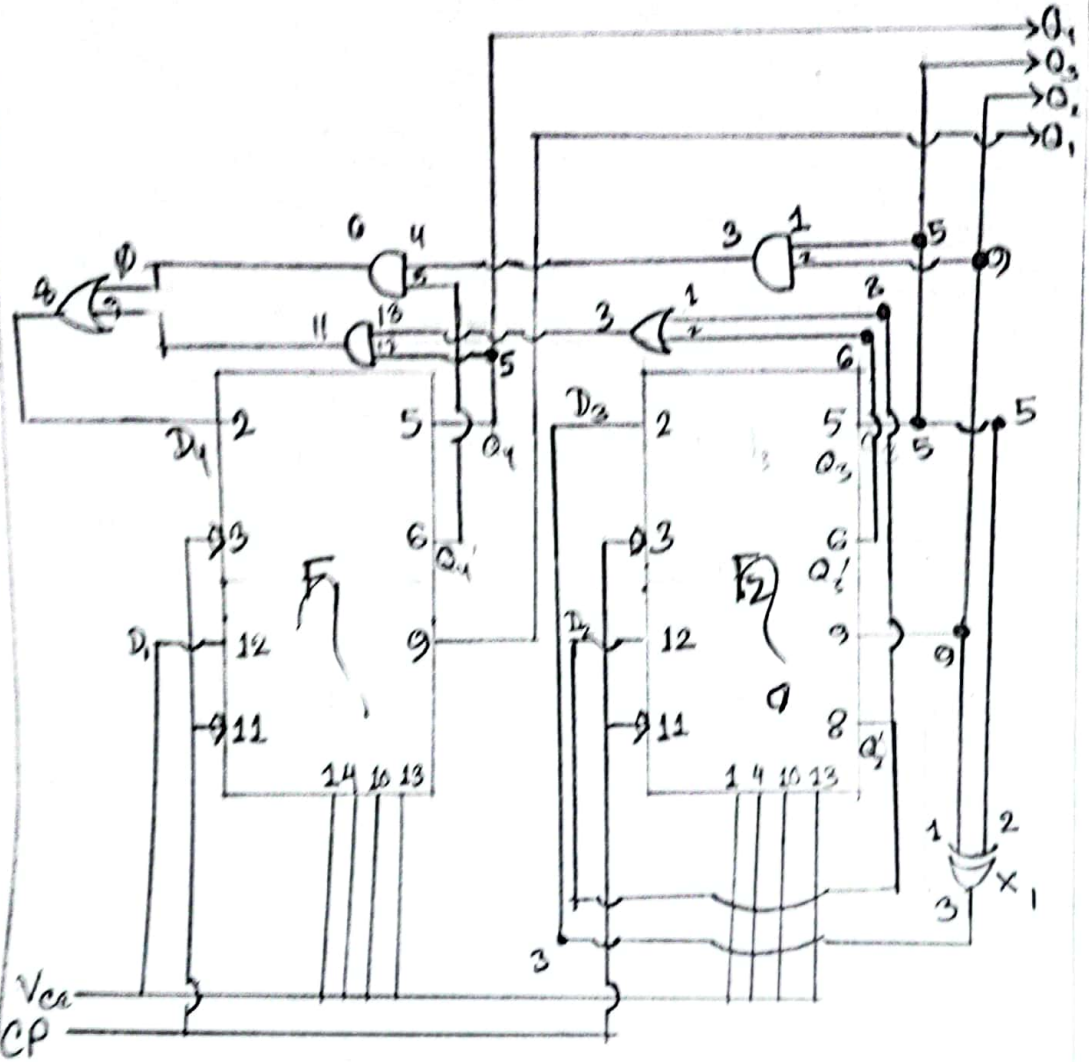
$\therefore D_2 = Q_2'$

For D_1 ;

Q_4Q_3 \ Q_2Q_1	$Q_2'Q_1'$	$Q_2'Q_1$	Q_2Q_1	Q_2Q_1'
$Q_4'Q_3'$	X	1	1	X
$Q_4'Q_3$	X	1	1	X
Q_4Q_3	X	1	1	X
Q_4Q_3'	X	1	1	X

$\therefore D_1 = 1$

Circuit Diagram and IC Pin Connections:



Required ICs:

i) A_1 — AND Gate (7404); Quantity: 1;

ii) O_1 — OR Gate (7432); Quantity: 1;

iii) X_1 — XOR Gate (7486); Quantity: 1;

iv) F_1, F_2 — D Flip-Flop (7474); Quantity: 2;

Discussion:

Through this experiment, we implemented two synchronous sequential circuits i.e. both circuits had the same clock pass. In the first experiment we implemented a random synchronous sequential clock counter using 3 JK flip-flops and in the second experiment we implemented an 4-bit odd counter using 4 D flip-flips.