Military Institute of Science and Technology
Department of Computer Science and Engineering
CSE-15, Level-3, Term-II
CSE-316 (Digital System Design Sessional)
Project-1

Problem:

Design a 4-bit combinational logic shifter having following operations. Consider S as output, F as input and H as selection variable.

H_2	H_1	H_0	Operation	Function
0	0	0	S ←F	Transfer
0	0	1	S ←F'	Complement transfer
0	1	0	S ←shr F	Logical shift right
0	1	1	S ←shl F	Logical shift left
1	0	0	S ← cshr F	Circular shift right
1	0	1	S ← cshl F	Circular shift left
1	1	0	S ← all 0's	Transfer 0's
1	1	1	S ← all 1's	Transfer 1's