Microprocessors

Section 2

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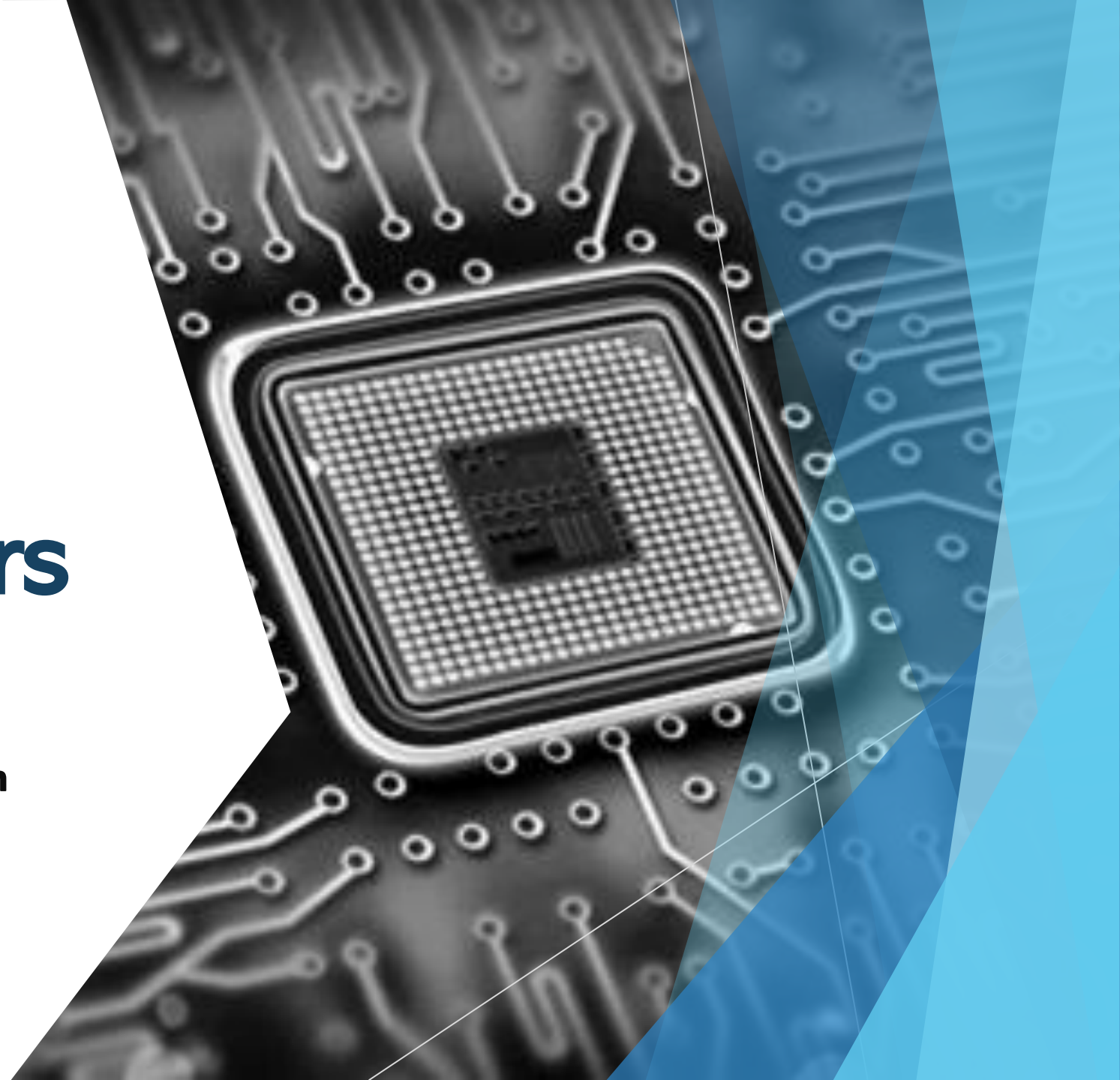
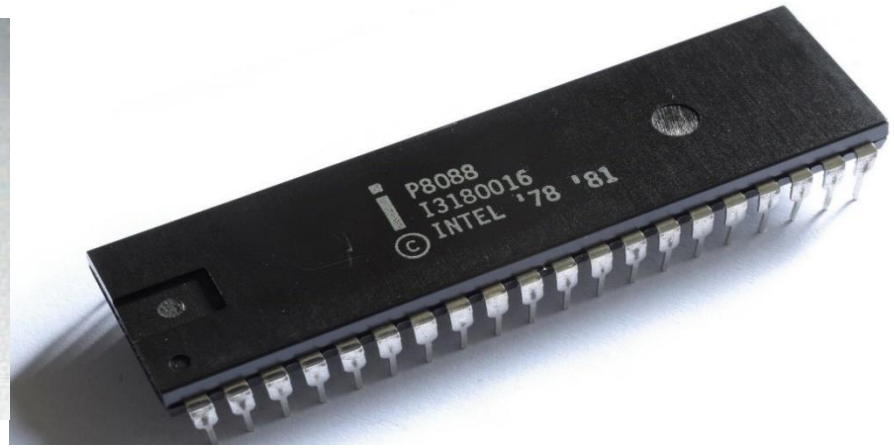


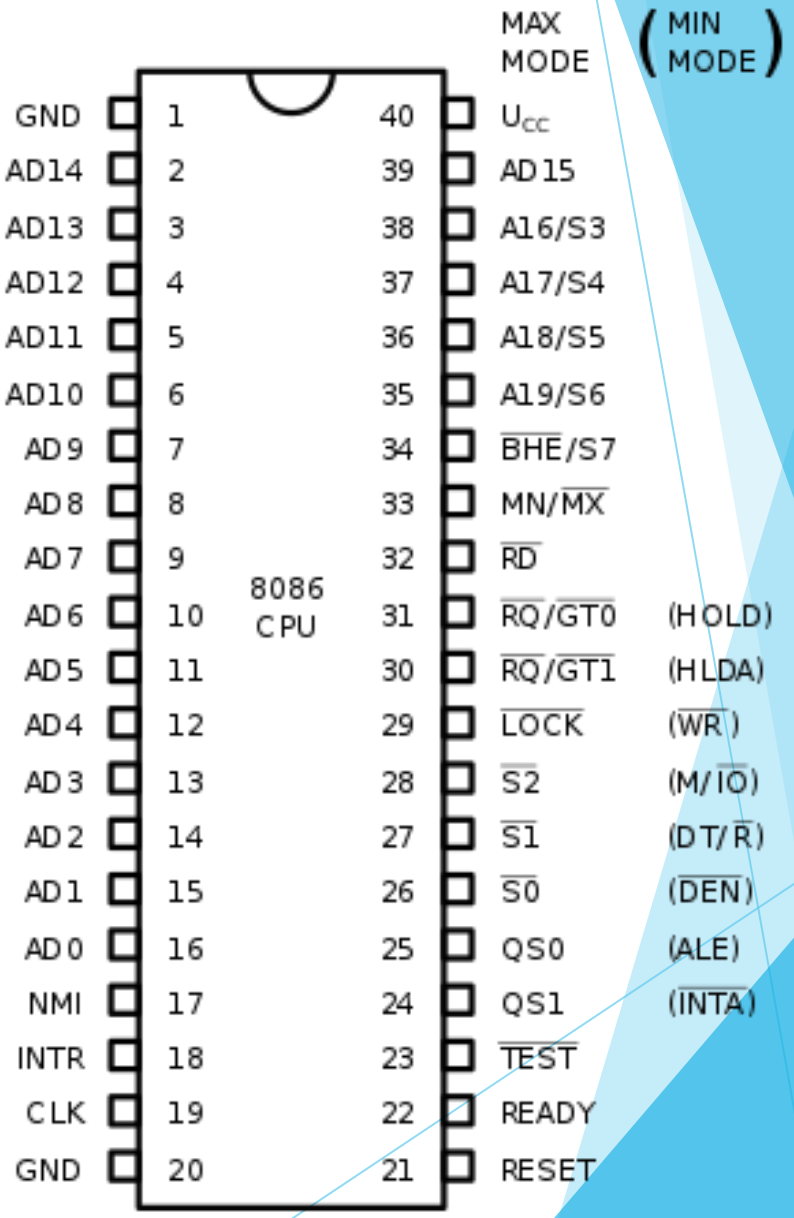
- There are two big microprocessors' families:
- Intel(80xxx), used in PCs, *like 8088,8086.*
- Motorola(68xxx) *like 6809,6800.*

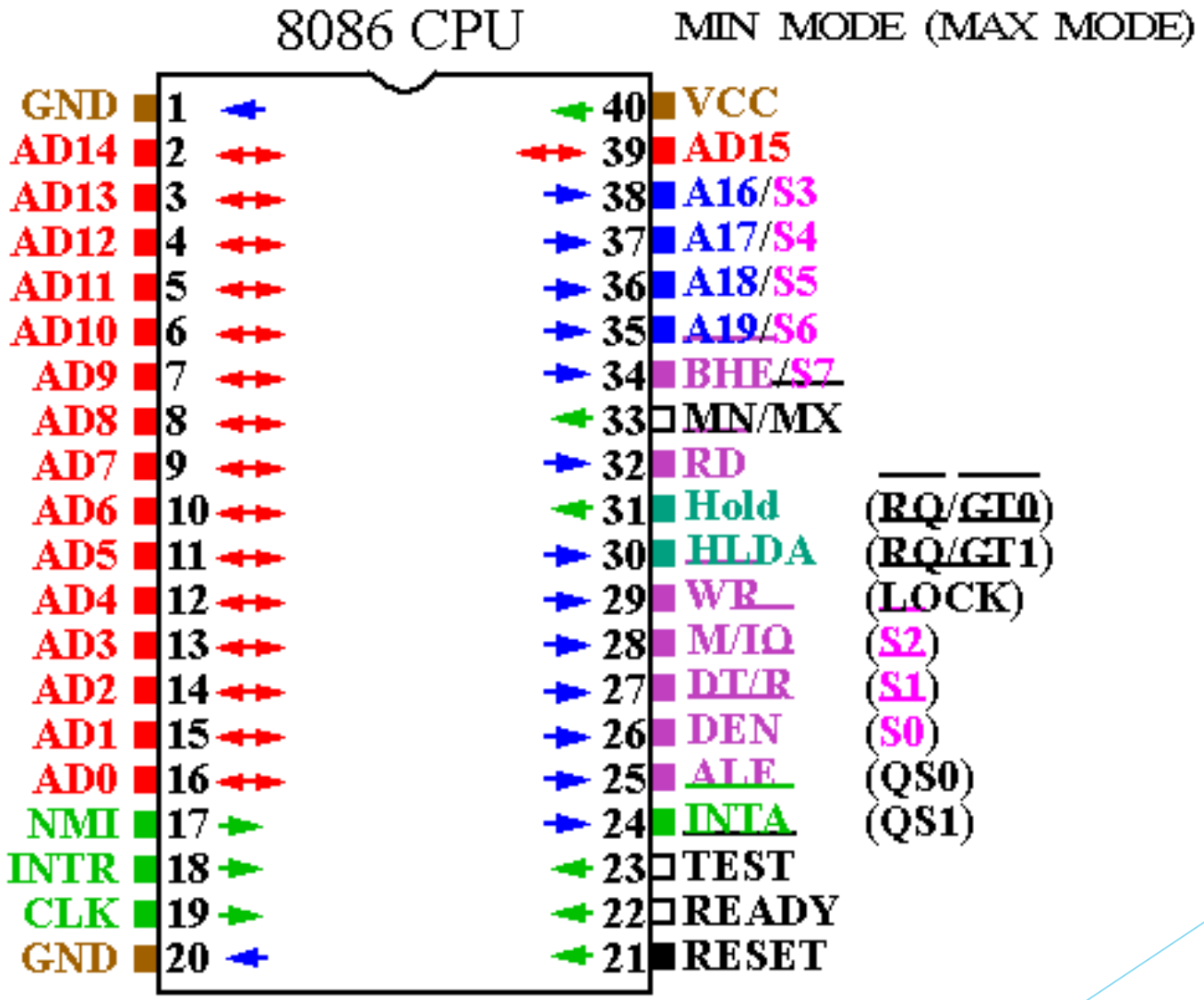


In this course, we will study the 8086 microprocessor.

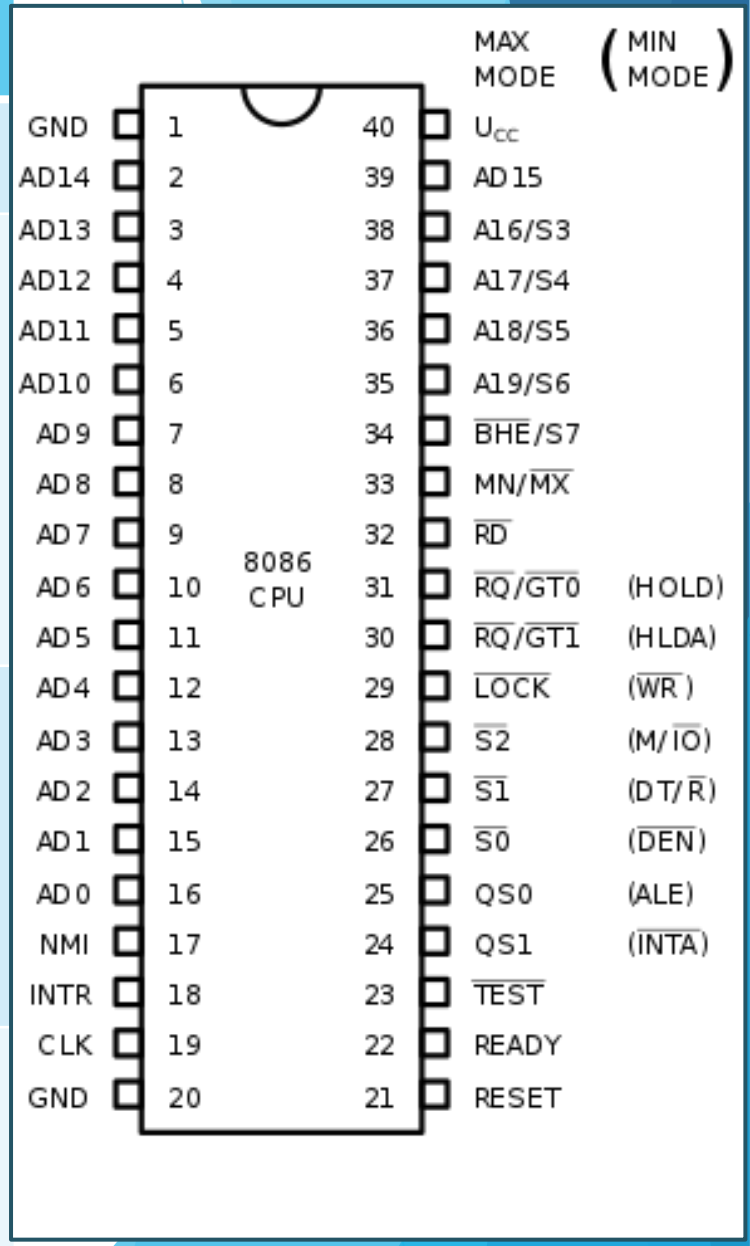
8086 Characteristics:

- 40 pins.
- 16-bit data bus.
- 1M byte memory.
- 20-bit address bus.



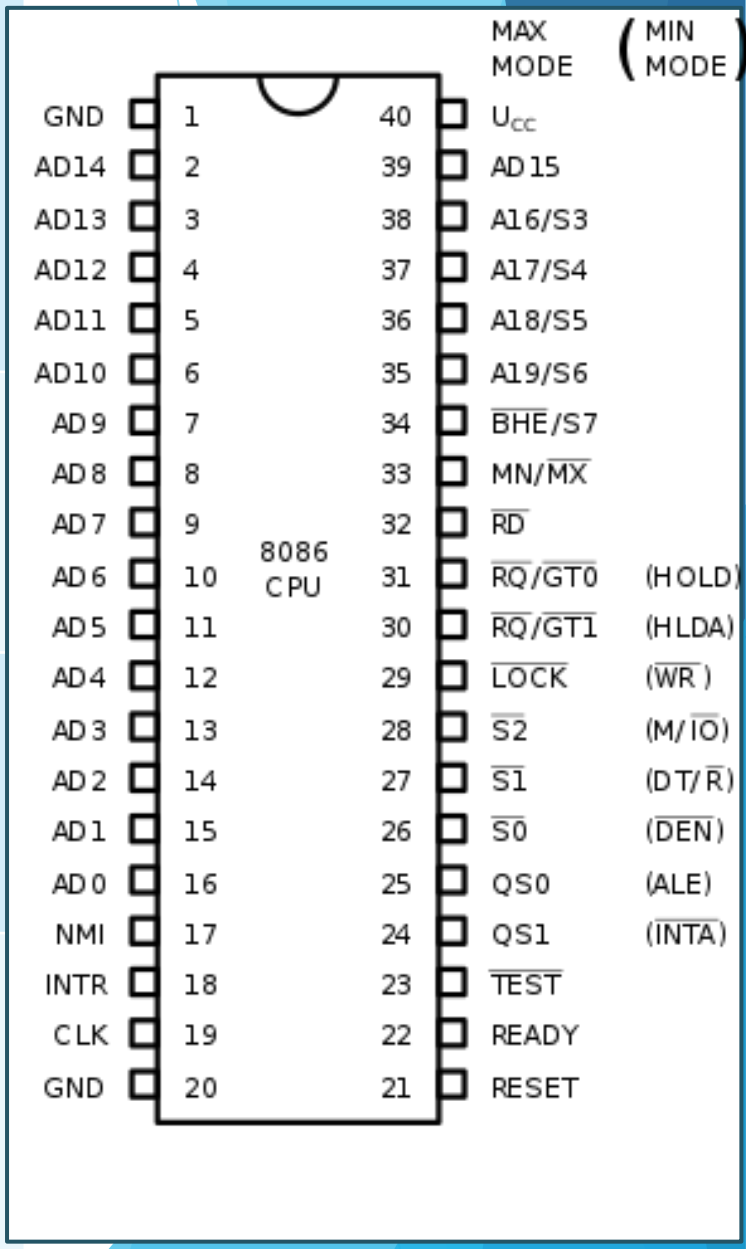

8086 CPU
MIN MODE (MAX MODE)
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 Hold (RQ/GT0)
30 HLDA (RQ/GT1)
29 WR (LOCK)
28 M/IO (S2)
27 DT/R (S1)
26 DEN (S0)
25 ALE (QS0)
24 INTA (QS1)
23 TEST
22 READY
21 RESET

Pin name	Pin function
VCC/GND	Power supply (5V) ➔ pin 40, and GND (0V) ➔ pin 1, 20.
AD15-AD0	Multiplexed address bus (ALE=1 [pin 25])/data bus(ALE=0). These are 16 address/data bus. AD0-AD7 carries low-order byte data and AD8-AD15 carries higher-order byte data. During the first clock cycle, it carries a 16-bit address; after that, it carries 16-bit data.
A19/S6-A16/S3	Multiplexed High order 4 bits of the 20-bit address/status bits S6-S3. Status bit S6 is always a logic 0, S5 indicates the condition of the IF flag bit, and S4 and S3 show which segment is accessed during the current bus cycle.
CLK	It provides timing to the processor for operations. Its frequency is different for different versions, i.e., 5 MHz, 8 MHz, and 10 MHz.

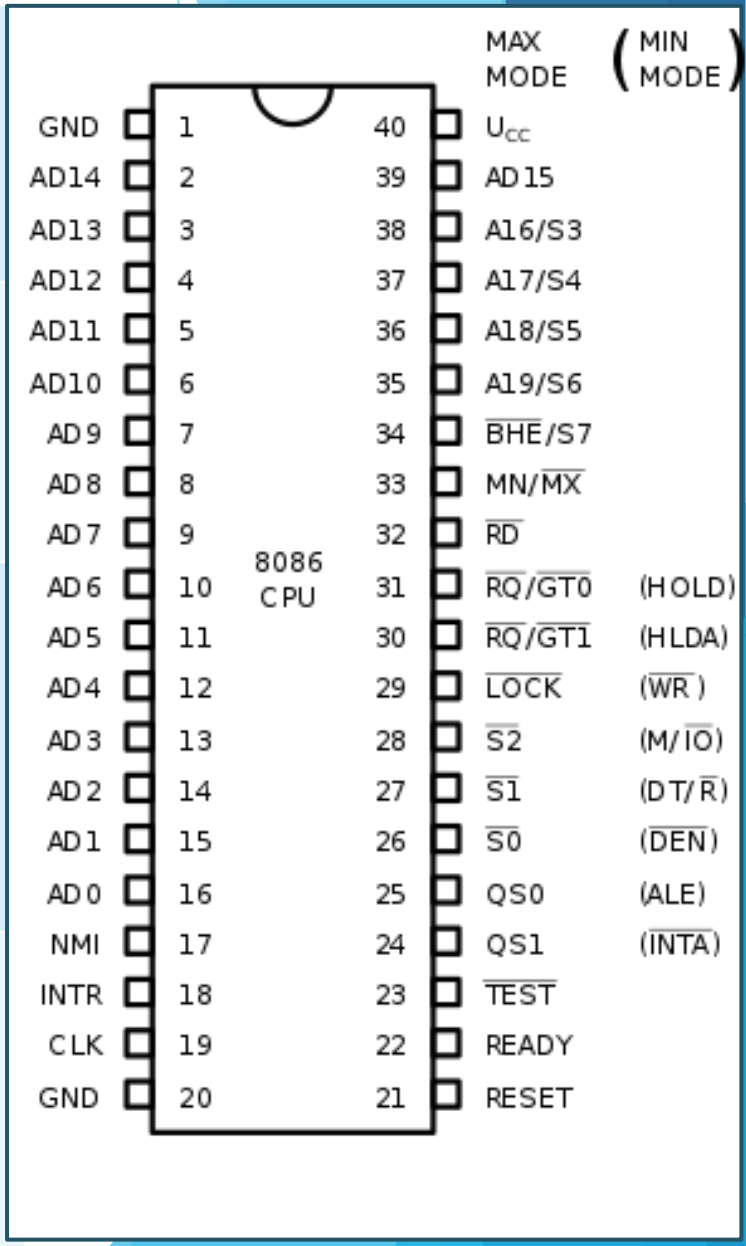


S_4	S_3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

Pin name	Pin function
INTR	The interrupt request is used to request a hardware interrupt. If INTR is held high when IF = 1, the microprocessor enters an interrupt acknowledge cycle after the current instruction has completed execution.
NMI	The non-maskable interrupt input is like INTR except that the NMI interrupt does not check to see whether the IF flag bit is a logic 1.
RESET	The microprocessor resets if this pin is held high for 4 clock periods. Instruction execution begins at FFFF0H. Also, the IF flag is cleared.
READY	**READY** input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the microprocessor enters wait states and remains idle.

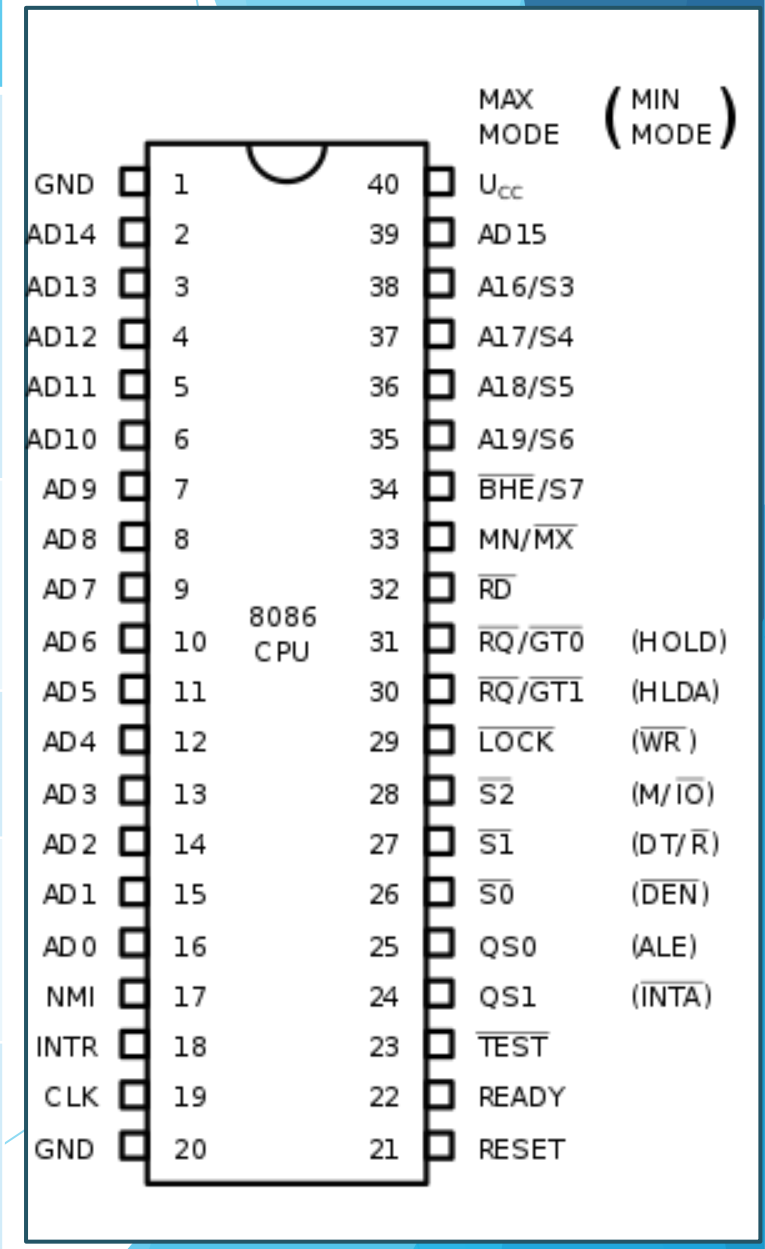


Pin name	Pin function
TEST'	Test pin is an input that is tested by the WAIT instruction. If is a logic 0, the WAIT instruction functions as an NOP. If is a logic 1, the WAIT instruction waits for it to become a logic 0.
Read(RD')	It is available at pin 32 and is used to read signals for Read operation. When RD= 0, the data bus is driven by memory or an I/O device.
MN/MX'	It stands for Minimum/Maximum. It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode. While it is low, the microprocessor works in the maximum mode
BHE'	The bus high enable pin is used in the 8086 to enable the most-significant data bus bits (D15–D8) during a read or a write operation. The state of S7 is always a logic 1



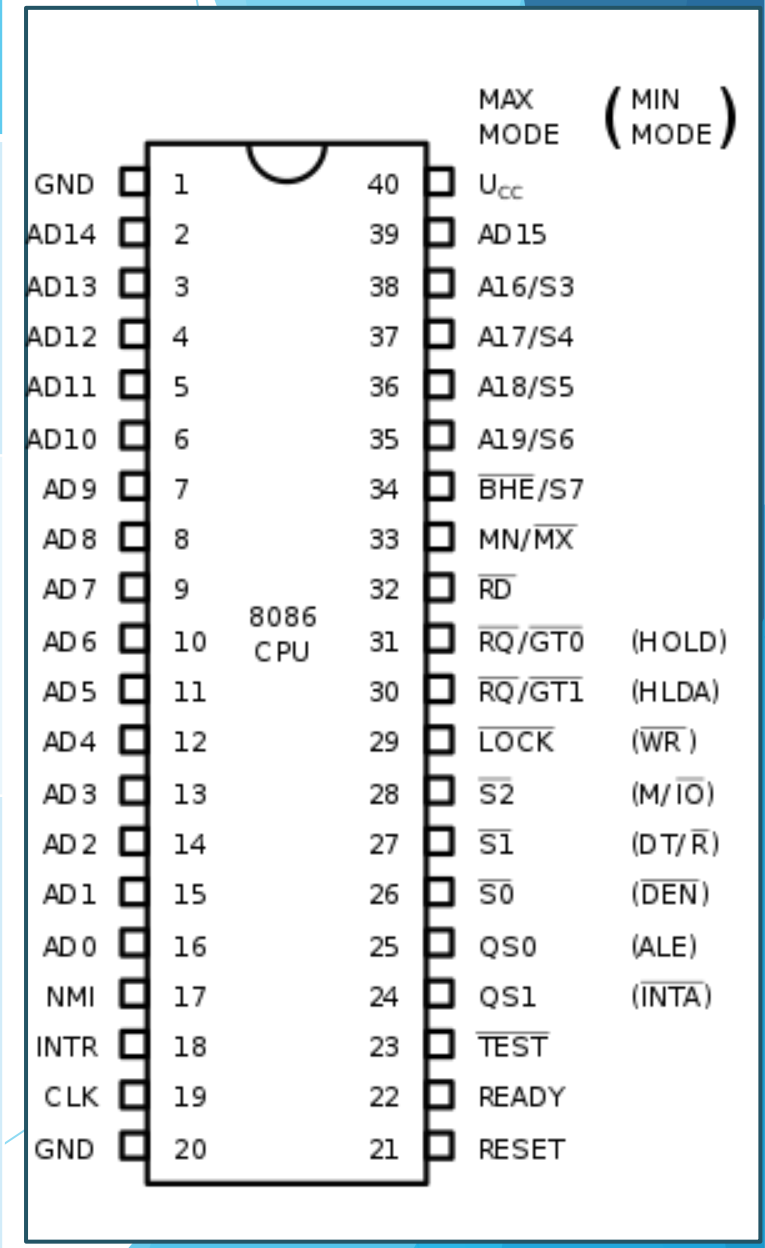
Minimum Mode Pins

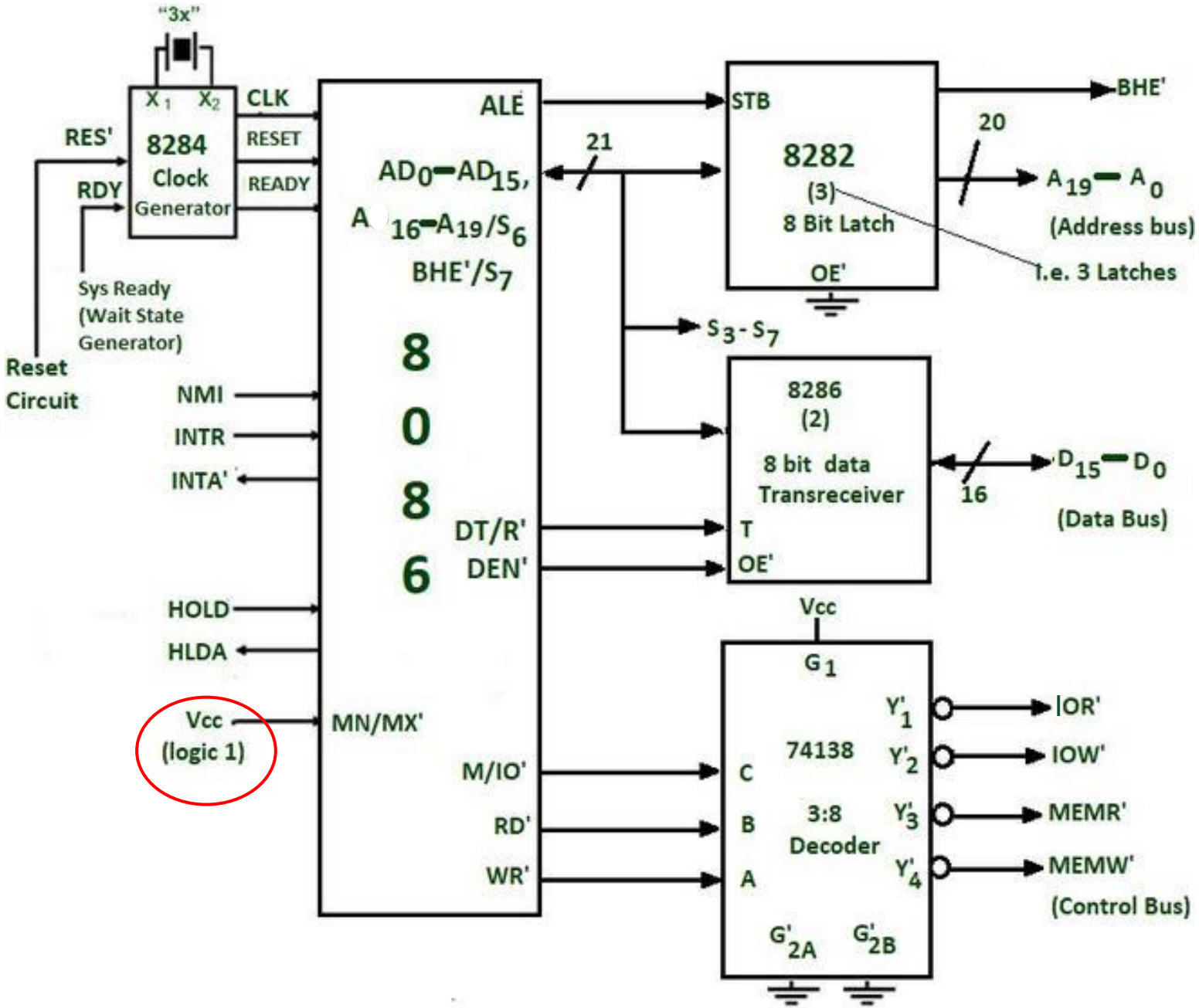
Pin	Function
INTA’	The interrupt acknowledgment signal is a response to INTR pin and is generated by the microprocessor. If an interrupt request is received at INTR, then the acknowledgment for it is sent through this pin. It causes the interrupt vector to be put auto data bus.
ALE	Address latch enable, if ALE=1 address/data bus (AD0-AD15) contains the memory address or I/O port number, else it will carry data.
DEN’	Data enable, activates the external data bus buffer. It is an active low signal.
DT/R’	Data transmission/receive, the microprocessor transfers the data when the pin is at 1, and at 0, it receives data.
M/IO’	This pin selects memory or I/O. This pin indicates that the microprocessor address bus contains either a memory address or an I/O port address.



Minimum Mode Pins

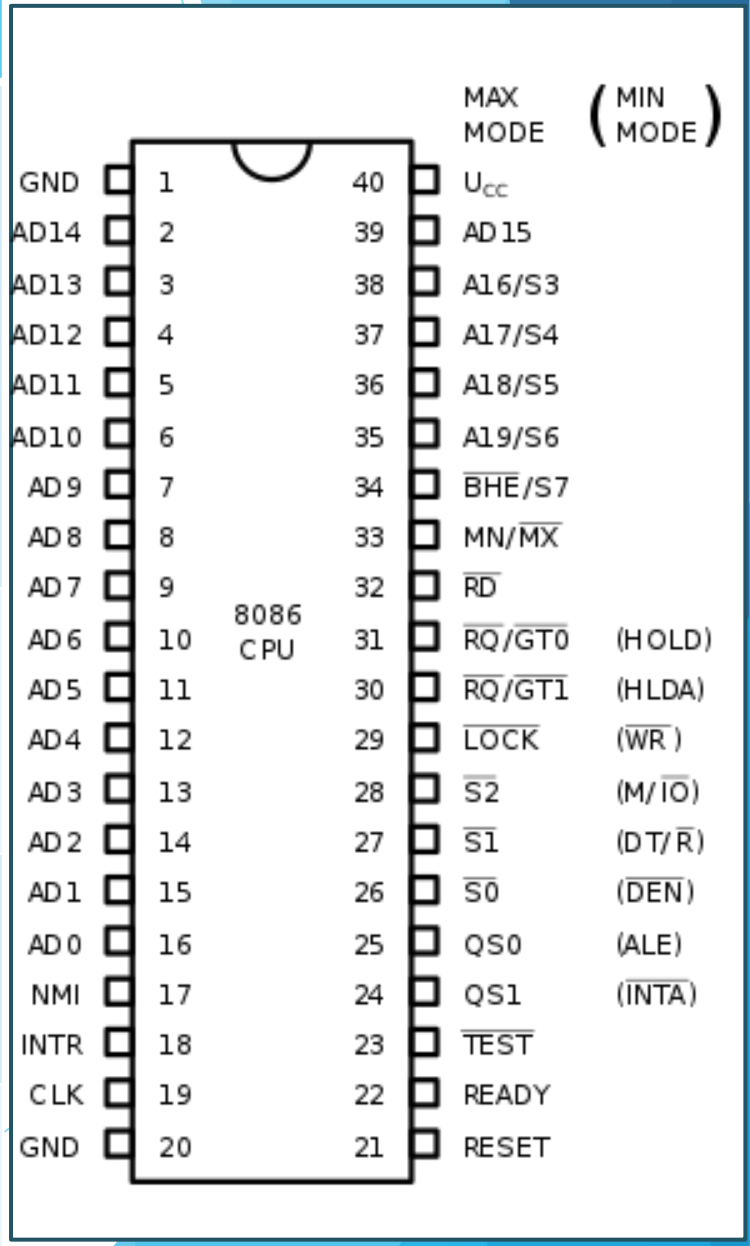
Pin	Function
WR’	This signal is used for writing purposes. It is an active low signal. This signal indicates transmitting data to memory or IO devices.
HLDA	Hold acknowledgment indicates that the 8086/8088 has entered the hold state.
HOLD	The hold input requests a direct memory access (DMA). If the HOLD signal is a logic 1, the microprocessor stops executing software and places its address, data, and control bus at the high-impedance state. If the HOLD pin is a logic 0, the microprocessor executes software normally




"3x"
X1
X2
8284
Clock
Generator
CLK
RESET
READY
RES'
RDY
Sys Ready
(Wait State
Generator)
Reset
Circuit
ALE
AD0–AD15,
A16–A19/S6
BHE'/S7
8
0
8
6
NMI
INTR
INTA'
HOLD
HLDA
Vcc
(logic 1)
MN/MX'
DT/R'
DEN'
M/IO'
RD'
WR'
21
STB
8282
(3)
8 Bit Latch
OE'
BHE'
20
A19 – A0
(Address bus)
i.e. 3 Latches
S3 - S7
8286
(2)
8 bit data
Transreceiver
T
OE'
16
D15 – D0
(Data Bus)
Vcc
G1
74138
3:8
Decoder
C
B
A
G'2A
G'2B
Y'1
Y'2
Y'3
Y'4
IOR'
IOW'
MEMR'
MEMW'
(Control Bus)

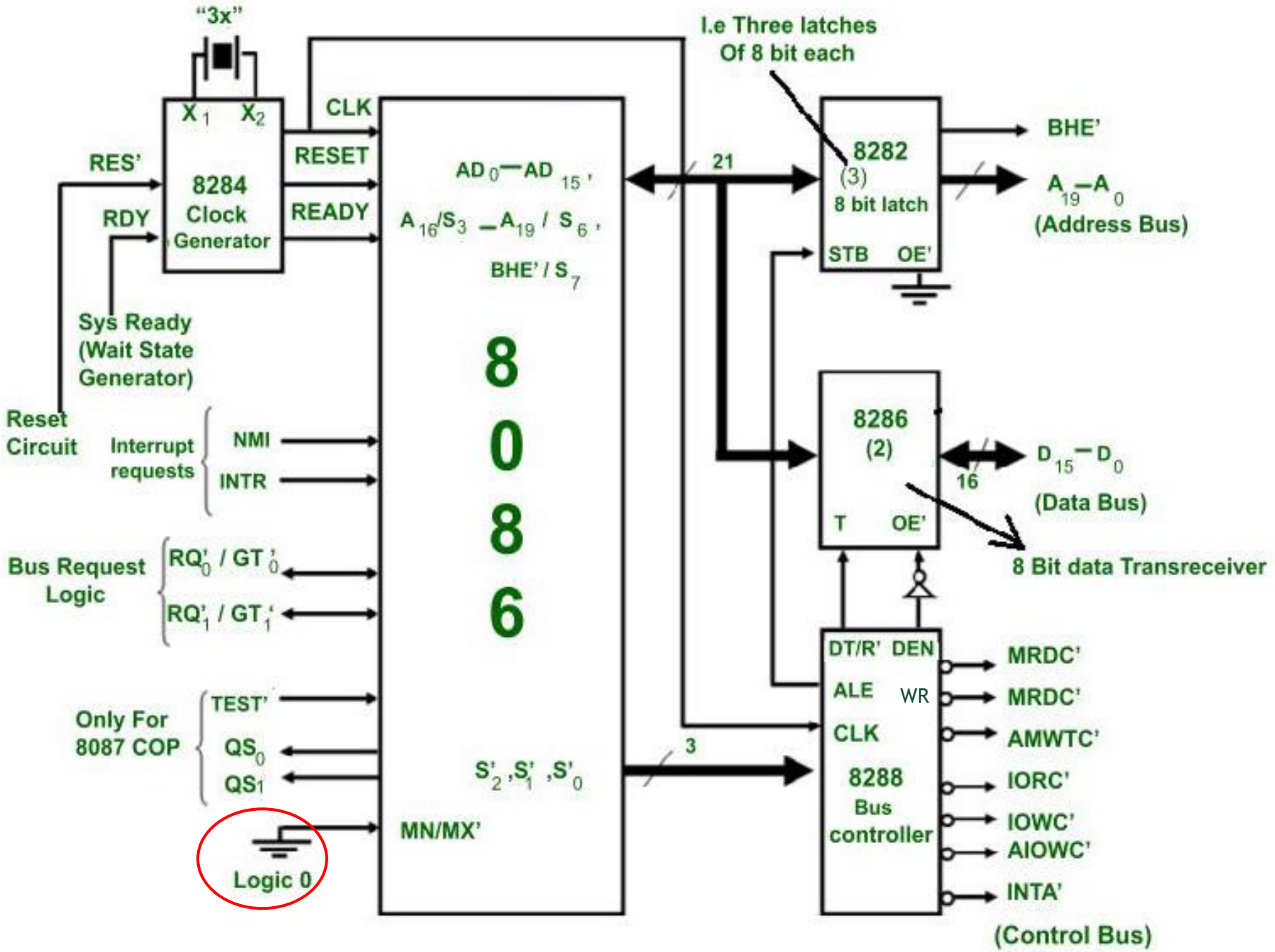
Maximum Mode Pins

Pin	Function
RQ'/GT0'and RQ'/GT1'	These two pins are used for bus requests and grant purposes. Through these pins, a connection is established between the DMA and the 8086 microprocessor. These lines are bidirectional and are used to both request and grant a DMA operation.
LOCK'	The **lock** output is used to lock peripherals off the system.
S0,S1, S2	Status bits, the different values of these pins are taken together to indicate the function of the current bus cycle.
QS0, QS1	The queue status bits show the status of the internal instruction queue.



S2	S1	S0	Function
0	0	0	INTA’
0	0	1	IO read
0	1	0	IO write
0	1	1	halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	passive

QS1	QS0	Function
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode


"3x"
X1
X2
8284
Clock
Generator
RES'
RDY
Sys Ready
(Wait State
Generator)
Reset
Circuit
CLK
RESET
READY
AD0—AD15 ,
A16/S3 —A19 / S6 ,
BHE' / S7
8
0
8
6
Interrupt
requests
NMI
INTR
Bus Request
Logic
RQ'0 / GT'0
RQ'1 / GT'1
Only For
8087 COP
TEST'
QS0
QS1
Logic 0
MN/MX'
S'2 ,S'1 ,S'0
3
I.e Three latches
Of 8 bit each
21
8282
(3)
8 bit latch
STB
OE'
BHE'
A19—A0
(Address Bus)
8286
(2)
T
OE'
16
D15—D0
(Data Bus)
8 Bit data Transreceiver
DT/R'
DEN
ALE
WR
CLK
8288
Bus
controller
MRDC'
MRDC'
AMWTC'
IORC'
IOWC'
AIOWC'
INTA'
(Control Bus)

Minimum mode	Maximum mode
In minimum mode there can be only one processor i.e. 8086.	In maximum mode there can be multiple processors with 8086, like 8087 and 8089.
$MN/\overline{MX}$ is 1 to indicate minimum mode.	$MN/\overline{MX}$ is 0 to indicate maximum mode.
ALE for the latch is given by 8086 as it is the only processor in the circuit.	ALE for the latch is given by 8288 bus controller as there can be multiple processors in the circuit.
$\overline{DEN}$ and $DT/\overline{R}$ for the trans-receivers are given by 8086 itself.	and$DT/\overline{R}$ for the trans-receivers are given by 8288 bus controller.
Direct control signals $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ are given by 8086.	Instead of control signals, each processor generates status signals called $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$.
Control signals $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ are decoded by a 3:8 decoder like 74138.	Status signals $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ are decoded by a bus controller like 8288 to produce control signals.
$\overline{INTA}$ is given by 8086 in response to an interrupt on INTR line.	$\overline{INTA}$ is given by 8288 bus controller in response to an interrupt on INTR line.
HOLD and HLDA signals are used for bus request with a DMA controller like 8237.	$\overline{RQ}/\overline{GT}$,lines are used for bus requests by other processors like 8087 or 8089.
The circuit is simpler.	The circuit is more complex.
Multiprocessing cannot be performed hence performance is lower.	As multiprocessing can be performed, it can give very high performance.