Student Names: Metin Dumandağ, Fatih İver
Section: 1
Group ID: 16

CMPE 240 Experiment 3 Preliminary Work

Truth Table:

#	Y1	Y0	X2	X1	X0	Z
0	0	0	0	0	0	0
1	0	0	0	0	1	0
2	0	0	0	1	0	1
3	0	0	0	1	1	1
4	0	0	1	0	0	0
5	0	0	1	0	1	1
6	0	0	1	1	0	0
7	0	0	1	1	1	1
8	0	1	0	0	0	0
9	0	1	0	0	1	1
10	0	1	0	1	0	0
11	0	1	0	1	1	1
12	0	1	1	0	0	0
13	0	1	1	0	1	1
14	0	1	1	1	0	0
15	0	1	1	1	1	1
16	1	0	0	0	0	1
17	1	0	0	0	1	1
18	1	0	0	1	0	1
19	1	0	0	1	1	1
20	1	0	1	0	0	0
21	1	0	1	0	1	1
22	1	0	1	1	0	0
23	1	0	1	1	1	0
24	1	1	0	0	0	1
25	1	1	0	0	1	1
26	1	1	0	1	0	0
27	1	1	0	1	1	0
28	1	1	1	0	0	1

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29	1	1	1	0	1	0
30	1	1	1	1	0	0
31	1	1	1	1	1	0

List of components used in the design:

1. 8-WAY MUX

2. 1 OR

3. 1 NAND

4. 3 NOT

Circuit: