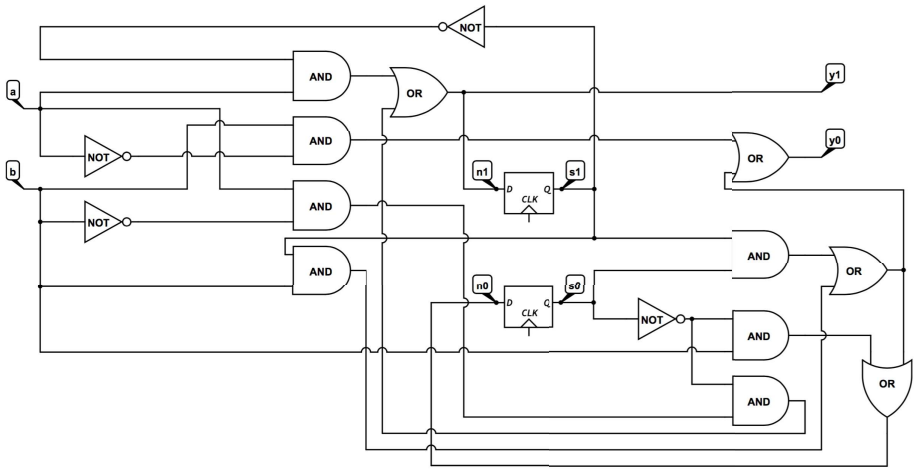
6.5 Experiment 5 (Analysis of a Sequential Circuit)

6.5.1 Aim

In this experiment, your will analyze a given sequential circuit.

6.5.2 Problem

In the circuit below, the initial state is $s_1 = 0, s_0 = 0$. a and b are inputs. y_1 and y_0 are outputs. Reset is synchronous.



6.5.3 Preliminary Work

1. State the inputs and outputs of the state registers.
2. State the inputs and outputs of the combinational block of the sequential circuit.
3. Draw the truth table for the combinational circuit.
4. Draw the finite state machine by using the table obtained in previous step.
5. Is this a Moore or Mealy Machine? (No explanation, only short answer)
6. Write the testbench and the **behavioral level** verilog code for the corresponding finite state machine.

6.5.4 Lab Work

1. Demonstrate your testbench for the preliminary work.
2. A new sequential system will be given. You are required to follow the same steps with the preliminary work for the new sequential circuit.