ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	2
EXPERIMENT DATE	:	22.02.2019
LAB SESSION	:	FRIDAY - 14.00
GROUP NO	:	G13

GROUP MEMBERS:

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

SPRING 2019

ETHIC FORM
for
BLG242E Logic Circuits Laboratory

As a student of

Istanbul Technical University Faculty of Computer and Informatics Engineering;

1. I will not attempt to cheat in quizes and final exam,
2. I will not use disallowed sources or tools (mobile phone, calculator etc.) during the exam,
3. I will not write any information (formula, text, figure etc.) on the table, sheets or books that are allowed to be used during the exam,
4. I will give reference when using printed or online published sources,
5. I will not use the results in a source as they are, or by changing a part of them without giving a reference,
6. I will not show unused sources as used,
7. I will not present someone elses idea as my own idea,
8. I will not make someone do my homework, project or thesis for money or anything else,
9. I will not take an exam or enter a lecture on behalf of others,
10. I will not make excuses for not attending in exams or lessons by taking reports from someone I know (medical doctor parents or relatives),
11. I will refrain from deliberately harming the public materials at our university,
12. I will comply with the safety rules in laboratory work,
13. I will behave in accordance with the rules of respect for the lecturers and teaching assistants

signed by

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

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1 INTRODUCTION

In this experiment we created truth tables for given functions then we implemented each and every function. We have compared our expected results to the outputs of the circuits we have built in order to prove given theorems or check our calculations.

2 REQUIREMENTS

Tools Used[1]

- C.A.D.E.T
- 74000 series ICs
  - 74x$x^1$04 - Hex Inverter
  - 74x$x^1$08 - Quadruple 2-input Positive AND Gates
  - 74x$x^1$32 - Quadruple 2-input Positive OR Gates

2.1 PART 1

In the first part of the experiment, the logic circuits are designed and implemented for the given expressions below.

- F_1(a,b) = a + $a \cdot b$
- F_2(a,b) = $(a + b) \cdot (a + b')$

First of all, truth tables are created for these expressions.

a	b	$a \cdot b$	a + $a \cdot b$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Table 1: Truth table of F_1

a	b	b’	a + b	a + b’	$(a+b)\cdot(a+b')$
0	0	1	0	1	0
0	1	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1

Table 2: Truth table of F_2

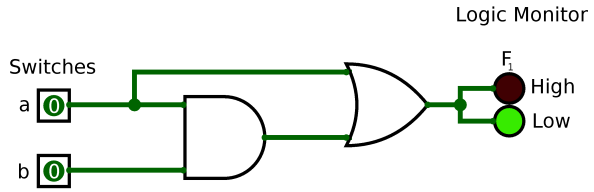

Figure 1: Circuit of F_1

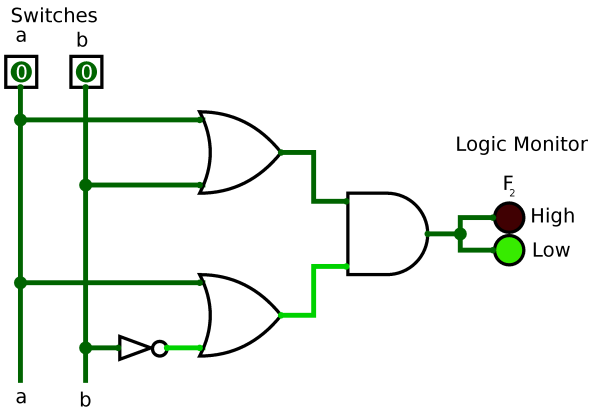

Figure 2: Circuit of F_2

In this part, hex inverter is used to invert the input value. 74xx108 AND gate and 74xx132 OR gate are used to implement necessary logic operations. The Vcc voltage is applied to the pins at the top right corner of each integrated circuit and the ground voltage is applied to the pins at the lower left corner of each integrated circuit.

To implement the first expression, the first input on the logic monitor(logic switches) is connected to the first pin on the left of the integrated circuit for OR operation. The first and second inputs on the logic monitor(logic switches) are connected to the first and second pin on the left of the integrated circuit for AND operation. The third pin on

the left of integrated circuit for and operation, output value of AND operation, is connected to the second pin on the left of the integrated circuit for OR operation. The third pin on the left of the integrated circuit for OR operation is connected to the one of the pins on the logic monitor to observe output value.

For the second expression, the first input on the logic monitor(logic switches) is connected to the the first and fourth pin on the left of the integrated circuit for OR operation. The second input on the logic monitor is connected to the first pin on the left of the hex inverter and the second pin on the left of the integrated circuit for OR operation. The second pin on the left of hex inverter, output value of inverting operation, is connected to the fifth pin on the left of the integrated circuit for OR operation. The third and sixth pin on the left of the integrated circuit for OR operation is connected to the first and second pin on the left of the integrated circuit for AND operation. The third pin on the left of the integrated circuit for AND operation, output value of AND operation, is connected to the one of the pins on the logic monitor and output values are obs.rved e

2.2 PART 2

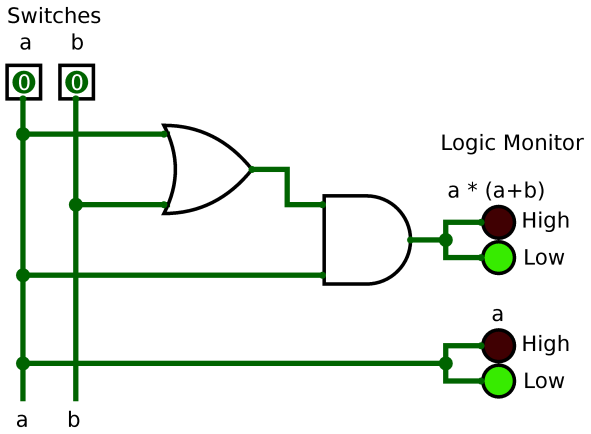

Figure 3: Circuit of Part 2

In the second part of the experiment, the logic circuit are designed and implemented for the dual of the expression below. At the end of the experiment it was shown that the expression's equal and its dual were equal.

- a $+ a \cdot b =$ a

To find dual of the boolean expressions, AND's replace with OR's and OR's replace with AND's. Dual of the expression a + $a \cdot b$ = a is shown below.

- $a \cdot (a + b)$ = a

a	b	b'	a + b	a + b'	$(a + b) \cdot (a + b')$
0	0	1	0	1	0
0	1	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1

Table 3: Truth table of Part 2

In this part, 74xx108 AND gate and 74xx132 OR gate are used to implement necessary logic operations. The Vcc voltage is applied to the pins at the top right corner of each of the integrated circuits and the ground voltage is applied to the pins at the lower left corner.

To implement the dual of the expression, the first input on the logic monitor(logic switches) connected to the first pin on the left of the integrated circuit for AND operation and the first pin on the left of the integrated circuit for OR operation. The second input of the logic monitor(logic switches) is connected to the second pin on the left of the logic monitor for OR operation. The third pin on the left of the integrated circuit for OR operation, output value of OR operation, is connected to the second pin on the left of the integrated circuit for AND operation. The third pin on the left of the integrated circuit for AND operation is connected to the one of the pins on the logic monitor and outpu tavule aesobserv d.re

When the table is examined, it can be seen that output value for the dual of the expression is equal to the output value of the expression itself.

2.3 PART 3

In the third part of the experiment, the logic circuit are designed and implemented for the complement of the expression below. Then, truth table is found for the expression. At the end of this part it was validated that output values of the complementary function on the logic monitor is consistent with output values on the truth table.

- F_3(a,b,c) = $(a \cdot b)$ + $(a' \cdot b)$

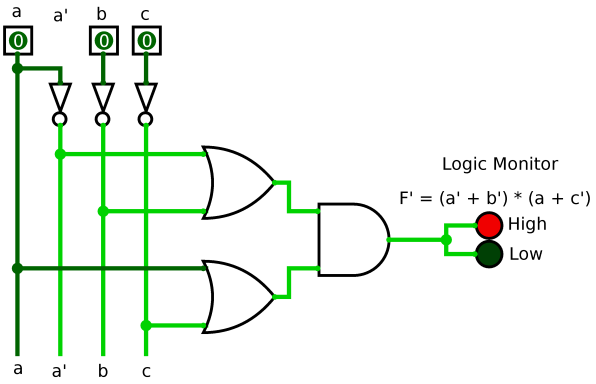

Figure 4: Circuit for complement of F3

To find the complement of any given boolean expressions AND's are replaced with OR's and OR's are replaced with AND's. Also, input variables are replaced with inverses of those variables. This way, complement of the expression above is found as the expression below.

- $F'_3(a,b,c) = (a' + b') \cdot (a + c')$

a	b	c	a'	$a \cdot b$	$a' \cdot c$	$F_3 = a \cdot b + a' \cdot c$	F'_3
0	0	0	1	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	1	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	0	1
1	1	0	0	1	0	1	0
1	1	1	0	1	0	1	0

Table 4: Truth table for F3 and it's complement

In this part, hex inverter is used to invert the input value. 74xx108 AND gate and 74xx132 OR gate are used to implement necessary logic operations. The Vcc voltage is applied to the pins at the top right corner of each of the integrated circuits and the ground voltage is applied to the pins at the lower left corner.

To implement complement of the expression, the first input on the logic monitor(logic switch) is connected to the first pin on the left of the hex inverter and the fourth pin on the left of the integrated circuit for OR operation. The second pin on the left of the hex

inverter is connected to the first pin on the left of the integrated circuit for OR operation. The second input on the logic monitor(logic switches) is connected to the third pin on the left of the hex inverter. The fourth pin on the left of the hex inverter is connected to the second pin of the integrated circuit for OR operation. The third input on the logic monitor is connected to the fifth pin on the left of the hex inverter. The sixth pin on the left of the hex inverter is connected to the fifth pin on the left of the integrated circuit for OR operation. The third and sixth pin on the left of the integrated circuit for OR operation are connected to the first and second pin on the left of the integrated circuit for AND operation. The third pin on the left of the integrated circuit for AND operation is connected to the one of the pins on the logic monitor to observe output value.

When the table is examined, it can be seen that output values of the expression on the truth table is consistent with output values on the logic monitor.

2.4 PART 4

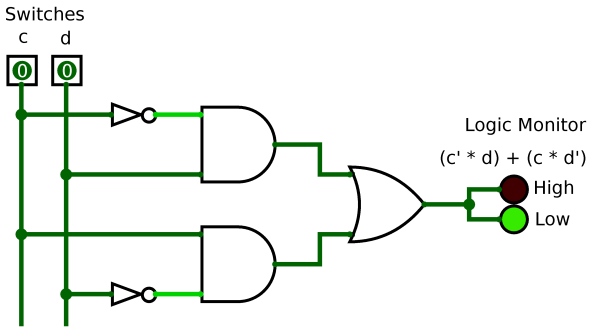

Figure 5: Circuit of F_4

In the final part of the experiment, the logic circuit are designed and implemented for the basic logical expression below.

- F_4(a,b,c,d) = U_1(1,2,5,6,9,10,13,14)

If we write the minterms of of given function F_4 we obtain the first canonical form of F_4

- $F_4(a, b, c, d) =$
  $(a'b'c'd) + (a'b'cd') + (a'bc'd) + (a'bcd') + (ab'c'd) + (ab'cd') + (abc'd) + (abc'd)$

a	b	c	d	c'	d'	$c' \cdot d$	$c \cdot d'$	$F_4 = c' \cdot d + c \cdot d'$
0	0	0	0	1	1	0	0	0
0	0	0	1	1	0	1	0	1
0	0	1	0	0	1	0	1	1
0	0	1	1	0	0	0	0	0
0	1	0	0	1	1	0	0	0
0	1	0	1	1	0	1	0	1
0	1	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	0
1	0	0	0	1	1	0	0	0
1	0	0	1	1	0	1	0	1
1	0	1	0	0	1	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	1	1	0	0	0
1	1	0	1	1	0	1	0	1
1	1	1	0	0	1	0	1	1
1	1	1	1	0	0	0	0	0

Table 5: Thruth table for F4

To find simplified expression the axioms and theorems of Boolean algebra are used.

$$
\begin{aligned}
F_4(a,b,c,d) &= (a'b'c'd) + (a'b'cd') + (a'bc'd) + (a'bcd') + (ab'c'd) + (ab'cd') + (abc'd) + (abc'd) \\
&= (ab'c'd) + (abc'd) + (a'b'cd') + (a'bcd') + (a'b'c'd) + (a'bc'd) + (ab'cd') + (abcd') \\
& \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \text{(Commutativity)} \\
&= ac'd(b'+b) + a'cd'(b'+b) + a'c'd(b'+b) + acd'(b'+b) \qquad \text{(Distribution)} \\
&= ac'd(1) + a'cd'(1) + a'c'd(1) + acd'(1) \qquad \text{(Inverse)} \\
&= ac'd + a'cd' + a'c'd + acd' \qquad \text{(Identitiy)} \\
&= ac'd + a'c'd + a'cd' + acd' \qquad \text{(Commutativity)} \\
&= c'd(a+a') + cd'(a'+a) \qquad \text{(Distribution)} \\
&= c'd + cd'
\end{aligned}
$$

- F_4(a,b,c,d) = $(c' \cdot d) + (c \cdot d')$

In this part, hex inverter is used for inverting input value. 74xx108 AND gate and 74xx132 OR gate are used to implement necessary logic operations. The vcc voltage is

applied to the pins at the top right corner of each of the integrated circuits and the ground voltage is applied to the pins at the lower left corner.

To implement the minimized expression, the first input of the logic monitor is connected to the first pin on the left of the hex inverter and the fourth pin on the left of the integrated circuit for AND operation. The second pin on the left of the hex inverter is connected to the first pin on the left of the integrated circuit for AND operation. The second input of the logic monitor is connected to the third pin on the left of the hex inverter and the second pin on the left of the integrated circuit for AND operation. The fourth pin on the left of the hex inverter is connected to the fifth pin on the left of the integrated circuit for AND operation. The third and sixth pin on the left of the integrated circuit, output values of AND operations, are connected to the first and second pin on the left of the integrated circuit for OR operation. The third pin on the left of the integrated circuit for OR operation is connected to the one of the pins on the logic monitor the observe output value.

When the output values are observed, output values of the circuit that implemented with the minimized expression is consistent with the output values of the expression on the truth table. Thus, axioms and theorems of Boolean algebra are validated.

3 INTERPRETATION OF THE RESULTS

Throughout the whole experiment results we observed were consistent with the theoretical results. Since all operations were logical operations there were no swings in voltage values that would cause us to get wrong result (Also no equipment failures occured).

4 CONCLUSION

For the most part we were able to go through each part without any big problems. Only issue worth mentioning was a confusion we had while plugging the cables for the last part of the experiment. Which resulted in us getting wrong logic results from the circuit. But we figured it out and corrected it rather quickly. We have seen that a little more care has to be taken while assembling the circuits in order not to make a mistake and be more efficient with time.

REFERENCES

[1] Istanbul Technical University Department of Computer Engineering. Blg 242e logic circuits laboratory experiments booklet version 1.9, Spring 2019.

[2] Overleaf documentation https://tr.overleaf.com/learn.

[3] Detailed info on writing reports https://projects.ncsu.edu/labwrite/res/res-studntintro-labparts.html.