ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	5
EXPERIMENT DATE	:	15.03.2019
LAB SESSION	:	FRIDAY - 14.00
GROUP NO	:	G13

GROUP MEMBERS:

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SPRING 2019

ETHIC FORM
for
BLG242E Logic Circuits Laboratory

As a student of

Istanbul Technical University Faculty of Computer and Informatics Engineering;

1. I will not attempt to cheat in quizes and final exam,
2. I will not use disallowed sources or tools (mobile phone, calculator etc.) during the exam,
3. I will not write any information (formula, text, figure etc.) on the table, sheets or books that are allowed to be used during the exam,
4. I will give reference when using printed or online published sources,
5. I will not use the results in a source as they are, or by changing a part of them without giving a reference,
6. I will not show unused sources as used,
7. I will not present someone elses idea as my own idea,
8. I will not make someone do my homework, project or thesis for money or anything else,
9. I will not take an exam or enter a lecture on behalf of others,
10. I will not make excuses for not attending in exams or lessons by taking reports from someone I know (medical doctor parents or relatives),
11. I will refrain from deliberately harming the public materials at our university,
12. I will comply with the safety rules in laboratory work,
13. I will behave in accordance with the rules of respect for the lecturers and teaching assistants

signed by

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

Contents

1 INTRODUCTION

In this experiment we have built various circuits in order to observe and understand the differences between TTL and CMOS gate families.

2 REQUIREMENTS

Tools Used[1]

- C.A.D.E.T
- Integrated Circuits
  - 74xx00 TTL NAND Gates
  - 4011 CMOS NAND Gates
- Oscilloscope
- 100Ω Resistor

2.1 Part 1

In this part of the experiment, every given circuit is built with NAND gates from both CMOS and TTL families. With the aid of the potentiometer, voltage values are changed on the circuit in order to record how NAND gates behave.

2.1.1 Part 1.a

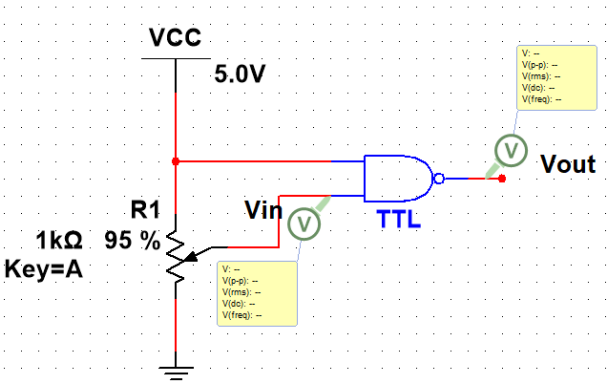

Figure 1: The circuit using TTL NAND gate.

	1	2	3	4	5	6	7
$V_{input}(Volt)$	0.00	0.35	1.04	2.27	3.43	4.60	4.96
$V_{output}(Volt)$	3.71	3.86	3.52	0.19	0.20	0.20	0.26

Table 1: Switching Characteristics of TTL

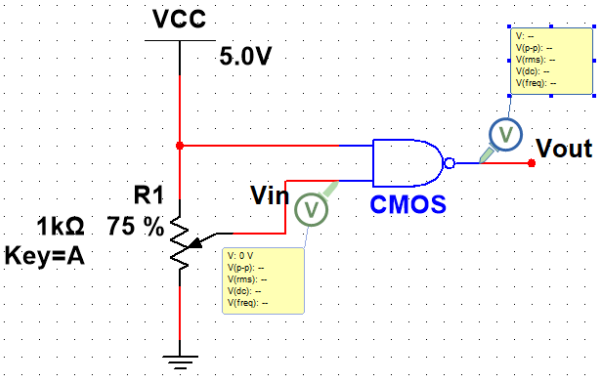

Figure 2: The circuit using CMOS NAND gate.

The circuit given in Figure 1 is implemented using a TTL NAND gate. Then with the aid of the potentiometer V_{input} is changed several times in order to observe it's effects on V_{output}. All results of the mentioned part are given in Table 1

The circuit given in Figure 2 is implemented using a CMOS NAND gate. Then with the aid of the potentiometer V_{input} is changed several times in order to see it's effects on V_{output}. All results of the mentioned part are given in Table 2.

	1	2	3	4	5	6	7
$V_{input}(Volt)$	0.00	0.74	1.66	2.94	3.49	4.39	4.96
$V_{output}(Volt)$	4.95	4.95	4.95	0.13	0.15	0.25	0.16

Table 2: Switching characteristics of CMOS

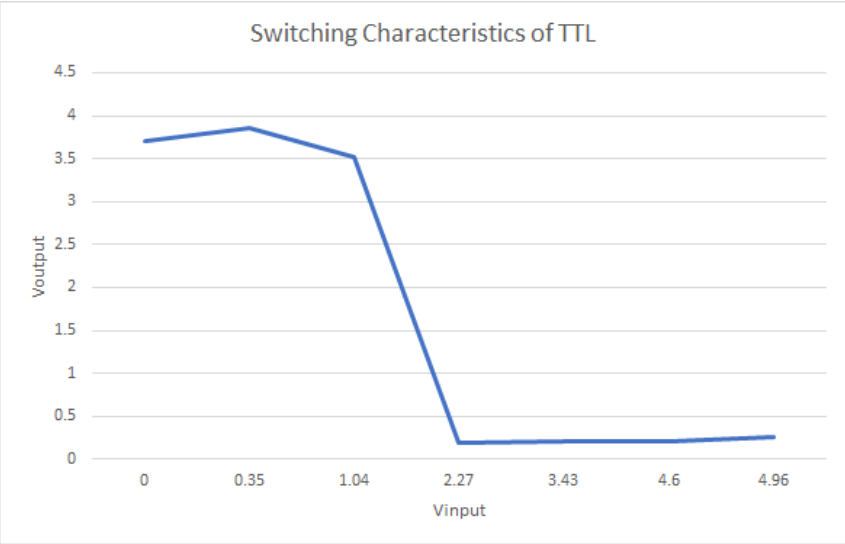

Figure 3: Switching characteristics of TTL

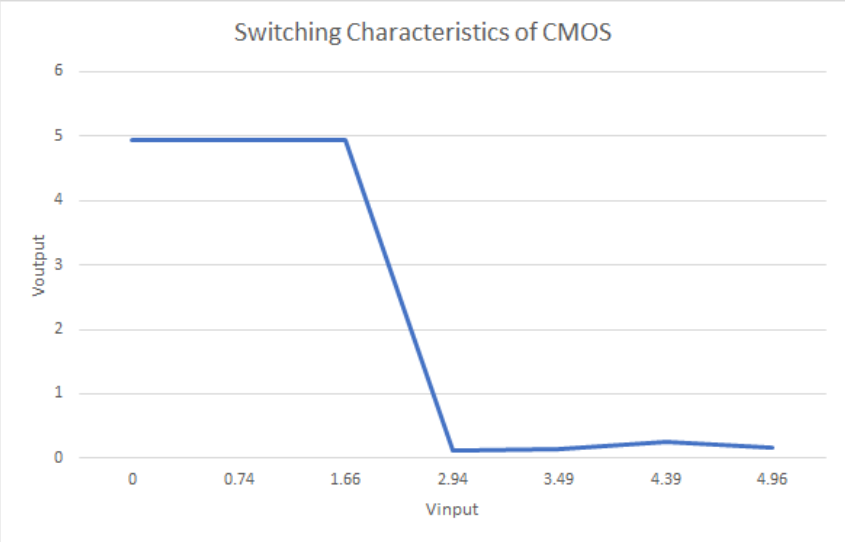

Figure 4: Switching characteristics of CMOS

Figure 3 and Figure 4 are the graphs of the function $f(V_{output}) = V_{output}$. It is a clear fact that CMOS is much more stable than TTL while producing high output. Both gates does not have state between low and high. Another information that can be extracted from these graphs is TTL's noise margin is greater than CMOS's.

2.1.2 Part 1.b

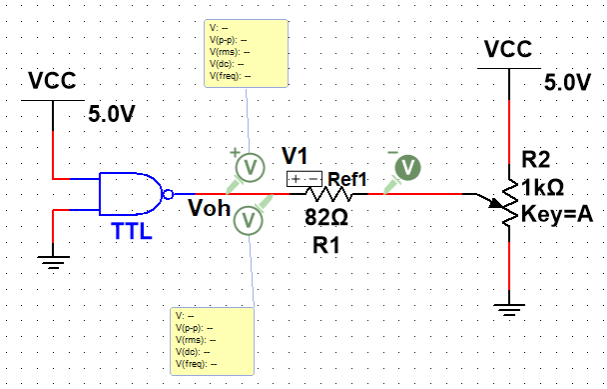

Figure 5: The circuit using a TTL NAND gate.

The circuit given in figure 5 is implemented using a TTL NAND gate. The aim of this part is to find the maximum possible value of I_{AB} when the output state of the gate is Logic-1. With the aid of the potentiometer V_{output} is changed several times in order to see it's effects on V_{AB}. I_{OH} values are calculated by using V_{OH}/R. All results are given in Table 3.

	1	2	3	4	5	6	7
$V_{AB}(Volt)$	2.12	1.72	1.25	0.87	0	0	0
$V_{OH}(Volt)$	2.20	2.50	2.85	3.12	3.96	4.54	4.95
$I_{OH}(mA)$	25.8	20.9	15.2	10.6	0	0	0

Table 3: $V_{OH} - I_{OH}$ Characteristics of TTL

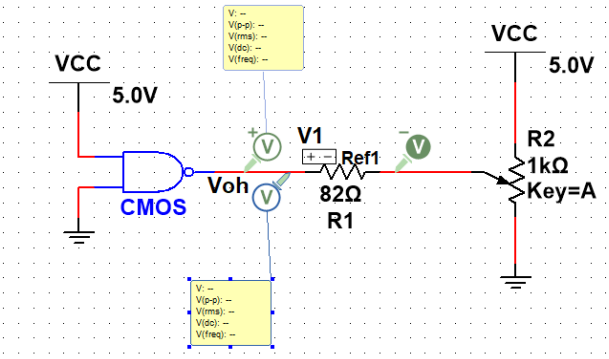

Figure 6: The circuit using a CMOS NAND gate.

The circuit given in figure 6 is implemented using a CMOS NAND gate. The aim of this part is to find the maximum possible value of I_{AB} when the output state of the gate is Logic-1. With the aid of the potentiometer V_{output} is changed several times in order to see it's effects on V_{AB}. I_{OH} values are calculated by using V_{OH}/R. All results of the mentioned part are given in Table 4.

	1	2	3	4	5	6	7
$V_{AB}(Volt)$	0.48	0.47	0.44	0.41	0.32	0.21	0.02
$V_{OH}(Volt)$	0.49	1.01	1.56	2.28	3.27	3.96	4.95
$I_{OH}(mA)$	5.85	5.73	5.37	5.00	3.90	2.56	0.24

Table 4: $V_{OH} - I_{OH}$ Characteristics of CMOS

In the figures below(Figure 7 and 8), we can see the switching characteristics for both CMOS and TTL for above mentioned circuits. We were able to observe a wider voltage range with CMOS than we were ablo to with TTL. This can be interpreted as TTL being less reactive to changes in resistance and therefore current in the circuit.

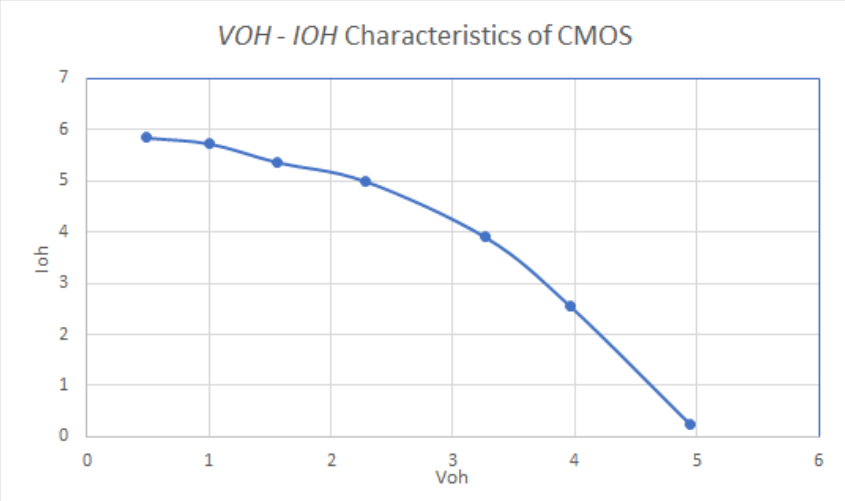

Figure 7: $V_{OH} - I_{OH}$ Characteristics of TTL

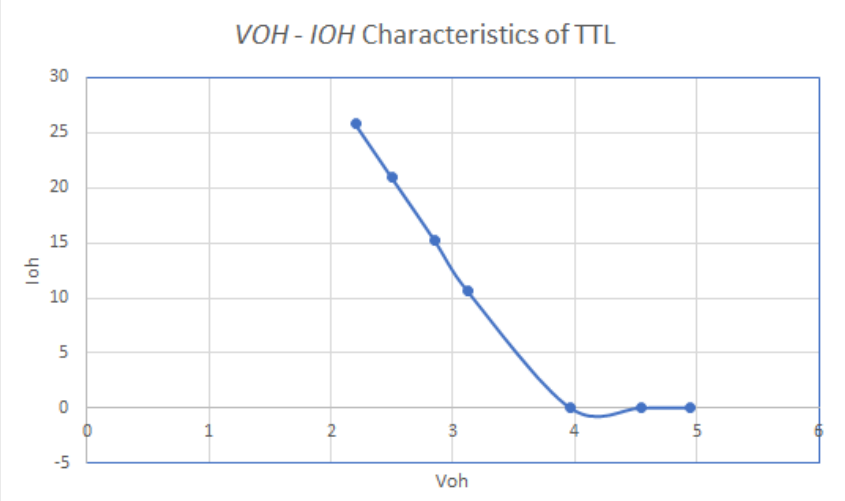

Figure 8: $V_{OH} - I_{OH}$ Characteristics of CMOS

2.1.3 Part 1.c

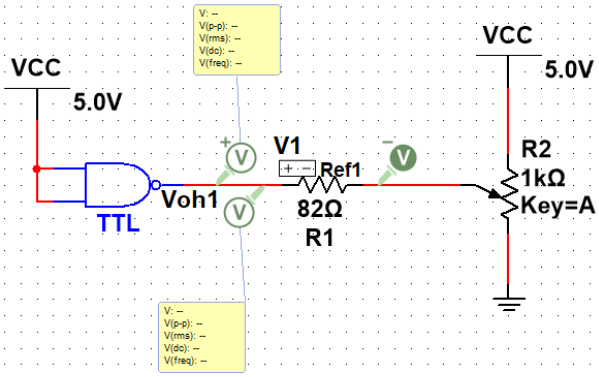

Figure 9: The circuit using a TTL NAND gate.

The circuit given in figure 9 is implemented using a TTL NAND gate. The aim of this part is to find the maximum possible value of I_{AB} when the output state of the gate is Logic-0. With the aid of the potentiometer V_{output} is changed several times in order to see it's effects on V_{AB}. I_{OH} values are calculated by using V_{OH}/R. All results of the mentioned part are given in Table 5.

	1	2	3	4	5	6	7
$V_{AB}(Volt)$	-0.14	-0.24	-0.50	-0.83	-1.36	-2.52	-4.17
$V_{OL}(Volt)$	0.14	0.19	0.24	0.28	0.32	0.42	0.57
$I_{OL}(mA)$	1.70	2.90	6.00	10.00	16.50	30.70	50.80

Table 5: $V_{OL} - I_{OL}$ Characteristics of TTL

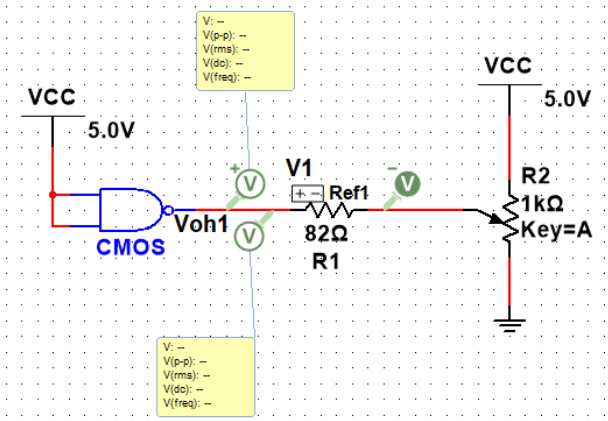

Figure 10: The circuit using a CMOS NAND gate.

The circuit given in figure 10 is implemented using a CMOS NAND gate. The aim of this part is to find the maximum possible value of I_{AB} when the output state of the gate is Logic-1. With the aid of the potentiometer V_{output} is changed several times in order to see it's effects on V_{AB}. I_{OH} values are calculated by using V_{OH}/R. All results are given in Table 6.

	1	2	3	4	5	6	7
$V_{AB}(Volt)$	0	-0.35	-0.51	-0.55	-0.56	-0.57	-0.58
$V_{OL}(Volt)$	0	0.77	1.52	2.20	2.96	3.90	4.30
$I_{OL}(mA)$	0	4.22	6.21	6.70	6.82	6.90	7.00

Table 6: $V_{OL} - I_{OL}$ Characteristics of CMOS

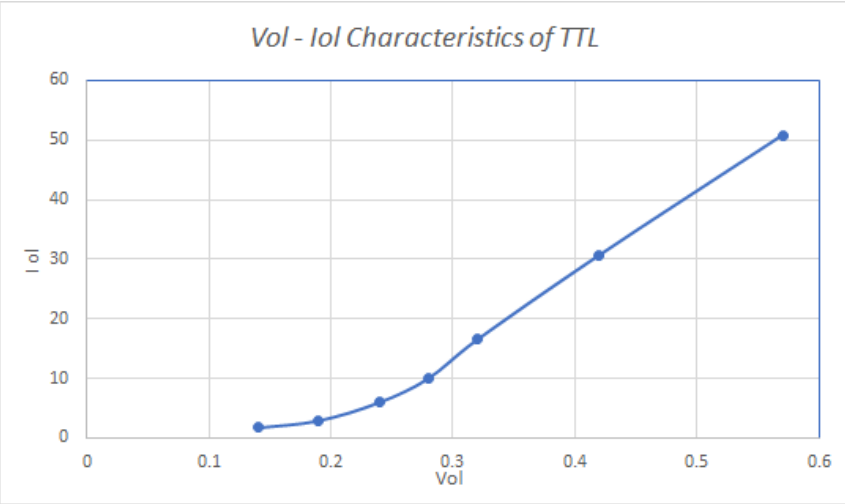

Figure 11: $V_{OL} - I_{OL}$ Characteristics of TTL

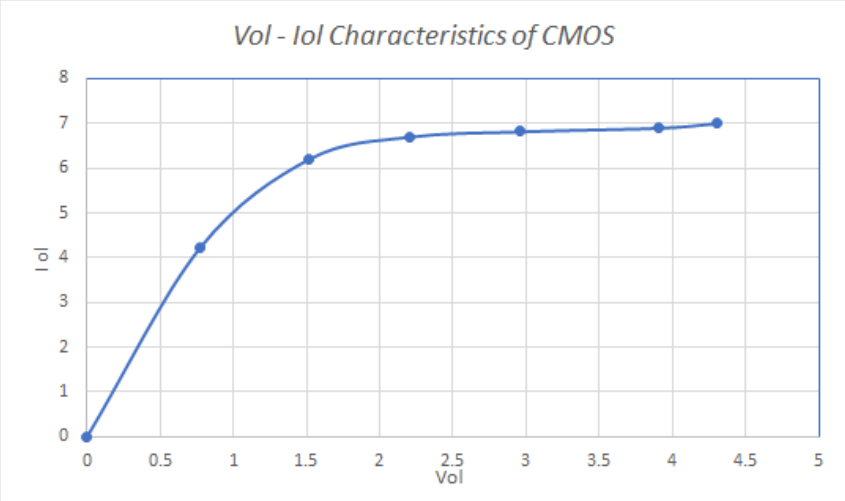

Figure 12: $V_{OL} - I_{OL}$ Characteristics of CMOS

With this circuit, we were able to observe a wider voltage range with CMOS than TTL once again. This is once again due to the different reaction of both type of gates. It can be said that TTL is less reactive to the changes in current.

2.1.4 Part 1.d

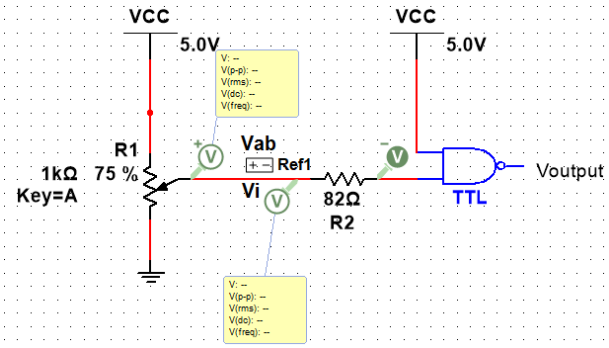

Figure 13: The circuit using a TTL NAND gate.

The circuit given in figure 13 is implemented using a TTL NAND gate. The aim of this part is to find I_{input} values for different V_{input}. With the aid of the potentiometer V_i is changed several times in order to see it's effects on V_{AB}. I_i values are calculated by using V_{AB}/R. All results of the mentioned part are given in Table 7.

	1	2	3	4	5	6	7
$V_{AB}(mV)$	-1.10	-83.00	-42	0	0	0	0
$V_i(Volt)$	0	0.992	1.15	1.68	3.04	3.91	4.96
$I_i(mA)$	1.35	1.01	0.51	0	0	0	0

Table 7: $V_i - I_i$ Characteristics of TTL

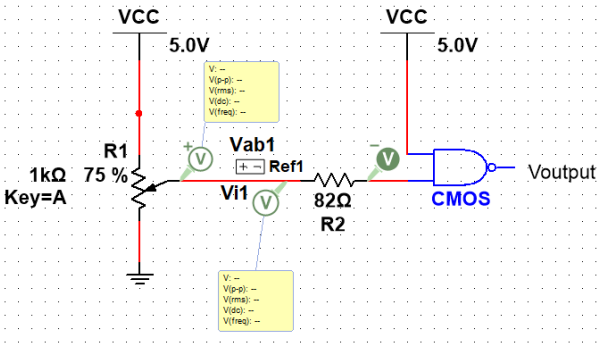

Figure 14: CMOS

The circuit given in figure 14 is implemented using a CMOS NAND gate. The aim of this part is to find I_{input} values for different V_{input}. With the aid of the potentiometer V_i is changed several times in order to see it's effects on V_{AB}. I_i values are calculated by using V_{AB}/R. All results of the mentioned part are given in Table 8.

	1	2	3	4	5	6	7
$V_{AB}(V)$	0	0	0	0	0	0	0
$V_i(Volt)$	0	0.65	1.18	2.16	3.60	4.40	4.97
$I_i(mA)$	0	0	0	0	0	0	0

Table 8: $V_i - I_i$ Characteristics of CMOS

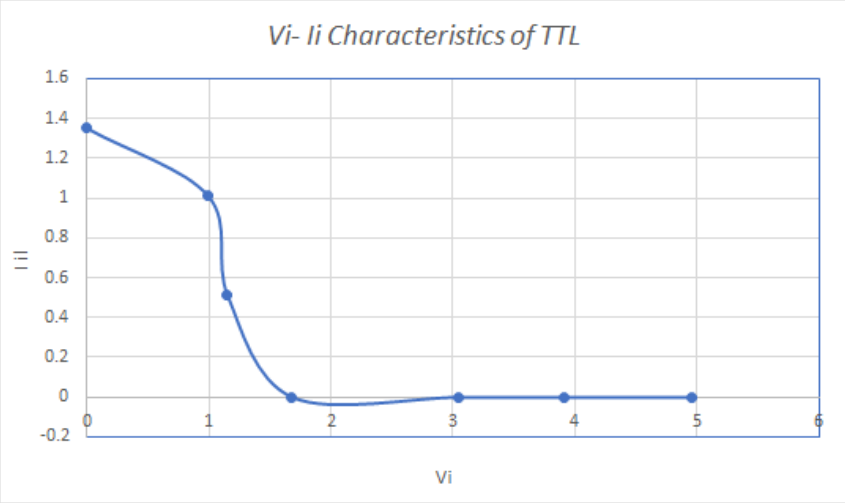

Figure 15: $V_i - I_i$ Characteristics of TTL

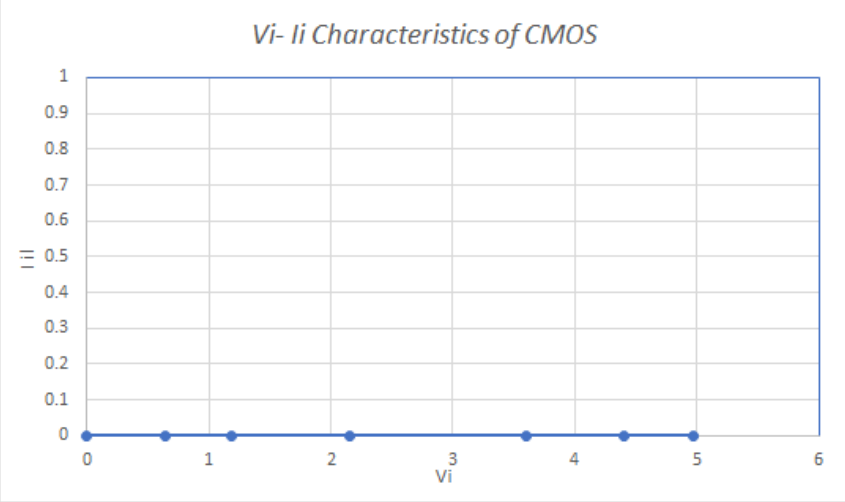

Figure 16: $V_i - I_i$ Characteristics of CMOS

In Figures 15 and 16, line graph of $V_i = f_4(I_i)$ is given. These lines do show how much a gate consumes when no output is connected. Figure 16 shows one of the benefits of using CMOS gates which is not consuming any power when it is not needed, which will indicate that more CMOS gates can be connected sequentially than TTL gates can.

2.2 Part 2

In the second part of the experiment, dynamic characteristics of TTL and CMOS NAND gates are observed.

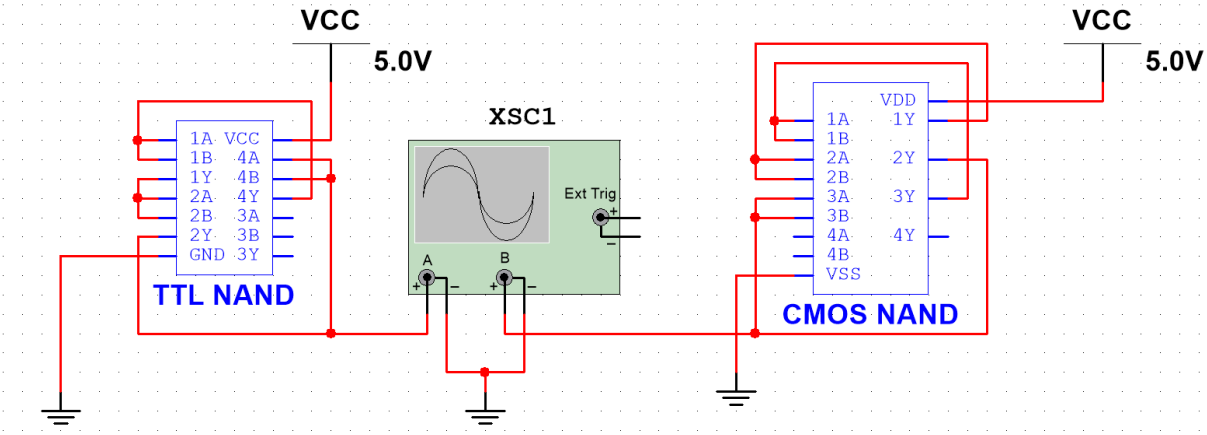

Figure 17: PART 2

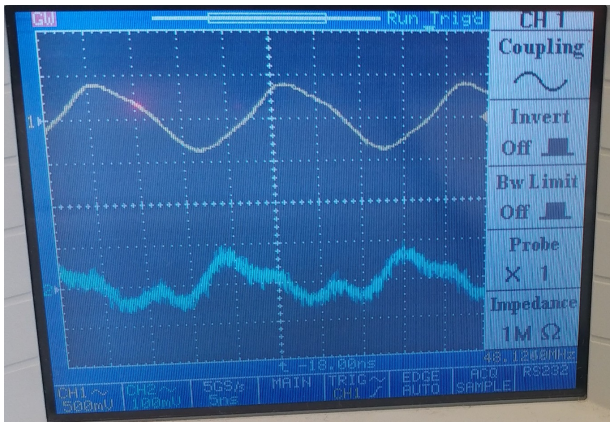

Figure 18: PART 2

The circuit in 17 was implemented using both CMOS and TTL gates. Both types of gates caused oscillation and that oscillation was monitored using the oscilloscope (as seen in 18). We also observed that there was some noise in the signal. But we were able to see a signal that was close to the result we were expecting for both types of gates. Frequency values for both circuits were close to 48 MHz, meaning the peroid was $2,08.10^{-9}$.

3 INTERPRETATION OF THE RESULTS

Most of the experiment results were the way we expected them to be. But for some circuits, our results contradicted with the theoretically calculated values. For instance we were not able to get voltage values to zero for some circuits, which in theory should have been possible. We believe that this situation occurred because of the limitations with the equipment that has been used (maximum values for the potentiometers etc.).

4 CONCLUSION

While doing this experiment we were able to inspect the differences between TTL and CMOS behaviours in real life situations. And by doing so, we have acquired an improved vision for choosing the one that will be more suitable for our future designs. Also for the first time in an experiment, we had to finish the task as a 2 person group because of the fact that our friend Cihat unfortunately was eliminated from the laboratory. This truly affected our performance through the rest of the experiment resulting in us failing to complete one of the tasks.

REFERENCES

[1] Istanbul Technical University Department of Computer Engineering. Blg 242e logic circuits laboratory experiments booklet version 1.9, Spring 2019.

[2] Overleaf documentation https://tr.overleaf.com/learn.

[3] Detailed info on writing reports https://projects.ncsu.edu/labwrite/res/res-studntintro-labparts.html.