ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	6
EXPERIMENT DATE	:	22.03.2019
LAB SESSION	:	FRIDAY - 14.00
GROUP NO	:	G13

GROUP MEMBERS:

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SPRING 2019

ETHIC FORM
for
BLG242E Logic Circuits Laboratory

As a student of

Istanbul Technical University Faculty of Computer and Informatics Engineering;

1. I will not attempt to cheat in quizes and final exam,
2. I will not use disallowed sources or tools (mobile phone, calculator etc.) during the exam,
3. I will not write any information (formula, text, figure etc.) on the table, sheets or books that are allowed to be used during the exam,
4. I will give reference when using printed or online published sources,
5. I will not use the results in a source as they are, or by changing a part of them without giving a reference,
6. I will not show unused sources as used,
7. I will not present someone elses idea as my own idea,
8. I will not make someone do my homework, project or thesis for money or anything else,
9. I will not take an exam or enter a lecture on behalf of others,
10. I will not make excuses for not attending in exams or lessons by taking reports from someone I know (medical doctor parents or relatives),
11. I will refrain from deliberately harming the public materials at our university,
12. I will comply with the safety rules in laboratory work,
13. I will behave in accordance with the rules of respect for the lecturers and teaching assistants

signed by

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

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1 INTRODUCTION

In this experiment, a data bus is implemented by using three-state buffers and ICs with open collector outputs. Main goal is understanding the behavior of a data bus and its basic principles.

2 REQUIREMENTS

Tools Used[1]

- C.A.D.E.T
- 74000 series ICs
  - 74xx241 Octal 3-State Buffer
  - 74xx05 Hex Inverters with Open-Collector Outputs
- Resistors
- 100Ω Resistor

2.1 PART 1

In the first part of the experiment, 4-bit data bus is implemented by using ICs with given outputs(given Hex Inverters with open collectors). $R_{C(max)}$ and $R_{C(min)}$ values are calculated for $V_{cc)}$=5.0V, N=1, K=2, $V_{IL(max)}$=0.8V, $V_{IH(min)}$=2.0V, $I_{IL(max)}$=0.4mA, $I_{OL(max)}$=8mA, $I_{OH(max)}$=100μA, $I_{IH(max)}$=20μA as given formulas. Resistances were used according to the results of the calculations.

- $R_{C(min)} = [V_{cc}$ - $V_{IL(max)}]/[I_{OL(max)}$-$I_{IL(max)} \cdot$ N]
- $R_{C(max)} = [V_{cc}$ - $V_{IH(min)}]/[I_{OH(max)} \cdot$ K + $I_{IH(max)} \cdot$ N]

When calculation is completed $R_{C(min)}$ and $R_{C(max)}$ values are found as 0.552kΩ and 13,636kΩ. In this experiment 4.7kΩ resistances are used suitability of the resistance value validated with the calculations.

Inputs are connected from logic switches to Octal 3-State Buffer. Output pins of Octal 3-State Buffer are inverted by using hex inverter. Output pins of hex inverters are connected to displays and results are observed as given circuit below. Results are validated with the information that bus behaves like a 'wired or' circuit.

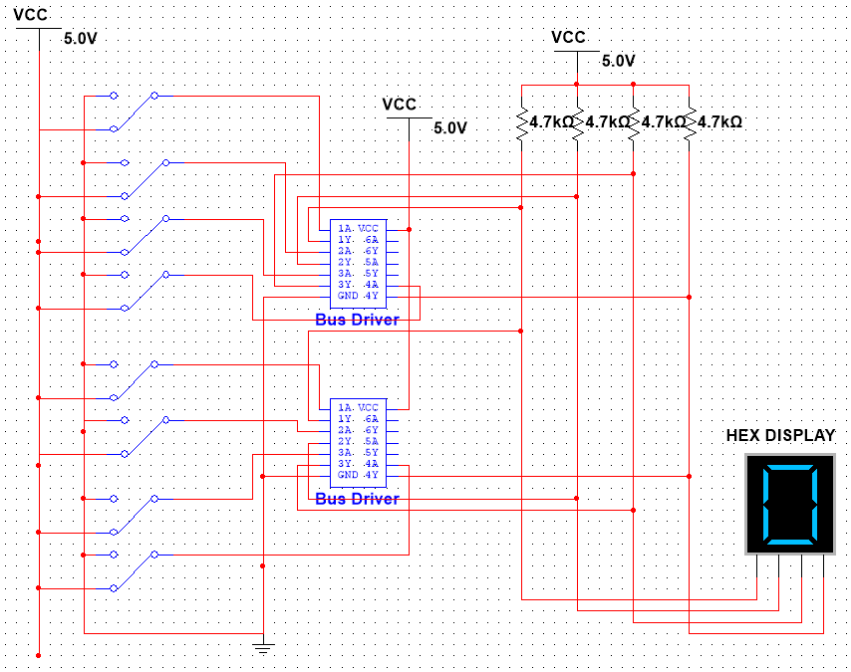

Figure 1: 4 bit data bus with 2 drivers with open collector outputs

1Ax	2Ax	Yx
1	1	0
1	0	0
0	1	0
0	0	1

Table 1: Results of Part 1

2.2 PART 2

In the second part of the experiment, 4-bit bus is implemented by using 3 state buffers. One of the SPDT switches is used for enable input of the 3 state buffers as given in circuit figure below. After the implementation, result is observed on the display. Behaviour of the circuit seems in the table below.

SPDT	A1	A2	Y
H	0xC	0xB	0xB
H	0x09	0x07	0x07
L	0xA	0xC	0xA
L	0x03	0xE	0x03

Table 2: 3 state buffers with SPDT switches

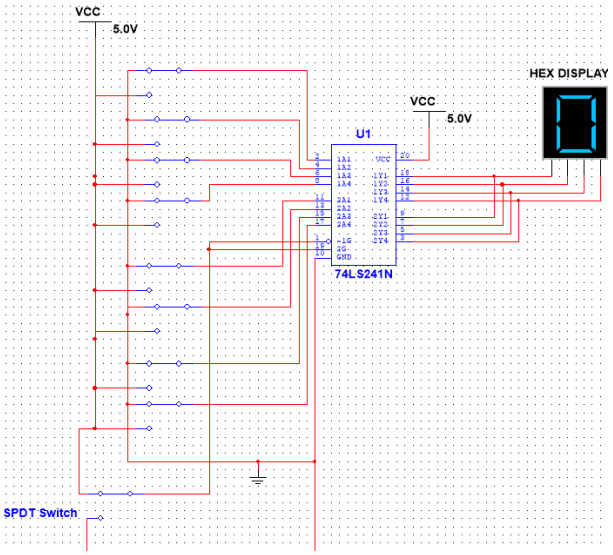

Figure 2: 4 bit data bus with 2 drivers with 3-state buffers

2.3 PART 3

In the final part of the experiment, the circuit is implemented as in the figure given below. The circuit contains 2-bit bus with two distinct outputs and inputs. One of the SPDT switches is used for enable input of the 3-state buffers.

Behaviour of the bus is validated according to the results observed on the LED outputs. Then, SPDT switch connection is detached and connected to the frequency generator instead of enable pin. Output of the circuit is observed changing frequency. Behaviour of the circuit is seems on the table below.

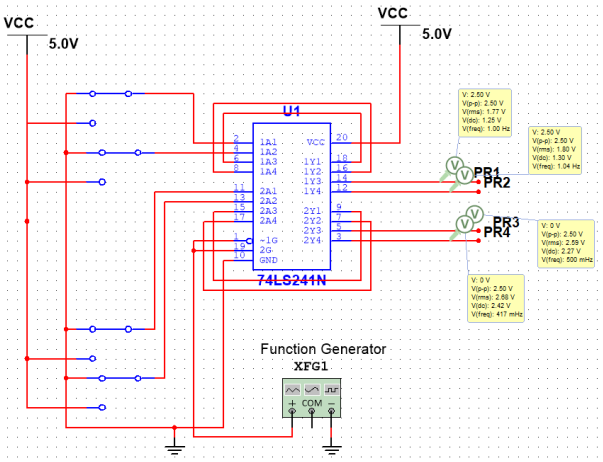

Figure 3: 2 bit data bus with 2 drivers and 2 readers

While CLK is High						While CLK is Low					
1A1	1A2	2A1	2A2	Y1	Y2	1A1	1A2	2A1	2A2	Y1	Y2
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	0	0
0	0	1	1	1	1	0	0	1	1	0	0
0	1	0	0	0	0	0	1	0	0	0	1
0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	1	1	0	0	1
0	1	1	1	1	1	0	1	1	1	0	1
1	0	0	0	0	0	1	0	0	0	1	0
1	0	0	1	0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	1	1	1	0	1	1	1	0
1	1	0	0	0	0	1	1	0	0	1	1
1	1	0	1	0	1	1	1	0	1	1	1
1	1	1	0	1	0	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1

Table 3: Results recorded in part3

3 INTERPRETATION OF THE RESULTS

Results throughout the whole experiment were consistent with the results we have calculated beforehand. Bus behaved as we expected in all off the circuits that were implemented.

4 CONCLUSION

Everything went as planned through the whole experiment, we did not have any difficulties completing the given tasks. All in all, we believe that this experiment helped us improve our knowledge of implementations of BUS.

REFERENCES

[1] Istanbul Technical University Department of Computer Engineering. Blg 242e logic circuits laboratory experiments booklet version 1.9, Spring 2019.

[2] Overleaf documentation https://tr.overleaf.com/learn.

[3] Detailed info on writing reports https://projects.ncsu.edu/labwrite/res/res-studntintro-labparts.html.