ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	4
EXPERIMENT DATE	:	08.03.2019
LAB SESSION	:	FRIDAY - 14.00
GROUP NO	:	G13

GROUP MEMBERS:

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

SPRING 2019

ETHIC FORM
for
BLG242E Logic Circuits Laboratory

As a student of

Istanbul Technical University Faculty of Computer and Informatics Engineering;

1. I will not attempt to cheat in quizes and final exam,
2. I will not use disallowed sources or tools (mobile phone, calculator etc.) during the exam,
3. I will not write any information (formula, text, figure etc.) on the table, sheets or books that are allowed to be used during the exam,
4. I will give reference when using printed or online published sources,
5. I will not use the results in a source as they are, or by changing a part of them without giving a reference,
6. I will not show unused sources as used,
7. I will not present someone elses idea as my own idea,
8. I will not make someone do my homework, project or thesis for money or anything else,
9. I will not take an exam or enter a lecture on behalf of others,
10. I will not make excuses for not attending in exams or lessons by taking reports from someone I know (medical doctor parents or relatives),
11. I will refrain from deliberately harming the public materials at our university,
12. I will comply with the safety rules in laboratory work,
13. I will behave in accordance with the rules of respect for the lecturers and teaching assistants

signed by

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

Contents

1 INTRODUCTION

In this experiment, logic circuits are implemented to make arithmetic operations on signed and unsigned binary numbers. An Arithmetic Logic Unit(ALU) is used and some operations are made.

2 REQUIREMENTS

Tools Used[1]

- C.A.D.E.T
- 74000 series ICs
  - 74xx08 - Quadruple 2-input Positive AND Gates
  - 74xx32 - Quadruple 2-input Positive OR Gates
  - 74xx83 - 4-bit Binary Full Adder
  - 74xx86 - Quadruple 2-input Positive Exclusive Or (XOR) Gates
  - 74xx174 - Hex D-Type Flip-Flops
  - 74xx181 - 4-Bit Arithmetic Logic Unit

2.1 PART 1

In the first part of the experiment, the circuit is designed as shown given diagram below. Logic switches are used for inputs and LED's on the monitor are used to observe output values.

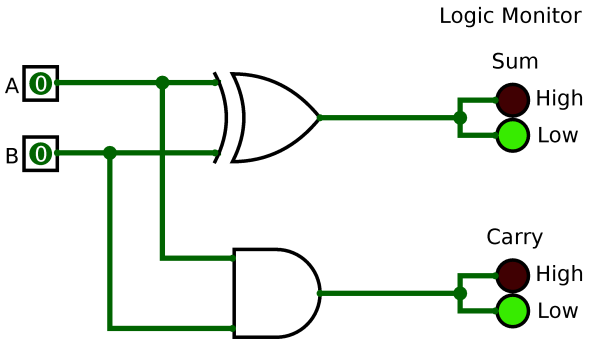

Figure 1: Half adder

The output values of the circuit are validated with the truth table below.

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1: Truth table of half adder.

2.2 PART 2

In the next part of the experiment, some changes are made on the circuit which it's diagram was drawn in the previous part. One more input and additional gates are added to make the full adder circuit.

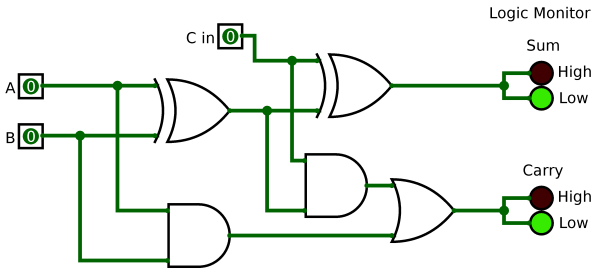

Figure 2: Full adder

The output values of the circuit are validated with the truth table below.

A	B	C_{in}	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 2: Truth table of full adder.

2.3 PART 3

In the next part of the experiment, the circuit is implemented using a 4-bit full adder(74xx83) as shown diagram below. The output values(Carry and Sum) are observed for some test cases given in the booklet. Addition and subtraction operations are made and output values are interpreted considering both signed and unsigned input values.

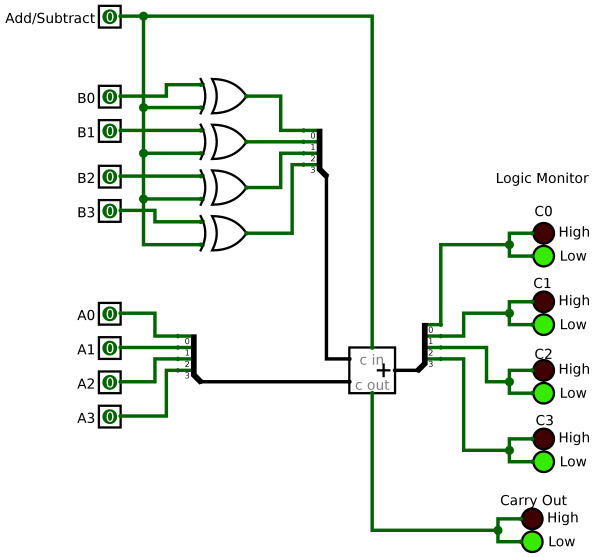

Figure 3: 4 bit full adder

Test Case	1	2	3	4
A	0101	1101	1111	0110
B	0111	1001	1111	1101

Table 3: Test cases for arithmetic operations.

A	B	Carry	Result in Binary	Result in Decimal
0101	0111	0	1100	12
1101	1001	1	0110	22
1111	1111	1	1110	30
0110	1101	1	0011	19

Table 4: Results of the unsigned sum $A + B$.

In Table 4, output values that obtained addition operation are interpreted as unsigned input values. It is observed that for the first case there is no carry and result can be

represented with 4 bit but for the other cases result cannot be represented with 4 bit and fifth bit(carry bit) is necessary.

A	B	Overflow	Result sign	Result in Binary	Result in Decimal
0101	0111	1	-	1100	-4
1101	1001	1	+	0110	6
1111	1111	0	-	1110	-2
0110	1101	0	+	0011	3

Table 5: Results of the signed sum $A + B$.

In the Table 5, output values that obtained addition operation are interpreted as signed input values. It is observed that results are not valid for the four cases. Overflow occurs for the first and second cases because signs of the input values are same but signs of the output values are different.

A	B	Borrow	Result in Binary	Result in Decimal
0101	0111	1	1110	14
1101	1001	0	0100	4
1111	1111	0	0000	0
0110	1101	1	1001	9

Table 6: Results of the unsigned subtraction $A - B$

In the Table 6, output values that were obtained by subtraction operation are interpreted as unsigned input values. It is observed that result is valid for the second and third cases and is not valid for the first and fourth cases by reason of presence of borrow. If there is a borrow this means second number is larger than the first one. The result which should be a negative number, cannot be represented with unsigned numbers.

A	B	Overflow	Result sign	Result in Binary	Result in Decimal
0101	0111	0	-	1110	-2
1101	1001	0	+	0100	4
1111	1111	0	+	0000	0
0110	1101	1	-	1001	-7

Table 7: Results of the signed subtraction $A - B$

In the Table 7, output values that obtained subtraction operation are interpreted as signed input values. It is observed that result is valid for all cases except the fourth one. Fourth case is not valid since subtracting a negative number from a positive one should yield a positive number. As can be seen in the table result is negative, which means overflow.

2.4 PART 4

In the final part of the experiment, the circuit shown below is implemented using a 4-Bit Arithmetic Logic Unit(74xx181) and a D type flip-flop(74xx174). Also hex inverters are used because of the fact that F outputs of ALU are in negative logic. Input values are controlled by the logic switches and output values are observed on the logic monitor LED's on the C.A.D.E.T. Clock, M, and clear are controlled by the logic switches as well. Cn input of ALU is connected to ground(0V).

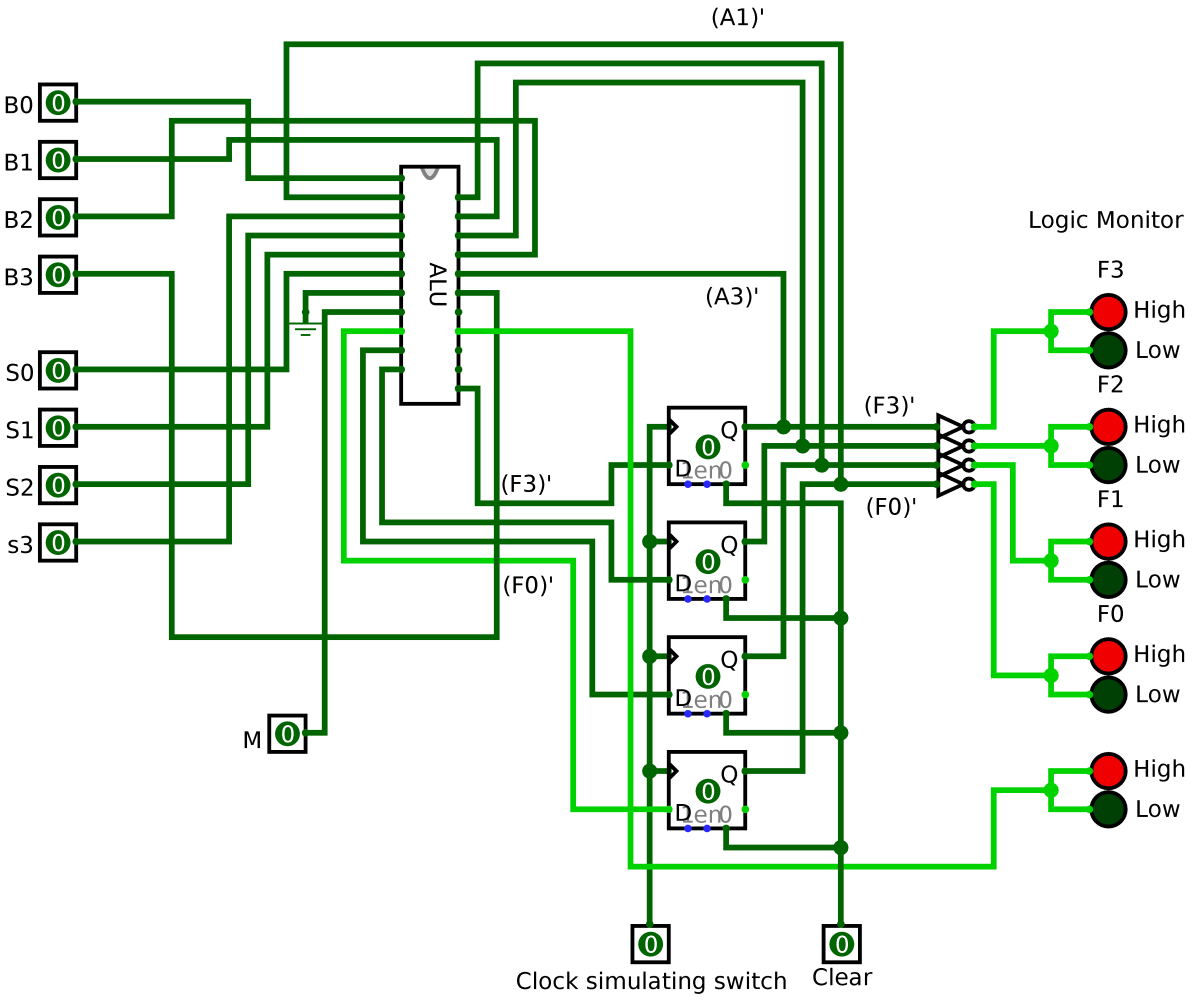

Figure 4: 4 bit full adder

3 INTERPRETATION OF THE RESULTS

In the first three parts of this experiment results were consistent with our calculations and our circuits worked without any problems.(Detailed information about design process and theory for each part is presented in the sections above.) For the 4th part, we did not get the result we expected. We believe that, this was caused by a problem that occured while we incorporated the flip flop in our design.

4 CONCLUSION

Except for the fourth part of the experiment, no problems occured through the experiment. We were able to observe the results desired and go through parts 1,2 and 4 pretty quickly. In part 4, we designed a circuit and built it on the breadboard. We were able to set values to the ALU with no problems occuring but addition operation did not work the way it was supposed to. Therefore we dissembled the circuit and built it from the start once again, that would have solved the issue in the case where it was about the cables. But that didn't work, so we decided to change the design. We made adjustments to the outputs of the D-Flip Flop 2 but unfortunately we couldn't find the problem and weren't able to fully complete the part.

REFERENCES

[1] Istanbul Technical University Department of Computer Engineering. Blg 242e logic circuits laboratory experiments booklet version 1.9, Spring 2019.