ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	8
EXPERIMENT DATE	:	12.04.2019
LAB SESSION	:	FRIDAY - 14.00
GROUP NO	:	G13

GROUP MEMBERS:

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

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SPRING 2019

ETHIC FORM
for
BLG242E Logic Circuits Laboratory

As a student of

Istanbul Technical University Faculty of Computer and Informatics Engineering;

1. I will not attempt to cheat in quizes and final exam,
2. I will not use disallowed sources or tools (mobile phone, calculator etc.) during the exam,
3. I will not write any information (formula, text, figure etc.) on the table, sheets or books that are allowed to be used during the exam,
4. I will give reference when using printed or online published sources,
5. I will not use the results in a source as they are, or by changing a part of them without giving a reference,
6. I will not show unused sources as used,
7. I will not present someone elses idea as my own idea,
8. I will not make someone do my homework, project or thesis for money or anything else,
9. I will not take an exam or enter a lecture on behalf of others,
10. I will not make excuses for not attending in exams or lessons by taking reports from someone I know (medical doctor parents or relatives),
11. I will refrain from deliberately harming the public materials at our university,
12. I will comply with the safety rules in laboratory work,
13. I will behave in accordance with the rules of respect for the lecturers and teaching assistants

signed by

150180704 : CİHAT AKKİRAZ

150180707 : FATİH ALTINPINAR

150180734 : SİNAN ŞAR

Contents

1 INTRODUCTION

In this experiment, several circuits are built in order to understand how counters function. Also an analysis is done for a given circuit as well. In this experiment, several circuits are implemented in order to understand how sequencial circuits work, how they can be analyized nasil yaziliyo lan

2 REQUIREMENTS

Tools Used[1]

- C.A.D.E.T
- 74000 series ICs
  - 74xx04 - Hex Inverters
  - 74xx08 - Quadruple 2-input Positive AND Gates
  - 74xx32 - Quadruple 2-input Positive OR Gates
  - 74xx161 - Synchronous 4-Bit Binary Counter
  - 74xx174 - Hex D-Type Flip-Flops

2.1 PART 1

In the first part of the experiment, the circuit is implemented as shown in the figure below. X input connected to a logic switch and the clock is connected to a debounced pushbutton. The output Y and flip-flop states are observed using LEDs on the logic monitor.

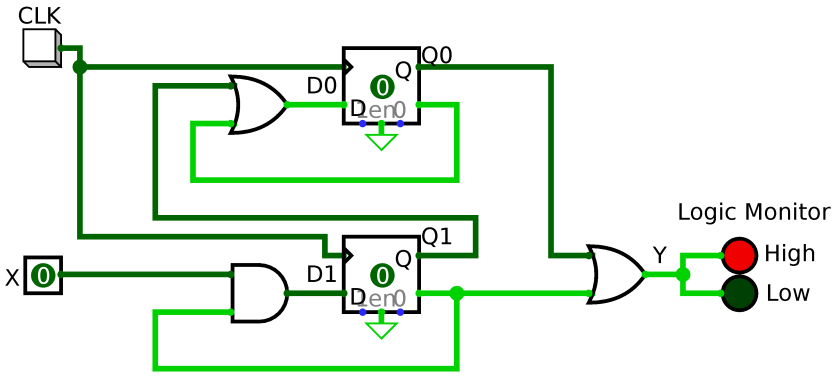

Figure 1: Circuit that is implemented in Part 1

Determining input expressions of the flip flops

$$D_0 = \bar{Q}_0 + Q_1$$

$$D_1 = X \cdot \bar{Q}_1$$

Characteristic equation of D flip flops

$$Q^+ = D$$

Determining next state expressions

$$Q_0^+ = \bar{Q}_0 + Q_1$$

$$Q_1^+ = X \cdot \bar{Q}_1$$

Determining output expression based on current state

$$Y = Q_0 + \bar{Q}_1$$

$Q_1^+Q_0^+$		X		
		0	1	Z
Q_1Q_0	00	01	11	1
	01	00	10	1
	11	01	01	1
	10	01	01	0

Table 1: Transition and output table

Q_1Q_0	State Label
00	A
01	B
11	C
10	D

Table 2: State table

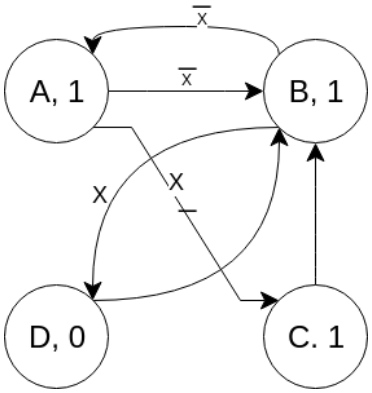

Figure 2: State diagram

2.2 PART 2

In the next part of the experiment, a 2-bit counter circuit that counts from 0 to 2 in a circular way is designed and implemented as shown in the figure below. When X input value is 1, the circuit is counting UP, when X input value is 0, the circuit is counting down. The clock is connected to a debounced push-button.

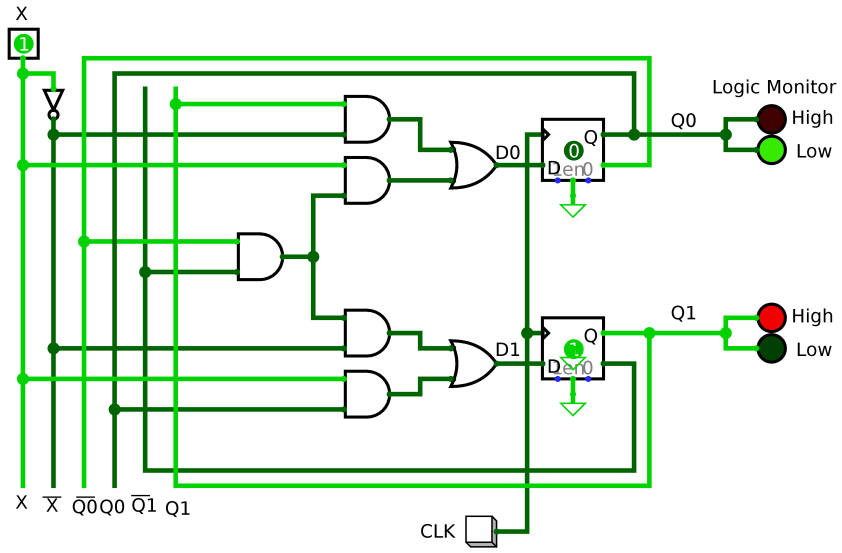

Figure 3: Counter that can count up and down depending on X

$Q_1^+Q_0^+$		X	
		0	1
Q_1Q_0	00	10	01
	01	00	10
	10	01	00
	11	$\phi\phi$	$\phi\phi$

Table 3: State transition table

$Q_1Q_1^+$		X	
		0	1
Q_1Q_0	00	01	00
	01	00	01
	10	10	10
	11	$\phi\phi$	$\phi\phi$

Table 4: Transition of table Q_1

$Q_1Q_1^+$		X	
		0	1
Q_1Q_0	00	α	0
	01	0	α
	10	β	β
	11	$\phi\phi$	$\phi\phi$

Table 5: Transition of table Q_1

$Q_0Q_0^+$		X	
		0	1
Q_1Q_0	00	00	01
	01	10	10
	10	01	00
	11	$\phi\phi$	$\phi\phi$

Table 6: Transition of table Q_0

$Q_0Q_0^+$		X	
		0	1
Q_1Q_0	00	0	α
	01	β	β
	10	α	0
	11	$\phi\phi$	$\phi\phi$

Table 7: Transition of table Q_0

symbol	QQ^+	D
0	00	0
α	01	1
β	10	0
1	11	1

Table 8: D flip-flop transition
ta tab:part 2_d

Expressions of inputs of D flip flops:

$$D_1 = X \cdot Q_0 + \bar{Q_0} \cdot \bar{Q_1} \cdot \bar{X}$$
$$D_0 = \bar{X} \cdot Q_1 + \bar{Q_0} \cdot \bar{Q_1} \cdot X \tag{1}$$

2.3 PART 3

In the final part of the experiment, a counter that counts from 0 to 5 in a circular way is implemented using the 74xx161 IC. Output values are observed using the seven segment display

D_1		X	
		0	1
Q_1Q_0	00	1	0
	01	0	1
	11	$\phi\phi$	$\phi\phi$
	10	0	0

Table 9: Karnaugh diagram for D_1

D_0		X	
		0	1
Q_1Q_0	00	0	1
	01	0	0
	11	$\phi\phi$	$\phi\phi$
	10	1	0

Table 10: Karnaugh diagram for D_0

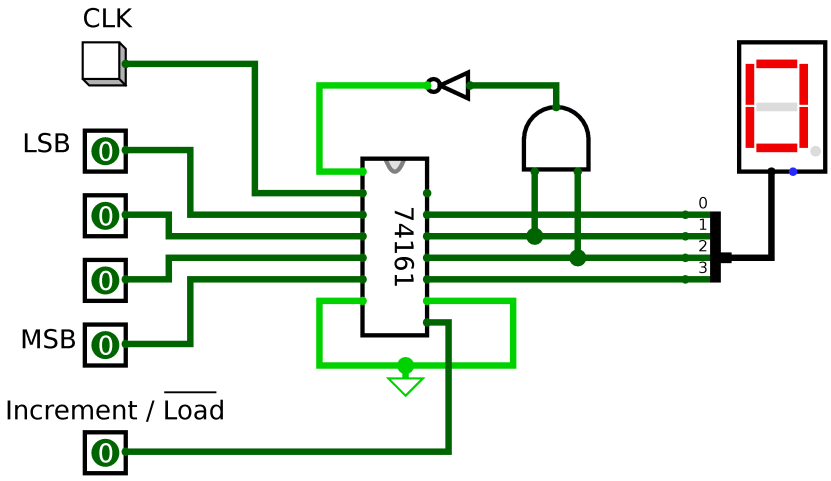

Figure 4: Circuit for counting from 0 to 5

3 INTERPRETATION OF THE RESULTS

For the first part of the experiment, we did implement the circuit without facing any issues. The results we observed were consistent with the truth tables we have constructed beforehand. While implementing part 2 however, we ran into an issue that we couldn't find the resolution to. Our counter could count up but would go from 2 to 0 when counting down and then wouldn't cycle. While doing part 3 of the experiment, we have encountered another rather interesting occurrence. We implemented the counter

that was described in the experiment booklet. It did work when the clock signal was frequent but didn't when it had a really low frequency. A few other lab groups also were having the same issue. We weren't able to determine its reason for sure but we believe it might be caused by different propagation delays of the units used.

4 CONCLUSION

We were not able to finish part 2 of the experiment which we addressed in detail in previous parts. Even though we had an issue with that part, this experiment helped us understand the working mechanism of a counter better.
We also believe that, being more efficient with time will allow us to be more successful in future experiment.

REFERENCES

[1] Istanbul Technical University Department of Computer Engineering. Blg 242e logic circuits laboratory experiments booklet version 1.9, Spring 2019.

[2] Overleaf documentation https://tr.overleaf.com/learn.

[3] Detailed info on writing reports https://projects.ncsu.edu/labwrite/res/res-studntintro-labparts.html.