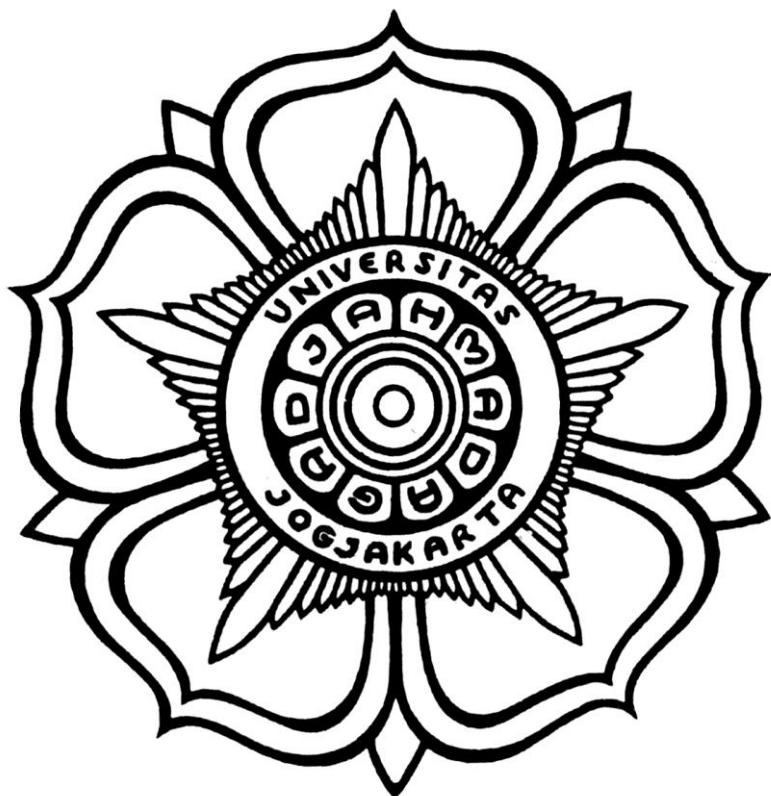


# **Advanced Power Electronics Final Exam**



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## Task 1

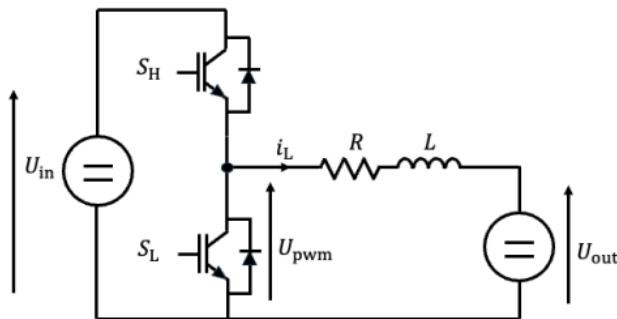
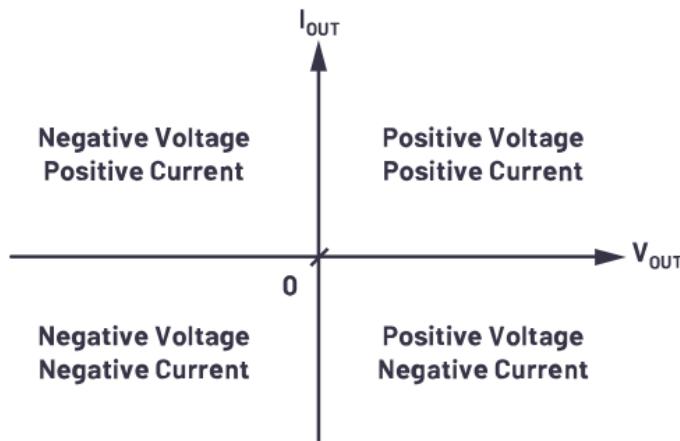


Figure 1 Synchronous Buck Converter

Consider the synchronous buck converter shown in Figure 1. The converter operates in continuous conduction mode (CCM) and has already reached steady-state. The high-side MOSFET  $S_H$  and the low-side MOSFET  $S_L$  are driven by complementary PWM signals. All parameters are specified by yourself.

### 1. Quadrant operation

In a synchronous buck converter, the output voltage remains strictly positive due to the step-down dc–dc conversion topology. Unlike a conventional buck converter that uses a diode, the synchronous implementation employs an actively controlled low-side MOSFET, which provides a bidirectional current path and allows the inductor current to flow in both positive and negative directions. This characteristic enables two-quadrant operation in terms of current. However, under normal continuous conduction mode (CCM) operation without regenerative braking, the inductor current remains positive while the output voltage stays positive. Therefore, the typical operating condition of a synchronous buck converter corresponds to **Quadrant I operation**, where both voltage and current are positive ( $V>0, I>0$ ) (Mohan et al, 2002).



*Figure 2 Four-quadrant voltage converter*

## 2. Determine steady state duty scale ( $d$ )

In steady-state operation of a synchronous buck converter, the average voltage across the inductor over one switching period must be zero in order to maintain a constant inductor current. This condition is known as the **volt second balance principle**.

During the ON interval, when the high-side MOSFET is conducting, the inductor is connected to the input source and the inductor voltage is given by the difference between the input voltage and the output voltage.

During the OFF interval, when the low-side MOSFET is conducting, the inductor voltage becomes negative and is equal to the negative of the output voltage. By applying the volt-second balance over one switching period, a relationship between the duty cycle and the converter voltages can be derived. Solving this relationship shows that the duty cycle of a synchronous buck converter operating in continuous conduction mode is equal to the ratio of the output voltage to the input voltage, confirming the step-down nature of the converter.

$$d = \frac{U_{\text{out}}}{U_{\text{in}}}$$

## 3. Plot waveform $U_{\text{pwm}}$ & $U_L$

The switching behavior of a synchronous buck converter can be analyzed by observing the PWM voltage and the resulting inductor voltage. The PWM voltage  $U_{\text{pwm}}$  is generated by the switching action of the high-side and low-side

MOSFETs and alternates between the input voltage  $U_{in}$  and zero. When the high-side switch is ON, the PWM voltage equals  $U_{in}$ , while during the OFF interval, the low-side switch conducts and the PWM voltage is clamped to zero.

The inductor voltage is defined as the difference between the PWM voltage and the output voltage:

$$u_L(t) = u_{PWM}(t) - U_{out}$$

Thus, during the ON interval, the inductor experiences a positive voltage  $u_L = U_{in} - U_{out}$ , causing the inductor current to increase. During the OFF interval, the inductor voltage becomes negative and equal to

$$u_L = -U_{out}$$

, resulting in a decreasing inductor current. When plotted over several switching cycles, the PWM voltage exhibits a rectangular waveform, while the inductor voltage alternates between two constant levels.

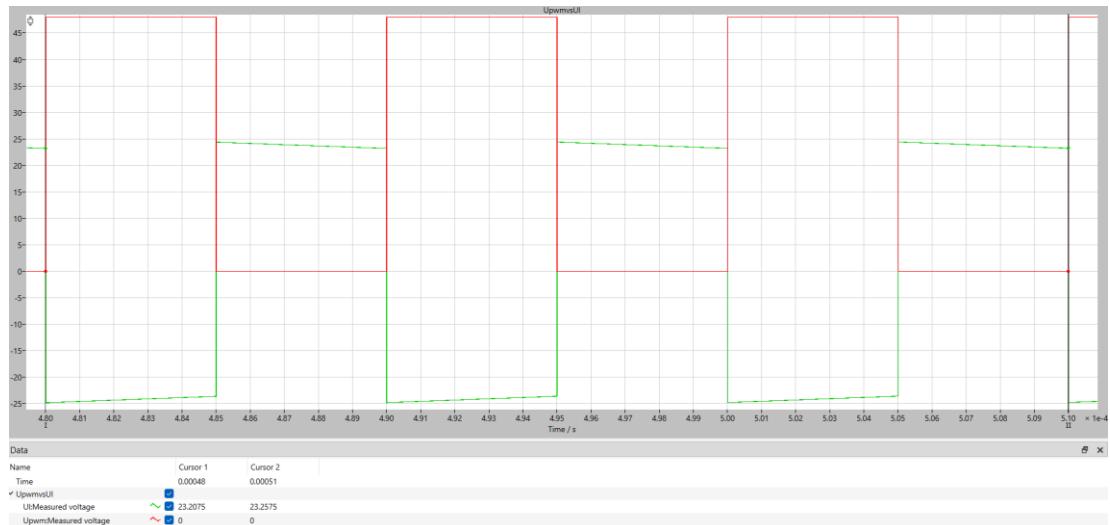


Figure 3 Plot  $U_{PWM}$  and  $U_L$  from PLECS Simulation

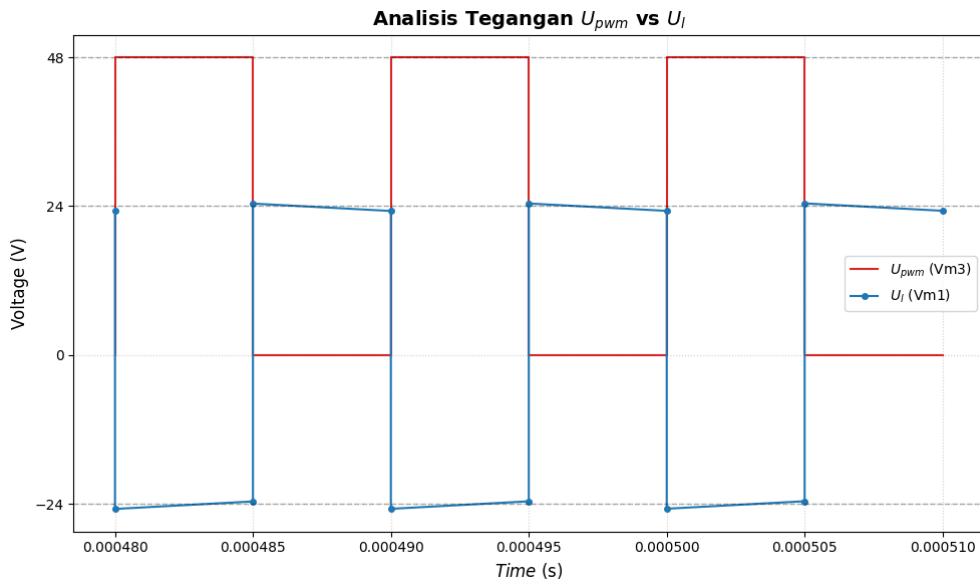


Figure 4 Plot  $U_{pwm}$  and  $U_L$

The PWM voltage  $u_{pwm}$  is a square waveform switching between  $U_{in}$  and 0. The inductor voltage  $u_L = u_{pwm} - U_{out}$  therefore alternates between  $U_{in} - U_{out}$  during the ON interval and  $-U_{out}$  during the OFF interval. This results in a triangular inductor current waveform due to the linear current change imposed by the inductor voltage.

#### 4. $U_L$ relates to the inductor current ripple

The inductor current is governed by the voltage–current relationship:

$$u_L(t) = L \frac{di_L(t)}{dt}$$

Rearranging:

$$\frac{di_L(t)}{dt} = \frac{u_L(t)}{L}$$

This equation shows that the slope of the inductor current is directly proportional to the applied inductor voltage.

In continuous conduction mode, the inductor voltage alternates between two constant values within one switching period  $T_s$ :

- ON interval ( $dT_s$ ):

$$u_L = U_{in} - U_{out}$$

- OFF interval  $((1 - d)T_s)$ :

$$u_L = -U_{out}$$

Over one switching period, the average inductor voltage is:

$$\langle u_L \rangle = \frac{1}{T_s} \int_0^{T_s} u_L(t) dt$$

In steady-state operation:

$$\boxed{\langle u_L \rangle = 0}$$

This condition ensures that the inductor current returns to the same value at the beginning of each switching cycle and does not drift over time.

### **Relation to Inductor Current Ripple**

Although the average inductor voltage is zero, the instantaneous inductor voltage during each switching interval is non-zero. These non-zero voltage levels cause the inductor current to increase and decrease linearly, producing a triangular current ripple.

The peak-to-peak inductor current ripple is obtained by integrating the inductor voltage over the ON interval:

$$\Delta i_L = \frac{1}{L} \int_0^{dT_s} (U_{in} - U_{out}) dt$$

$$\boxed{\Delta i_L = \frac{(U_{in} - U_{out}) d T_s}{L}}$$

Thus, the inductor current ripple is directly proportional to:

- the magnitude of the applied inductor voltage,
- the duration of the switching interval, and inversely proportional to the inductance.

### **5. The ripple of the inductor current $i_L$ at nominal load shall be limited to 5% of the average output current**

- a. We can get an expression for the inductor current ripple like the equation before,

$$\Delta i_L = \frac{1}{L} \int_0^{T_s} (U_{in} - U_{out}) dt$$

$$\boxed{\Delta i_L = \frac{(U_{in} - U_{out}) d T_s}{L}}$$

- b. For a synchronous buck converter operating in continuous conduction mode (CCM), the peak-to-peak inductor current ripple is given by:

$$\Delta i_L = \frac{(U_{in} - U_{out}) d T_s}{L}$$

where the duty cycle is:

$$d = \frac{U_{out}}{U_{in}}$$

The design requirement specifies that the inductor current ripple must not exceed 5% of the average output current:

$$\Delta i_L \leq 0.05 I_{out}$$

with:

$$I_{out} = \frac{U_{out}}{R}$$

By equating the ripple expression to the ripple limit, the minimum inductance is obtained as:

$$\boxed{L_{min} = \frac{(U_{in} - U_{out}) d T_s}{0.05 I_{out}}}$$

$$\boxed{L_{min} = \frac{U_{out}(U_{in} - U_{out}) T_s}{0.05 U_{in} I_{out}}}$$

This inductance ensures that the inductor current ripple does not exceed 5% of the output current under nominal operating conditions.

So from our parameters

- $U_{in} = 48 \text{ V}$
- $U_{out} = 24 \text{ V}$
- $R = 1 \text{ k}\Omega$
- $f_s = 100 \text{ kHz}$

We can get  $L_{min} = 0.1 \text{ H}$

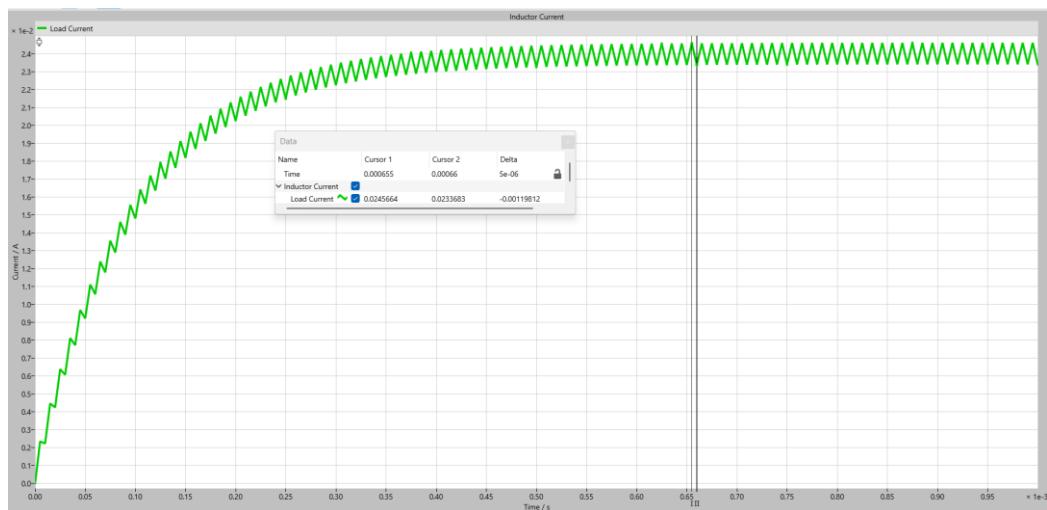


Figure 5 Inductor Current Waveform from PLECS Simulation

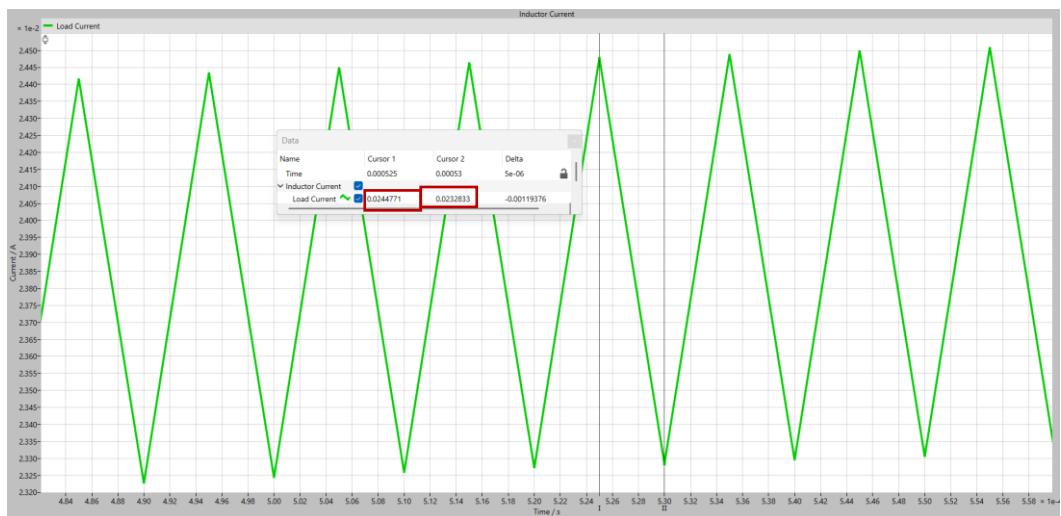


Figure 6 Inductor Current Waveform from PLECS Simulation Zoom

- c. With  $L = 0.1$  H, the peak-to-peak inductor current ripple is:

$$\Delta i_L = 0.0012 \text{ A}$$

The inductor current therefore oscillates around its average value  
 $I_{out} = 0.024 \text{ A}$   
with:

$$i_{L,max} = I_{out} + \frac{\Delta i_L}{2} = 0.024 + 0.0006 = [0.0246 \text{ A}]$$

$$i_{L,min} = I_{out} - \frac{\Delta i_L}{2} = 0.024 - 0.0006 = [0.0234 \text{ A}]$$

Since the inductor current never reaches zero, the converter operates in **continuous conduction mode (CCM)**.

- d. Verification CCM under varying load

- **Nominal load ( $R = 1 \text{ k}\Omega$ )**

$$i_{L,min} = 0.0234 \text{ A} > 0$$

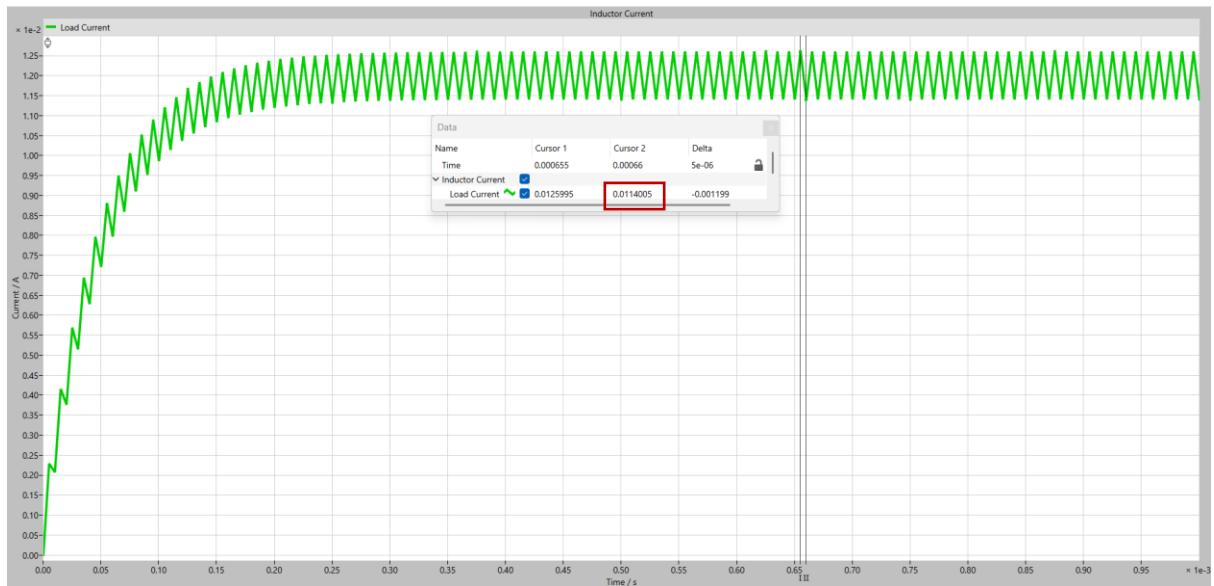
**CCM**

- **50% nominal load ( $R = 2 \text{ k}\Omega$ )**

$$I_{out,50\%} = \frac{24}{2000} = 0.012 \text{ A}$$

$$i_{L,min} = 0.012 - 0.0006 = [0.0114 \text{ A} > 0]$$

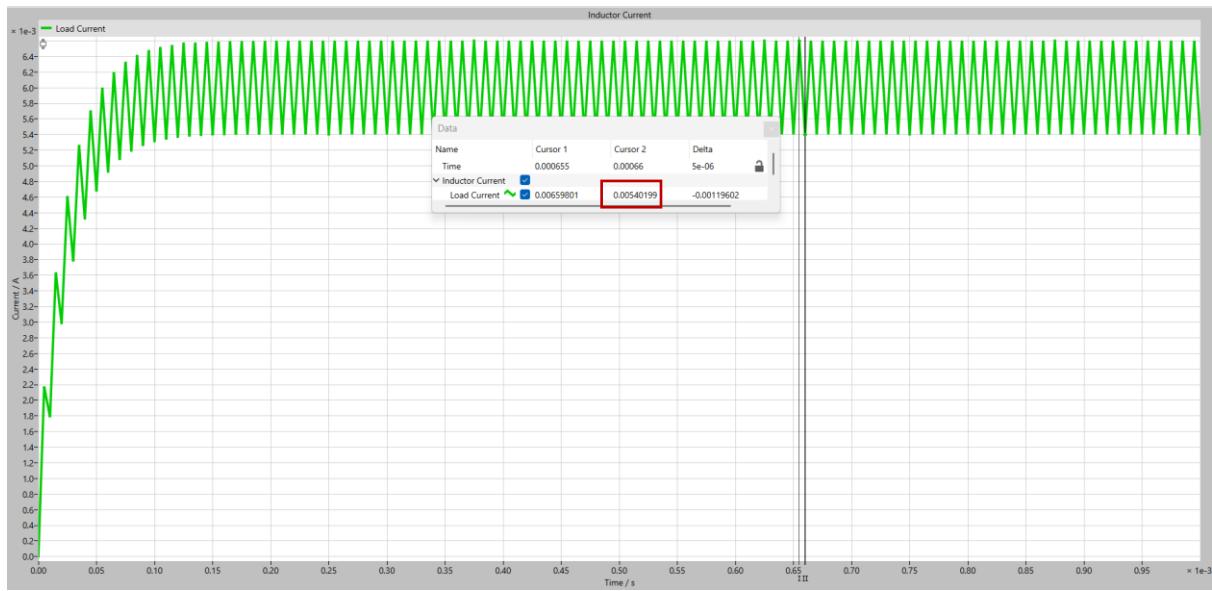
**CCM**



- **25% nominal load ( $R = 4 \text{ k}\Omega$ )**

$$I_{out,25\%} = \frac{24}{4000} = 0.006 \text{ A}$$

$$i_{L,min} = 0.006 - 0.0006 = [0.0054 \text{ A} > 0]$$



## CCM

Using the minimum inductance of 0.1 H derived from the 5% ripple constraint, the synchronous buck converter operates in continuous conduction mode at nominal load as well as at 50% and 25% load conditions.

## Task 2

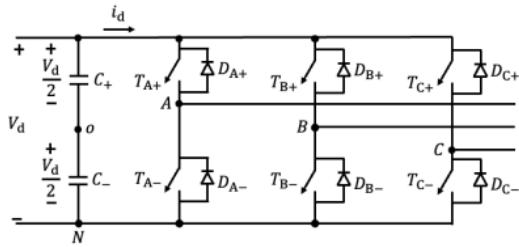


Figure 7 Three Phase inverter

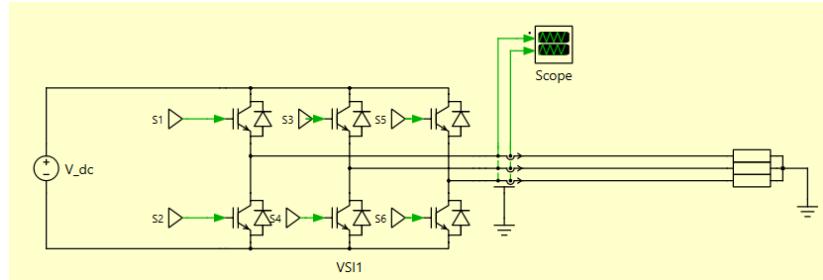


Figure 8 Three phase inverter without filter

This task investigates the operation of a voltage source inverter (VSI) using sinusoidal pulse-width modulation (SPWM). The influence of the modulation index on the inverter output voltage is analyzed in both time and frequency domains. Furthermore, a second-order LC output filter is designed to attenuate switching harmonics while preserving the fundamental component. The improvement in output voltage quality is then verified through simulation.

### 1. Plot output without filter

#### a. Generate the switching waveforms of the output voltage $v_o(t)$ using SPWM.

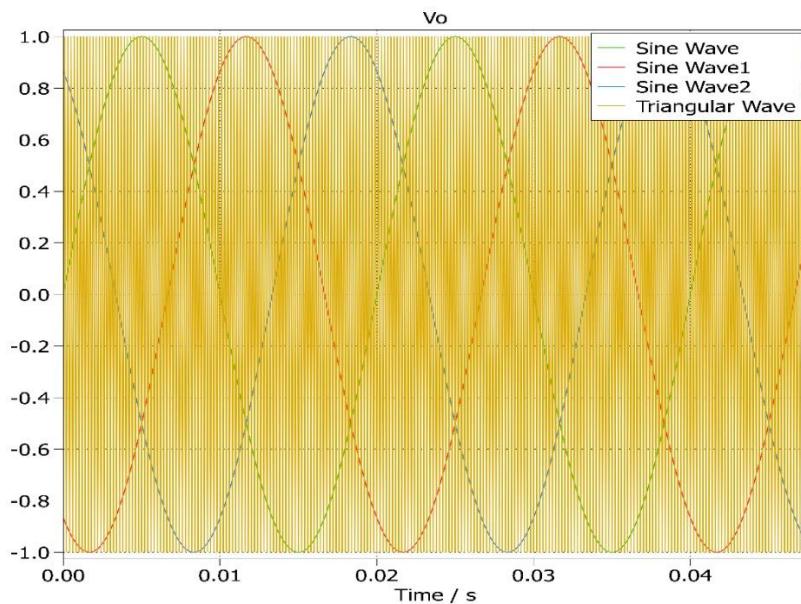
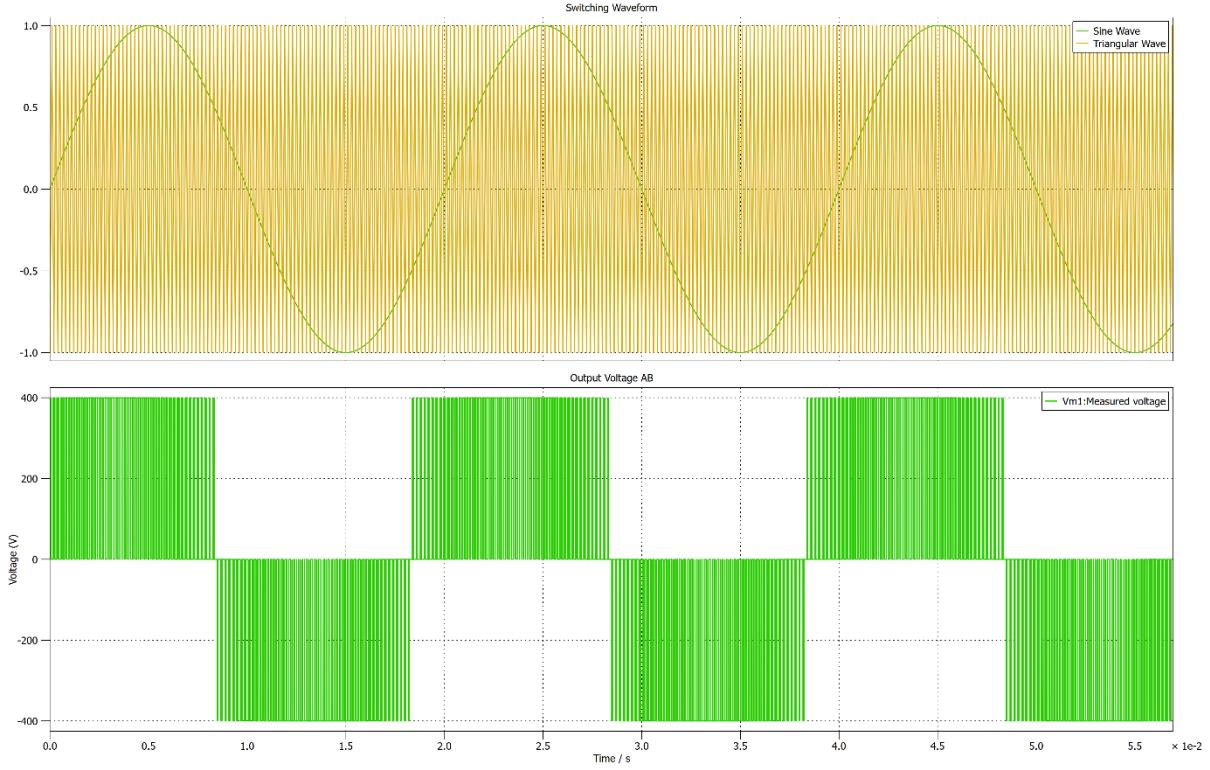
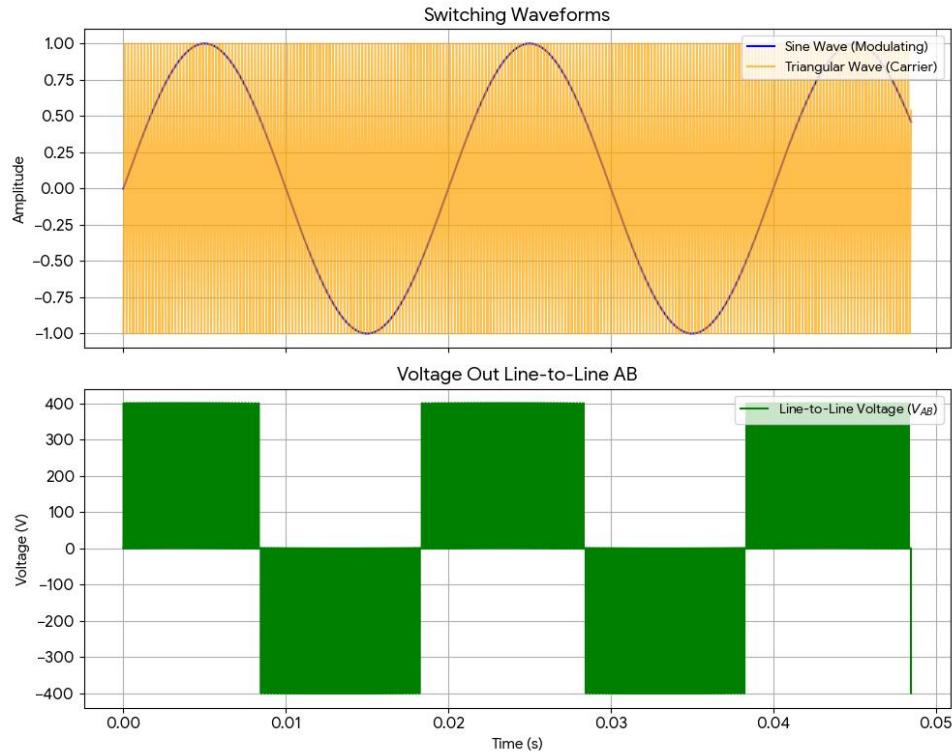


Figure 9 Switching Waveforms



*Figure 10 Switching Waveform and output voltage line to line AB from PLECS simulation*



*Figure 11 Switching Waveform and output voltage line to line AB*

In sinusoidal pulse-width modulation (SPWM), the switching signals of the inverter are generated by comparing a low-frequency sinusoidal reference signal with a high-frequency triangular carrier signal.

The sinusoidal reference signal is defined as:

$$v_{ref}(t) = V_{ref,peak} \sin(2\pi f_1 t)$$

where:

$f_1 = 50$  Hz is the fundamental frequency, and

$V_{ref,peak}$  determines the modulation index.

The carrier signal is a symmetrical triangular waveform with frequency  $f_s$ , which is much higher than the fundamental frequency:

$$f_s \gg f_1$$

At each instant, the reference signal is compared with the carrier signal:

- If  $v_{ref}(t) > v_c(t)$ , the upper switch of the inverter leg is turned ON.
- If  $v_{ref}(t) < v_c(t)$ , the lower switch is turned ON.

This comparison generates a pulse-width-modulated switching signal whose duty ratio varies sinusoidally over time.

As a result, the inverter output voltage  $v_o(t)$  is a two-level waveform that switches between  $+V_{dc}/2$  and  $-V_{dc}/2$  (for a full-bridge inverter). Although the waveform contains high-frequency switching components, its average value over one switching period follows the shape of the sinusoidal reference signal.

The first plot at **Figure 9** shows the three-phase sinusoidal reference signals used for SPWM generation. The signals labeled *Sine Wave 1*, *Sine Wave 2*, and *Sine Wave 3* correspond to phase A, phase B, and phase C, respectively. Each phase has the same amplitude and frequency, while being phase-shifted by  $120^\circ$  with respect to each other, forming a balanced three-phase system.

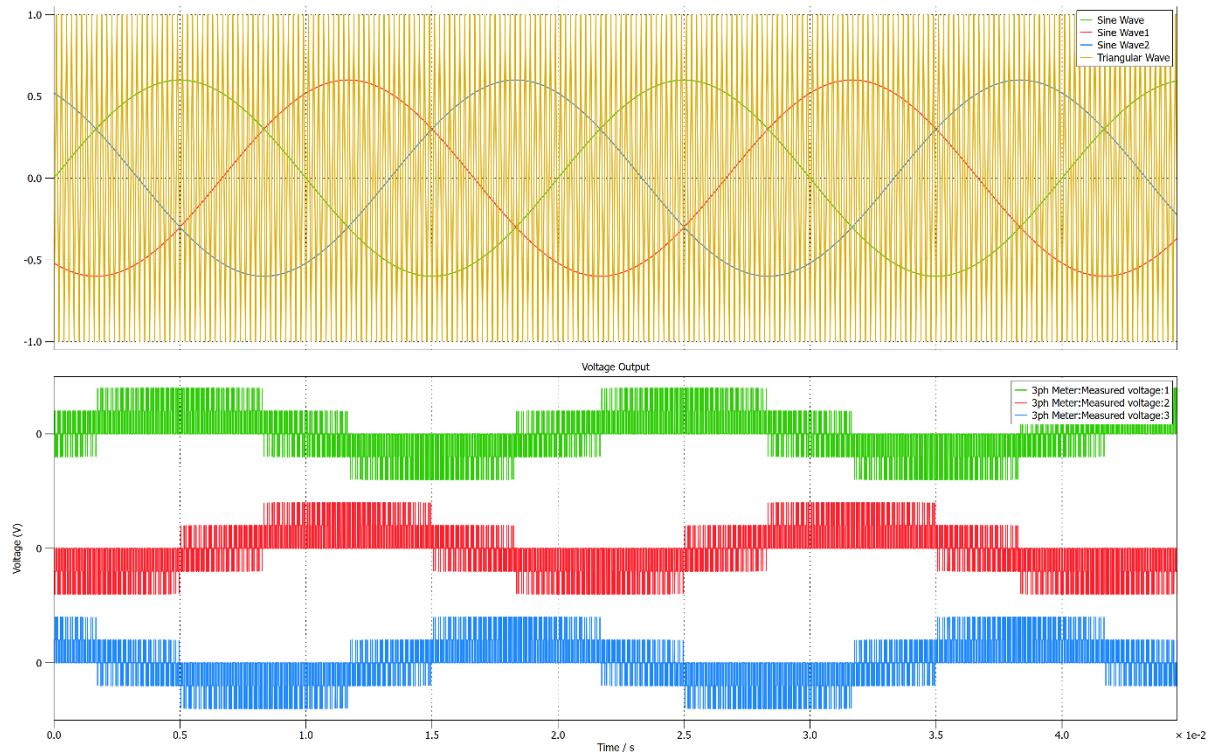
These sinusoidal reference signals are compared with a high-frequency triangular carrier to generate the gating signals for the inverter switches. The relative phase displacement ensures that the resulting inverter output voltages are balanced and symmetrical, which is essential for proper three-phase inverter operation.

The second plot at **Figure 10** compares the sinusoidal voltage of a single phase (phase A) with the corresponding line-to-line voltage  $V_{AB}$ . The phase voltage represents the voltage of phase A with respect to the neutral point, while the line-to-line voltage is obtained as the difference between phase A and phase B voltages:

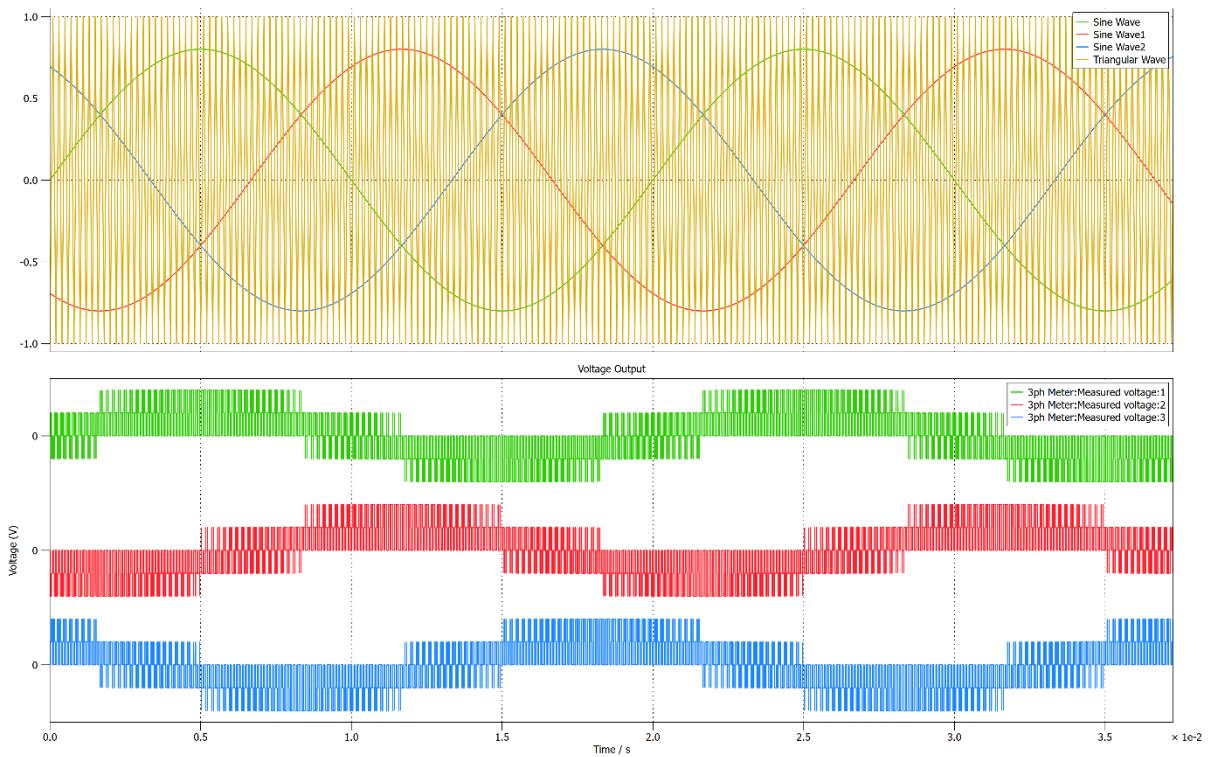
$$V_{AB} = V_A - V_B$$

The line-to-line voltage  $V_{AB}$  exhibits a switching waveform with peak values reaching  $\pm 400$  V, which is equal to the dc-link voltage. This behavior is expected in a two-level VSI, since the line-to-line voltage is obtained from the difference of two phase-leg voltages, each switching between  $\pm V_{dc}/2$ . The sinusoidal fundamental component will be revealed after filtering.

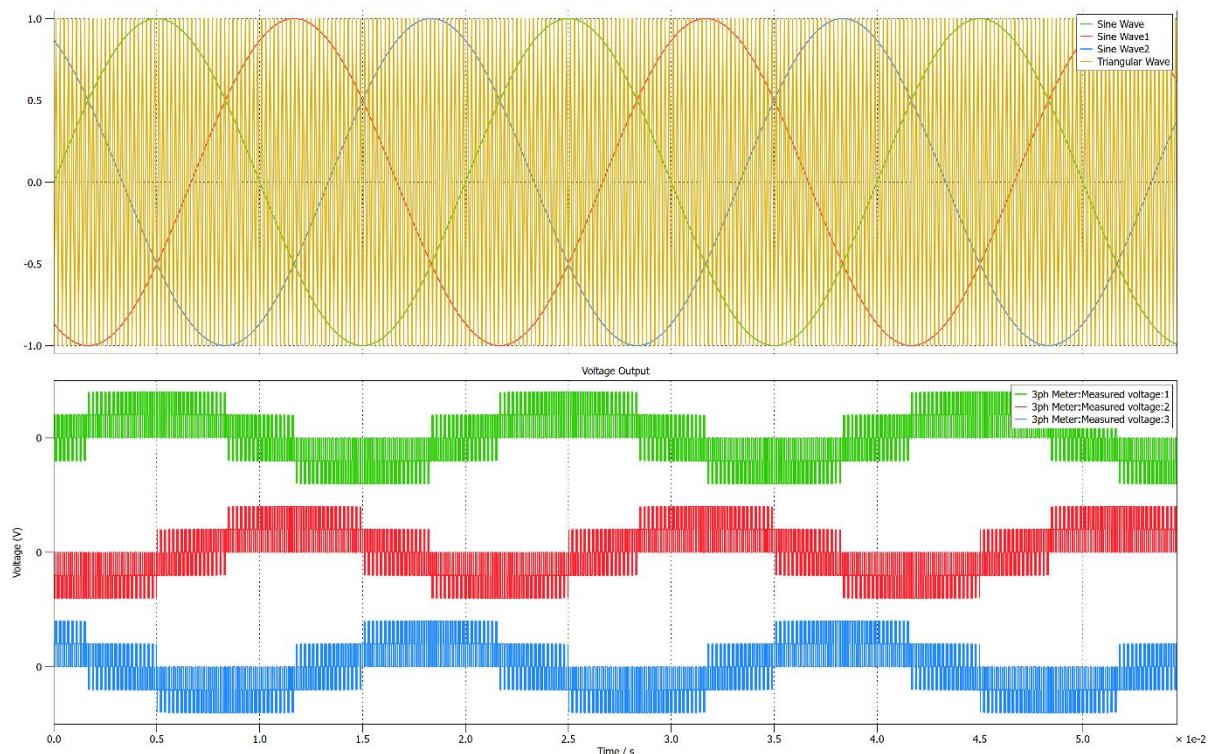
**b. Plot the time domain waveform of the output voltage at diggerent modulation indices  $m_a$**



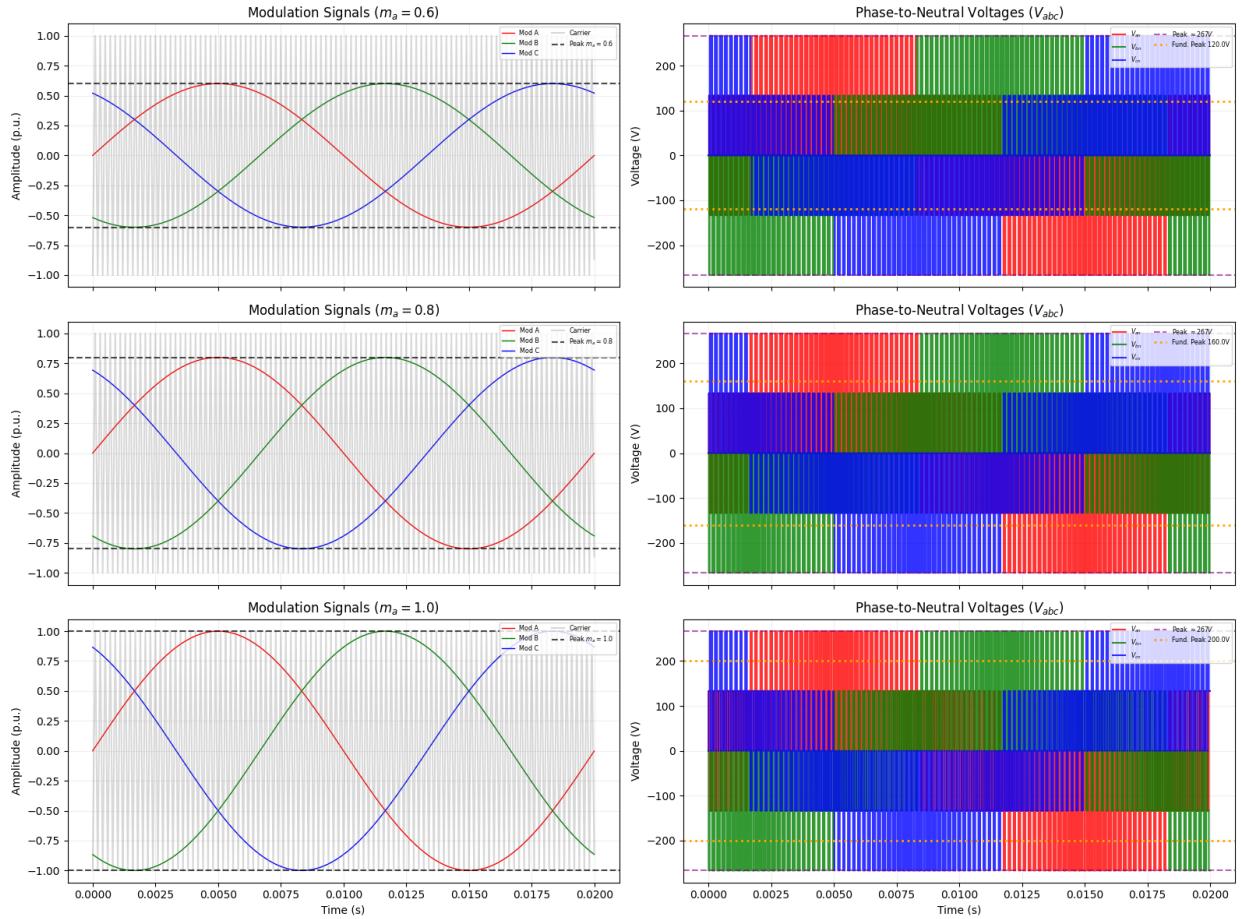
*Figure 12 Plot time domain waveform of the output voltage  $ma = 0.6$*



*Figure 13 Plot time domain waveform of the output voltage  $ma = 0.8$*



*Figure 14 Plot time domain waveform of the output voltage  $ma = 1$*



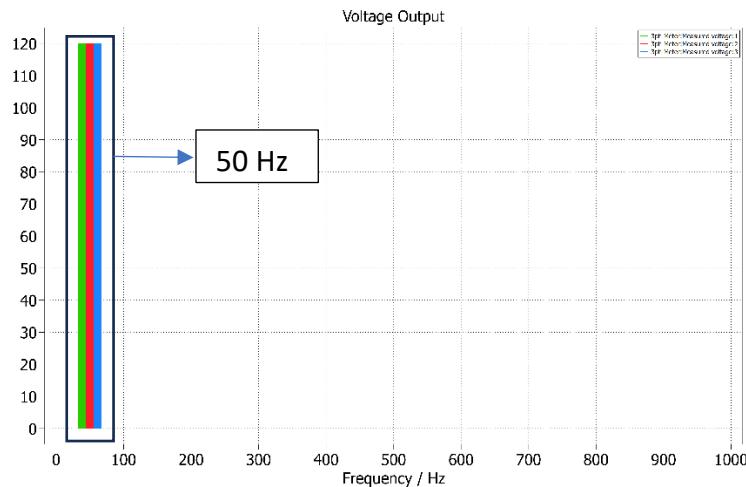
*Figure 15 Merge all plot waveforms modulation 0.6; 0.8, and 1*

The output phase voltage  $v_{aN}(t)$  is plotted in the time domain for different modulation indices without using an output filter. Although the instantaneous peak values remain limited by the DC-link voltage, the effect of the modulation index can be observed in the envelope of the waveform. As the modulation index increases, the amplitude of the fundamental component increases proportionally, while the switching frequency remains unchanged.

Although the peak value of the phase-to-neutral voltage remains constant at  $\pm 266.67$  V for all modulation indices, this behavior is expected because the instantaneous output voltage of a two-level inverter is limited by the DC-link voltage. The effect of the modulation index is reflected in the duty ratio of the switching pulses and consequently in the amplitude of the fundamental component, rather than in the instantaneous peak value.

### c. Frequency domain representation

From the FFT spectrum, as we can see at Figure 15 the fundamental component is clearly identified as the dominant low-frequency peak at 50 Hz. In contrast, the dominant switching harmonics appear as high-frequency spectral clusters centered around the switching frequency and its multiples. These harmonics are inherent to the SPWM process and are well separated from the fundamental component, enabling effective filtering.



*Figure 16 Plot frequency domain fundamental component at 50 Hz*

Component	Frekuensi		
Fundamental	50 Hz	Reference sine	$\propto (m_a)$
Switching harmonics (Erickson, R.W 2020)	$(f_s, 2f_s, \dots)$	PWM	Independen dari $(m_a)$

At this point we use  $f_s = 10000$  Hz, so switching harmonics at Figure 16, dominant at 10000 Hz, 20000 Hz, 30000 Hz, and next.

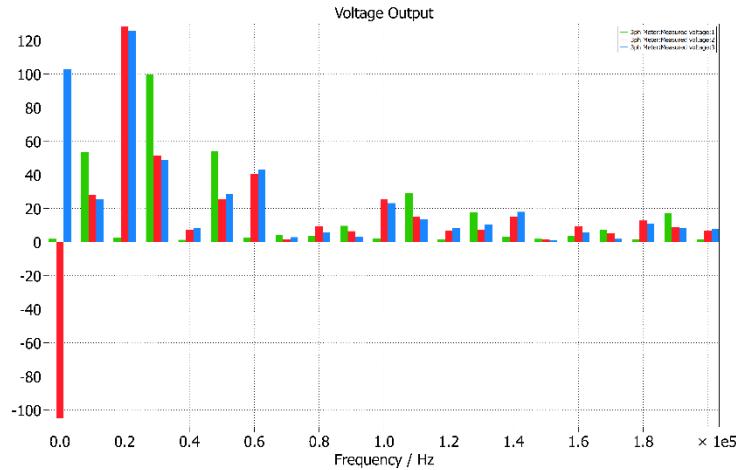


Figure 17 Plot frequency domain of the dominant switching harmonics

## 2. Design a second order output filter

### a. Design objective

A second order LC filter provides a -40 dB/decade roll off after the cutoff frequency.

- **Attenuating Switching Harmonics:** The cutoff frequency ( $f_c$ ) must be significantly lower than the switching frequency ( $f_{sw}$ ) to suppress the PWM carrier noise.
- **Preserving Fundamental:**  $f_c$  must be significantly higher than the fundamental frequency 50 Hz, to avoid phase shifts and voltage drops in the desired output.

### b. Calculation inductor capacitor

**Preserve the fundamental output voltage (50 Hz)** with minimal amplitude and phase distortion.

Therefore, the cutoff frequency of the filter must satisfy:

$$f_{fundamental} \ll f_c \ll f_{switching}$$

Given:

- Fundamental frequency:

$$f_1 = 50 \text{ Hz}$$

- Switching frequency:

$$f_s = 10 \text{ kHz}$$

A common engineering rule:

$$f_c = 10 \times f_1 \text{ and } f_c \leq \frac{f_s}{10}$$

Chosen cutoff frequency:

$$f_c = 1000 \text{ Hz}$$

### LC Filter Transfer Function

For a second-order LC low-pass filter:

$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

Rearranged:

$$\begin{aligned} LC &= \frac{1}{(2\pi f_c)^2} \\ L &= \frac{V_{dc}}{4 \times \Delta I_l \times f_{sw}} \\ L &= \frac{400}{4 \times 2 \text{ A} \times 10000} = 5 \times 10^{-3} \end{aligned}$$

Substitute  $f_c = 1000 \text{ Hz}$ :

$$LC = \frac{1}{(2\pi \cdot 1000)^2 \times 0.005} = 5.07 \times 10^{-6}$$

**Final selected values:**

$$L = 5 \text{ mH}, C = 5 \mu$$

F

### Trade offs

- **Trade-off 1 (Size vs. Performance):** Increasing  $L$  or  $C$  lowers the cutoff frequency (better filtering), but increases the physical size, cost, and weight of the inverter.
  - **Trade-off 2 (Reactive Power):** A larger capacitor improves filtering but draws more reactive current from the inverter, even at no-load, which can reduce efficiency.
- c. Simulate the inverter with filter

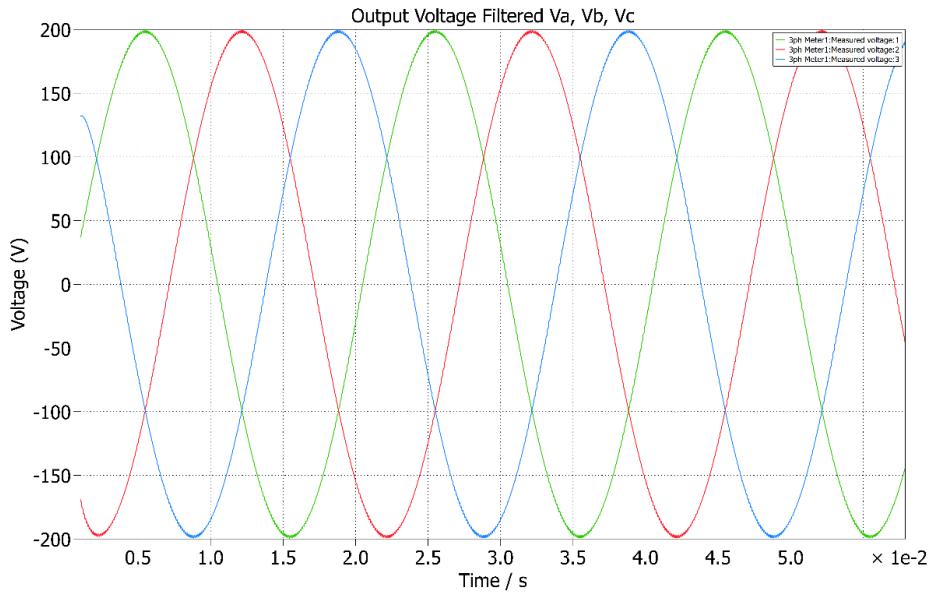


Figure 18 Output voltage filtered

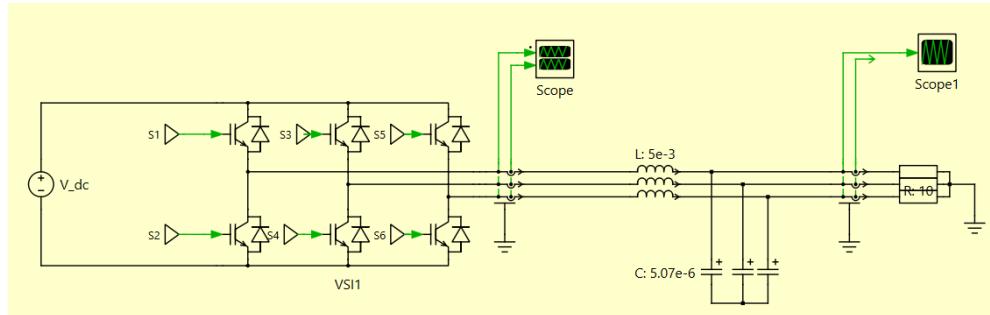


Figure 19 Diagram of three phase inverter with filter

In a three-phase two-level voltage source inverter using sinusoidal pulse-width modulation (SPWM), the amplitude of the **fundamental component** of the phase-to-neutral output voltage is directly proportional to the modulation index  $m_a$ .

The peak value of the fundamental phase-to-neutral voltage is given by:

$$\hat{V}_{an} = m_a \cdot \frac{V_{dc}}{2}$$

For the given system parameters:

- DC-link voltage:  $V_{dc} = 400 \text{ V}$
- Modulation index:  $m_a = 1$

Substituting these values:

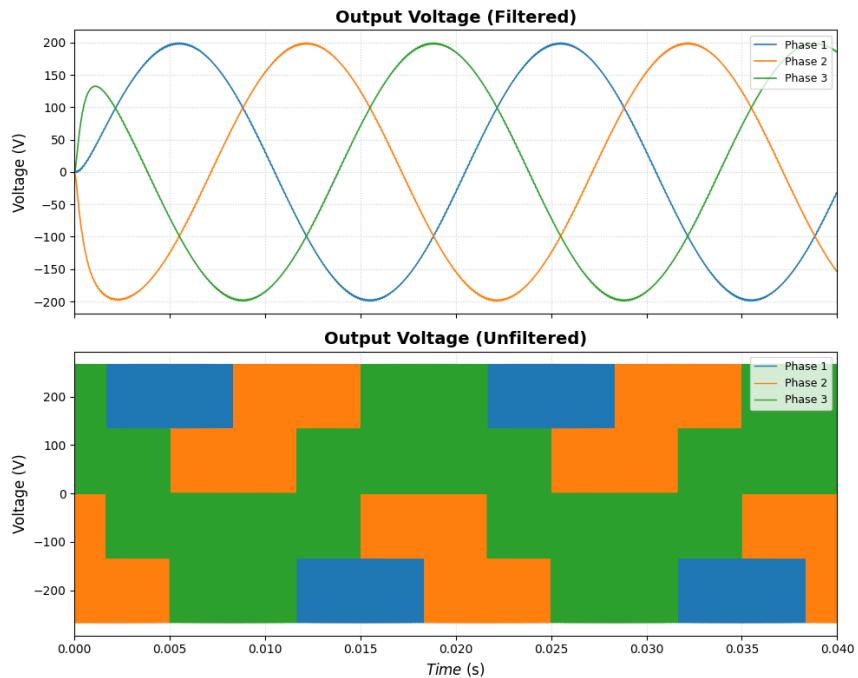
$$\hat{V}_{an} = 1 \cdot \frac{400}{2} = \boxed{200 \text{ V}}$$

This result indicates that when the modulation index reaches unity, the inverter operates at the maximum linear modulation range, and the amplitude of the fundamental phase-to-neutral voltage reaches its highest achievable value without entering overmodulation.

Without the output filter, the inverter phase voltage exhibits a highly distorted waveform characterized by:

- High-frequency switching ripples caused by SPWM.
- Sharp voltage transitions between discrete voltage levels.
- A spectrum dominated by switching harmonics around the carrier frequency and its sidebands.

Although the fundamental component at 50 Hz is present, it is masked by high-frequency components, resulting in poor waveform quality and increased total harmonic distortion (THD).



*Figure 20 Comparison Unfiltered and Filtered Waveforms*

After applying the LC filter, the output voltage waveform becomes nearly sinusoidal. The improvement in waveform quality can be explained as follows:

- The LC filter acts as a low-pass filter that strongly attenuates high-frequency switching harmonics while allowing the fundamental component to pass with minimal attenuation. The second-order filter provides a  $-40$  dB/decade attenuation slope beyond the cutoff frequency, effectively suppressing the switching-frequency components.

- The fundamental frequency (50 Hz) lies well below the cutoff frequency, ensuring that its amplitude and phase are preserved. As a result, the high-frequency voltage ripple observed in the unfiltered waveform is largely eliminated, and the output voltage closely follows an ideal sinusoidal shape.

The peak value of the unfiltered phase voltage reaches  $\pm 266.67$  V, which corresponds to the maximum instantaneous switching voltage of a two-level inverter and is determined by the DC-link voltage. After applying the LC filter, the high-frequency switching components are effectively attenuated, and the output voltage is dominated by the fundamental component. Consequently, the filtered waveform exhibits a reduced peak value of 200 V, which corresponds to the theoretical fundamental phase-to-neutral voltage at a modulation index of  $m_a = 1$ . This behavior confirms the correct operation of both the SPWM strategy and the output filter.

### Task 3

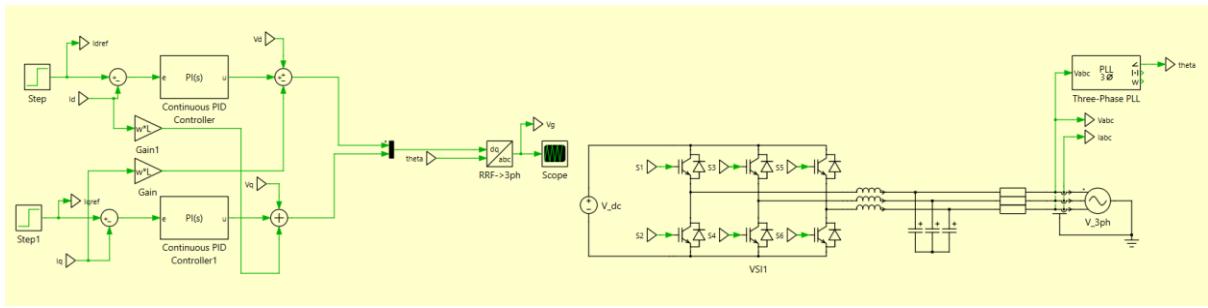


Figure 21 Circuit Diagram of Grid following three phase voltage source inverter with filter

In this task, a grid-following three-phase voltage source inverter (VSI) is designed and simulated. The inverter is connected to the utility grid through an LC filter and synchronized using a Phase-Locked Loop (PLL). A decoupled current control strategy in the synchronous  $dq$ -reference frame is implemented to independently regulate active and reactive power injection.

for  $L$ :

$$L = \frac{\Delta V_L}{\Delta i \cdot f_s}$$

$$\Delta i = 10\% \times 20 = 2 \text{ A}$$

So we can get  $L$  :

$$L = \frac{400}{20,000}$$

$$L = 0.02 \text{ H} = 20 \text{ mH}$$

Find  $C$

$$C = \frac{1}{(2\pi f_c)^2 L}$$

Substitute

$$C = \frac{1}{(2\pi \cdot 500)^2 \cdot 0.02}$$

$$C \approx 5 \mu F$$

Key system parameters:

- DC-link voltage:  $V_{dc} = 800 \text{ V}$
- Grid voltage (phase-to-neutral, RMS):  $220 \text{ V}$
- Grid frequency:  $50 \text{ Hz}$

- Filter inductance:  $L = 20 \text{ mH}$
- Filter capacitor =  $C = 5 \mu\text{H}$
- resistance:  $R = 1 \Omega$
- Reference frame aligned with grid voltage (PLL)

In the synchronous reference frame, the inverter output voltage equations are given by:

$$\begin{aligned} u_d &= -\omega L i_q + R i_d + u_{gd} \\ u_q &= \omega L i_d + R i_q + u_{gq} \end{aligned}$$

To achieve decoupled control, the cross-coupling terms  $\pm\omega L i$  and the grid voltage feedforward terms are compensated in the controller.

### 1. Current tracking performance in the dq-axis

The current tracking performance in the synchronous dq reference frame is evaluated by comparing the measured currents  $i_d$  and  $i_q$  with their respective reference values. The simulation results show that the d-axis current accurately tracks its reference with fast transient response and negligible steady-state error. Meanwhile, the q-axis current remains close to its reference value, indicating effective decoupling between the two axes. These results confirm the effectiveness of the PI-based current controller and the proper operation of the PLL.

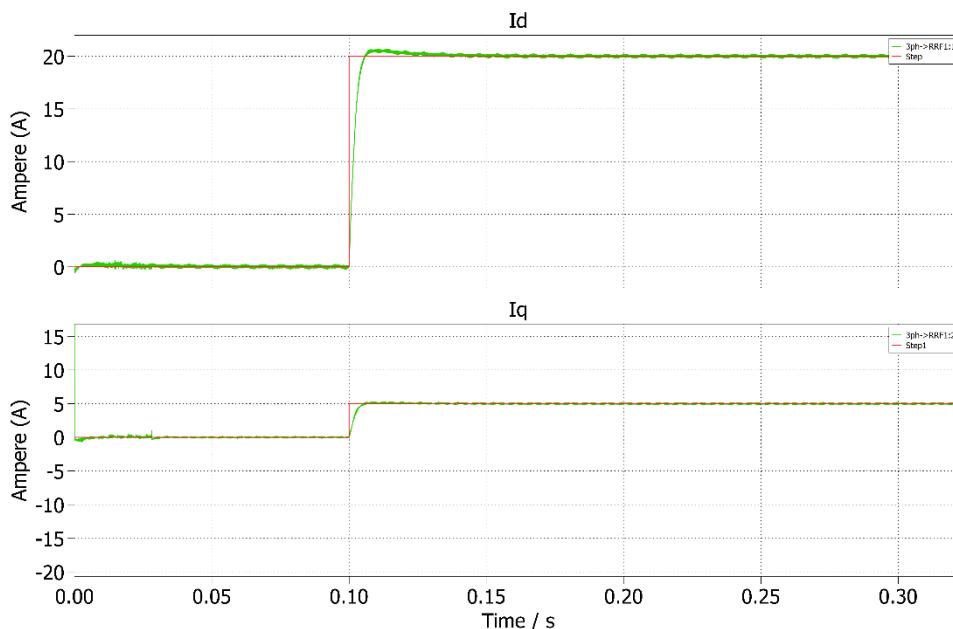


Figure 22 Plot Id Iq current tracking

To evaluate the current tracking performance of the grid-following inverter, step changes are applied to the current references in the synchronous dq reference frame.

The reference currents are defined as:

- d-axis current reference:

$$i_{d,ref} = 20 \text{ A}$$

- q-axis current reference:

$$i_{q,ref} = 5 \text{ A}$$

At the beginning of the simulation ( $t < 0.1$  s), both current references are set to zero. At  $t = 0.1$  s, step changes are applied simultaneously to  $i_{d,ref}$  and  $i_{q,ref}$ .

The grid voltage and frequency remain constant during this test, and the phase-locked loop (PLL) is assumed to be locked, ensuring proper alignment of the dq reference frame with the grid voltage.

### **d-axis Current Tracking**

After the step change at  $t = 0.1$  s, the measured d-axis current  $i_d$  increases rapidly and converges to the reference value of 20 A. The transient response is characterized by:

- Fast rise time
- Minimal overshoot
- Negligible steady-state error

This behavior indicates that the current controller effectively regulates the active power component of the inverter current.

### **q-axis Current Tracking**

Similarly, the q-axis current  $i_q$  follows its reference value of 5 A after the step at  $t = 0.1$  s. The tracking response demonstrates:

- Stable convergence to the reference
- Minimal interaction with the d-axis current
- Absence of oscillatory behavior

The accurate tracking of  $i_q$  confirms the proper functioning of the decoupling terms in the dq current controller, allowing independent control of active and reactive current components.

## 2. Disturbance rejection capability under grid voltage variations

In this scenario, a voltage disturbance is introduced on the grid side while the current references remain unchanged.

- Initial grid voltage (peak):

$$V_g = 311 \text{ V}$$

- Disturbed grid voltage (peak):

$$V_g = 280 \text{ V}$$

- Disturbance time:

$$t = 0.2 \text{ s}$$

The voltage drop corresponds to a grid sag of approximately:

$$\frac{311 - 280}{311} \times 100\% \approx 10\%$$

The current references are maintained at:

$$i_{d,ref} = 20 \text{ A}, i_{q,ref} = 5 \text{ A}$$

When the grid voltage drops at  $t = 0.2 \text{ s}$ , the following behavior is observed:

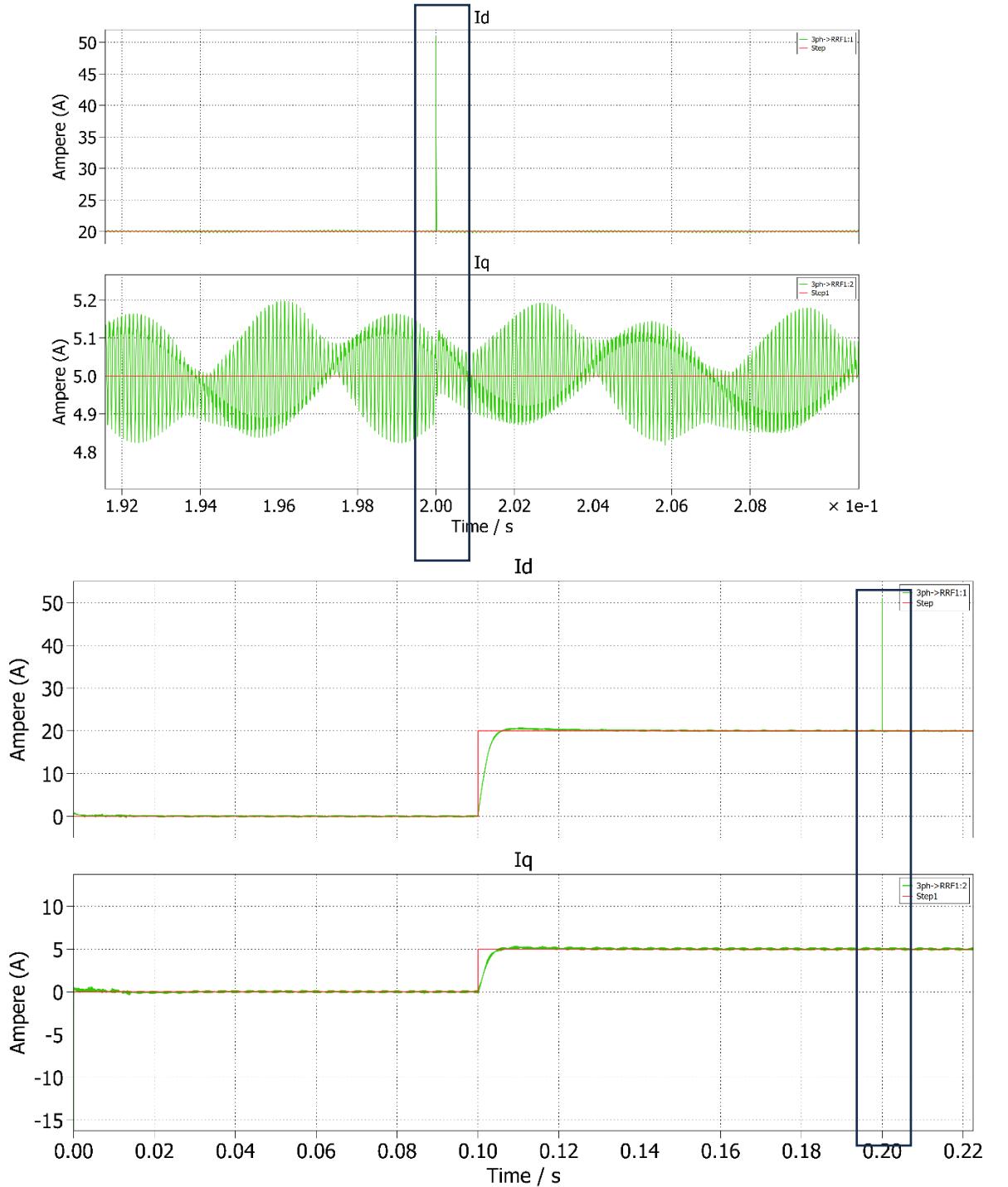


Figure 23  $I_d$   $I_q$  plot when under grid voltage variations

#### d-axis Current Response

The d-axis current  $i_d$  experiences a brief transient deviation immediately after the voltage disturbance. However, the current controller rapidly compensates for the reduced grid voltage by adjusting the inverter output voltage reference. As a result:

- $i_d$  quickly returns to its reference value of 20 A

- Steady-state tracking accuracy is preserved
- No sustained oscillations are observed

This confirms that the controller effectively regulates the active current component despite variations in grid voltage magnitude.

### **q-axis Current Response**

Similarly, the q-axis current  $i_q$  remains well regulated following the voltage drop. After a short transient:

- $i_q$  converges back to its reference value of 5 A
- Cross-coupling effects between the d- and q-axes remain minimal

This behavior demonstrates that the decoupling terms in the current controller remain effective under grid voltage disturbances.

The ability of the inverter to maintain accurate current tracking during a grid voltage sag indicates strong disturbance rejection capability. Although the grid voltage magnitude decreases, the current controller compensates by modifying the commanded inverter voltage, thereby maintaining the desired current injection into the grid.

## **3. Steady state current ripple**

In steady state, the dq-axis currents exhibit small high-frequency oscillations superimposed on their average values. These oscillations are primarily caused by:

- The finite switching frequency of the inverter.
- Residual switching harmonics not fully eliminated by the LC filter.
- Discretization effects in the digital control implementation.

### **a. d-axis Current Ripple**

The d-axis current  $i_d$  oscillates around its reference value of 20 A with a small peak-to-peak ripple. The ripple magnitude is significantly smaller than the average current, indicating effective attenuation of switching harmonics.

This behavior confirms that the LC filter and current controller work together to smooth the injected active current.

### **b. q-axis Current Ripple**

Similarly, the q-axis current  $i_q$  exhibits a small steady-state ripple around its reference value of 5 A. The ripple level remains low and does not affect the mean value of the reactive current, demonstrating stable and accurate reactive power control.

In steady state, the d-axis current exhibits a small peak-to-peak ripple of approximately 0.3 A around its average value of 20 A, corresponding to a ripple of about 3%. Similarly, the q-axis current shows a peak-to-peak ripple of approximately 0.3 A around its reference value of 5 A. These ripple levels are sufficiently small and indicate effective suppression of switching harmonics by the LC filter and current controller.

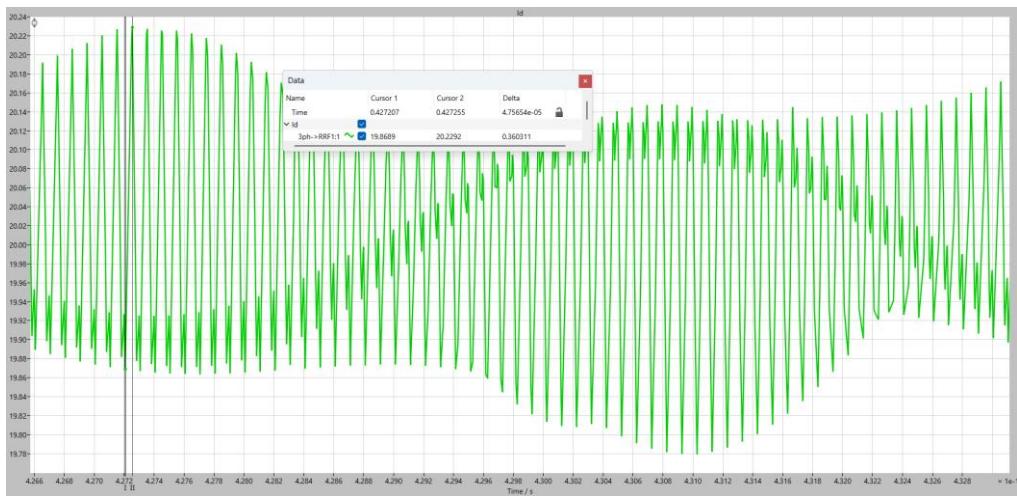


Figure 24  $Id$  ripple plot

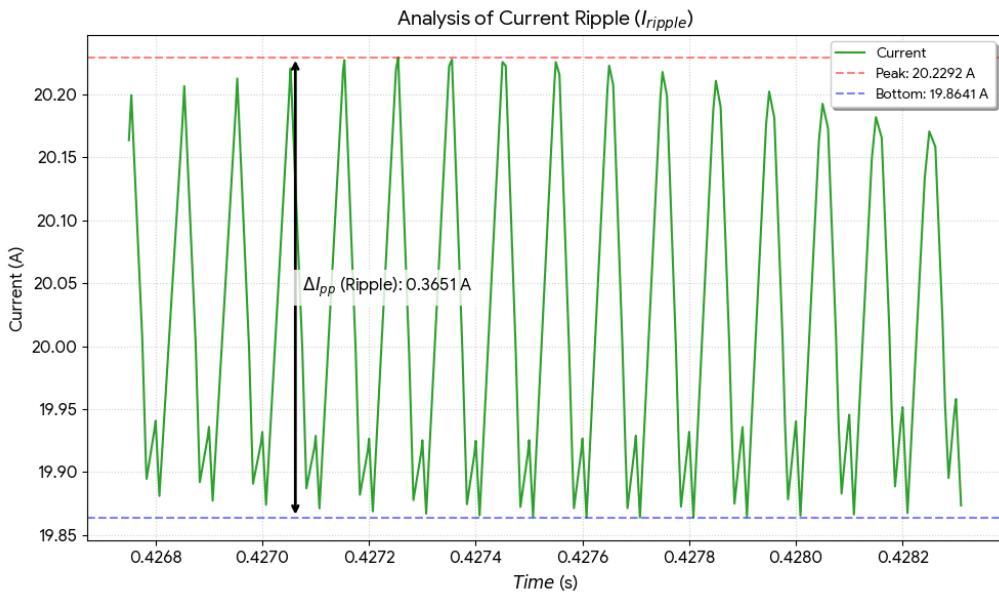


Figure 25 Peak to peak  $Id$  Current

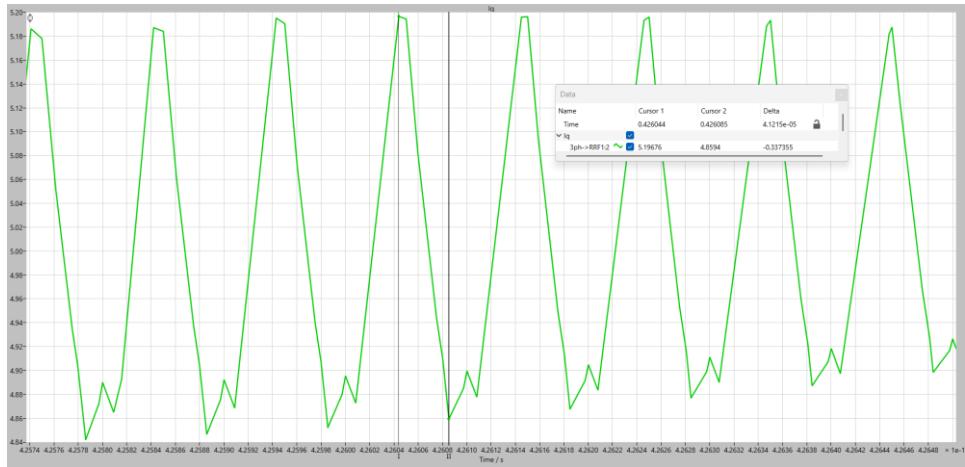


Figure 26  $I_q$  ripple plot

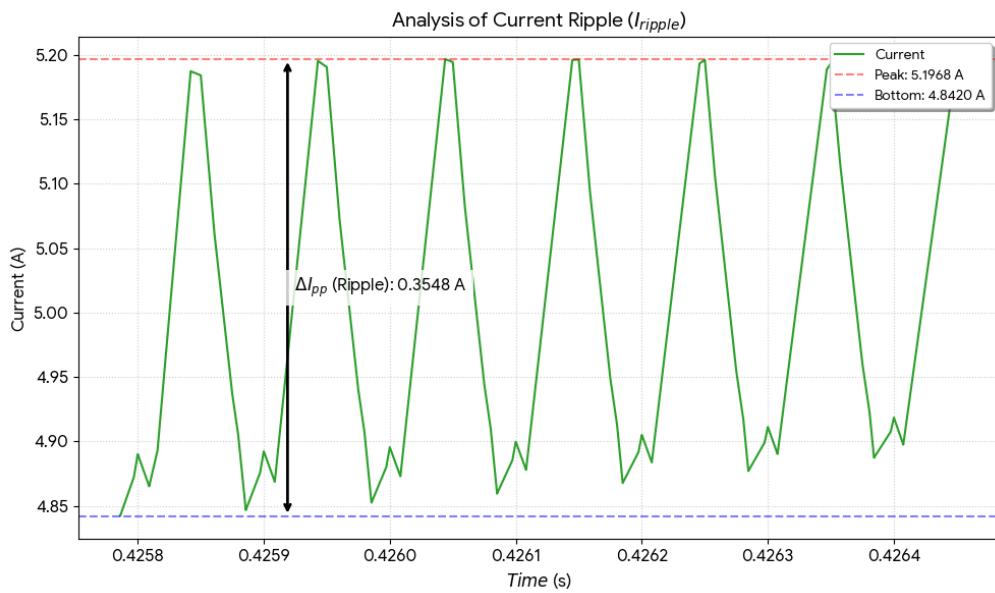


Figure 27  $I_q$  ripple Peak to peak

#### 4. Closed loop response to a load step from 50% to 100%

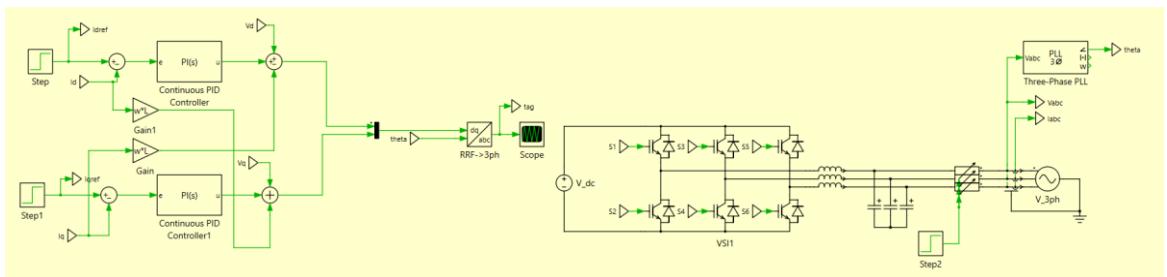


Figure 28 Diagram Circuit of closed loop response

A load change is applied at  $t = 0.5$  s, where the equivalent load resistance is reduced from:

$$1 \Omega \rightarrow 0.5 \Omega$$

This load step causes a transient variation in the inverter output current as we can see at Figure 29. Immediately after the disturbance, deviations in the dq-axis currents are observed. However, the current controller responds rapidly and restores the currents to their reference values.

The d-axis current shows a short transient before stabilizing, while the q-axis current remains well regulated, indicating effective decoupling. The system remains stable throughout the load change, demonstrating robust closed-loop performance under load variations.

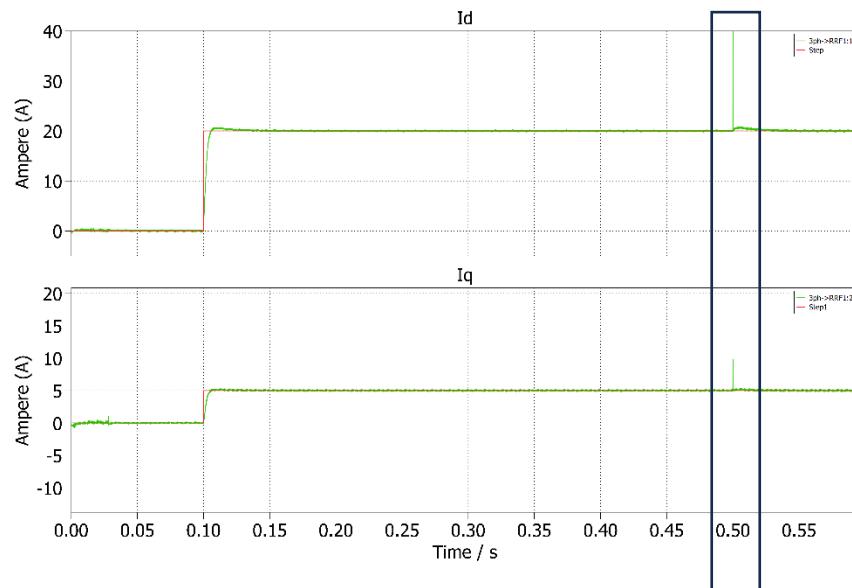


Figure 29 Plot  $I_d$  and  $I_q$  at load step

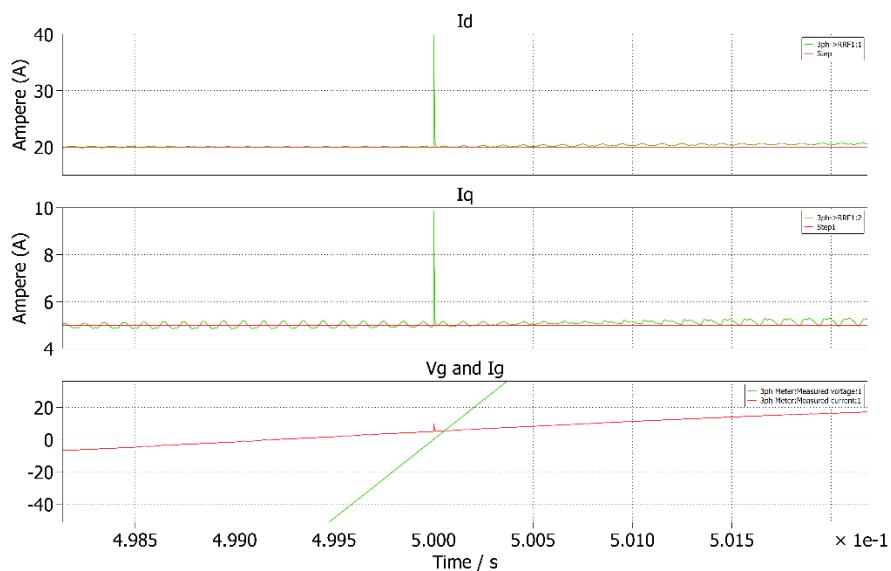


Figure 30 A load change is applied at  $t = 0.5$  s

## 5. Inverter operation at unity power factor, as well as leading lagging power factor

In grid-connected voltage source inverters (VSI), the capability to operate at different power factors is achieved through the independent control of active and reactive power. This is typically implemented using a Synchronous Reference Frame (dq-axis) control strategy. In this control structure, the grid current is decomposed into two orthogonal components: the direct-axis current ( $I_d$ ) and the quadrature-axis current ( $I_q$ ). The  $I_d$  component is responsible for regulating the active power (P) transferred to the grid, while the  $I_q$  component directly governs the reactive power exchange (Q). This decoupling allows the inverter to mimic the behavior of a capacitor or an inductor purely through software control, without changing physical components (Xiao, et al 2025).

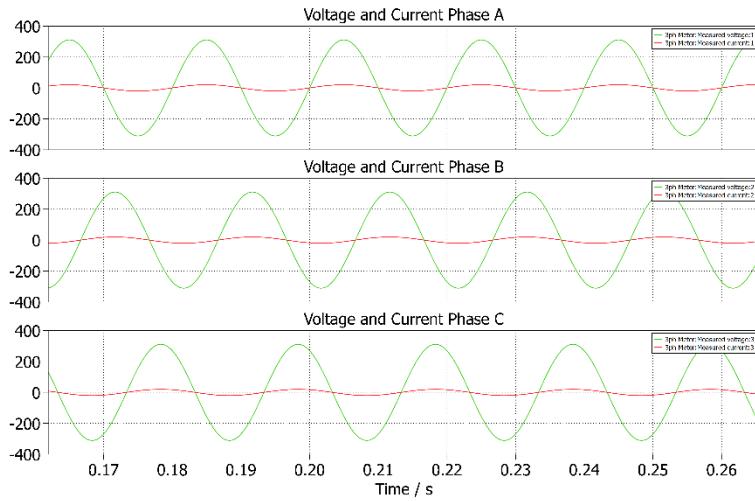
To achieve **Unity Power Factor** operation, the control system is designed to inject only active power into the grid. Mathematically, this corresponds to maintaining the reactive power exchange at zero. In the simulation, this is realized by setting the reference value for the quadrature current ( $I_{q\_ref}$ ) to zero. Under these conditions, the output current waveform is perfectly synchronized with the grid voltage waveform. The peaks and zero-crossings of both signals align precisely, indicating that the inverter appears as a purely resistive load or source to the grid.

For **Lagging and Leading Power Factor** operations, the inverter is instructed to exchange reactive power with the grid to support voltage stability. To simulate a lagging power factor (inductive mode), the controller is given a non-zero reference for  $I_q$ . Depending on the specific coordinate transformation used, a **positive**  $I_{q\_ref}$  will cause the inverter to inject reactive power, resulting in the current waveform shifting to the right so that it lags behind the voltage waveform.

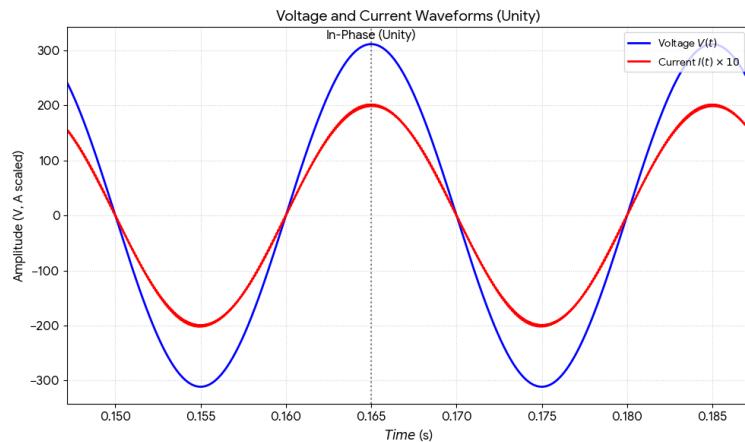
Conversely, for a leading power factor (capacitive mode), **the  $I_{q\_ref}$  is set to a negative value**. This causes the current waveform to shift to the left, peaking before the grid voltage. This flexibility demonstrates the inverter's ability to provide ancillary services, such as reactive power compensation, which is a significant advantage over traditional synchronous generators.

### Change value $I_{q\_ref}$ :

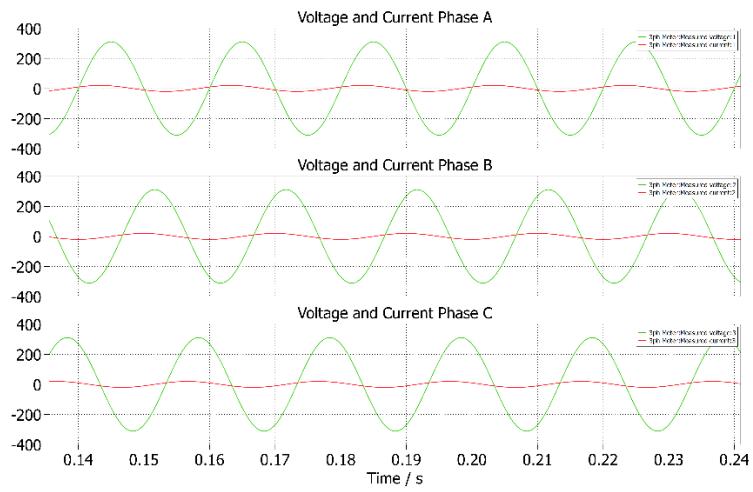
- **For Unity PF:** Set  $I_{q\_ref} = 0$ .
- **For Lagging PF:** Change  $I_{q\_ref}$  to be positive value +5 A.
- **For Leading PF:** Change  $I_{q\_ref}$  to be negative value -5 A.



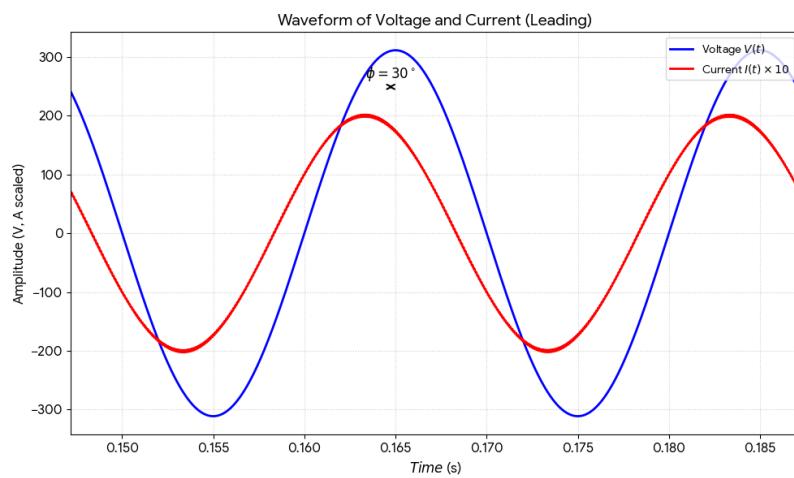
*Figure 31 Voltage and Current Waveforms per phase A, B, and C Unity*



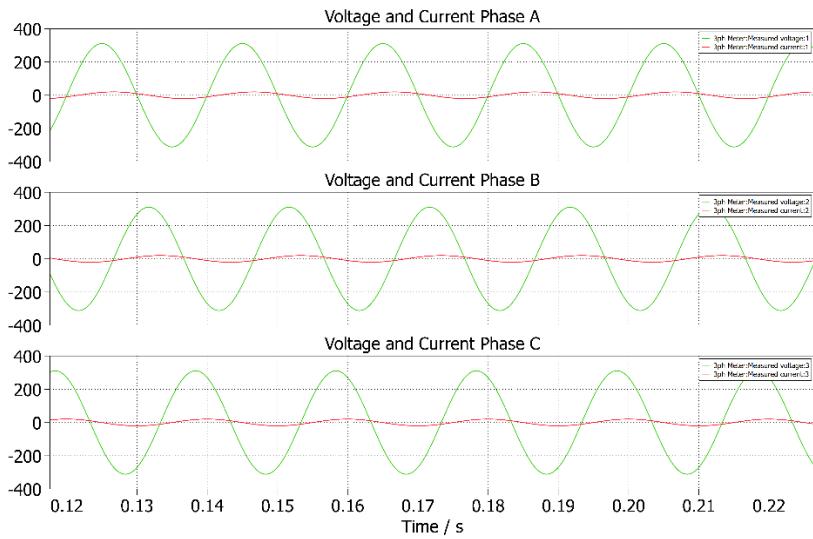
*Figure 32 Voltage and Current Waveforms Unity*



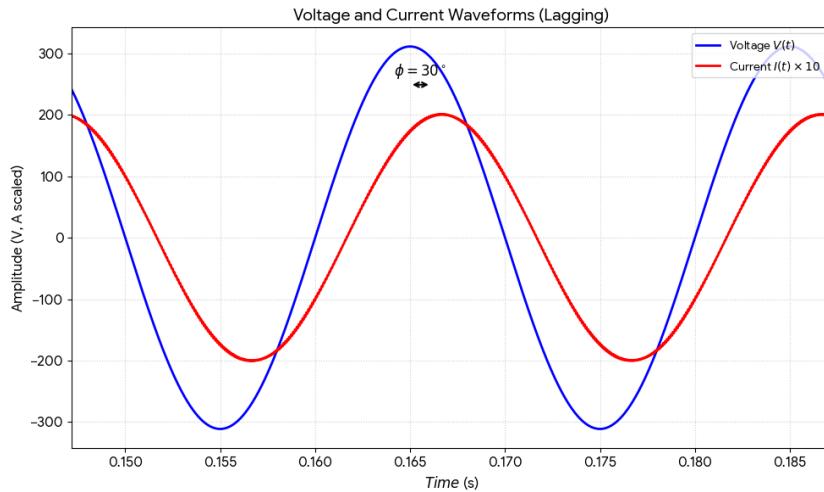
*Figure 33 Voltage and Current Waveforms per phase A, B, and C Leading*



*Figure 34 Voltage and Current Waveforms Leading*



*Figure 35 Voltage and Current Waveforms per phase A, B, and C Lagging*



*Figure 36 Voltage and Current Waveforms Lagging*

## 6. Phasor diagram

In the analysis of AC power systems, phasors (phase vectors) are utilized to represent sinusoidal waveforms of voltage and current. A phasor is a rotating vector where the length represents the magnitude (amplitude or RMS value) of the signal, and the angle represents its phase relative to a reference. In the context of a Grid-Connected Inverter, the Grid Voltage ( $V_g$ ) is typically aligned with the direct axis (d-axis) of the Synchronous Reference Frame, serving as the reference phasor with an angle of  $0^\circ$ .

The control of the inverter is implemented using the  $dq$ -axis decoupling method. This strategy allows for the independent control of active and reactive power by decomposing the grid current into two orthogonal components (Xiao et al, 2025):

- **$I_d$  (Direct-axis current):** Responsible for active power ( $P$ ) transfer.
- **$I_q$  (Quadrature-axis current):** Responsible for reactive power ( $Q$ ) exchange.

Unity Power Factor ( $\text{PF} = 1.0$ ) represents the ideal condition for active power transmission. In this mode, the inverter acts as a purely resistive load or source. Physically, the current phasor is perfectly aligned with the voltage phasor, meaning there is zero phase shift ( $\theta = 0^\circ$ ). In the control simulation, this is achieved by setting the quadrature current reference,  $I_{q\_ref}$ , to zero. Consequently, the total current consists solely of the active component ( $I_{total} = I_d$ ). In the time-domain waveforms, the zero-crossings and peaks of the current signal occur at the exact same instant as those of the grid voltage.

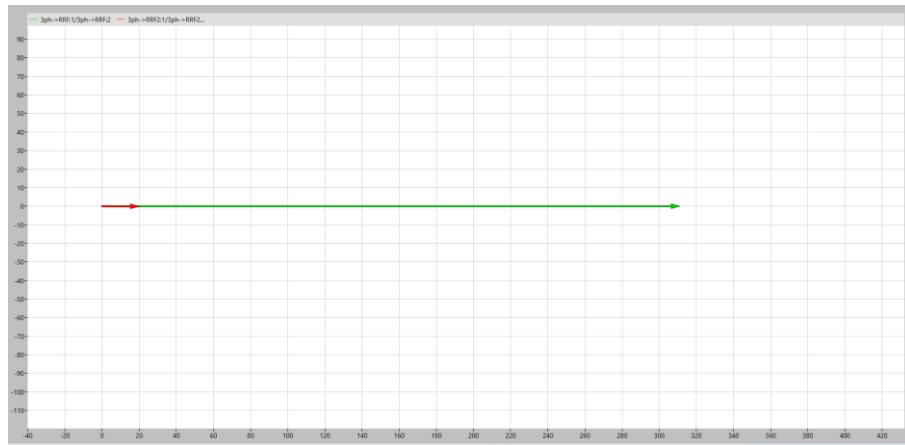
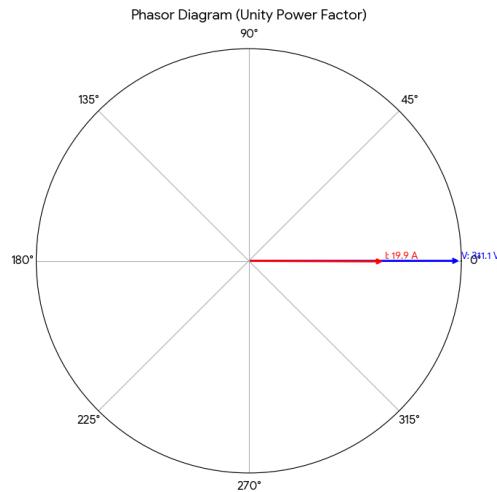


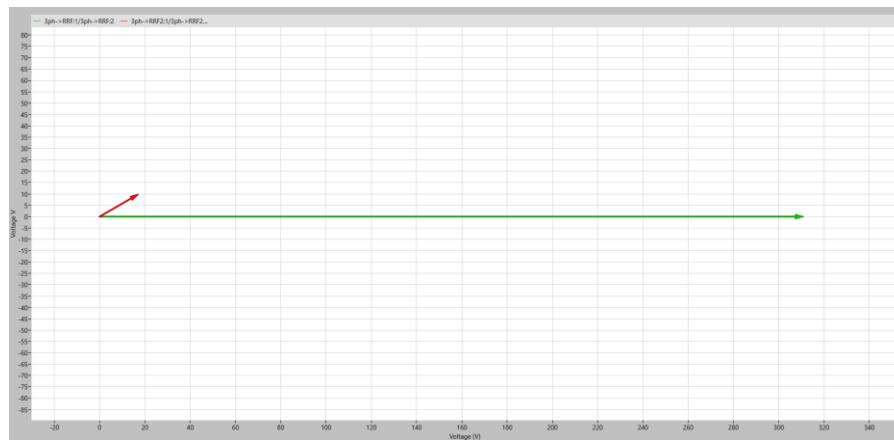
Figure 37 Phasor Diagram Unity



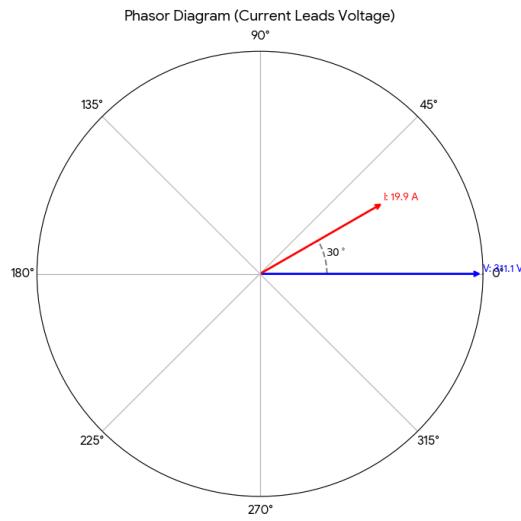
*Figure 38 Phasor Diagram Unity*

Leading Power Factor occurs when the inverter mimics a capacitive element. In this operational mode, the current phasor rotates ahead of the voltage phasor. This is typically used when the grid requires voltage suppression or when the inverter needs to compensate for other inductive loads on the network.

In the control loop, this is implemented by applying an  $I_{q\_ref}$  with the opposite sign to that of the lagging mode. This causes the total current vector to shift counter-clockwise, leading the voltage vector. In the time-domain simulation, the peaks of the current waveform will appear to the left of (or before) the voltage peaks.



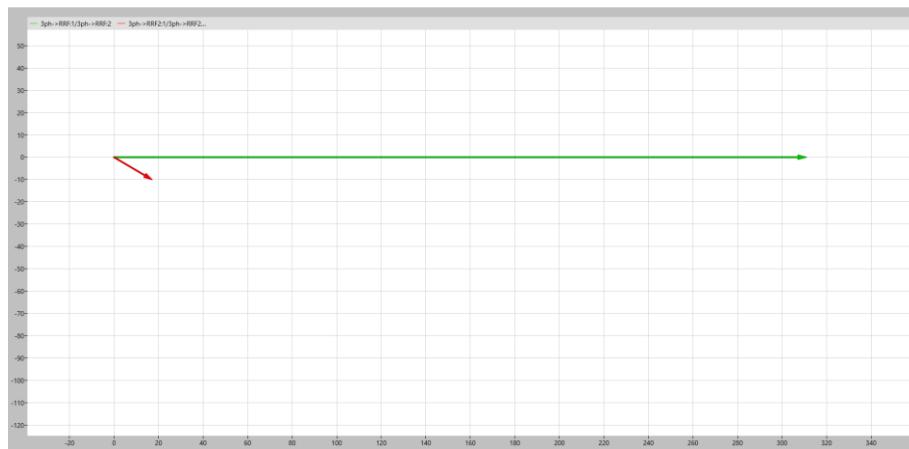
*Figure 39 Phasor Diagram Leading*



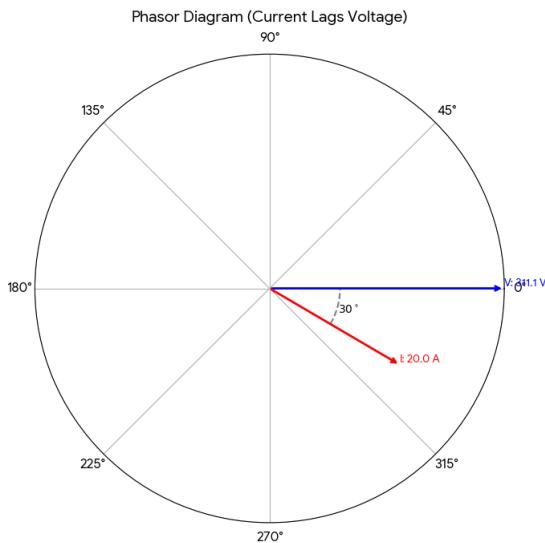
*Figure 40 Phasor Diagram Leading*

**Lagging Power Factor** occurs when the inverter mimics the behavior of an inductive load. In this state, the current phasor rotates behind the voltage phasor, creating a negative phase shift. This mode implies that the inverter is either absorbing reactive power (acting as a load) or injecting reactive power to support a voltage drop, depending on the system convention.

To achieve this in the simulation, a **non-zero value is assigned to  $I_{q\_ref}$** .



*Figure 41 Phasor Diagram Lagging*



*Figure 42 Phasor Diagram Lagging*

The relationship between the physical phasor angle ( $\theta$ ) and the control variables in the initialization script is defined by trigonometric projection.

$$I_d = I_{peak} \cdot \cos(\theta)$$

$$I_q = I_{peak} \cdot \sin(\theta)$$

Here,  $\theta$  represents the desired power factor angle.

- Setting  $\theta = 0^\circ$  results in  $I_q = 0$  (Unity).
- Setting  $\theta = 30^\circ$  results in a non-zero  $I_q$  (Non-Unity).

## References

- Mohan, N., Undeland, T. M., & Robbins, W. P. (2002). *Power electronics: Converters, applications, and design* (3rd ed.). Wiley.
- Erickson, R. W., & Maksimović, D. (2020). *Fundamentals of power electronics* (3rd ed.). Springer Nature.
- Xiao, H., & Li, M. (2025). *Advanced Control Techniques for Grid-Connected Inverters*. Springer.