ISTANBUL TECHNICAL UNIVERSITY COMPUTER ENGINEERING DEPARTMENT

BLG 222E COMPUTER ORGANIZATION PROJECT REPORT

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GROUP NO : G15

GROUP MEMBERS:

150180921 : EARTA JOCA

150180922 : INES MUKA

150180924 : GRETA ISARAJ

150180905 : FATIMA RAHIMOVA

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Contents

FRONT COVER

1	INTRODUCTION	1
2	MATERIALS AND METHODS	1
3	RESULTS	87
4	DISCUSSION	88
5	CONCLUSION	89

1 INTRODUCTION

Control Unit(CU) is the part of the computer's central processing unit (CPU). It directs the flow of data between the computer's memory and the several peripherals. There are two major categories of CU:

- Hardwired-control unit
- Microprogrammable control unit

We already designed hardwired control unit in the previous project. In this project, we designed a software-based (microprogrammed) control unit of basic computer using the structure shown in Figure 1.

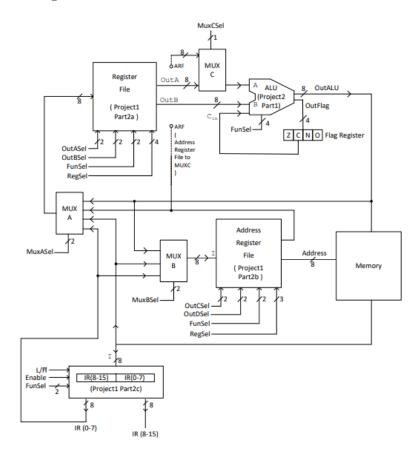


Figure 1: Slightly Modified Version of Project 2

2 MATERIALS AND METHODS

There are two types of instructions as described below.

(1) Instructions with address reference has the format as a given below:

- \bullet The OPCODE is a 5-bit field .
- \bullet The REGSEL is a 2-bit field .
- The ADDRESSING MODE is a 1-bit field .
- The ADDRESS is 8 bits .

OPCODE REGSEL	ADDRESSING MODE	ADDRESS
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Figure 2: Instructions with an address reference

- (2) Instructions without address reference has the format as a given below:
- The OPCODE is a 5-bit field
- DESTREG is a 3-bit field which specifies the destination register .
- SRCREG1 is a 3-bit field which specifies the first source register .
- SRCREG2 is a 3-bit field which specifies the second source register .
- The least significant two bits are unused and have the value 00.

OPCODE	DESTREG	SRCREG1	SRCREG2 00	C

Figure 3: Instructions without an address reference

• Operations

In this project CU can perform 18 different operations in the Figure 2.

Figure 2: OPCODE field and symbols for operations and their descriptions

OPCODE (HEX)	SYMB	ADDRESSING MODE	DESCRIPTION
0x00	LD	IM, D	Rx ← Value (Value is described in Table 3)
0x01	ST	D	Value ← Rx
0x02	MOV	N/A	DESTREG ← SRCREG1
0x03	PSH	N/A	$M[SP] \leftarrow Rx, SP \leftarrow SP - 1$
0x04	PUL	N/A	$SP \leftarrow SP + 1$, $Rx \leftarrow M[SP]$
0x05	ADD	N/A	DESTREG ← SRCREG1 + SRCREG2
0x06	SUB	N/A	DESTREG ← SRCREG2 - SRCREG1
0x07	DEC	N/A	DESTREG ← SRCREG1 - 1
0x08	INC	N/A	DESTREG ← SRCREG1 + 1
0x09	AND	N/A	DESTREG ← SRCREG1 AND SRCREG2
0x0A	OR	N/A	DESTREG ← SRCREG1 OR SRCREG2
0x0B	NOT	N/A	DESTREG ← NOT SRCREG1
0x0C	LSL	N/A	DESTREG ← LSL SRCREG1
0xOD	LSR	N/A	DESTREG ← LSR SRCREG1
0x0E	BRA	IM	PC ← Value
0x0F	BEQ	IM	IF Z=1 THEN PC ← Value
0x10	BNE	IM	IF Z=0 THEN PC ← Value
0x11	CALL	IM	$M[SP] \leftarrow PC, SP \leftarrow SP - 1, PC \leftarrow Value$
0x12	RET	N/A	$SP \leftarrow SP + 1, PC \leftarrow M[SP]$

Figure 3: REGSEL (Left) and DESTREG/SRCREG1/SRCREG2 (Right) select the register of interest for a particular instruction

REGSEL	REGISTER	
00	R0	
01	R1	
10	R2	
11	R3	

DESTREG/SRCREG1/SRCREG2	REGISTER
000	R0
001	R1
010	R2
011	R3
100	PC
101	PC
110	AR
111	SP

Figure 4: Addressing modes

ADDRESSING MODE	MODE	SYMB	Value
0	Immediate	IM	ADDRESS Field
1	Direct	D	M[AR]

In the microprogrammed control unit, we have a ROM that stores all the possible operations that can be executed by our control unit. These instructions and the fields they contain generate the control signals that make everything possible. Choosing the next address of ROM to go to is one of the main issues in microprogrammed control unit. For the next address, we can choose between the address that comes from the current microinstruction, the one that comes as a result of mapping, incrementing the current address, and the return address stored when we have a subroutine call and have to return to where we left it off. We have 2 registers in this part of the circuit, CAR (Control Address Register) and SBR (Subroutine Address Register). We have a logic which chooses between these options by using the condition and type of branching that was specified.

For each of the instructions that we have to perform with our control unit, we have specified the contents of the control memory (the ROM), the mapping logic and the control signals that should be generated.

Microinstruction format: F1 F2 F3 F4 CD BR NextAddress

F1 (5 bits) - Taken by the opcode of the instruction

F2 (3 bits) - Most of the time comes from DESTREG F3 (3 bits) - Most of the time comes from SRCREG1 F4 (3 bits) - Most of the time comes from SRCREG2 CD - the condition to check

(00 - condition always 1, 01 - Z, 10 - Z', 11 - S)

BR - the type of branching

(00 - jump, 01 - subroutine call, 10 - subroutine return, 11 - map)

Next address (13 bits) - where to go after this

$0~LD~Rx \leftarrow Value$

Has 2 addressing modes

Next address – fetch for all

hex: 0000: 02DA1300

hex: 0001: 00001300

hex: 0002: 00001300

hex: 0021: 00801300

hex: 0022: 00801300

hex: 0041: 01001300

hex: 0042: 01001300

hex: 0061: 01801300

hex: 0062: 01801300

Mapping: Opcode 0 Rx 000 A A'

A=0: MuxASel=00 (SelectIR(7-0))

RegSelRegister – depends on Rx – feed the decoded Rx: $00 \rightarrow 0001$ (will activate R0) $01 \rightarrow 0010$, $10 \rightarrow 0100$, $11 \rightarrow 1000$ FunSelReg \rightarrow Load = 01

A = 1: OutDSel = 01 (should show AR)

RAM - Sel = 1, MuxDSel = 0, LD = 1

MuxASel = 01

RegSelRegister - decode Rx and FunSelReg = 01 (Load) - the same

1 ST Value \leftarrow Rx

With address: Mode only direct here - Value is M[AR] Will use the 2 LSB of the destination register location

hex: 0100: 04001300

hex: 0120: 04801300

hex: 0140: 05001300

hex: 0160: 05801300

Mapping: Opcode 0 Rx 00000

OutBSel – Rx, FunSelAlu – 0001 (forward B to OutALU),

OutDSel = 01 (AR) (the value stored in AR is being sent to the address input in the

RAM)

RAM: Sel = 1, Str = 1

$2 \text{ MOV F2} \leftarrow \text{F3}$

hex: 0200: 08001300

we make a subroutine call to here and then want to return

hex: 0201: 08005300

hex: 0204: 08101300

hex: 0205: 08105300

hex: 0208: 08201300

hex: 0209: 08205300

hex: 020C: 08301300

hex: 020D: 08305300

hex: 0210: 08401300

hex: 0211: 08405300

hex: 0218: 08601300

hex: 0219: 08605300

hex: 021C: 08701300

hex: 021D: 08705300

R1:

hex: 0220: 08801300

hex: 0221: 08805300

hex: 0225: 08905300

hex: 0228: 08A01300

hex: 0229: 08A05300

hex: 022C: 08B01300

 $\leftarrow PC$

hex: 0230: 08C01300

hex: 0231: 08C05300

hex: 0238: 08E01300

hex: 0239: 08E05300

hex: 023C: 08F01300

hex: 023D: 08F05300

R2:

hex: 0240: 09001300

hex: 0241: 09005300

hex: 0244: 09101300

hex: 0245: 09105300

hex: 0248: 09201300

hex: 0249: 09205300

hex: 024C: 09301300

 $00010\ 010\ 011\ 01:\ 00010\ 010\ 011\ 000\ 00\ 10\ 10011\ 000\ 000\ 00$

hex: 024D: 09305300

hex: 0250: 09401300

hex: 0251: 09405300

hex: 0258: 09601300

hex: 0259: 09605300

hex: 025C: 09701300

hex: 025D: 09705300

R3:

hex: 0260: 09801300

hex: 0261: 09805300

hex: 0264: 09901300

hex: 0265: 09905300

hex: 0268: 09A01300

hex: 0269: 09A05300

hex: 026C: 09B01300

hex: 026D: 09B05300

hex: 0270: 09C01300

hex: 0271: 09C05300

hex: 0278: 09E01300

hex: 0279: 09E05300

hex: 027C: 09F01300

hex: 027D: 09F05300

PC:

hex: 0280: 0A001300

hex: 0281: 0A005300

hex: 0284: 0A101300

hex: 0285: 0A105300

hex: 0288: 0A201300

hex: 0289: 0A205300

hex: 028C: 0A301300

 $00010\ 100\ 011\ 01:\ 00010\ 100\ 011\ 000\ 00\ 10\ 10011\ 000\ 000\ 00$

hex: 028D: 0A305300

hex:0290: 0A401300

hex:0291: 0A405300

hex: 0298: 0A601300

hex:0299: 0A605300

hex: 029C: 0A701300

hex: 029D: 0A705300

AR:

hex: 02C0: 0B001300

hex: 02C1: 0B005300

hex: 02C4: 0B101300

hex: 02C5: 0B105300

hex: 02C8: 0B201300

hex: 02C9: 0B205300

hex: 02CC: 0B301300

hex: 02CD: 0B305300

hex: 02D0: 0B401300

hex: 02D1: 0B405300

hex: 02D8: 0B601300

hex: 02D9: 0B605300

hex: 02DC: 0B701300

hex: 02DD: 0B705300

SP:

hex: 02E0: 0B801300

hex: 02E1: 0B805300

hex: 02E4: 0B901300

hex: 02E5: 0B905300

hex: 02E8: 0BA01300

hex: 02E9: 0BA05300

hex: 02EC: 0BB01300

hex: 02ED: 0BB05300

hex: 02F0: 0BC01300

hex: 02F1: 0BC05300

hex: 02F8: 0BE01300

hex: 02F9: 0BE05300

hex: 02FC: 0BF01300

hex: 02FD: 0BF05300

Put a Mux – when DESTREG is 101 it will forward 100 – this is what we use in our microinstructions.

The select for this MUX is DR(2) AND DR(1)' AND DR(0) - this gives 1 only when the 101 combo is present and for select = 1 it will forward 100, for select = 0 it will forward whatever DESTREG is.

(To avoid complications will only use 100 for PC - make sure 101 from outside is converted to 100)

When referring to DESTREG, SRCREG1, SRCREG2 in the mapping from now on, we will be referring to their modified versions.

 $\begin{array}{c} {\rm Mapping-Opcode\ DESTREG\ SRCREG1\ 00} \\ {\rm (DESTREG\ and\ RCREG1-will\ be\ modified\)} \end{array}$

Control Signals:

• F2 and F3 both belong to RegisterFile

OutBSel – the 2 LSB of F3, FunSelALU – 0001 (buffer B) MuxASel = 11,

RegSelReg =decode F2 and take the 4 LSB outputs of the decoder FunSelRegister = 01 (Load)

• F2 and F3 both belong to AddressRegister

OutCSel – depends on F3 OutCSel:

We can decode the F3.

Decoder 100: 00010000, 101: 00100000, 110: 01000000, 111: 10000000

Will take Bit 7, 6 of the output of the decoder and send to OutCSel The 101 combination as a select for the decoder – will not appear

MuxCSel = 0 (the OutCSel will be forwarded to the A input of the ALU)

FunSelALU = 0000 (forward A)

MuxBSel = 11 (the OutALU)

RegSelAdd:

Can decode the F2

Decoder 100: 00010000, 101: 00100000, 110: 01000000, 111: 10000000 Take bits 7,6,4 of the output of the decoder and send as RegSelAddress FunSelAddress = 01 (load)

• F2 – AddressRegister, F3 – RegisterFile

OutBSel = the 2 LSB of F3, FunSelALU = 0001

MuxBSel = 11,

RegSelAdd – decode the F2 and take bits 7, 6, 4 of the output of the decoder FunSelAddress = 01 (load)

• F2 – RegisterFile, F3 – AddressRegister

OutCSel – decode the F3 and take bits 7, 6 of the output of the decoding MuxASel = 10, RegSelR – decode F2 and take the 4 LSB outputs of the decoder, Fun-SelReg = 01

$$3 \text{ PSH M[SP]} \leftarrow \text{Rx}, \text{SP} \leftarrow \text{SP} - 1$$

CD BR and then Address of SP \leftarrow SP - 1, just need to jump to here

Just make sure that when the PSH operation comes into the IR – make the check here, it does not make the S bit = 1 otherwise when it goes to SP \leftarrow SP -1 will treat it as a subroutine and not a jump

 $SP \leftarrow SP - 1$

hex: 0300: 0C0007E1

 $SP \leftarrow SP - 1$

hex: 0320: 0C8007E1

 $SP \leftarrow SP - 1$

hex: 0340: 0D0007E1

 $SP \leftarrow SP - 1$

hex: 0360: 0D8007E1

 $SP \leftarrow SP - 1$

hex: 0380: 0E0007E1

 $M[SP] \leftarrow PC$ is also used as a subroutine-

so instead just for this one:

May do a conditional jump to the return from subroutine part –

If not the case will move on to the next address which holds the jump to decrement SP

NOP: 101 101 101 – this combination!

101 won't appear in any of the instructions that deal with F3 F4 and F2

• Have modified it to go to 100 (PC) if that combination comes

hex: 0381: 0EDA07E1

 $SP \leftarrow SP - 1$

hex: 03C0: 0F0007E1

 $SP \leftarrow SP - 1$

hex: 03E0: 0F8007E1

Here we finish after decrementing SP so we don't need to call it as a subroutine but can only jump to it (unconditional jump to decrement SP).

Afterwards branch to subroutine where $SP \leftarrow SP - 1$: it is saved in the decrement part Mapping: Opcode DESTREG (modified) 00000

• F2 – is from the RegisterFile

OutDSel = 10, Str = 1, Sel = 1

OutBSel – the 2 LSB of F2, FunSelALU = 0001 (buffer B)

• F2 – Address File

OutDSel = 10, Str = 1, Sel = 1

OutCSel = the 2 MSB (bit 7, 6) of decoding of F2

MuxCSel = 0, FunSelALU = 0000 (buffer A)

$4 \text{ PUL SP} \leftarrow \text{SP} + 1, \text{Rx} \leftarrow \text{M[SP]}$

First branch to the subroutine which increment SP – it is in the increment part

Then continue

We call the subroutine but it must be able to return

00100 000 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP + 1

hex: 0400:12DA28E1

CD = 00 (condition is 1, unconditional), BR = 01 – subroutine call, Address of SP \leftarrow SP + 1

Should i be representing NOP like this – with 101 101?

?(00100 101 101 00 00 01 01000 111 000 01) (hex: 12D05161)

hex: 0401: 10001300

00100 001 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+ 1

hex: 0420: 12DA28E1

hex: 0421: 10801300

00100 010 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+1

hex: 0440: 12DA28E1

hex: 0441: 11001300

00100 011 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+ 1

hex: 0460: 12DA28E1

hex: 0461: 11801300

00100 100 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+1

hex: 0480: 12DA28E1

hex: 0481: 12001300

00100 110 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+1

hex: 04C0: 12DA28E1

hex: 04C1: 13001300

00100 111 000 00: 00100 101 101 101 00 01 01000 111 000 01 - subroutine call SP \leftarrow SP

+1

hex: 04E0: 12DA28E1

hex: 04E1: 13801300

Mapping: Opcode DESTREG 000 00

• F2 – RegisterFile

OutDSel = 10 (SP), LD = 1, Sel = 1 (MuxDSel = 0)

MuxASel = 01, RegSelReg = decode F2 and take the 4 LSB outputs of the decoder

FunSel = 01

• F2 – AddressRegister

OutDSel = 10, LD = 1, Sel = 1, (MuxDSel = 0)

MuxBSel = 10,

RegSelAdd = like above – bits 7,6, 0 of the output of decoding the 2 LSB of F2

FunSelAdd = 01 (Load)

$5 \text{ ADD } \text{F2} \leftarrow \text{F3} + \text{F4}$

R0:

fetch

hex: 0500: 14001300

fetch

hex: 0501: 14021300

hex: 0502: 14041300

hex: 0503: 14061300

hex: 0504: 14081300

hex: 0506: 140C1300

hex: 0507: 140E1300

hex: 0509: 14121300

hex: 050A: 14141300

hex: 050B: 14161300

hex: 050C: 14181300

hex: 050E: 141C1300

hex: 050F: 141E1300

hex: 0512: 14241300

hex: 0513: 14261300

hex: 0514: 14281300

hex: 0516: 142C1300

hex: 0517: 142E1300

hex: 051B: 14361300

hex: 051C: 14381300

hex: 051E: 143C1300

hex: 051F: 143E1300

22 instructions for first case

R1:

Address given like that to display the mapping

hex: 0520: 14801300

hex: 0521: 14821300

hex: 0522: 14841300

hex: 0523: 14861300

hex: 0524: 14881300

hex: 0526: 148C1300

hex: 0527: 148E1300

hex: 0529: 14921300

hex: 052A: 14941300

hex: 052B: 14961300

hex: 052C: 14981300

hex: 052e: 149C1300

hex: 052f: 149E1300

hex: 0532: 14A41300

hex: 0533: 14A61300

hex: 0534: 14A81300

hex: 0536: 14AC1300

hex: 0537: 14AE1300

hex: 053B: 14B61300

hex: 053C: 14B81300

hex: 053E: 14BC1300

hex: 053F: 14BE1300

R2:

hex: 0540: 15001300

hex: 0541: 15021300

hex: 0542: 15041300

hex: 0543: 15061300

hex: 0544: 15081300

hex: 0546: 150C1300

hex: 0547: 150E1300

hex: 0549: 15121300

hex: 054A: 15141300

hex: 054B: 15161300

hex: 054C: 15181300

hex: 054E: 151C1300

hex: 054F: 151E1300

hex: 0552: 15241300

hex: 0553: 15261300

hex: 0554: 15281300

hex: 0556: 152C1300

hex: 0557: 152E1300

hex: 055B: 15361300

hex: 055C: 15381300

hex: 055E: 153C1300

hex: 055F: 153E1300

R3:

hex: 0560: 15801300

hex: 0561: 15821300

hex: 0562: 15841300

hex: 0563: 15861300

hex: 0564: 15881300

hex: 0566: 158C1300

hex: 0567: 158E1300

hex: 0569: 15921300

hex: 056A: 15941300

hex: 056B: 15961300

hex: 056C: 15981300

hex: 056E: 159C1300

hex: 056F: 159E1300

hex: 0572: 15A41300

hex: 0573: 15A61300

hex: 0574: 15A81300

hex: 0576: 15AC1300

hex: 0577: 15AE1300

hex: 057B: 15B61300

hex: 057C: 15B81300

hex: 057E: 15BC1300

hex: 057F: 15BE1300

PC:

hex: 0580: 16001300

hex: 0581: 16021300

hex: 0582: 16041300

hex: 0583: 16061300

hex: 0584: 16081300

hex: 0586: 160C1300

hex: 0587: 160E1300

hex: 0589: 16121300

hex: 058A: 16141300

hex: 058B: 16161300

hex: 058C: 16181300

hex: 058E: 161C1300

hex: 058F: 161E1300

hex: 0592: 16241300

hex: 0593: 16261300

hex: 0594: 16281300

hex: 0596: 162C1300

hex: 0597: 162E1300

hex: 059B: 16361300

hex: 059C: 16381300

hex: 059E: 163C1300

hex: 059F: 163E1300

AR:

hex: 05C0: 17001300

hex: 05C1: 17021300

hex: 05C2: 17041300

hex: 05C3: 17061300

hex: 05C4: 17081300

hex: 05C6: 170C1300

hex: 05C7: 170E1300

hex: 05C9: 17121300

hex: 05CA: 17141300

hex: 05CB: 17161300

hex: 05CC: 17181300

hex: 05CE: 171C1300

hex: 05CF: 171E1300

hex: 05D2: 17241300

hex: 05D3: 17261300

hex: 05D4: 17281300

hex: 05D6: 172C1300

hex: 05D7: 172E1300

hex: 05DB: 17361300

hex: 05DC: 17381300

hex: 05DE: 173C1300

hex: 05DF: 173E1300

SP:

Hex: 05E0: 17801300

Hex: 05E1: 17821300

Hex: 05E2: 17841300

Hex: 05E3: 17861300

Hex: 05E4: 17881300

Hex: 05E6: 178C1300

Hex: 05E7: 178E1300

Hex: 05E9: 17921300

Hex: 05EA: 17941300

Hex: 05EB: 17961300

Hex: 05EC: 17981300

Hex: 05EE: 179C1300

Hex: 05EF: 179E1300

Hex: 05F2: 17A41300

Hex: 05F3: 17A61300

Hex: 05F4: 17A81300

Hex: 05F6: 17AC1300

Hex: 05F7: 17AE1300

Hex: 05FB: 17B61300

Hex: 05FC: 17B81300

Hex: 05FE: 17BC1300

Hex: 05FF: 17BE1300

Opcode - DESTREG - 2 LSB of new SRCREG1 - new SRCREG2

We make a different modification here. It has to do with the design and the microinstruction saved in ROM.in addition we may switch the places of the operands but it is still the same operation. For this reason, we only keep one order of the combination in ROM, and find the new SRCREG1 and SRCREG2 so we can map correctly, no matter the order in which they are given in the instruction.

New SRCREG1 – the smallest between SRCREG1 and SRCREG2 New SRCREG1 – the largest

In the microinstruction in ROM for addition, SRCREG1 is always smaller (the binary code which symbolizes it), than SRCREG2.

• F2 – RegisterFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = 2 LSB of F3, MuxCSel = 1, OutBSel = 2 LSB of F4

FunSelALU = 0100, MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder

FunSelRegister = 01 (Load)

• F2 – RegFile, F3 – RegFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4, MuxCSel = 0

OutBSel = the 2 LSB of F3, FunSelALU = 0100,

MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder

FunSelR = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, OutBSel = the 2 LSB of F4

FunSelALU = 0100, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding F2

FunSelAdd = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4

MuxCSel = 0,

OutBSel = the 2 LSB of F3

FunSelALU = 0100, MuxBSel = 11,

RegSelAdd = bits 7, 6, 4 of the output of decoding F2

FunSelAdd = 01

$\mathbf{6} \ \mathbf{SUB} \ \mathbf{F2} \leftarrow \mathbf{F3} \ \textbf{-} \ \mathbf{F4}$

R0:

Hex: 0600: 18001300

Hex: 0601: 18021300

Hex: 0602: 18041300

Hex: 0603: 18061300

Hex: 0604: 18101300

Hex: 0605: 18121300

Hex: 0606: 18141300

Hex: 0607: 18161300

Hex: 0608: 18201300

Hex: 0609: 18221300

Hex: 060A: 18241300

Hex: 060B: 18261300

Hex: 060C: 18301300

Hex: 060D: 18321300

Hex: 060E: 18341300

Hex: 060F: 18361300

Hex: 0610: 18401300

Hex: 0611: 18421300

Hex: 0612: 18441300

Hex: 0613: 18461300

For simplicity in mapping

Hex: 0618: 18601300

Hex: 0619: 18621300

Hex: 061A: 18641300

Hex: 061B: 18661300

Hex: 061C: 18701300

Hex: 061D: 18721300

Hex: 061E: 18741300

Hex: 061F: 18761300

Opcode F2 F3 F4 – the 2 LSB (it can only be a R0 – R3)

28 operations

R1:

Hex: 0620: 18801300

Hex: 0621: 18821300

Hex: 0622: 18841300

Hex: 0623: 18861300

Hex: 0624: 18901300

Hex: 0625: 18921300

Hex: 0626: 18941300

Hex: 0627: 18961300

Hex: 0628: 18A01300

Hex: 0629: 18A21300

Hex: 062A: 18A41300

Hex: 062B: 18A61300

Hex: 062C: 18B01300

hex: 062D: 18B21300

Hex: 062E: 18B41300

Hex: 062F: 18B61300

Hex: 0630: 18C01300

Hex: 0631: 18C21300

Hex: 0632: 18C41300

Hex: 0633: 18C61300

Hex: 0638: 18E01300

Hex: 0639: 18E21300

Hex: 063A: 18E41300

Hex: 063B: 18E61300

Hex: 063C: 18F01300

Hex: 063D: 18F21300

Hex: 063E: 18F41300

Hex: 063F: 18F61300

R2:

Hex: 0640: 19001300

Hex: 0641: 19021300

Hex: 0642: 19041300

Hex: 0643: 19061300

Hex: 0644: 19101300

Hex: 0645: 19121300

Hex: 0646: 19141300

Hex: 0647: 19161300

Hex: 0648: 19201300

Hex: 0649: 19221300

Hex: 064A: 19241300

Hex: 064B: 19261300

Hex: 064C: 19301300

Hex: 064D: 19321300

Hex: 064E: 19341300

Hex: 064F: 19361300

Hex: 0650: 19401300

Hex: 0651: 19421300

Hex: 0652: 19441300

Hex: 0653: 19461300

Hex: 0658: 19601300

Hex: 0659: 19621300

Hex: 065A: 19641300

Hex: 065B: 19661300

Hex: 065C: 19701300

Hex: 065D: 19721300

Hex: 065E: 19741300

Hex: 065F: 19761300

R3:

Hex: 0660: 19801300

Hex: 0661: 19821300

Hex: 0662: 19841300

Hex: 0663: 19861300

Hex: 0664: 19901300

Hex: 0665: 19921300

Hex: 0666: 19941300

Hex: 0667: 19961300

Hex: 0668: 19A01300

Hex: 0669: 19A21300

Hex: 066A: 19A41300

Hex: 066B: 19A61300

Hex: 066C: 19B01300

Hex: 066D: 19B21300

Hex: 066E: 19B41300

Hex: 066F: 19B61300

Hex: 0670: 19C01300

Hex: 0671: 19C21300

Hex: 0672: 19C41300

Hex: 0673: 19C61300

Hex: 0678: 19E01300

Hex: 0679: 19E21300

Hex: 067A: 19E41300

Hex: 067B: 19E61300

Hex: 067C: 19F01300

Hex: 067D: 19F21300

Hex: 067E: 19F41300

Hex: 067F: 19F61300

PC:

Hex: 0680: 1A001300

Hex: 0681: 1A021300

Hex: 0682: 1A041300

Hex: 0683: 1A061300

Hex: 0684: 1A101300

Hex: 0685: 1A121300

Hex: 0686: 1A141300

Hex: 0687: 1A161300

Hex: 0688: 1A201300

Hex: 0689: 1A221300

Hex: 068A: 1A241300

Hex: 068B: 1A261300

Hex: 068C: 1A301300

Hex: 068D: 1A321300

Hex: 068E: 1A341300

Hex: 068F: 1A361300

Hex: 0690: 1A401300

Hex: 0691: 1A421300

Hex: 0692: 1A441300

Hex: 0693: 1A461300

Hex: 0698: 1A601300

Hex: 0699: 1A621300

Hex: 069A: 1A641300

Hex: 069B: 1A661300

Hex: 069C: 1A701300

Hex: 069D: 1A721300

Hex: 069E: 1A741300

Hex: 069F: 1A761300

AR:

Hex: 06C0: 1B001300

Hex: 06C1: 1B021300

Hex: 06C2: 1B041300

Hex: 06C3: 1B061300

Hex: 06C4: 1B101300

Hex: 06C5: 1B121300

Hex: 06C6: 1B141300

Hex: 06C7: 1B161300

Hex: 06C8: 1B201300

Hex: 06C9: 1B221300

Hex: 06CA: 1B241300

Hex: 06CB: 1B261300

Hex: 06CC: 1B301300

Hex: 06CD: 1B321300

Hex: 06CE: 1B341300

Hex: 06CF: 1B361300

Hex: 06D0: 1B401300

Hex: 06D1: 1B421300

Hex: 06D2: 1B441300

Hex: 06D3: 1B461300

Hex: 06D8: 1B601300

Hex: 06D9: 1B621300

Hex: 06DA: 1B641300

Hex: 06DB: 1B661300

Hex: 06DC: 1B701300

Hex: 06DD: 1B721300

Hex: 06DE: 1B741300

Hex: 06DF: 1B761300

SP:

Hex: 06E0: 1B801300

Hex: 06E1: 1B821300

Hex: 06E2: 1B841300

Hex: 06E3: 1B861300

Hex: 06E4: 1B901300

Hex: 06E5: 1B921300

Hex: 06E6: 1B941300

Hex: 06E7: 1B961300

Hex: 06E8: 1BA01300

Hex: 06E9: 1BA21300

Hex: 06EA: 1BA41300

Hex: 06EB: 1BA61300

Hex: 06EC: 1BB01300

Hex: 06ED: 1BB21300

Hex: 06EE: 1BB41300

Hex: 06EF: 1BB61300

Hex: 06F0: 1BC01300

Hex: 06F1: 1BC21300

Hex: 06F2: 1BC41300

Hex: 06F3: 1BC61300

Hex: 06F8: 1BE01300

Hex: 06F9: 1BE21300

Hex: 06FA: 1BE41300

Hex: 06FB: 1BE61300

Hex: 06FC: 1BF01300

Hex: 06FD: 1BF21300

Hex: 06FE: 1BF41300

Hex: 06FF: 1BF61300

Mapping: Opcode - DESTREG - SRCREG1 - the 2 LSB of SRCREG2 (it can only be a $\mathrm{R0}-\mathrm{R3}$)

• F2 – RegisterFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = 2 LSB of F3, MuxCSel = 1, OutBSel = 2 LSB of F4 FunSelALU = 0110, MuxASel = 11, RegSelR = decode F2 and take the 4 LSB outputs of the decoder FunSelRegister = 01 (Load)

• F2 – RegFile, F3 – AddressFile, F4 – RegFile

OutCSel = the 2 MSB (bit 7, 6) of decoding the F3, MuxCSel = 0

OutBSel = the 2 LSB of F4, FunSelALU = 0110,

MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder

FunSelR = 01

• F2 – AddressFile , F3 – RegisterFile, F4 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, OutBSel = the 2 LSB of F4

FunSelALU = 0110, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding the F2

FunSelAdd = 01

• F2 – AddressFile, F3 – AddressFile, F4 – RegisterFile

OutCSel = the 2 MSB (bit 7, 6) of decoding the F3

MuxCSel = 0,

OutBSel = the 2 LSB of F4

FunSelALU = 0110, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding of F2

FunSelAdd = 01

 $7 \text{ DEC F3} \leftarrow \text{F3} - 1$

2 clock cycles – first $F2 \leftarrow F3$, then decrement F2

Can already used previous microinstructions

R0:

Hex: 0700: 1EDA2201

Hex: 0701: 1C001300

Hex: 0704: 1EDA2205

- they hold the same thing Hex: 0705: 0705 00111 000 010 00: 00111 101 101 101 00 01

00010 000 010 01 Subroutine to R0 \leftarrow R2

Hex: 0708: 1C001300

0709: 1C001300

00111 000 011 00: 00111 101 101 101 00 01 00010 000 011 01 Subroutine to R0 \leftarrow R3

Hex: 070C: 1EDA220D

070D: 1C001300

00111 000 100 00: 00111 101 101 101 00 01 00010 000 100 01 Subroutine to R0 \leftarrow PC

Hex: 0710: 1EDA2211

0711: 1C001300

00111 000 110 00: 00111 101 101 101 00 01 00010 000 110 01 Subroutine to R0 \leftarrow AR

Hex: 0718: 1EDA2219

0719: 1C001300

00111 000 111 00: 00111 101 101 101 00 01 00010 000 111 01 Subroutine to R0 \leftarrow SP

Hex: 071C: 1EDA221D

071D: 1C001300

R1:

00111 001 000 00: 00111 101 101 101 00 01 00010 001 000 01 Subroutine to R1 \leftarrow R0

Hex: 0720: 1EDA2221

Hex: 0721: 1C901300

Hex: 0724: 1EDA2225

0725: 1C901300

00111 001 010 00: 00111 101 101 101 00 01 00010 001 010 01 Subroutine to R1 \leftarrow R2

Hex: 0728: 1EDA2229

0729: 1C901300

00111 001 011 00: 00111 101 101 101 00 01 00010 001 011 01 Subroutine to R1 \leftarrow R3

Hex: 072C: 1EDA222D

072D: 1C901300

00111 001 100 00: 00111 101 101 101 00 01 00010 001 100 01 Subroutine to R1 \leftarrow PC

Hex: 0730: 1EDA2231

0731: 1C901300

00111 001 110 00: 00111 101 101 101 00 01 00010 001 110 01 Subroutine to R1 \leftarrow AR

Hex: 0738: 1EDA2239

0739: 1C901300

00111 001 111 00: 00111 101 101 101 00 01 00010 001 111 01 Subroutine to R1 \leftarrow SP

Hex: 073C: 1EDA223D

073D: 1C901300

R2:

Hex: 0740: 1EDA2241

Hex: 0741: 1D201300

Hex: 0744: 1EDA2245

0745: 1D201300

0748: 1EDA2249

0749: 1D201300

Hex: 074C: 1EDA224D

074D: 1D201300

Hex: 0750: 1EDA2251

0751: 1D201300

Hex: 0758: 1EDA2259

0759: 1D201300

Hex: 075C: 1EDA225D

075D: 1D201300

R3:

00111 011 000 00: 00111 101 101 101 00 01 00010 011 000 01 Subroutine to R3 \leftarrow R0

Hex: 0760: 1EDA2261

Hex: 0761: 1DB01300

Hex: 0764: 1EDA2265

0765: 1DB01300

00111 011 010 00: 00111 101 101 101 00 01 00010 011 010 01 Subroutine to R3 \leftarrow R2

Hex: 0768: 1EDA2269

0769: 1DB01300

Hex: 076C: 1EDA226D

076D: 1DB01300

00111 011 100 00: 00111 101 101 101 00 01 00010 011 100 01 Subroutine to R3 \leftarrow PC

Hex: 0770: 1EDA2271

0771: 1DB01300

00111 011 110 00: 00111 101 101 101 00 01 00010 011 110 01 Subroutine to R3 \leftarrow AR

Hex: 0778: 1EDA2279

0779: 1DB01300

00111 011 111 00: 00111 101 101 101 00 01 00010 011 111 01 Subroutine to R3 \leftarrow SP

Hex: 077C: 1EDA227D

077D: 1DB01300

PC:

00111 100 000 00: 00111 101 101 101 00 01 00010 100 000 01 Subroutine to PC \leftarrow R0

Hex: 0780: 1EDA2281

Hex: 0781: 1E401300

Hex: 0784: 1EDA2285

0785: 1E401300

00111 100 010 00: 00111 101 101 101 00 01 00010 100 010 01 Subroutine to PC \leftarrow R2

Hex: 0788: 1EDA2289

0789: 1E401300

00111 100 011 00: 00111 101 101 101 00 01 00010 100 011 01 Subroutine to PC \leftarrow R3

Hex: 078C: 1EDA228D

078D: 1E401300

Hex: 0790: 1EDA2291

0791: 1E401300

00111 100 110 00: 00111 101 101 101 00 01 00010 100 110 01 Subroutine to PC \leftarrow AR

Hex: 0798: 1EDA2299

0799: 1E401300

00111 100 111 00: 00111 101 101 101 00 01 00010 100 111 01 Subroutine to PC \leftarrow SP

Hex: 079C: 1EDA229D

079D: 1E401300

AR:

00111 110 000 00: 00111 101 101 101 00 01 00010 110 000 01 Subroutine to AR \leftarrow R0

Hex: 07C0: 1EDA22C1

Hex: 07C1: 1F601300

Hex: 07C4: 1EDA22C5

07C5: 1F601300

00111 110 010 00: 00111 101 101 101 00 01 00010 110 010 01 Subroutine to AR \leftarrow R2

Hex: 07C8: 1EDA22C9

07C9: 1F601300

00111 110 011 00: 00111 101 101 101 00 01 00010 110 011 01 Subroutine to AR \leftarrow R3

Hex: 07CC: 1EDA22CD

07CD: 1F601300

Hex: 07D0: 1EDA22D1

07D1: 1F601300

Hex: 07D8: 1EDA22D9

07D9: 1F601300

Hex: 07DC: 1EDA22DD

07DD: 1EDA22DD

SP:

00111 111 000 00: 00111 101 101 101 00 01 00010 111 000 01 Subroutine to SP \leftarrow R0

07E0: 1EDA22E1

Hex: 07E1: 1FF01400– goes to check subroutine part

Hex: 07E4: 1EDA22E5

00111 111 001 01: 00111 101 101 101 00 01 00010 111 001 01

07E5: 1FF01400

00111 111 010 00: 00111 101 101 101 00 01 00010 111 010 01 Subroutine to SP \leftarrow R2

Hex: 07E8: 1EDA22E9

00111 111 010 01: 00111 101 101 101 00 01 00010 111 001 01

07E9: 1FF01400

00111 111 011 00: 00111 101 101 101 00 01 00010 111 011 01 Subroutine to SP \leftarrow R3

Hex: 07EC: 1EDA22ED

00111 111 011 01: 00111 101 101 101 00 01 00010 111 001 01

07ED: 1FF01400

00111 111 100 00: 00111 101 101 101 00 01 00010 111 100 01 Subroutine to SP \leftarrow PC

Hex: 07F0: 1EDA22F1

00111 111 100 01: 00111 101 101 101 00 01 00010 111 001 01

07F1: 1FF01400

00111 111 110 00: 00111 101 101 101 00 01 00010 111 110 01 Subroutine to SP \leftarrow AR

Hex: 07F8: 1EDA22F9

00111 111 110 01: 00111 101 101 101 00 01 00010 111 001 01

07F9: 1FF01400

Hex: 07FC: 1EDA22FD

07FD: 1FF01400

Mapping: Opcode DESTREG SRCREG1 00

• F2 – RegFile

RegSelRegister = decode F2 and take the 4 LSB outputs of the decoder FunSelR = 11 (decrement)

• F2 – AddressFile

RegSelAddress = bits 7,6, 4 of the output of decoding F2

FunSelAdd= 11

8 INC F2 \leftarrow F3 + 1

2 clock cycles – first $F2 \leftarrow F3$, then increment F2

Can already used previous microinstructions

R0:

Hex: 0800: 22DA2201

Hex: 0801: 20001300

Hex: 0804: 22DA2205

hex: 0805: 20001300

01000 000 010 00: 01000 101 101 101 00 01 00010 000 010 01 Subroutine to R0 \leftarrow R2

Hex: 0808: 22DA2209

hex: 0809: 20001300

01000 000 011 00: 01000 101 101 101 00 01 00010 000 011 01 Subroutine to R0 \leftarrow R3

Hex: 080C: 22DA220D

hex: 080D: 20001300

01000 000 100 00: 01000 101 101 101 00 01 00010 000 100 01 Subroutine to R0 \leftarrow PC

Hex: 0810: 22DA2211

hex: 0811: 20001300

01000 000 110 00: 01000 101 101 101 00 01 00010 000 110 01 Subroutine to R0 \leftarrow AR

Hex: 0818: 22DA2219

hex: 0819: 20001300

01000 000 111 00: 01000 101 101 101 00 01 00010 000 111 01 Subroutine to R0 \leftarrow SP

Hex: 081C: 22DA221D

hex: 081D: 20001300

R1:

01000 001 000 00: 01000 101 101 101 00 01 00010 001 000 01 Subroutine to R1 \leftarrow R0

Hex: 0820: 22DA2221

Hex: 0821: 20901300

Hex: 0824: 22DA2225

hex: 0825: 20901300

01000 001 010 00: 01000 101 101 101 00 01 00010 001 010 01 Subroutine to R1 \leftarrow R2

Hex: 0828: 22DA2229

hex: 0829: 20901300

01000 001 011 00: 01000 101 101 101 00 01 00010 001 011 01 Subroutine to R1 \leftarrow R3

Hex: 082C: 22DA222D

hex: 082D: 20901300

01000 001 100 00: 01000 101 101 101 00 01 00010 001 100 01 Subroutine to R1 \leftarrow PC

Hex: 0830: 22DA2231

hex: 0831: 20901300

01000 001 110 00: 01000 101 101 101 00 01 00010 001 110 01 Subroutine to R1 \leftarrow AR

Hex: 0838: 22DA2239

hex: 0839: 20901300

01000 001 111 00: 01000 101 101 101 00 01 00010 001 111 01 Subroutine to R1 \leftarrow SP

Hex: 083C: 22DA223D

hex: 083D: 20901300

R2:

Hex: 0840: 22DA2241

Hex: 0841: 21201300

Hex: 0844: 22DA2245

hex: 0845: 21201300

Hex: 0848: 22DA2249

hex: 0849: 21201300

Hex: 084C: 22DA224D

hex: 084D: 21201300

Hex: 0850: 22DA2251

hex: 0851: 21201300

Hex: 0858: 22DA2259

hex: 0859: 21201300

Hex: 085C: 22DA225D

hex: 085D: 21201300

R3:

01000 011 000 00: 01000 101 101 101 00 01 00010 011 000 01 Subroutine to R3 \leftarrow R0

Hex: 0860: 22DA2261

Hex: 0861: 21B01300

Hex: 0864: 22DA2265

hex: 0865: 21B01300

01000 011 010 00: 01000 101 101 101 00 01 00010 011 010 01 Subroutine to R3 \leftarrow R2

Hex: 0868: 22DA2269

hex: 0869: 21B01300

Hex: 086C: 22DA226D

hex: 086D: 21B01300

01000 011 100 00: 01000 101 101 101 00 01 00010 011 100 01 Subroutine to R3 \leftarrow PC

Hex: 0870: 22DA2271

hex: 0871: 21B01300

01000 011 110 00: 01000 101 101 101 00 01 00010 011 110 01 Subroutine to R3 \leftarrow AR

Hex: 0878: 22DA2279

hex: 0879: 21B01300

01000 011 111 00: 01000 101 101 101 00 01 00010 011 111 01 Subroutine to R3 \leftarrow SP

Hex: 087C: 22DA227D

hex: 087D: 21B01300

PC:

01000 100 000 00: 01000 101 101 101 00 01 00010 100 000 01 Subroutine to PC \leftarrow R0

Hex: 0880: 22DA2281

Hex: 0881: 22401300

Could add a new address and hold the special $PC \leftarrow PC + 1$ that is used as a subroutine:

Hex: 0882: 22405300

Hex: 0884: 22DA2285

hex: 0885: 22401300

 $01000\ 100\ 010\ 00$: $01000\ 101\ 101\ 101\ 00\ 01\ 00010\ 100\ 010\ 01\ Subroutine to PC \leftarrow R2$

Hex: 0888: 22DA2289

hex: 0889: 22401300

01000 100 011 00: 01000 101 101 101 00 01 00010 100 011 01 Subroutine to PC \leftarrow R3

Hex: 088C: 22DA228D

hex: 088D: 22401300

Hex: 0890: 22DA2291

hex: 0891: 22401300

01000 100 110 00: 01000 101 101 101 00 01 00010 100 110 01 Subroutine to PC \leftarrow AR

Hex: 0898: 22DA2299

hex: 0899: 22401300

01000 100 111 00: 01000 101 101 101 00 01 00010 100 111 01 Subroutine to PC \leftarrow SP

Hex: 089C: 22DA229D

hex: 089D: 22401300

AR:

01000 110 000 00: 01000 101 101 101 00 01 00010 110 000 01 Subroutine to AR \leftarrow R0

Hex: 08C0: 22DA22C1

Hex: 08C1: 23601300

Hex: 08C4: 22DA22C5

hex: 08C5: 23601300

01000 110 010 00: 01000 101 101 101 00 01 00010 110 010 01 Subroutine to AR \leftarrow R2

Hex: 08C8: 22DA22C9

hex: 08C9: 23601300

01000 110 011 00: 01000 101 101 101 00 01 00010 110 011 01 Subroutine to AR \leftarrow R3

Hex: 08CC: 22DA22CD

hex: 08CD: 23601300

Hex: 08D0: 22DA22D1

hex: 08D1: 23601300

Hex: 08D8: 22DA22D9

hex: 08D9: 23601300

Hex: 08DC: 22DA22DD

hex: 08DD: 23601300

need to jump to the subroutine return check when for $SP \leftarrow SP + 1$

SP:

01000 111 000 00: 01000 101 101 101 00 01 00010 111 000 01 Subroutine to SP \leftarrow R0

Hex: 08E0: 22DA22E1

Hex: 08E1: 23F01400

Hex: 08E4: 22DA22E5

 $01000\ 111\ 001\ 01:\ 01000\ 111\ 111\ 000\ 00\ 00\ 10100\ 000\ 000\ 00$

hex: 08E5: 23F01400

01000 111 010 00: 01000 101 101 101 00 01 00010 111 010 01 Subroutine to SP \leftarrow R2

Hex: 08E8: 22DA22E9

hex: 08E9: 23F01400

01000 111 011 00: 01000 101 101 101 00 01 00010 111 011 01 Subroutine to SP \leftarrow R3

Hex: 08EC: 22DA22ED

hex: 08ED: 23F01400

01000 111 100 00: 01000 101 101 101 00 01 00010 111 100 01 Subroutine to SP \leftarrow PC

Hex: 08F0: 22DA22F1

hex: 08F1: 23F01400

01000 111 110 00: 01000 101 101 101 00 01 00010 111 110 01 Subroutine to SP \leftarrow AR

Hex: 08F8: 22DA22F9

hex: 08F9: 23F01400

Hex: 08FC: 22DA22FD

 $01000\ 111\ 111\ 01:\ 01000\ 111\ 111\ 000\ 00\ 00\ 10100\ 000\ 00$

hex: 08FD: 23F01400

Mapping: Opcode DESTREG SRCREG1 00

• F2 – RegFile

RegSelRegister = decode F2 and take the 4 LSB outputs of the decoder FunSelR = 10 (increment)

• F2 – AddressFile

RegSelAddress = bits 7, 6, 4 of the output of decoding F2 FunSelAdd= 10

$9 \text{ F2} \leftarrow \text{F3 AND F4}$

R0:

Hex: 0900: 24001300

Hex: 0901: 24021300

Hex: 0902: 24041300

Hex: 0903: 24061300

Hex: 0904: 24081300

Hex: 0906: 240C1300

Hex: 0907: 240E1300

Hex: 0909: 24121300

Hex: 090A: 24141300

Hex: 090B: 24161300

Hex: 090C: 24181300

Hex: 090E: 241C1300

Hex: 090F: 241E1300

Hex: 0912: 24241300

Hex: 0913: 24261300

Hex: 0914: 24281300

Hex: 0916: 242C1300

Hex: 0917: 242E1300

Hex: 091B: 24361300

Hex: 091C: 24381300

Hex: 091E: 243C1300

Hex: 091F: 243E1300

22 instructions for first case

R1:

Hex: 0920: 24801300

Hex: 0921: 24821300

Hex: 0922: 24841300

Hex: 0923: 24861300

Hex: 0924: 24881300

Hex: 0926: 248C1300

Hex: 0927: 248E1300

Hex: 0929: 24921300

Hex: 092A: 24941300

Hex: 092B: 24961300

Hex: 092C: 24981300

Hex: 092E: 249C1300

Hex: 092F: 249E1300

Hex: 0932: 24A41300

Hex: 0933: 24A61300

Hex: 0934: 24A81300

Hex: 0936: 24AC1300

Hex: 0937: 24AE1300

Hex: 093B: 24B61300

Hex: 093C: 24B81300

Hex: 093E: 24BC1300

Hex: 093F: 24BE1300

R2:

Hex: 0940: 25001300

Hex: 0941: 25021300

Hex: 0942: 25041300

Hex: 0943: 25061300

Hex: 0944: 25081300

Hex: 0946: 250C1300

Hex: 0947: 250E1300

Hex: 0949: 25121300

Hex: 094A: 25141300

Hex: 094B: 25161300

Hex: 094C: 25181300

Hex: 094E: 251C1300

Hex: 094F: 251E1300

Hex: 0952: 25241300

 $01001\ 010\ 100\ 11$: $01001\ 010\ 011\ 00\ 11$ 00 00 10011 000 000 00 R2 \leftarrow R2 AND R3

Hex: 0953: 25261300

Hex: 0954: 25281300

Hex: 0956: 252C1300

Hex: 0957: 252E1300

Hex: 095B: 25361300

Hex: 095C: 25381300

Hex: 095E: 253C1300

Hex: 095F: 253E1300

Remember – we cant have 2 address file registers on the right hand side – only 1

R3:

Hex: 0960: 25801300

Hex: 0961: 25821300

Hex: 0962: 25841300

Hex: 0963: 25861300

Hex: 0964: 25881300

Hex: 0966: 258C1300

Hex: 0967: 258E1300

 $01001\ 011\ 010\ 01$: $01001\ 011\ 001\ 001\ 00\ 10011\ 000\ 000\ 000\ R3 \leftarrow R1\ AND\ R1$

Hex: 0969: 25921300

Hex: 096A: 25941300

Hex: 096B: 25961300

Hex: 096C: 25981300

Hex: 096E: 259C1300

Hex: 096F: 259E1300

Hex: 0972: 25A41300

Hex: 0973: 25A61300

Hex: 0974: 25A81300

Hex: 0976: 25AC1300

Hex: 0977: 25AE1300

Hex: 097B: 25B61300

Hex: 097C: 25B81300

Hex: 097E: 25BC1300

Hex: 097F: 25BE1300

PC:

Hex: 0980: 26001300

Hex: 0981: 26021300

Hex: 0982: 26041300

Hex: 0983: 26061300

Hex: 0984: 26081300

Hex: 0986: 260C1300

Hex: 0987: 260E1300

Hex: 0989: 26121300

Hex: 098A: 26141300

Hex: 098B: 26161300

Hex: 098C: 26181300

Hex: 098E: 261C1300

Hex: 098F: 261E1300

Hex: 0992: 26241300

Hex: 0993: 26261300

Hex: 0994: 26281300

Hex: 0996: 262C1300

Hex: 0997: 262E1300

Hex: 099B: 26361300

Hex: 099C: 26381300

Hex: 099E: 263C1300

Hex: 099F: 263E1300

AR:

Hex: 09C0: 27001300

Hex: 09C1: 27021300

Hex: 09C2: 27041300

Hex: 09C3: 27061300

Hex: 09C4: 27081300

Hex: 09C6: 270C1300

Hex: 09C7: 270E1300

Hex: 09C9: 27121300

Hex: 09CA: 27141300

Hex: 09CB: 27161300

Hex: 09CC: 27181300

Hex: 09CE: 271C1300

Hex: 09CF: 271E1300

Hex: 09D2: 27241300

Hex: 09D3: 27261300

Hex: 09D4: 27281300

Hex: 09D6: 272C1300

Hex: 09D7: 272E1300

Hex: 09DB: 27361300

Hex: 09DC: 27381300

Hex: 09DE: 273C1300

Hex: 09DF: 273E1300

SP:

Hex: 09E0: 27801300

Hex: 09E1: 27821300

Hex: 09E2: 27841300

Hex: 09E3: 27861300

Hex: 09E4: 27881300

Hex: 09E6: 278C1300

Hex: 09E7: 278E1300

Hex: 09E9: 27921300

Hex: 09EA: 27941300

Hex: 09EB: 27961300

Hex: 09EC: 27981300

Hex: 09EE: 279C1300

Hex: 09EF: 279E1300

Hex: 09F2: 27A41300

Hex: 09F3: 27A61300

Hex: 09F4: 27A81300

Hex: 09F6: 27AC1300

Hex: 09F7: 27AE1300

Hex: 09FB: 27B61300

Hex: 09FC: 27B81300

Hex: 09FE: 27BC1300

Hex: 09FF: 27BE1300

Mapping the same as the AND:

Opcode - DESTREG - 2 LSB of new SRCREG1 - new SRCREG2

• F2 – RegisterFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = 2 LSB of F3, MuxCSel = 1, OutBSel = 2 LSB of F4

FunSelALU = 0111, MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder

FunSelRegister = 01 (Load)

• F2 – RegFile, F3 – RegFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4, MuxCSel = 0

OutBSel = the 2 LSB of F3, FunSelALU = 0111,

MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder FunSelR = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, OutBSel = the 2 LSB of F4

FunSelALU = 0111, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding F2

FunSelAdd = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4

MuxCSel = 0,

OutBSel = the 2 LSB of F3

FunSelALU = 0111, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding the 2 LSB of F2

FunSelAdd = 01

A OR $F2 \leftarrow F3$ OR F4

R0:

Hex: 0A00: 28001300

Hex: 0A01: 28021300

Hex: 0A02: 28041300

Hex: 0A03: 28061300

Hex: 0A04: 28081300

Hex: 0A06: 280C1300

Hex: 0A07: 280E1300

Hex: 0A09: 28121300

Hex: 0A0A: 28141300

Hex: 0A0B: 28161300

Hex: 0A0C: 28181300

Hex: 0A0E: 281C1300

Hex: 0A0F: 281E1300

Hex: 0A12: 28241300

Hex: 0A13: 28261300

Hex: 0A14: 28281300

Hex: 0A16: 282C1300

Hex: 0A17: 282E1300

Hex: 0A1B: 28361300

Hex: 0A1C: 28381300

Hex: 0A1E: 283C1300

Hex: 0A1F: 283E1300

22 instructions for first case

R1:

Hex: 0A20: 28801300

Hex: 0A21: 28821300

Hex: 0A22: 28841300

Hex: 0A23: 28861300

Hex: 0A24: 28881300

Hex: 0A26: 288C1300

Hex: 0A27: 288E1300

Hex: 0A29: 28921300

Hex: 0A2A: 28941300

Hex: 0A2B: 28961300

Hex: 0A2C: 28981300

Hex: 0A2E: 289C1300

Hex: 0A2F: 289E1300

Hex: 0A32: 28A41300

Hex: 0A33: 28A61300

Hex: 0A34: 28A81300

Hex: 0A36: 28AC1300

Hex: 0A37: 28AE1300

Hex: 0A3B: 28B61300

Hex: 0A3C: 28B81300

Hex: 0A3E: 28BC1300

Hex: 0A3F: 28BE1300

R2:

Hex: 0A40: 29001300

Hex: 0A41: 29021300

Hex: 0A42: 29041300

Hex: 0A43: 29061300

Hex: 0A44: 29081300

Hex: 0A46: 290C1300

Hex: 0A47: 290E1300

Hex: 0A49: 29121300

Hex: 0A4A: 29141300

Hex: 0A4B: 29161300

Hex: 0A4C: 29181300

Hex: 0A4E: 291C1300

Hex: 0A4F: 291E1300

Hex: 0A52: 29241300

Hex: 0A53: 29261300

Hex: 0A54: 29281300

Hex: 0A56: 292C1300

Hex: 0A57: 292E1300

Hex: 0A5B: 29361300

Hex: 0A5C: 29381300

Hex: 0A5E: 293C1300

Hex: 0A5F: 293E1300

R3:

hex: 0A60: 29801300

Hex: 0A61: 29821300

Hex: 0A62: 29841300

Hex: 0A63: 29861300

Hex: 0A64: 29881300

Hex: 0A66: 298C1300

Hex: 0A67: 298E1300

Hex: 0A69: 29921300

Hex: 0A6A: 29941300

Hex: 0A6B: 29961300

Hex: 0A6C: 29981300

Hex: 0A6E: 299C1300

Hex: 0A6F: 299E1300

Hex: 0A72: 29A41300

Hex: 0A73: 29A61300

Hex: 0A74: 29A81300

Hex: 0A76: 29AC1300

Hex: 0A77: 29AE1300

Hex: 0A7B: 29B61300

Hex: 0A7C: 29B81300

Hex: 0A7E: 29BC1300

Hex: 0A7F: 29BE1300

PC:

Hex: 0A80: 2A001300

Hex: 0A81: 2A021300

Hex: 0A82: 2A041300

Hex: 0A83: 2A061300

Hex: 0A84: 2A081300

Hex: 0A86: 2A0C1300

Hex: 0A87: 2A0E1300

Hex: 0A89: 2A121300

Hex: 0A8A: 2A141300

Hex: 0A8B: 2A161300

Hex: 0A8C: 2A181300

Hex: 0A8E: 2A1C1300

Hex: 0A8F: 2A1E1300

Hex: 0A92: 2A241300

Hex: 0A93: 2A261300

Hex: 0A94: 2A281300

Hex: 0A96: 2A2C1300

Hex: 0A97: 2A2E1300

Hex: 0A9B: 2A361300

Hex: 0A9C: 2A381300

Hex: 0A9E: 2A3C1300

Hex: 0A9F: 2A3E1300

AR:

Hex: 0AC0: 2B001300

Hex: 0AC1: 2B021300

Hex: 0AC2: 2B041300

Hex: 0AC3: 2B061300

Hex: 0AC4: 2B081300

Hex: 0AC6: 2B0C1300

Hex: 0AC7: 2B0E1300

Hex: 0AC9: 2B121300

Hex: 0ACA: 2B141300

Hex: 0ACB: 2B161300

Hex: 0ACC: 2B181300

Hex: 0ACE: 2B1C1300

Hex: 0ACF: 2B1E1300

Hex: 0AD2: 2B241300

Hex: 0AD3: 2B261300

Hex: 0AD4: 2B281300

Hex: 0AD6: 2B2C1300

Hex: 0AD7: 2B2E1300

Hex: 0ADB: 2B361300

Hex: 0ADC: 2B381300

Hex: 0ADE: 2B3C1300

Hex: 0ADF: 2B3E1300

SP:

Hex: 0AE0: 2B801300

Hex: 0AE1: 2B821300

Hex: 0AE2: 2B841300

Hex: 0AE3: 2B861300

Hex: 0AE4: 2B881300

Hex: 0AE6: 2B8C1300

Hex: 0AE7: 2B8E1300

Hex: 0AE9: 2B921300

Hex: 0AEA: 2B941300

Hex: 0AEB: 2B961300

Hex: 0AEC: 2B981300

Hex: 0AEE: 2B9C1300

Hex: 0AEF: 2B9E1300

Hex: 0AF2: 2BA41300

Hex: 0AF3: 2BA61300

Hex: 0AF4: 2BA81300

Hex: 0AF6: 2BAC1300

Hex: 0AF7: 2BAE1300

Hex: 0AFB: 2BB61300

Hex: 0AFC: 2BB81300

Hex: 0AFE: 2BBC1300

Hex: 0AFF: 2BBE1300

Mapping: Opcode - DESTREG - 2 LSB of new SRCREG1 - new SRCREG2

Just like AND

• F2 – RegisterFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = 2 LSB of F3, MuxCSel = 1, OutBSel = 2 LSB of F4FunSelALU = 1000, MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder FunSelRegister = 01 (Load)

• F2 – RegFile, F3 – RegFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4, MuxCSel = 0

OutBSel = the 2 LSB of F3, FunSelALU = 1000,

MuxASel = 11,

RegSelR = decode F2 and take the 4 LSB outputs of the decoder

FunSelR = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, OutBSel = the 2 LSB of F4

FunSelALU = 1000, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding F2

FunSelAdd = 01

• F2 – AddressFile, F3 – RegisterFile, F4 – AddressFile

OutCSel = the 2 MSB (bit 7, 6) of decoding F4

MuxCSel = 0, OutBSel = the 2 LSB of F3

FunSelALU = 1000, MuxBSel = 11,

RegSelAdd = bits 7,6, 4 of the output of decoding F2

FunSelAdd = 01

B NOT F2 \leftarrow NOT F3

Rn.

Hex: 0B00: 2C001300

Hex: 0B04: 2C101300

Hex: 0B08: 2C201300

Hex: 0B0C: 2C301300

Hex: 0B10: 2C401300

Hex: 0B18: 2C601300

Hex: 0B1C: 2C701300

R1:

Hex: 0B20: 2C801300

Hex: 0B24: 2C901300

Hex: 0B28: 2CA01300

Hex: 0B2C: 2CB01300

Hex: 0B30: 2CC01300

Hex: 0B38: 2CE01300

Hex: 0B3C: 2CF01300

R2:

Hex: 0B40: 2D001300

Hex: 0B44: 2D101300

Hex: 0B48: 2D201300

Hex: 0B4C: 2D301300

Hex: 0B50: 2D401300

Hex: 0B58: 2D601300

Hex: 0B5C: 2D701300

R3:

Hex: 0B60: 2D801300

Hex: 0B64: 2D901300

Hex: 0B68: 2DA01300

Hex: 0B6C: 2DB01300

Hex: 0B70: 2DC01300

Hex: 0B78: 2DE01300

Hex: 0B7C: 2DF01300

PC:

Hex: 0B80: 2E001300

Hex: 0B84: 2E101300

Hex: 0B88: 2E201300

Hex: 0B8C: 2E301300

Hex: 0B90: 2E401300

Hex: 0B98: 2E601300

Hex: 0B9C: 2E701300

AR:

Hex: 0BC0: 2F001300

Hex: 0BC4: 2F101300

Hex: 0BC8: 2F201300

Hex: 0BCC: 2F301300

Hex: 0BD0: 2F401300

Hex: 0BD8: 2F601300

Hex: 0BDC: 2F701300

SP:

Hex: 0BE0: 2F801300

Hex: 0BE4: 2F901300

Hex: 0BE8: 2FA01300

Hex: 0BEC: 2FB01300

Hex: 0BF0: 2FC01300

Hex: 0BF8: 2FE01300

Hex: 0BFC: 2FF01300

Mapping: Opcode DESTREG SRCREG1 00

Similar to MOV but not quite (the last case - need to pass through the ALU)

• F2 and F3 both belong to RegisterFile

 $OutBSel-the\ 2\ LSB\ of\ F3,\ FunSelALU-0011\ not\ B)$

MuxASel = 11,

RegSelReg = decode F2 and take the 4 LSB outputs of the decoder

FunSelRegister = 01 (Load)

• F2 and F3 both belong to AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F3

MuxCSel = 0(OutCSel will be forwarded to the A input of the ALU)

FunSelALU = 0010 (not A)

MuxBSel = 11 (the OutALU)

RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2

FunSelAddress = 01 (load)

• F2 – AddressRegister, F3 – RegisterFile

OutBSel = the 2 LSB of F3, FunSelALU = 0011(not B)

MuxBSel = 11,

RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2

FunSelAddress = 01 (load)

• F2 – RegisterFile, F3 – AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F3

MuxCSel = 0, FunSelALU = 0010 (not A)

MuxASel = 11,

RegSelR – decode F2 and take the 4 LSB outputs of the decoder

FunSelReg = 01

$C LSL F2 \leftarrow LSL F3$

R0:

Hex: 0C00: 30001300

Hex: 0C04: 30101300

Hex: 0C08: 30201300

Hex: 0C0C: 30301300

Hex: 0C10: 30401300

Hex: 0C18: 30601300

Hex: 0C1C: 30701300

R1:

Hex: 0C20: 30801300

Hex: 0C24: 30901300

Hex: 0C28: 30A01300

Hex: 0C2C: 30B01300

Hex: 0C30: 30C01300

Hex: 0C38: 30E01300

Hex: 0C3C: 30F01300

R2:

Hex: 0C40: 31001300

Hex: 0C44: 31101300

Hex: 0C48: 31201300

Hex: 0C4C: 31301300

Hex: 0C50: 31401300

Hex: 0C58: 31601300

Hex: 0C5C: 31701300

R3:

Hex: 0C60: 31801300

Hex: 0C64: 31901300

Hex: 0C68: 31A01300

Hex: 0C6C: 31B01300

Hex: 0C70: 31C01300

Hex: 0C78: 31E01300

Hex: 0C7C: 31F01300

PC:

Hex: 0C80: 32001300

Hex: 0C84: 32101300

Hex: 0C88: 32201300

Hex: 0C8C: 32301300

Hex: 0C90: 32401300

Hex: 0C98: 32601300

Hex: 0C9C: 32701300

AR:

Hex: 0CC0: 33001300

Hex: 0CC4: 33101300

Hex: 0CC8: 33201300

Hex: 0CCC: 33301300

Hex: 0CD0: 33401300

Hex: 0CD8: 33601300

Hex: 0CDC: 33701300

Hex: 0CE0: 33801300

Hex: 0CE4: 33901300

Hex: 0CE8: 33A01300

Hex: 0CEC: 33B01300

Hex: 0CF0: 33C01300

Hex: 0CF8: 33E01300

Hex: 0CFC: 33F01300

Opcode DESTREG SRCREG1 00

Like not – change ALU operation and make sure that SRCREG1 is at input A of ALU (we can perform LSL and LSR only on A)

• F2 and F3 both belong to RegisterFile

OutASel – the 2 LSB of F3, MuxCSel = 1, FunSelALU – 1010 (LSL A) MuxASel = 11,

 $RegSelReg = decode\ F2$ and take the 4 LSB outputs of the decoder FunSelRegister = 01 (Load)

• F2 and F3 both belong to AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F3

MuxCSel = 0 (the OutCSel will be forwarded to the A input of the ALU)

FunSelALU = 1010 (LSL A)

MuxBSel = 11 (the OutALU)

RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2

FunSelAddress = 01 (load)

• F2 – AddressRegister, F3 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, FunSelALU = 1010 (LSL A)

MuxBSel = 11,

RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2

FunSelAddress = 01 (load)

• F2 – RegisterFile, F3 – AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F2

MuxCSel = 0, FunSelALU = 1010 (LSL A)

MuxASel = 11,

RegSelR – decode F2 and take the 4 LSB outputs of the decoder

FunSelReg = 01

D LSR F2 \leftarrow LSR F3 R0:

Hex: 0D00: 34001300

Hex: 0D04: 34101300

Hex: 0D08: 34201300

Hex: 0D0C: 34301300

Hex: 0D10: 34401300

Hex: 0D18: 34601300

Hex: 0D1C: 34701300

R1:

Hex: 0D20: 34801300

Hex: 0D24: 34901300

Hex: 0D28: 34A01300

Hex: 0D2C: 34B01300

Hex: 0D30: 34C01300

Hex: 0D38: 34E01300

Hex: 0D3C: 34F01300

R2:

Hex: 0D40: 35001300

Hex: 0D44: 35101300

Hex: 0D48: 35201300

Hex: 0D4C: 35301300

Hex: 0D50: 35401300

Hex: 0D58: 35601300

Hex: 0D5C: 35701300

R3:

Hex: 0D60: 35801300

Hex: 0D64: 35901300

Hex: 0D68: 35A01300

Hex: 0D6C: 35B01300

Hex: 0D70: 35C01300

Hex: 0D78: 35E01300

Hex: 0D7C: 35F01300

PC:

Hex: 0D80: 36001300

Hex: 0D84: 36101300

Hex: 0D88: 36201300

Hex: 0D8C: 36301300

Hex: 0D90: 36401300

Hex: 0D98: 36601300

Hex: 0D9C: 36701300

AR:

Hex: 0DC0: 37001300

Hex: 0DC4: 37101300

Hex: 0DC8: 37201300

Hex: 0DCC: 37301300

Hex: 0DD0: 37401300

Hex: 0DD8: 37601300

Hex: 0DDC: 37701300

SP:

Hex: 0DE0: 37801300

Hex: 0DE4: 37901300

Hex: 0DE8: 37A01300

Hex: 0DEC: 37B01300

Hex: 0DF0: 37C01300

Hex: 0DF8: 37E01300

Hex: 0DFC: 37F01300

Opcode DESTREG SRCREG1 00

Like not – change ALU operation and make sure that SRCREG1 is at input A of ALU

• F2 and F3 both belong to RegisterFile

OutASel – the 2 LSB of F3, MuxCSel = 1, FunSelALU – 1011 (LSR A) MuxASel = 11, RegSelReg = decode F2 and take the 4 LSB outputs of the decoder FunSelRegister = 01 (Load)

• F2 and F3 both belong to AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F3

MuxCSel = 0 (the OutCSel will be forwarded to the A input of the ALU)

FunSelALU = 1011 (LSR A)

MuxBSel = 11 (the OutALU)

RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2

FunSelAddress = 01 (load)

• F2 – AddressRegister, F3 – RegisterFile

OutASel = the 2 LSB of F3, MuxCSel = 1, FunSelALU = 1011 (LSR A) MuxBSel = 11, RegSelAdd = like above – bits 7,6, 4 of the output of decoding F2 FunSelAddress = 01 (load)

• F2 – RegisterFile, F3 – AddressRegister

OutCSel = the 2 MSB (bit 7, 6) of decoding F3 MuxCSel = 0, FunSelALU = 1011 (LSR A) MuxASel = 11, RegSelR – decode F2 and take the 4 LSB outputs of the decoder FunSelReg = 01

$E BRA IM PC \leftarrow VALUE$

- value is the address field of the instruction

Hex: 0E00: 38001300

Mapping: Opcode 000 000 00

MuxBSel = 01, RegSelAddress = 001 (PC), FunSelAdd = 01 (Load)

F BEQ IM – check condition if Z = 1 then $PC \leftarrow VALUE$

Address in control memory of $PC \leftarrow Value$

true (=1) – jump to the PC \leftarrow Value

Hex: 0F00: 3C008E00

Mapping: Opcode 000 000 00

10 BNE IM – check condition if Z = 0 then $PC \leftarrow VALUE$

0, jump to PC \leftarrow Value

Hex: 1000: 40010E00

Z' is a separate status bit -Z' = 1 means that Z = 0

Mapping: Opcode $000\ 000\ 00$

11 CALL IM M[SP] \leftarrow PC, SP \leftarrow SP - 1, PC \leftarrow VALUE

- IM so that its address field of the microinstruction

 \leftarrow PC, (use subroutine call and return)

Hex: 1100: 44002380

(can make the subroutine call to that address only with the modifications on Push routine

which makes the M[SP] \leftarrow PC)

call

Hex: 1101: 46DA27E1

Go to $SP \leftarrow SP - 1$ subroutine

10001 000 000 10: NOP 00 00 01110 000 000 00 Go to PC \leftarrow VALUE

Hex: 1102: 46DA0E00

Mapping: Opcode 000 000 00

12 RET SP \leftarrow SP + 1, PC \leftarrow M[SP]

Or maybe it should store no operation and then make the unconditional jump to subroutine

10010 000 000 00: 10010 101 101 101 00 01 01000 111 000 01– go to subroutine SP \leftarrow SP + 1

Hex: 1200: 4ADA28E1

unconditional jump Hex: 1201: 4ADA0481

Mapping: Opcode 000 000 00

FETCH SUBROUTINE

10011 000 000 10: 10011 101 101 101 00 01 01000 100 000 10 -NOP and jump to PC \leftarrow PC + 1 (the special one, that acts as a subroutine) Hex: 1302: 4EDA2882

Last bit = 0

OutDSel = 00 (PC), Sel = 1, LD = 1

MuxDSel = 1 (the higher bits)

L/H = 1, FunSelIR = 11, E = 1

FunSelIR will always be 1 – we only load to it – if its not enabled nothing will be changed

Last bit = 1

OutDSel = 00 (PC), Sel = 1, LD = 1

MuxDSel = 0 (the lower bits)

L/H = 0, FunSelIR = 11, E = 1

SUBROUTINE RETURN CHECK ROUTINE

 $10100\ 000\ 000\ 00$: $10100\ 101\ 101\ 101\ 11\ 00\ 10100\ 000\ 000\ 11$ – NOP jump to this address if S is 1 - to the address that makes the subroutine return.

1400: 52DB9403

S is a special status bit, used to show whether we the instruction that we are performing has a subroutine call.

There are certain routines stored in ROM which may either be used on their own or as subroutine calls, and their next address changes according to the situation If it was a subroutine call, it returns from the subroutine, to the address stored in the SBR (Subroutine Register). If not it goes to fetch.

If BR is 10 – it does not depend on the condition bit, it will make the return anyway, this first instruction is to check the condition.

If the S status bit is 0 – means this was not a subroutine call and we come to the next address which realizes a jump to fetch.

 $10100\ 000\ 000\ 01$: $10100\ 101\ 101\ 101\ 00\ 00\ 10011\ 000\ 000\ 00$ - NOP and go to fetch 1401: $52\mathrm{DA}1300$

3 RESULTS

We tried to implement the example program that was given in the file. First of all, we converted the instructions into hex code and decided the address in RAM where they should be written.

Table 1: Example Program

Address in memory	Instruction in hex	Instruction description
0x00	7020	ORG 0x20 (BRA instruction)
0x20	0005	LD R0 IM 0x05
0x21	0200	LD R1 IM 0x00
0x22	04A0	LD R2 IM 0xA0
0x23	1640	MOV AR R2
0x24	0500	LD R2 D (LABEL)
0x25	46C0	INC AR AR
0x26	2928	ADD R1 R1 R2
0x27	3800	DEC R0 R0
0x28	8024	BNE IM LABEL
0x29	0b00	ST R1 D

As displayed in the following figure, We wrote them into RAM according to table 1.

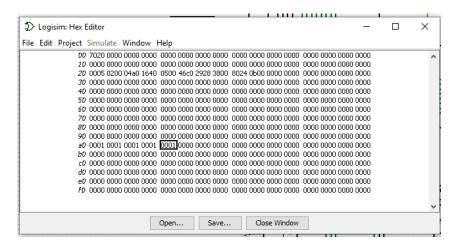


Figure 5: Entering the program into RAM

The aim of the program is to perform M[A0] + M[A1] + M[A2] + M[A3] + M[A4] and store it at M[A5]. We chose some arbitrary values for M[A0 - A4]. In our case we wrote a 0x01 value in all those memory addresses of the RAM. When executing their sum, 0x05 was computed and it was successfully stored in memory address A5, as displayed in the figure 6.

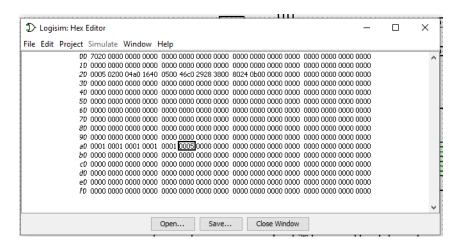


Figure 6: The result of executing the program

4 DISCUSSION

Microprogram consists of microinstructions and it is program stored in memory that generates all the control signals required to execute the instruction set correctly. Microinstruction contains a control word and a sequencing word. In this project we designed microprogrammed control unit. CPU gives instructions to the control unit and control unit performs the actual physical transfer of data. The microinstructions stored in the

ROM will be the same for the different programs that we may try to implement. The programs will be loaded in the RAM and will be executed accordingly.

Generally, our team tried to complete the requirements flawlessly in the most effective way as much as possible without any complex design.

5 CONCLUSION

By doing last 2 projects we are more familiar with Control Unit (CU) design which is a component of a computer's central processing unit (CPU). CPU is one of the most important parts of computer, so we can say that CU is also an important component of the basic computer. CU which we designed can perform 18 different operations. All in all, we gained experience on software-based implementing of CU.

REFERENCES

[1] BLG 222E - Computer Organization Course. Slide week 9-10. Available : https://ninova.itu.edu.tr/Sinif/3557.42763/SinifDosyalari?g1827319