SMV Tutorial

CS4211 - Formal Methods for Software Engineering

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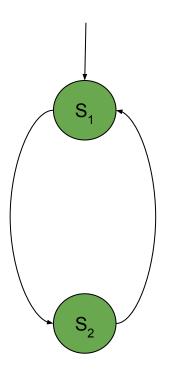
Writing First Program Simple Transition



Demo Code

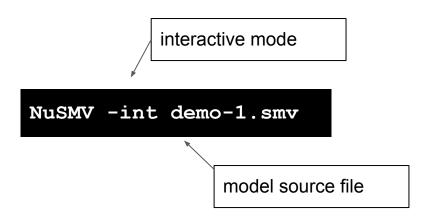
```
MODULE main
VAR
     state: {s1, s2};

ASSIGN
     init(state) := s1;
     next(state) := case
          state = s1 : s2;
          state = s2 : s1;
          esac;
```





Build Model



Commands:

- op go
 - read model
 - flatten_hierarchy
 - encode variables
 - build_model
- o goto state
- o pick_state
- print current state
- o print reachable states
- o simulate
- o show_traces



Load & Build Model

```
NuSMV > read_model -i demo-1.smv
NuSMV > flatten_hierarchy
NuSMV > encode_variables
NuSMV > build_model
NuSMV > go
```



Describe a Model

```
NuSMV > print_reachable_states -v
```



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Infinite Loop Traffic Light





Traffic Light Code





Run a Simulation (random)

```
NuSMV > pick_state -r
NuSMV > simulate -r -k 5
NuSMV > print_current_state -v

******** Simulation Starting From State 1.1  *******
Current state is 1.6
light = red
```



Show Trace

```
NuSMV > show_traces -t
NuSMV > show_traces 1
```



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Run a Simulation (interactive)

```
NuSMV > pick_state -i
NuSMV > simulate -i -k 5
NuSMV > print_current_state -v

******* Simulation Starting From State 1.1  *******
Current state is 1.6
light = green
```



Revisit a State and Replay

```
NuSMV > goto_state 1.11
NuSMV > simluate -r -k 4
NuSMV > show traces -v
  Trace Description: Simulation Trace
Trace Type: Simulation
 -> State: 3.1 <-
   light = green
 -> State: 3.2 <-
   light = yellow
 -> State: 3.3 <-
   light = red
```



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Process Communication Alternate Bit Protocol



ABP Code

```
MODULE receiver (input, output)
MODULE main
                                               ASSIGN
VAR
                                                   next(output) := input;
    toS: boolean;
                                               FATRNESS
    toR: boolean;
                                                   running
    rcvr: process receiver(toR, toS);
    sndr: process sender(toS, toR);
                                               MODULE receiver (input, output)
ASSIGN
                                               ASSIGN
    init(toS):= FALSE;
                                                   next(output) := !input;
    init(toR):= FALSE;
                                               FAIRNESS
                                                   running
```





Multiple Processes Dining Troopers

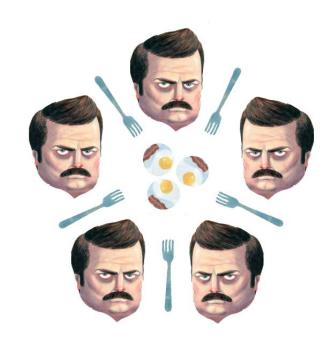




The dining philosophers problem is a classic concurrency problem dealing with synchronization.

Source:

http://adit.io/posts/2013-05-11-The-Dining-Philosophers-Problem-With-Ron-Swanson.html





Now, each philosopher has two forks: left fork and right fork. If a Philosopher gets two forks, he can eat!



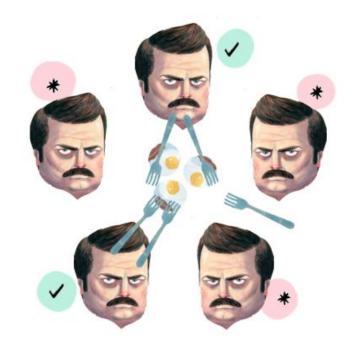
If Ron gets two forks, he can eat!



If he only has one fork he can't eat:(



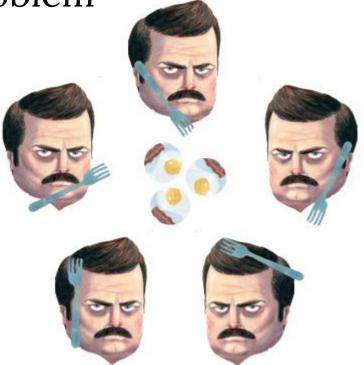
The dining philosophers problem is: how do you make sure every Philosopher gets to eat?





every Philosopher grabbed a fork: and then they waited for someone to give up their fork so they could eat. But of course, "a Philosopher never gives up his fork!" sigh So they waited forever and eventually died in their cabin.

Great job, guys. When all Philosophers are stuck, that is called **deadlock**.





```
MODULE trooper (forks)
VAR
     state: {not-eating, eating, waiting};
ASSIGN
     init(state) := not-eating;
     next(state) := case
                         state = not-eating & forks > 0 : waiting;
                         state = waiting & forks > 0 : eating;
                         state = eating : not-eating;
                         TRUE: state;
                    esac:
     next(forks) := case
                    state = not-eating & forks > 0: forks -1;
                    state = waiting & forks > 0 : forks -1;
                    state = eating : 2;
                    TRUE: forks:
                    esac;
```





Dining Troopers

Is everything implemented correctly?

How can we verify our implementation is correct?



```
LTLSPEC G !((troop_1.state = eating) & (troop_2.state = eating))
LTLSPEC G(F (troop_1.state = eating) | F (troop_2.state = eating))
```

```
NuSMV troops.smv
-- specification G !(troop1.state = eating & troop2.state = eating) is true

-- specification G ( F troop1.state = eating | F troop2.state = eating) is false
-- as demonstrated by the following execution sequence

Trace Description: LTL Counterexample
Trace Type: Counterexample
```



DEADLOCK



```
MODULE trooper (forks)
 VAR
      state: {not-eating, eating, waiting};
 ASSIGN
      init(state) := not-eating;
      next(state) := case
                           state = not-eating & forks > 0 : waiting;
                           state = waiting & forks > 0 : eating;
                           state = waiting & forks = 0 : not-eating;
                           state = eating : not-eating;
                           TRUE: state;
                      esac:
      next(forks) := case
                      state = not-eating & forks > 0 : forks -1;
                      state = waiting & forks > 0 : forks -1;
                      state = waiting & forks = 0 : forks + 1;
                      state = eating : 2;
                      TRUE: forks:
                      esac;
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```





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```
LTLSPEC G !((troop_1.state = eating) & (troop_2.state = eating))
LTLSPEC G(F (troop1.state = eating) | F (troop2.state = eating))
```

```
NuSMV troops.smv
-- specification G !(troop1.state = eating & troop2.state = eating) is true

-- specification G (F troop1.state = eating | F troop2.state = eating) is false
-- as demonstrated by the following execution sequence
Trace Description: LTL Counterexample
Trace Type: Counterexample
```



LIVELOCK

```
MODULE trooper (forks)
VAR
     state: {not-eating, eating};
ASSIGN
     init(state) := not-eating;
     next(state) := case
                          state = not-eating & forks = 2 : eating;
                          state = eating : not-eating;
                          TRUE: state;
                    esac;
     next(forks) := case
                    state = not-eating & forks = 2 : 0;
                    state = eating : 2;
                    TRUE: forks;
                    esac;
```



```
LTLSPEC G !((troop_1.state = eating) & (troop_2.state = eating))

LTLSPEC G(F (troop1.state = eating) | F (troop2.state = eating))

LTLSPEC G(F (troop1.state = eating) & F (troop2.state = eating))

NuSMV troops.smv

-- specification G !(troop1 state = eating & troop2 state
```

```
NuSMV troops.smv
-- specification G !(troop1.state = eating & troop2.state = eating) is true

-- specification G ( F troop1.state = eating | F troop2.state = eating) is true

-- specification G ( F troop1.state = eating & F troop2.state = eating) is false

-- as demonstrated by the following execution sequence
```

STARVATION





Q&A



Thank You!

