
STM32
CubeMX

1. Description

1.1. Project

Project Name	G05_SEM4405_2024
Board Name	NUCLEO-H7A3ZI-Q
Generated with:	STM32CubeMX 6.10.0
Date	03/11/2024

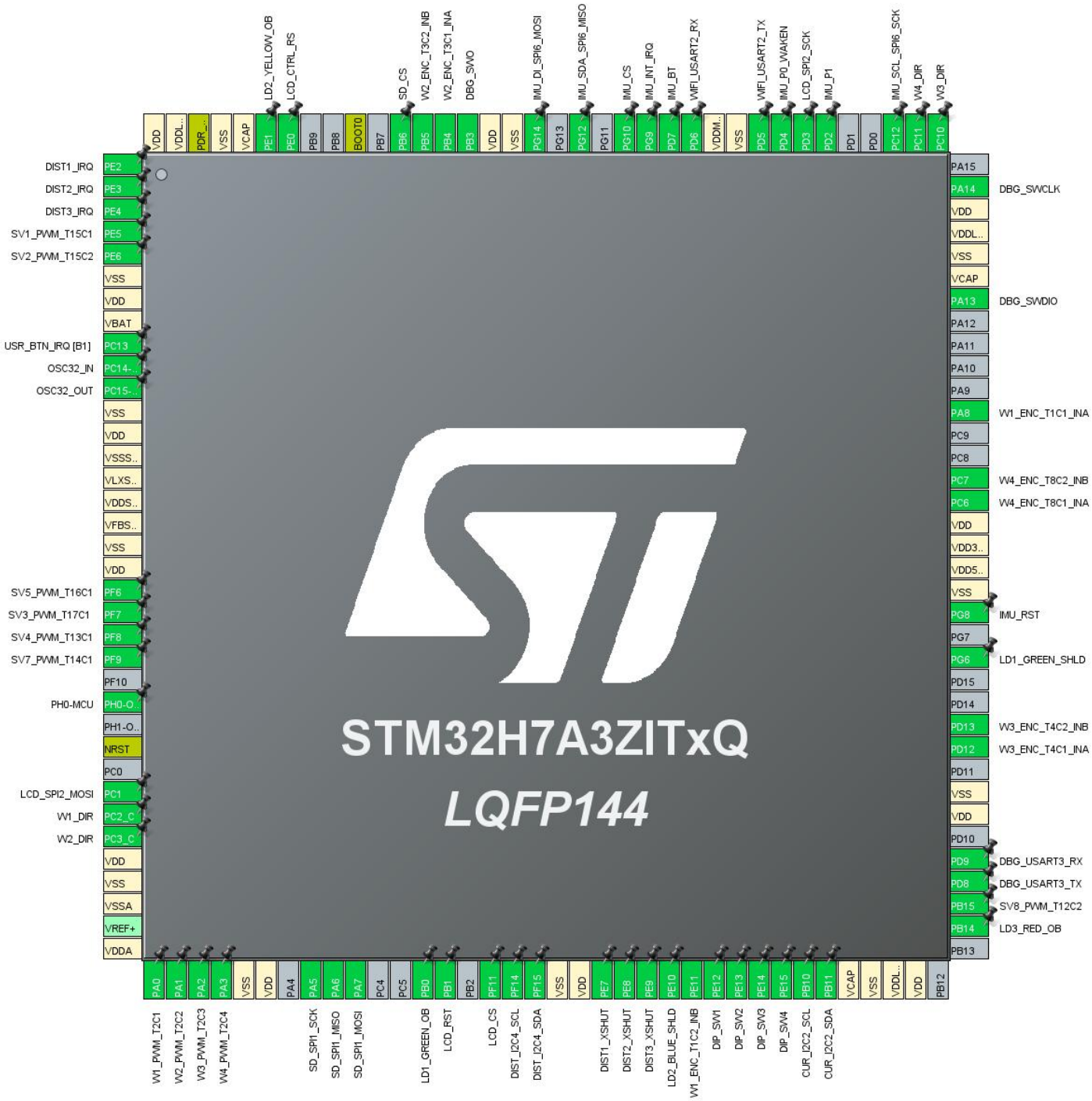
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7A3/7B3
MCU name	STM32H7A3ZITxQ
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	DIST1_IRQ
2	PE3	I/O	GPIO_EXTI3	DIST2_IRQ
3	PE4	I/O	GPIO_EXTI4	DIST3_IRQ
4	PE5	I/O	TIM15_CH1	SV1_PWM_T15C1
5	PE6	I/O	TIM15_CH2	SV2_PWM_T15C2
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
9	PC13	I/O	GPIO_EXTI13	USR_BTN_IRQ [B1]
10	PC14-OSC32_IN	I/O	RCC_OSC32_IN	OSC32_IN
11	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	OSC32_OUT
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
20	PF6	I/O	TIM16_CH1	SV5_PWM_T16C1
21	PF7	I/O	TIM17_CH1	SV3_PWM_T17C1
22	PF8	I/O	TIM13_CH1	SV4_PWM_T13C1
23	PF9	I/O	TIM14_CH1	SV7_PWM_T14C1
25	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-MCU
27	NRST	Reset		
29	PC1	I/O	SPI2_MOSI	LCD_SPI2_MOSI
30	PC2_C *	I/O	GPIO_Output	W1_DIR
31	PC3_C *	I/O	GPIO_Output	W2_DIR
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
37	PA0	I/O	TIM2_CH1	W1_PWM_T2C1
38	PA1	I/O	TIM2_CH2	W2_PWM_T2C2
39	PA2	I/O	TIM2_CH3	W3_PWM_T2C3
40	PA3	I/O	TIM2_CH4	W4_PWM_T2C4

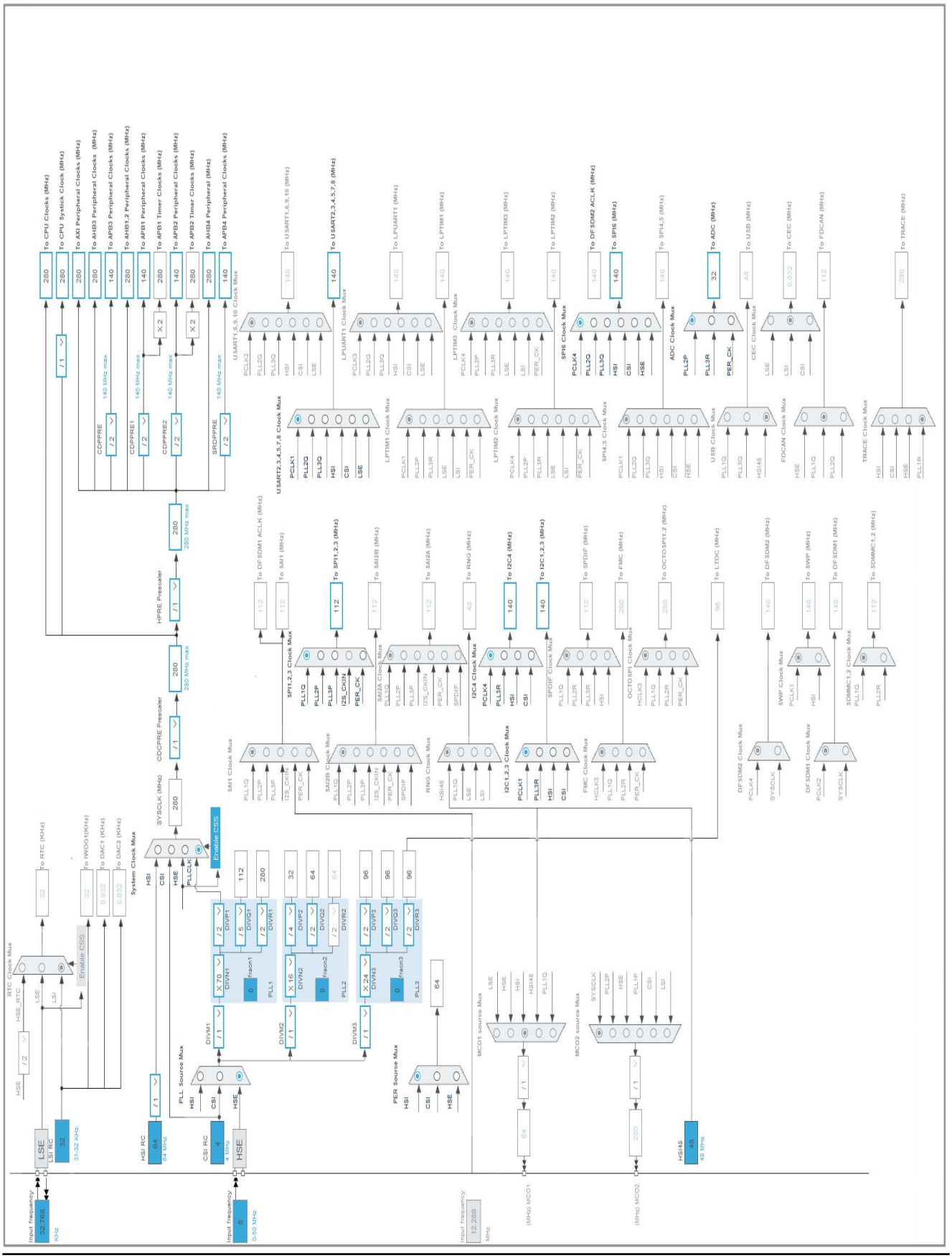
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	VSS	Power		
42	VDD	Power		
44	PA5	I/O	SPI1_SCK	SD_SPI1_SCK
45	PA6	I/O	SPI1_MISO	SD_SPI1_MISO
46	PA7	I/O	SPI1_MOSI	SD_SPI1_MOSI
49	PB0 *	I/O	GPIO_Output	LD1_GREEN_OB
50	PB1 *	I/O	GPIO_Output	LCD_RST
52	PF11 *	I/O	GPIO_Output	LCD_CS
53	PF14	I/O	I2C4_SCL	DIST_I2C4_SCL
54	PF15	I/O	I2C4_SDA	DIST_I2C4_SDA
55	VSS	Power		
56	VDD	Power		
57	PE7 *	I/O	GPIO_Output	DIST1_XSHUT
58	PE8 *	I/O	GPIO_Output	DIST2_XSHUT
59	PE9 *	I/O	GPIO_Output	DIST3_XSHUT
60	PE10 *	I/O	GPIO_Output	LD2_BLUE_SHLD
61	PE11	I/O	TIM1_CH2	W1_ENC_T1C2_INB
62	PE12 *	I/O	GPIO_Input	DIP_SW1
63	PE13 *	I/O	GPIO_Input	DIP_SW2
64	PE14 *	I/O	GPIO_Input	DIP_SW3
65	PE15 *	I/O	GPIO_Input	DIP_SW4
66	PB10	I/O	I2C2_SCL	CUR_I2C2_SCL
67	PB11	I/O	I2C2_SDA	CUR_I2C2_SDA
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
74	PB14 *	I/O	GPIO_Output	LD3_RED_OB
75	PB15	I/O	TIM12_CH2	SV8_PWM_T12C2
76	PD8	I/O	USART3_TX	DBG_USART3_TX
77	PD9	I/O	USART3_RX	DBG_USART3_RX
79	VDD	Power		
80	VSS	Power		
82	PD12	I/O	TIM4_CH1	W3_ENC_T4C1_INA
83	PD13	I/O	TIM4_CH2	W3_ENC_T4C2_INB
86	PG6 *	I/O	GPIO_Output	LD1_GREEN_SHLD
88	PG8 *	I/O	GPIO_Output	IMU_RST
89	VSS	Power		
90	VDD50_USB	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
91	VDD33_USB	Power		
92	VDD	Power		
93	PC6	I/O	TIM8_CH1	W4_ENC_T8C1_INA
94	PC7	I/O	TIM8_CH2	W4_ENC_T8C2_INB
97	PA8	I/O	TIM1_CH1	W1_ENC_T1C1_INA
102	PA13	I/O	DEBUG_JTMS-SWDIO	DBG_SWDIO
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14	I/O	DEBUG_JTCK-SWCLK	DBG_SWCLK
109	PC10 *	I/O	GPIO_Output	W3_DIR
110	PC11 *	I/O	GPIO_Output	W4_DIR
111	PC12	I/O	SPI6_SCK	IMU_SCL_SPI6_SCK
114	PD2 *	I/O	GPIO_Output	IMU_P1
115	PD3	I/O	SPI2_SCK	LCD_SPI2_SCK
116	PD4 *	I/O	GPIO_Output	IMU_P0_WAKEN
117	PD5	I/O	USART2_TX	WIFI_USART2_TX
118	VSS	Power		
119	VDDMMC	Power		
120	PD6	I/O	USART2_RX	WIFI_USART2_RX
121	PD7 *	I/O	GPIO_Output	IMU_BT
122	PG9	I/O	GPIO_EXTI9	IMU_INT_IRQ
123	PG10 *	I/O	GPIO_Output	IMU_CS
125	PG12	I/O	SPI6_MISO	IMU_SDA_SPI6_MISO
127	PG14	I/O	SPI6_MOSI	IMU_DI_SPI6_MOSI
128	VSS	Power		
129	VDD	Power		
130	PB3	I/O	DEBUG_JTDO-SWO	DBG_SWO
131	PB4	I/O	TIM3_CH1	W2_ENC_T3C1_INA
132	PB5	I/O	TIM3_CH2	W2_ENC_T3C2_INB
133	PB6 *	I/O	GPIO_Output	SD_CS
135	BOOT0	Boot		
138	PE0 *	I/O	GPIO_Output	LCD_CTRL_RS
139	PE1 *	I/O	GPIO_Output	LD2_YELLOW_OB
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Reset		
143	VDDLDO	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	G05_SEM4405_2024
Project Folder	C:\STM32_ECE225\G05_SEM4405_2024
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART3_UART_Init	USART3
4	MX_SPI1_Init	SPI1
5	MX_USART2_UART_Init	USART2
6	MX_I2C2_Init	I2C2
7	MX_I2C4_Init	I2C4
8	MX_SPI2_Init	SPI2
9	MX_FATFS_Init	FATFS
10	MX_ADC2_Init	ADC2
11	MX_CRC_Init	CRC

Rank	Function Name	Peripheral Instance Name
12	MX_SPI6_Init	SPI6
13	MX_TIM1_Init	TIM1
14	MX_TIM2_Init	TIM2
15	MX_TIM3_Init	TIM3
16	MX_TIM4_Init	TIM4
17	MX_TIM5_Init	TIM5
18	MX_TIM8_Init	TIM8
19	MX_TIM12_Init	TIM12
20	MX_TIM13_Init	TIM13
21	MX_TIM14_Init	TIM14
22	MX_TIM15_Init	TIM15
23	MX_TIM16_Init	TIM16
24	MX_TIM17_Init	TIM17

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7A3/7B3
MCU	STM32H7A3ZITxQ
Datasheet	DS13139_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

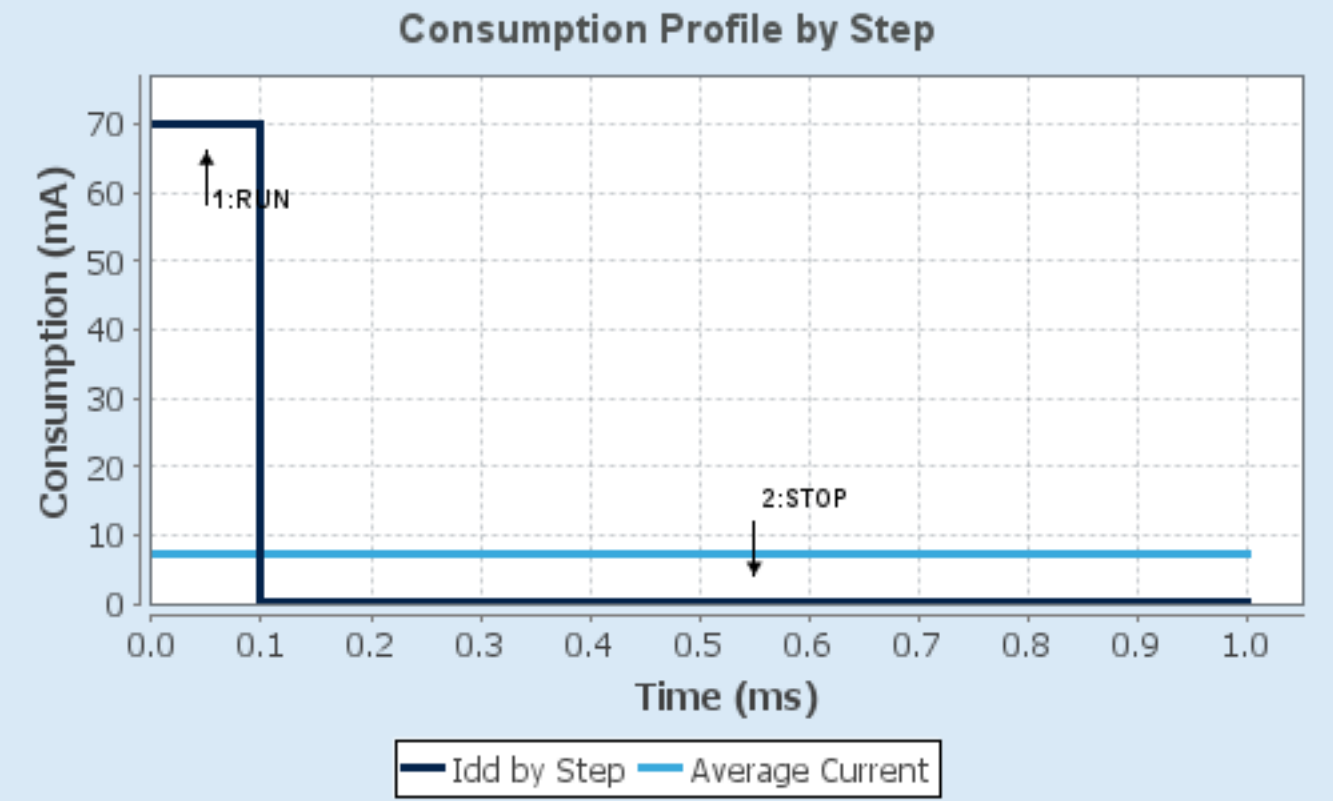
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0	SVOS5
SRDomain	DRUN	DSTOP
n/a	SRDRUN	SRDSTOP
Fetch Type	ITCM/DTCM/Cache	NA
CPU Frequency	280 MHz	64 MHz
Clock Configuration	HSE PLL	HSI Flash-ON
Clock Source Frequency	16 MHz	64 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	69.92 mA	263.82 µA
Duration	0.1 ms	0.9 ms
DMIPS	599.0	0.0
Ta Max	115.77	124.97
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	7.23 mA
Battery Life	19 days, 14 hours	Average DMIPS	599.2 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
70
60
50
40
30
20
10
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC2

mode: Temperature Sensor Channel

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel Temperature Sensor
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. CRC

mode: Activated

2.2.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

2.3. DEBUG

Debug: Trace Asynchronous Sw

2.4. I2C2

I2C: I2C

2.4.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00D04BFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	**0x40 ***

2.5. I2C4

I2C: I2C

2.5.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00D04BFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	**0x29 ***

2.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.6.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

2.7. SPI1

Mode: Full-Duplex Master

2.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**437.5 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.8. SPI2

Mode: Transmit Only Master

2.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**28.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.9. SPI6

Mode: Full-Duplex Master

2.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**1.09375 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

2.10. SYS

Timebase Source: TIM7

2.11. TIM1

Combined Channels: Encoder Mode

2.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

2.12. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

2.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**13999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1

Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.13. TIM3

Combined Channels: Encoder Mode

2.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

2.14. TIM4

Combined Channels: Encoder Mode

2.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

2.15. TIM5

Clock Source : Internal Clock

2.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**279 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

2.16. TIM8

Combined Channels: Encoder Mode

2.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

2.17. TIM12

Channel2: PWM Generation CH2

2.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.18. TIM13

mode: Activated

Channel1: PWM Generation CH1

2.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.19. TIM14

mode: Activated

Channel1: PWM Generation CH1

2.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.20. TIM15

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

2.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable

BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.21. TIM16

mode: Activated

Channel1: PWM Generation CH1

2.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.22. TIM17

mode: Activated

Channel1: PWM Generation CH1

2.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**85 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65115 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	

- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**4883 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.23. USART2

Mode: Asynchronous

2.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.24. USART3

Mode: Asynchronous

2.24.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.25. FATFS

mode: User-defined

2.25.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId_t
FS_LOCK (Number of files opened simultaneously)	2

2.26. FREERTOS

Interface: CMSIS_V2

2.26.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	**1024 ***
MAX_TASK_NAME_LEN	**18 ***
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**204800 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled

MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	2048

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

2.26.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled

xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.26.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	DBG_SWDIO
	PA14	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	DBG_SWCLK
	PB3	DEBUG_JTDO-SWO	n/a	n/a	n/a	DBG_SWO
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	CUR_I2C2_SCL
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	CUR_I2C2_SDA
I2C4	PF14	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	DIST_I2C4_SCL
	PF15	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	DIST_I2C4_SDA
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	OSC32_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	OSC32_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-MCU
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SD_SPI1_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	**Pull-up ***	**Very High ***	SD_SPI1_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	**Pull-up ***	**Very High ***	SD_SPI1_MOSI
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LCD_SPI2_MOSI
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LCD_SPI2_SCK
SPI6	PC12	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SCL_SPI6_SCK
	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SDA_SPI6_MISO
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_DI_SPI6_MOSI

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM1	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	W1_ENC_T1C2_INB
	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	W1_ENC_T1C1_INA
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	W1_PWM_T2C1
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	W2_PWM_T2C2
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	W3_PWM_T2C3
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	W4_PWM_T2C4
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	W2_ENC_T3C1_INA
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	W2_ENC_T3C2_INB
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	W3_ENC_T4C1_INA
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	W3_ENC_T4C2_INB
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	W4_ENC_T8C1_INA
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	W4_ENC_T8C2_INB
TIM12	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV8_PWM_T12C2
TIM13	PF8	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV4_PWM_T13C1
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV7_PWM_T14C1
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV1_PWM_T15C1
	PE6	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV2_PWM_T15C2
TIM16	PF6	TIM16_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV5_PWM_T16C1
TIM17	PF7	TIM17_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SV3_PWM_T17C1
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	WIFI_USART2_TX
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	WIFI_USART2_RX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DBG_USART3_TX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DBG_USART3_RX
GPIO	PE2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIST1_IRQ
	PE3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIST2_IRQ
	PE4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	DIST3_IRQ
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USR_BTN_IRQ [B1]
	PC2_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W1_DIR
	PC3_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W2_DIR
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1_GREEN_OB
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_CS
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIST1_XSHUT
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIST2_XSHUT
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIST3_XSHUT
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2_BLUE_SHLD
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_SW1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_SW2
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_SW3
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_SW4
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3_RED_OB
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1_GREEN_SHLD
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_RST
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W3_DIR
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W4_DIR
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_P1
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_P0_WAKEN
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_BT
	PG9	GPIO_EXTI9	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	IMU_INT_IRQ
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_CS
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CS
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_CTRL_RS
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2_YELLOW_OB

3.2. DMA configuration

nothing configured in DMA service

3.3. BDMA1 configuration

nothing configured in DMA service

3.4. BDMA2 configuration

nothing configured in DMA service

3.5. MDMA configuration

nothing configured in DMA service

3.6. NVIC configuration

3.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line2 interrupt	true	5	0
EXTI line3 interrupt	true	5	0
EXTI line4 interrupt	true	5	0
ADC1 and ADC2 global interrupts	true	5	0
EXTI line[9:5] interrupts	true	5	0
SPI2 global interrupt	true	5	0
USART2 global interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
TIM7 global interrupt	true	15	0
SPI6 global interrupt	true	5	0
PVD and PVM interrupts through EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
TIM15 global interrupt	unused		
TIM16 global interrupt	unused		
TIM17 global interrupt	unused		
HSEM1 global interrupt	unused		
ECC diagnostic Global Interrupt	unused		

3.6.2. NVIC Code generation

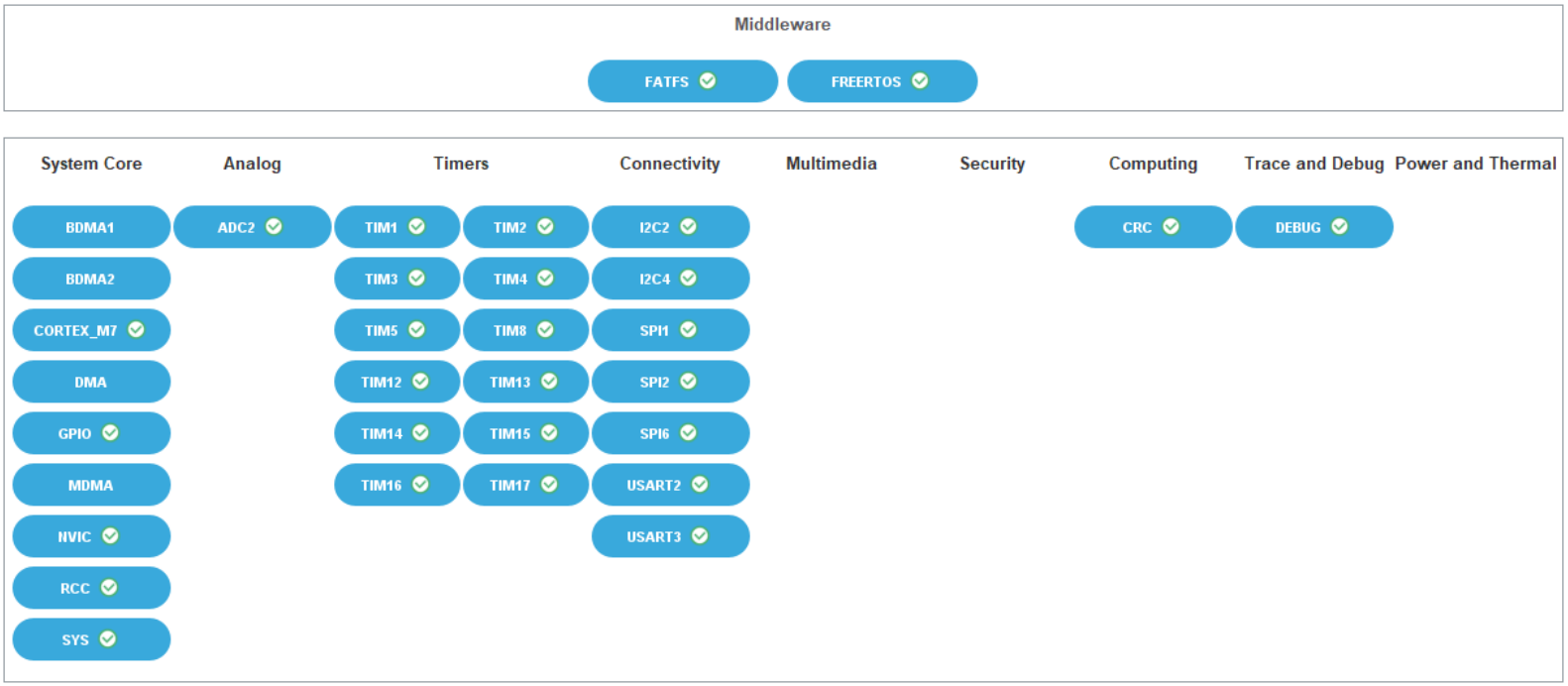
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI line2 interrupt	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line4 interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
EXTI line[9:5] interrupts	false	true	true
SPI2 global interrupt	false	true	true
USART2 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM7 global interrupt	false	true	true
SPI6 global interrupt	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current



5. Docs & Resources

Type	Link