

**CSE 331 – COMPUTER ORGANIZATION**  
**HW-2 REPORT**



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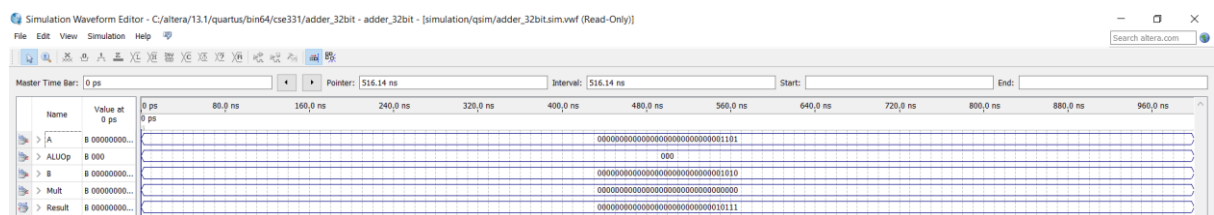
## PART 2 – ALU

### 1) 32-Bit Adder

- ⇒ Inputs: A [32], B [32], Carry\_In
- ⇒ Outputs: Sum[32], Carry\_Out, Carry\_Overflow

Inside the adder I used FA and HA just like on the lesson.

This is the test of the adder:

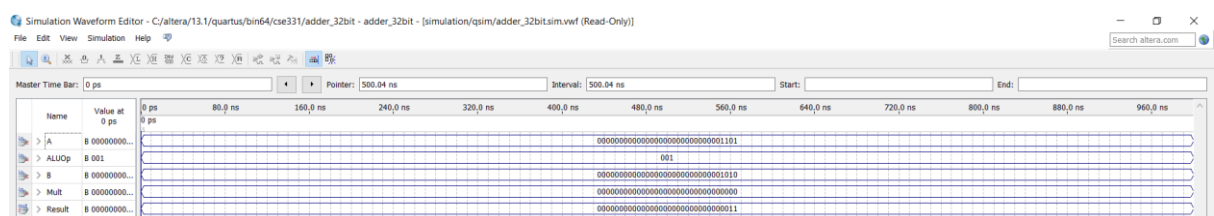


### 2) 32-Bit Subs

- ⇒ Inputs: A [32], B [32], Carry\_In
- ⇒ Outputs: Sum[32], Carry\_Out, Carry\_Overflow

I used the one adder for subs, add, slt so inputs are same of the alls.

This is the test of the subs:



### 3) 32-Bit Mult

- ⇒ I can not do this part.

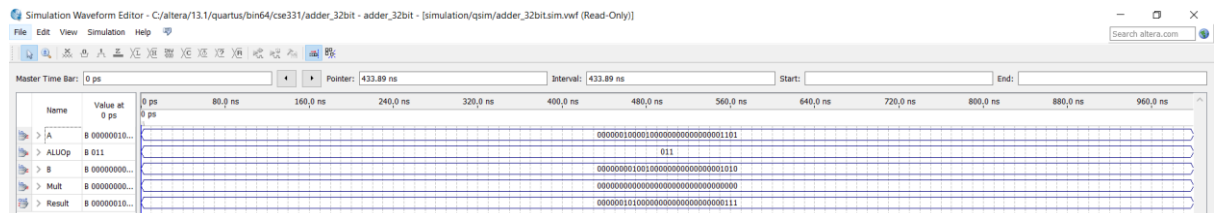
#### 4) 32-Bit XOR

⇒ Inputs: A [32], B [32]

⇒ Outputs: Out[32]

I XOR ed all bits one by one.

This is the test of the XOR :



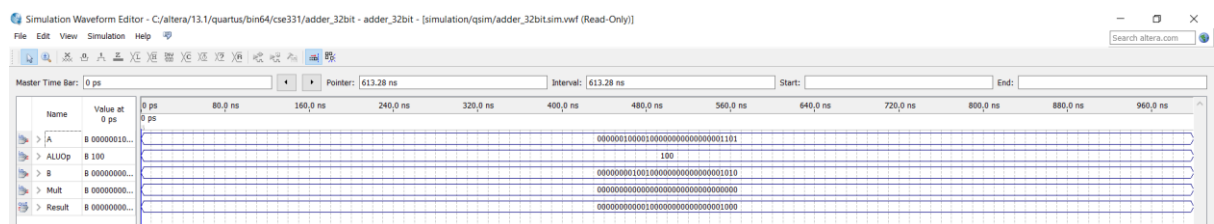
#### 5) 32-Bit AND

⇒ Inputs: A [32], B [32]

⇒ Outputs: Out[32]

I AND ed all bits one by one.

This is the test of the AND :



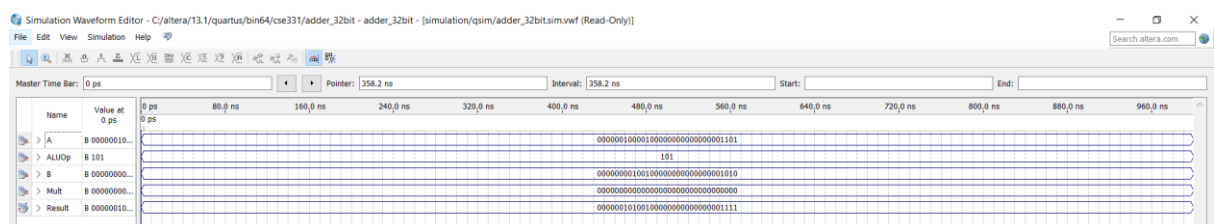
#### 6) 32-Bit OR

⇒ Inputs: A [32], B [32]

⇒ Outputs: Out[32]

I OR ed all bits one by one.

This is the test of the OR :



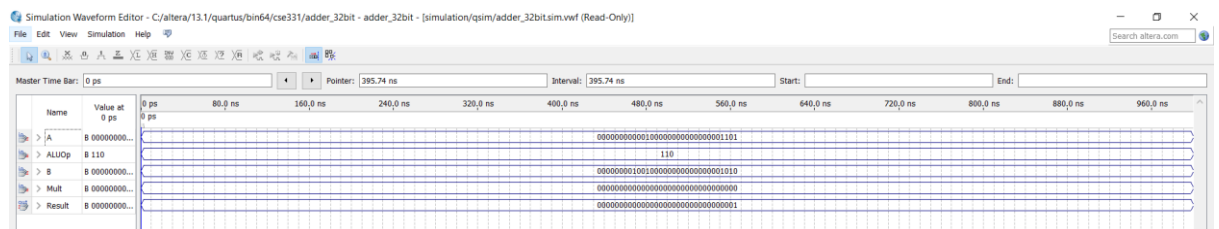
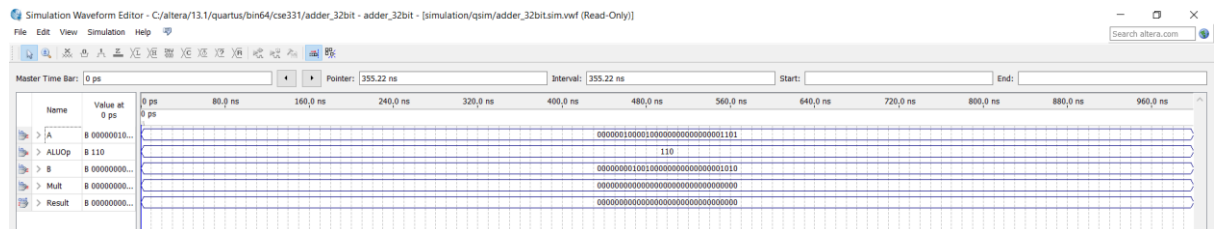
## 7) 32-Bit SLT

⇒ Inputs: A [32], B [32], Carry\_In

⇒ Outputs: Sum[32], Carry\_Out, Carry\_Overflow

I used the one adder for subs, add, slt so inputs are same of the alls.

This is the test of the SLT :



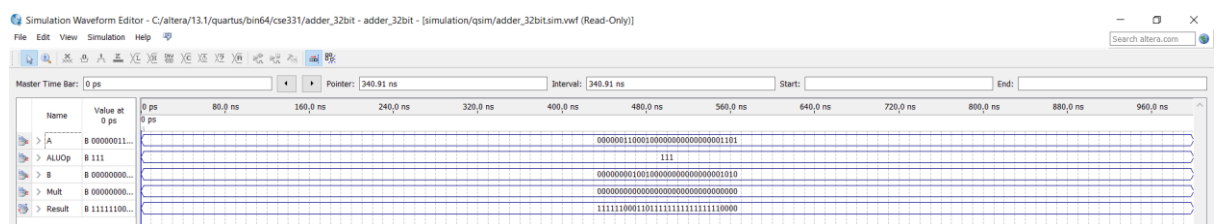
## 8) 32-Bit NOR

⇒ Inputs: A [32], B [32]

⇒ Outputs: Out[32]

I NOR ed all bits one by one.

This is the test of the NOR :



### 9) 32-Bit 8x1 MUX

- ⇒ Inputs: In0 [32], In1 [32] , In2 [32] , In3 [32] , In4 [32] , In5 [32] ,
- ⇒ In6 [32], In7 [32]
- ⇒ Outputs: Out[32]

I make 1-Bit 2x1 MUX for  $\Rightarrow \text{Sum} = (\text{In0} \& \sim S) + (\text{In1} \& S)$

Then I make 32-Bit 2x1 MUX for using 1-Bit 2x1 MUX 32 times.

Then I make 32-Bit 8x1 MUX for using 32-Bit 2x1 MUX 7 times.

## **PART 1 – MULT**

In here I try to make controller and datapath like PS's. I am not sure these are true or false. Because I can not do mult32.v file so I can not try to test cases.

But I am believe that my datapath and controller are true. And of course I do the adder.v for ALU and in according to my design mult, add, sub and slt is working same adder.

**NOTE:** I created the testbench for each .v file but I can not use because I can not understand how these are using. So I try to enter values my hand one by one and then I screenshot each of them.