Beulah Works LLC

Software Verification & Validation Plan (SVVP) Version 1.0

UML Sequence Diagram File Generator

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Approvals:

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Revision History

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1 Purpose

The purpose of this Software Verification and Validation Plan (SVVP) is to establish the requirements for the Verification and Validation (V&V) process to be applied to the UML Sequence Diagram File Generator software developed for Beulah Works LLC. This SVVP defines when, how, and by whom specific V&V activities are to performed, and description of the various V&V methodologies used. This SVVP is prepared in accordance with the guidelines described in IEEE Standard for Software Verification and Validation.

1.1 Scope

The Software Verification and Validation Plan (SVVP) is produced for and limited to Beulah Works LLC. The SVVP is produced using the IEEE Standard for Software Verification and Validation Plans as a model. Software V&V employs, review, analysis, and testing techniques to determine whether a software product and its intermediate deliverables comply with requirements. These requirements include both business functional capabilities and quality attributes.

1.2 Objectives

The objectives of the V&V effort are to find defects and to determine if required functions and attributes are built into the software system. V&V activities are designed to support:

1. Verification that the products of each software life cycle phase:
    a. Satisfy the standards, policies, practices, procedures, and conventions of the phase.
    b. Establish the proper basis for initiating the next life cycle phase.

2. Validate that the completed end product complies with established software and system requirements.

2 Referenced Documents

- Software Configuration Management Plan
- Software Project Management Plan

3 Definitions

- Verification: confirms that work products properly reflect the requirements specified for them. In other words, verification ensures that we are building the right product.
- Validation: confirms that the product, as provided, will fulfill its intended use. In other words, validation ensures that we built the right thing.

SVVP	Software Verification/Validation Plan
IEEE	Institute of Electrical and Electronics Engineers
V&V	Verification & Validation
SRS	Software Requirements Specifications
FR	Functional Requirement
IDE	Integrated Development Environment
UML	Unified Modeling Language

4 V&V OVERVIEW

4.1 Organization

The verification and validation of the application known as "UML Sequence Diagram File Generator" is coordinated with each phase of every iteration. The entire team will review and validate each artifact related to the project after it is generated and nearing finalization.

4.2 Master Schedule

The verification and validation schedule is described as a part of the project of the project schedule in the Software Project Management Plan for the application known as "UML Sequence Diagram File Generator".

4.3 Resource Summary

Both Verification and Validation will be performed Internally by the development team.

4.4 Software Integrity Level Scheme

The "UML Sequence Diagram File Generator" application is required to have moderate integrity.

4.5 Responsibilities

The development team members will

- Perform verification activities throughout the project, including inspections within all phases
- Perform and document all unit testing in JUnit
- Validate requirements documents with the customer

The QA engineer will:

- Verify that the team has followed its documented procedures, including those described in this document
- Perform all post-unit testing
- Report the results to the team and management
- Maintain the document

4.6 Tools, Techniques, and Methodologies

- This section intentionally left blank.

5 Life Cycle V&V

5.1 Management of V&V

The V&V effort on UML Sequence Diagram File Generator (internal) will be supervised by the manager of Quality Assurance.

5.2 Acquisition V&V

The external tools that are required to be used to develop UML Sequence Diagram File Generator are validated externally by Beulah Works LLC.

5.3 Development V&V

5.3.1 Concept V&V

Conceptual work on the UML Sequence Diagram File Generator concept will be verified by answering the following questions.

- Are all critical marketing factors identified?
- Does any concept imply a significant risk to protect completion? If so, should that concept be mitigated?

5.3.2 Requirements V&V

The UML Sequence Diagram File Generator SRS will be verified by answering the following questions:

- Are all critical requirements that were identified during the concept phase specified?
- Is the SRS organized In a way that facilitates traceability?
- Does the SRS account for all required interfaces with other systems?
- Does any requirement imply a significant risk to project completion? If so, should that requirement be mitigated?

5.3.3 Design V&V

- Are all requirements accommodated by the design?

5.3.4 Implementation V&V

The Implementation of UML Sequence Diagram File Generator will be verified by answering the following questions:

- Are all requirements fully verified?
- Is the code organized in a way that facilitates traceability back to design and requirements?
- Is all code documented according to standards?
- Is all code thoroughly documented?

5.3.5 Test V&V

The test documentatIon of UML Sequence Diagram File Generator will be verified by answering the following verification questions, and the validation questions that follow:

- Are all critical requirements intended to be fully tested at every level of detail (e.g., human safety)?
- Is the test philosophy adequate for the requirements?
- Are the test plans complete as specified in the test philosophy?
- Are the test cases complete as specified in the test philosophy?

5.4 Operation V&V

- This section intentionally left blank.

5.5 Maintenance V&V

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6 Reporting Requirements

6.1 Reporting

The QA person attached to the project reports the status of V&V weekly to the manager of QA and copies the team leader.

6.2 Administrative

The project leader is responsible for ensuring that all V&V reporting is performed.

6.3 Documentation

A single report that includes all versions of the results of the tasks described in this document is maintained.

7 V&V Administrative Requirements

7.1 Anomaly Reporting and Discussion

The QA engineer attached to the UML Sequence Diagram File Generator project will maintain the current state and the history of each defect found. The QA engineer will maintain all metrics identified in the SQAP on a Web site and will e·mail a list of all anomalies (including defects) that he or she deem to have excessive repair timelines. This includes defects with no repair duration estimates and those that have exceeded their planned completion date.

7.2 Task Iteration Policy

V&V tasks will be repeated at the discretIon of the QA representative, but these will include the following criteria.

- An inspection whose defects count is more than 20 percent greater than the norm
- A test whose defects count iS more than 20 percent greater than the norm.
- An entire phase if the previous phase change by more than 20 percent.

7.3 Deviation Policy

Any proposal to deviate from this plan requires the approval 01 the QA manager and the project manager.

7.4 Standards, Practices, and Conventions

This project will use Google's coding style standards.

8 V&V Documentation Requirements

Documents shall be written in Times New Roman with 11 font except for subheaders/headers. Everything should be single spaced except for breaks in between sections.