EEE 120

Lab 1 Answer Sheet

Half Adder, Full Adder, 4-bit Incrementer and Adder

Name: Fauzan Amaan Mohammed Instructor/Time: Josh Hihath (Tus & Thurs 3:00 – 4:15)

Date: Tuesday, 11th February 2024 .

**Task 1-1: Build and Test the 1-Bit Half-Adder**

Include a picture of your circuit in Digital here:

A black background with blue lines and red dots

AI-generated content may be incorrect.

Please comment on the single biggest issue you were facing when designing the circuit.

No Issues

Include a picture of your waveform (timing diagram) here:

A screenshot of a computer

AI-generated content may be incorrect.

Did the circuit behave as expected? If no, what was wrong?

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues

**Task 1-2: Build and Test a 4-Bit Increment Circuit**

Include a picture of your circuit in Digital here:

A computer screen shot of a diagram

AI-generated content may be incorrect.

Please comment on the single biggest issue you were facing when designing the circuit.

Include a picture of your waveform (timing diagram) here:

A screenshot of a computer

AI-generated content may be incorrect.

Did the circuit behave as expected? If no, what was wrong?

The circuit behave as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues

**Task 1-3: Build and Test a 1-bit Full Adder**

Include a picture of your circuit in Digital here:

A blue lines on a black background

AI-generated content may be incorrect.

Please comment on the single biggest issue you were facing when designing the circuit.

Laying out the wires.

Include a picture of your waveform (timing diagram) here:

A screenshot of a computer

AI-generated content may be incorrect.

Did the circuit behave as expected? If no, what was wrong?

1. The circuit behaved as expected where the sum and carry out works as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues

**Task 1-4: Build and Test a 4-Bit Full Adder**

Include a picture of your circuit in Digital here:

A computer screen shot of a computer

AI-generated content may be incorrect.

Please comment on the single biggest issue you were facing when designing the circuit.

The multiple wires used and gets confusing where each wire starts and ends.

Include a picture of your waveform (timing diagram) here:

A screenshot of a computer

AI-generated content may be incorrect.

Which tests did you perform and why? Use the following table to describe your test sequence. You need to make sure to perform a sufficient number of tests to check the circuit for eventual faults. Each row of the first column corresponds to a row of stimulus from your four\_bit\_adder\_stim.txt file. Note that you only need to use as many tests as needed. Extra space is provided for enthusiastic students.

| **Test stimulus** | **Test motivation** | **Pass/Fail** |
| --- | --- | --- |
| 0\_0\_0\_0\_0 | Check for stuck-at-1 faults (this makes sure none of the wires were accidentally connected to power) | Pass |
| 0\_2\_0\_1\_1 | Basic addition: 1 + 1 + 0 = 2 | Pass |
| 0\_5\_0\_2\_3 | Basic addition: 2 + 3 + 0 = 5 | Pass |
| 0\_9\_0\_4\_5 | Basic addition: 4 + 5 + 0 = 9 | Pass |
| 0\_F\_0\_7\_8 | Signed overflow test: 7 + 8 = 15 (boundary case for two’s complement) | Pass |
| 1\_E\_0\_F\_F | Unsigned overflow test: 15 + 15 = 30 (carry-out should be set) | Pass |
| 0\_3\_1\_1\_1 | Carry-in test: 1 + 1 + 1 = 3 (ensures carry-in works correctly) | Pass |
| 0\_8\_1\_3\_4 | Carry-in test: 3 + 4 + 1 = 8 | Pass |
| 0\_6\_1\_2\_3 | Carry-in test: 2 + 3 + 1 = 6 | Pass |
| 0\_A\_1\_5\_4 | Carry-in test: 5 + 4 + 1 = 10 | Pass |
| 1\_0\_1\_8\_7 | Unsigned overflow: 8 + 7 + 1 = 16 (carry-out should be set) | Pass |
| 1\_F\_1\_F\_F | Maximum input test: 15 + 15 + 1 = 31 (ensures adder handles max values) | Pass |
| 0\_7\_0\_3\_4 | Basic addition: 3 + 4 + 0 = 7 | Pass |
| 0\_C\_1\_6\_5 | Carry-in test: 6 + 5 + 1 = 12 | Pass |
| 1\_1\_0\_9\_8 | Unsigned overflow test: 9 + 8 = 17 | Pass |
| 1\_2\_1\_A\_7 | Unsigned overflow test: 10 + 7 + 1 = 18 | Pass |

Please comment on the single biggest issue you were facing when simulating the circuit.

The terminal showed error in the test cases but the waveform didn’t which made me confused on whether my circuit was built incorrectly. I reconfirm by using start simulation and the waveform to test whether the test cases worked.

**Task 1-5: Create a video and submit your report.**

Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

**Video Link:** [**https://asu.zoom.us/rec/share/JCKfrnUT2vJyiO9F5owCb4PWMGIpUoNAEqCwDKUEW\_WZcMa9gVSP190OutVTvHf2.310BegGoJvyJeCVT?startTime=1739418607000**](https://asu.zoom.us/rec/share/JCKfrnUT2vJyiO9F5owCb4PWMGIpUoNAEqCwDKUEW_WZcMa9gVSP190OutVTvHf2.310BegGoJvyJeCVT?startTime=1739418607000)

**Passcode: KGW?35+G**

**At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.**

**Make sure all your files are in the Lab1 directory. Create a zip file of the Lab1 directory. Remember to turn in the zip file and your completed template on Canvas!**

**Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!**

Lab 1: Lab Report Grade Sheet

|  |  |
| --- | --- |
| **Name:** |  |

**NOTE: You submit the zip file in order to show your work.  
If the zip file is not submitted you will receive a 0 for this lab!**

## Instructor Assessment

| **Grading Criteria** | **Max Points** | **Points Lost** |
| --- | --- | --- |
| **Description of Assigned Tasks, Work Performed & Outcomes Met** |  |  |
| Task 1-1: Build and Test a 1-Bit Half-Adder | 10 |  |
| Task 1-2: Build and Test a 4-Bit Increment Circuit | 10 |  |
| Task 1-3: Build and Test a 1-Bit Full Adder | 10 |  |
| Task 1-4: Build and Test a 4-Bit Full Adder | 10 |  |
| Task 1-5: Create a video and submit your report. | 10 |  |
|  | **Points Lost** |  |
| Lab Score (50 points total) | **Late Lab** |  |
|  | **Lab Score** |  |