Johns Hopkins University

Whiting School of Engineering

525.642 FPGA Design Using VHDL

Laboratory No. 4

VGA Checkerboard Display

Student: Fawei Zhang

Major: Computer Engineering

Date: 02/27/2023

Resources	Used
Registers as Flip Flop	205
Register as Latches	0
Clock Buffers	1
Number of IOs	36

Table 1: Device Utilization Comparison Between Estimate Used and Actual Used

Summary: In the table 1 shown above, there's only one clock buffer required since we only use the one 100MHz clock input on board and used to with clock divider to generate the 25MHz pixel clock for the VGA monitor. For the number of FPGA IOs used, we can count there's one clock input port, one reset slider switch, four push button: up, down, left, right, eight seven-segment display cathode and anode pins, pins for VGA are VGA_HS, VGA_VS, 4 bits of VGA_R, VGA_G, VGA_B which used a total of 36 (1+1+4+8+8+1+1+4+4+4) GPIO pins and it's matched the actual used.

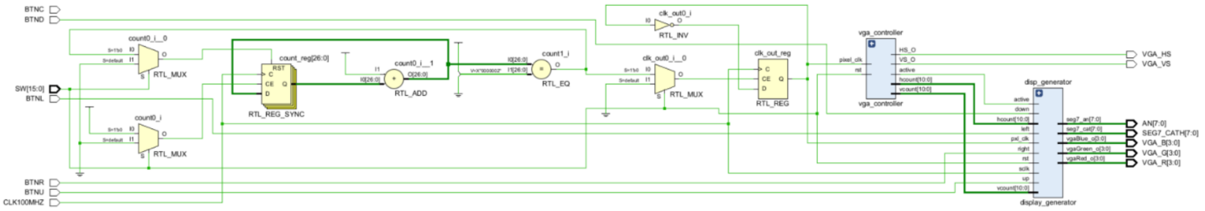
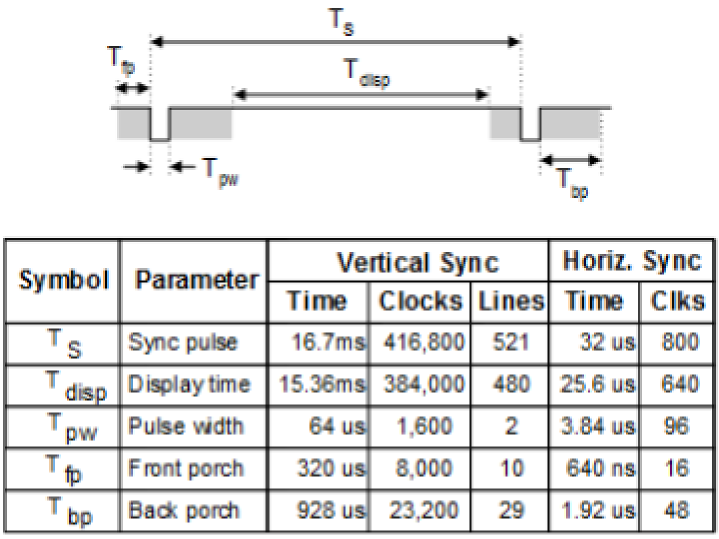


Figure 1: Lab 4 RTL schematic

For this project, we will be displaying video data at 60 Hz refresh rate, meaning 60 frames per second. It will be using an active area of 640 by 480 which means 640 columns and 480 rows in the active area run by a 25MHz pixel clock from the on-board 100MHz system clock. There are a total of 800 columns horizontal sync pulse and 521 vertical sync pulse, this is total of 800*521 = 416,800 pixels. So, to draw one pixel per clock cycle, it will take 416,800 / 25,000,000 = 0.0167 second = 16.7ms to draw an entire frame which match the reference rate of 1/60Hz = 16.7ms per frame. Due to the way how CRT display work, there's Front Porch and Back Porch that will shift that active area around our VGA monitor, and we can think it as the modification to our HSync and VSync pulses timing signal as shown in Figure 8.1.3 (Figure 2 below) of the Board Reference Manual. In order to display different color via VGA, it will require an analog voltage that represents the color value driven on the VGA_Red, VGA_Blue and VGA_Green color inputs signals. Each color (Red, Green, Blue) has 4-bits in the Nexys 4 Board, which give us a total of 2^12 = 4096 possible colors. For example, for an analog voltage of 1.0 volts to represent full on for this particular color, if we make red to 1.0 V, blue to 0 V and green to 0 V which sets RGB outputs to be 1111, 0000 and 0000, then the monitor will display a full red image, this is the processing of digital to analog output voltage that is drive by a resistor divider.



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 2: Signal Timing for a 60 x 480 display using a 25MHz pixel clock and 60Hz vertical refresh.

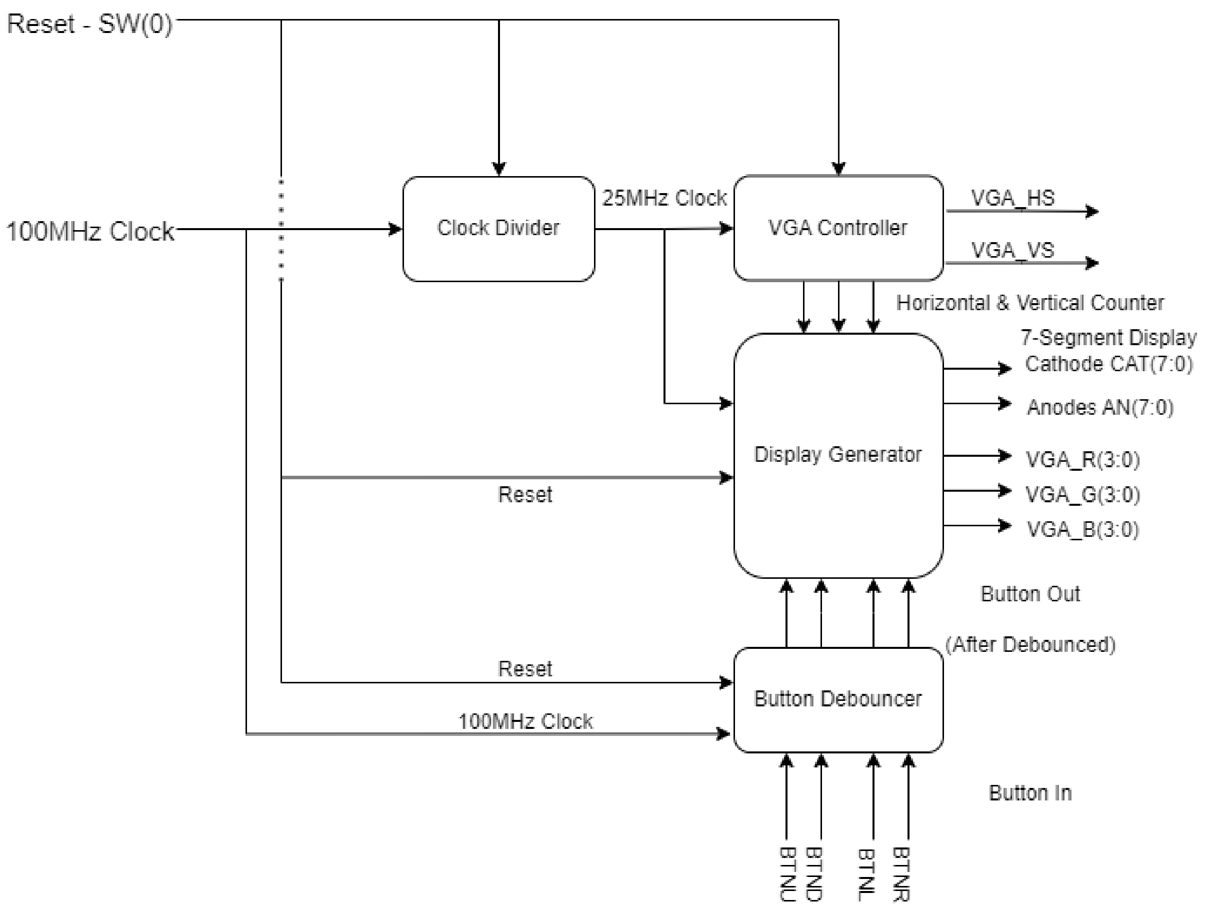


Figure 3: Lab 4 Top Level Block Diagram

The figure 3 showing above is the overall block diagram where it generate 25MHz pixel clock require to drive VGA monitor from the on-board 100MHz system clock then VGA Controller decodes the output of the horizontal-sync counter to locate any pixel location on a given row and vertical-sync counter to locate any pixel location on a given column by this pixel clock to generate the HS and VS signal timings. Then it out put these horizontal and vertical counters to the display generator to display the checkboard patterns by 15 rows and 20 columns that occupying the total visible area of 640x480 pixels where each square has the size of 32x32 pixels with blue and green checked pattern color along the entire screen. There's also a button denouncer to eliminate the push button bouncing to counter that increments as long as the press button, if the counter is excess the certain limit, then we acknowledge button pressed. After that we can used this de-bouncer button to move the red square that we generated in the checkboard pattern to move it in any directions according to the which button is been pressed. Finally, we can use the coordinates of the X and Y axis of the red box square and display its location on the 7-segement display as shown in the Figure 4 of this lab report that showing the VGA controller and display generator logic block diagram.

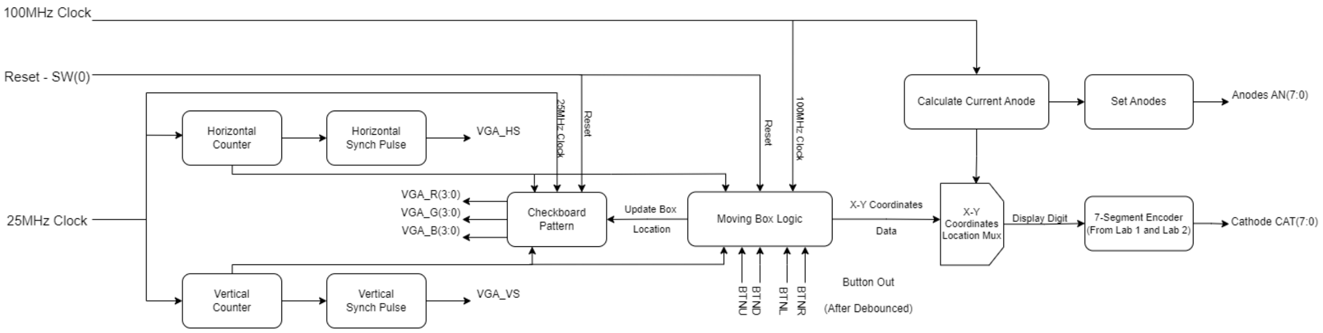


Figure 4: Lab 4 VGA controller and Display Logic Block Diagram