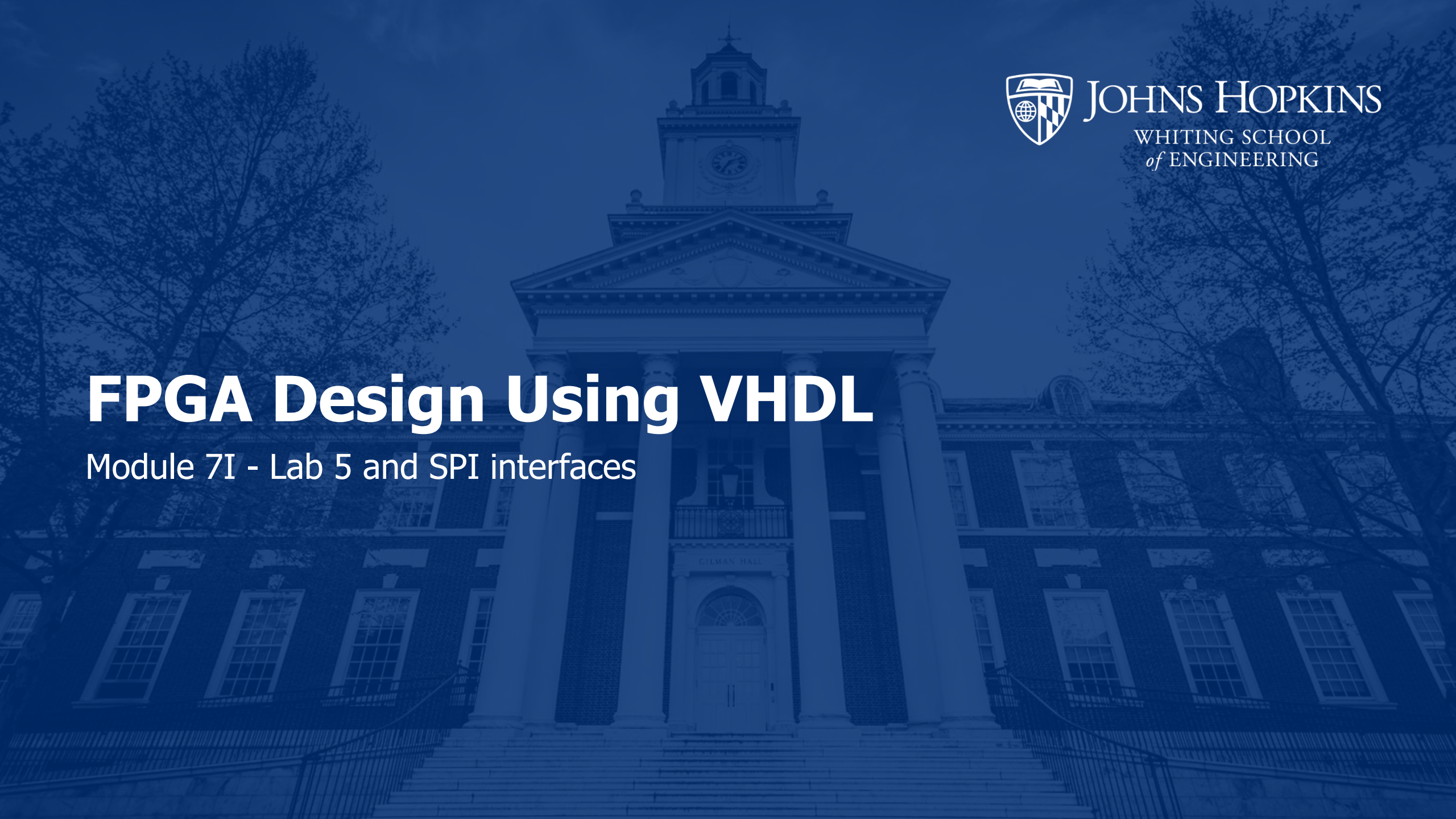

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FPGA Design Using VHDL

Module 7I - Lab 5 and SPI interfaces

Lab 5 Overview

- Builds upon Lab 4 by adding an SPI interface to accelerometer for control
- Main requirement is working with SPI component and reading the associated datasheet
- SPI device:
  - Analog Devices ADXL362

SPI Interfaces

- SPI is Serial Peripheral Interface
  - Synchronous serial communication with master driven SCLK
  - Common as interface between ICs
  - Master/Slave Architecture with MOSI and MISO signals for sending and receiving data
  - Slave Select or Chip Select for enabling remote device

SPI Interface with ADXL362

- Supports SCLK speeds of 1MHz to 8 MHz, I recommend starting with 1 MHz
- Only need CSb, MOSI, MISO, and SCLK signals
- Register map is shown in ADXL datasheet on page 23

Table 11. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	DEVID_AD	[7:0]	DEVID_AD[7:0]								0xAD	R
0x01	DEVID_MST	[7:0]	DEVID_MST[7:0]								0x1D	R
0x02	PARTID	[7:0]	PARTID[7:0]								0xF2	R
0x03	REVID	[7:0]	REVID[7:0]								0x01	R
0x08	XDATA	[7:0]	XDATA[7:0]								0x00	R
0x09	YDATA	[7:0]	YDATA[7:0]								0x00	R
0x0A	ZDATA	[7:0]	ZDATA[7:0]								0x00	R

ADXL362 Read Operation

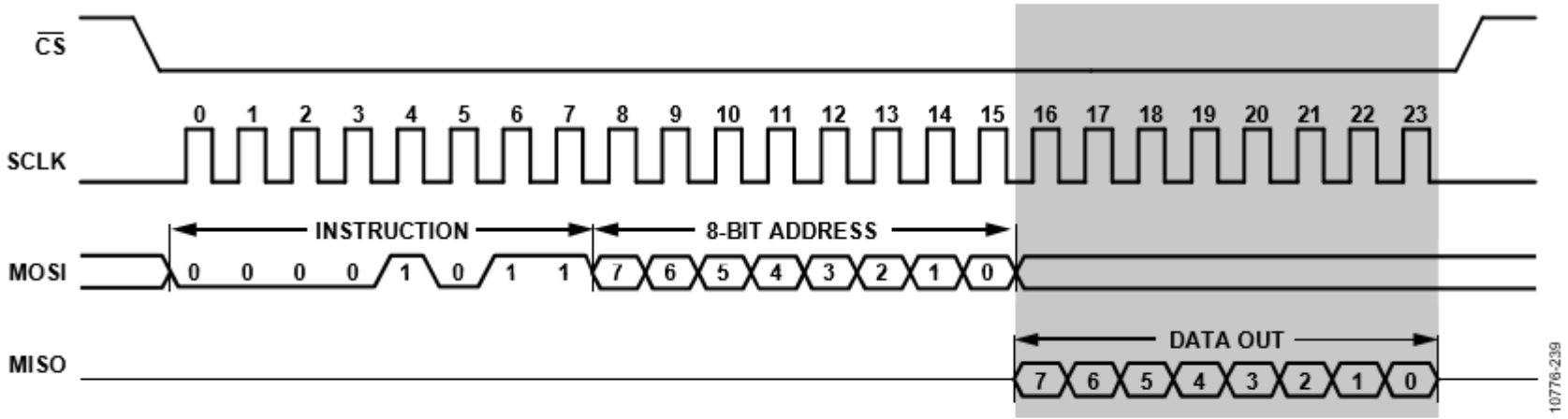

Figure 36. Register Read

ADXL362 Write Operation

- ADXL362

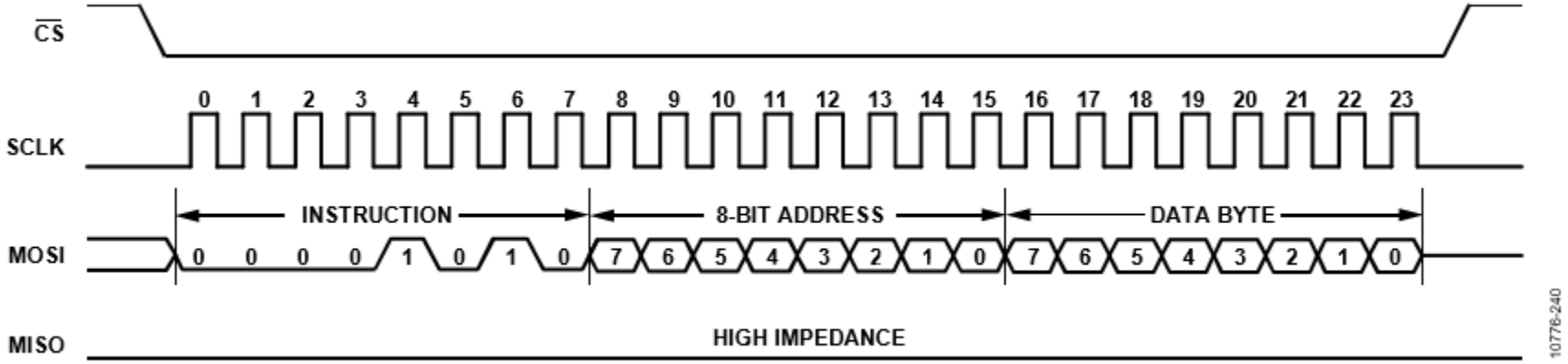

Figure 37. Register Write (Receive Instruction Only)