VC709 EVALUATION PLATFORM HW-V7-VC709

(XC7VX690T-FFG1761)

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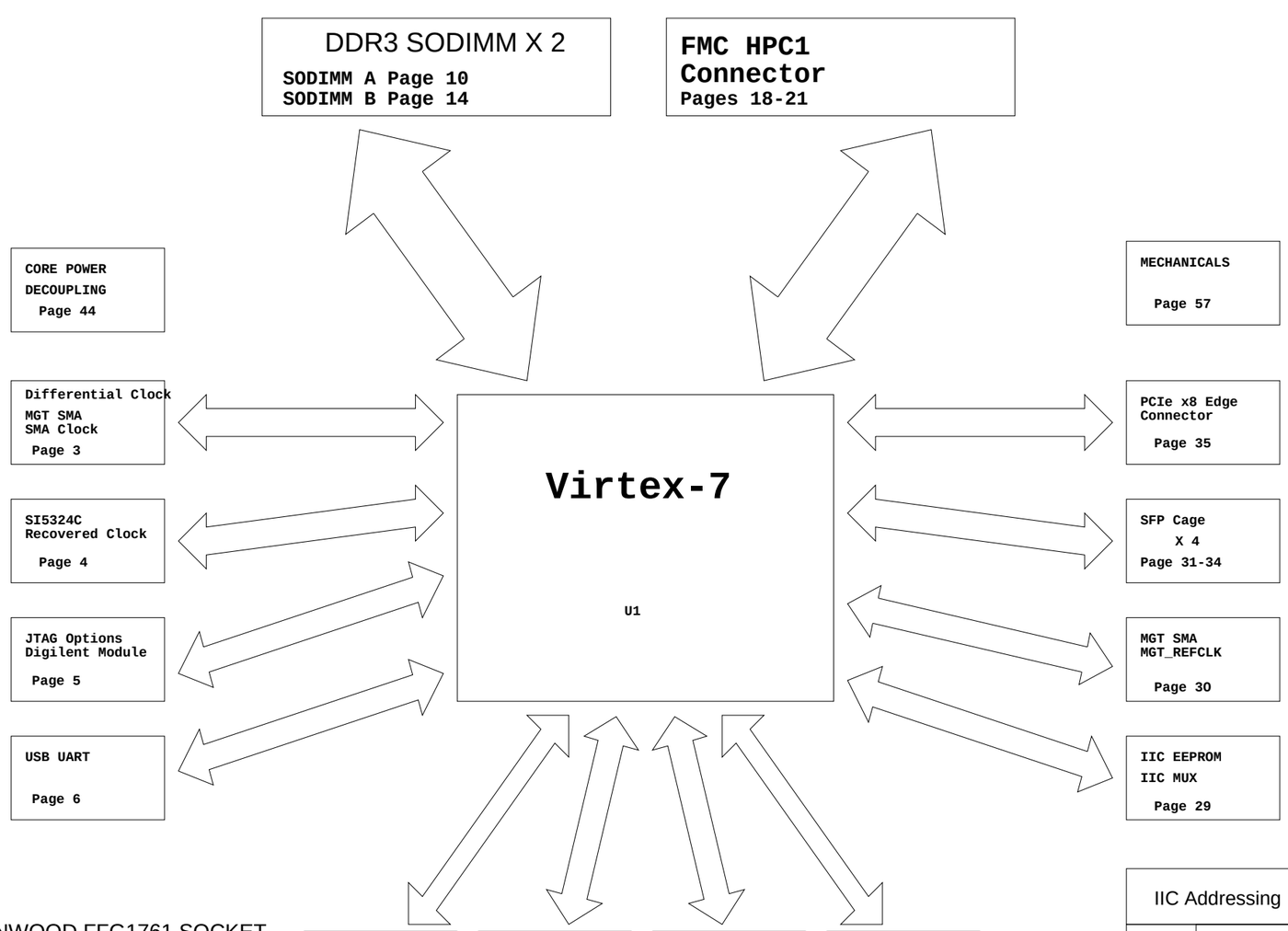
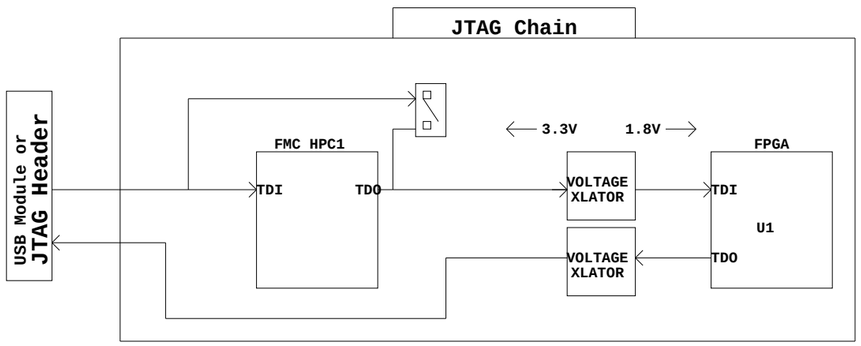
SCH P/N: 0381499

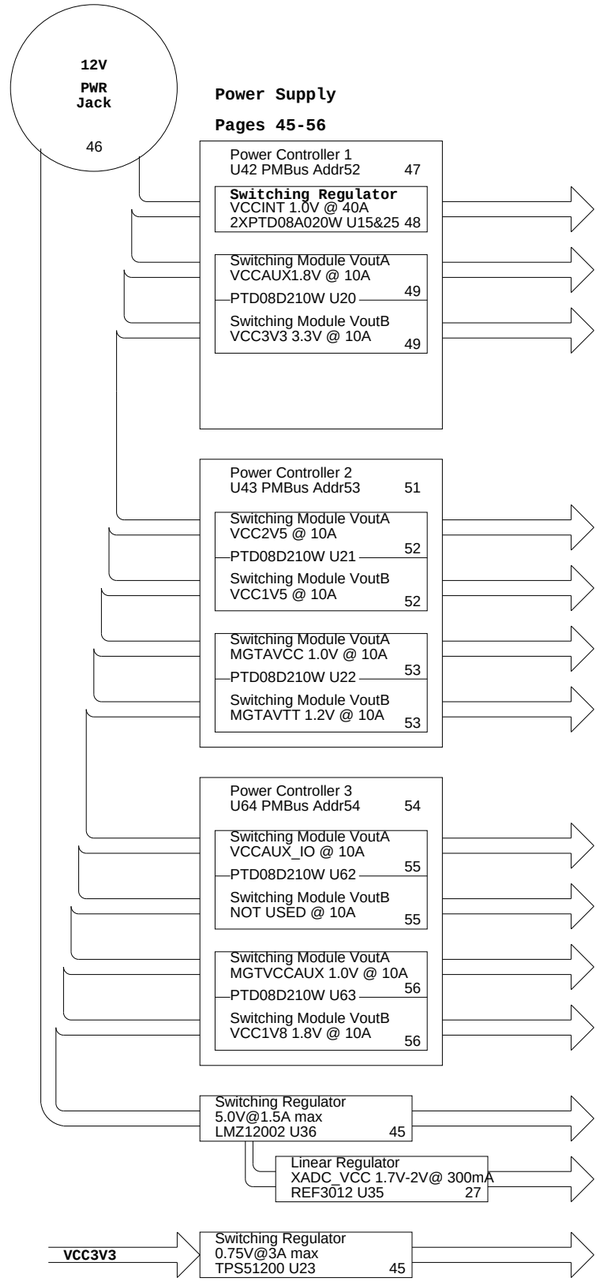
Title:	DISCLAIMER SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	1 of 57	Drawn By	DN



IRONWOOD FFG1761 SOCKET
SUPPORTS MULTIPLE DEVICES
REFER TO BOARD BILL OF
MATERIALS ON XILINX.COM
TO CONFIRM FPGA PROVIDED



IIC Addressing	
0b1110100	PCA9548A
0b1011101	SI570
0bxxxxx00	FMC HPC
0b1010100	IIC EEPROM
0b1110101	PCA9546A
0b1010000	SFP+ (4X)
0b1010001 0b0011001	DDR3 SODIMM J1
0b1010010 0b0011010	DDR3 SODIMM J3
0b1101000	SI5324



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Title: vc709_rev1.0 Block Diagram
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	9-19-2012_15:39	Ver:	1.0
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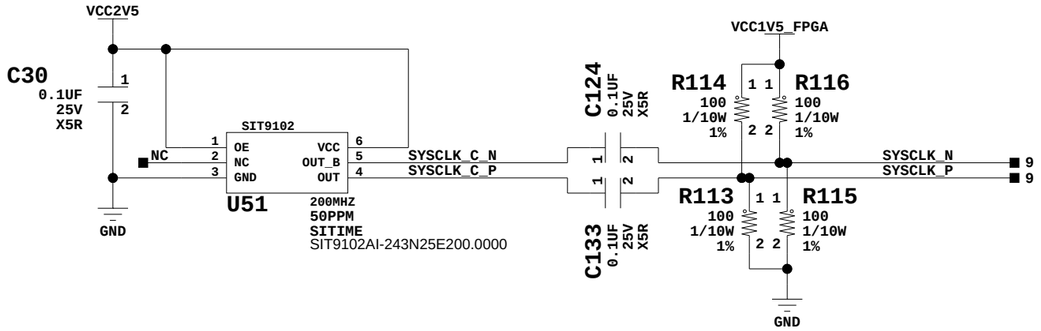

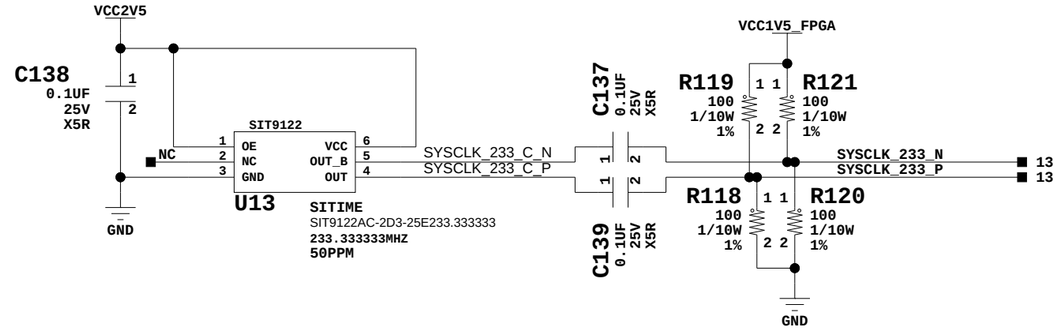

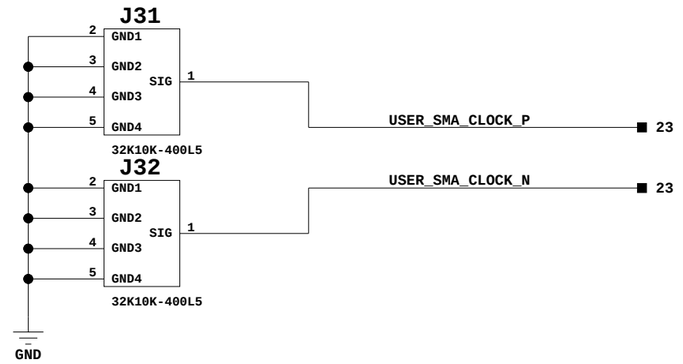

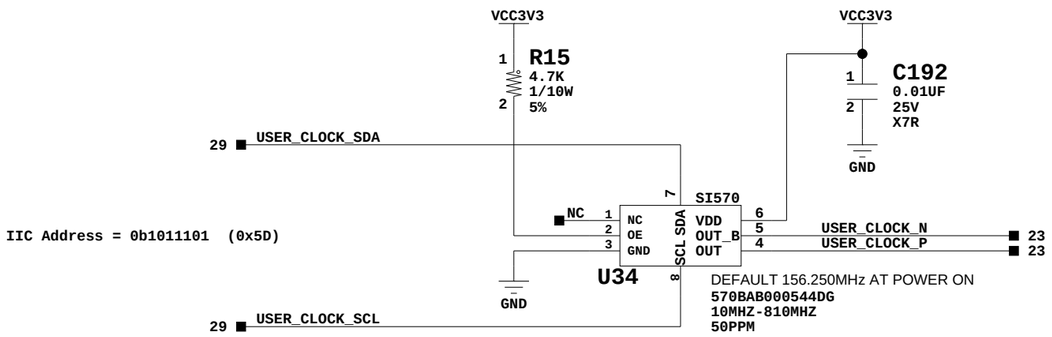

Clocks and SMA Connectors

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SCH P/N: 0381499

Title:	Clocks and SMA Connectors SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
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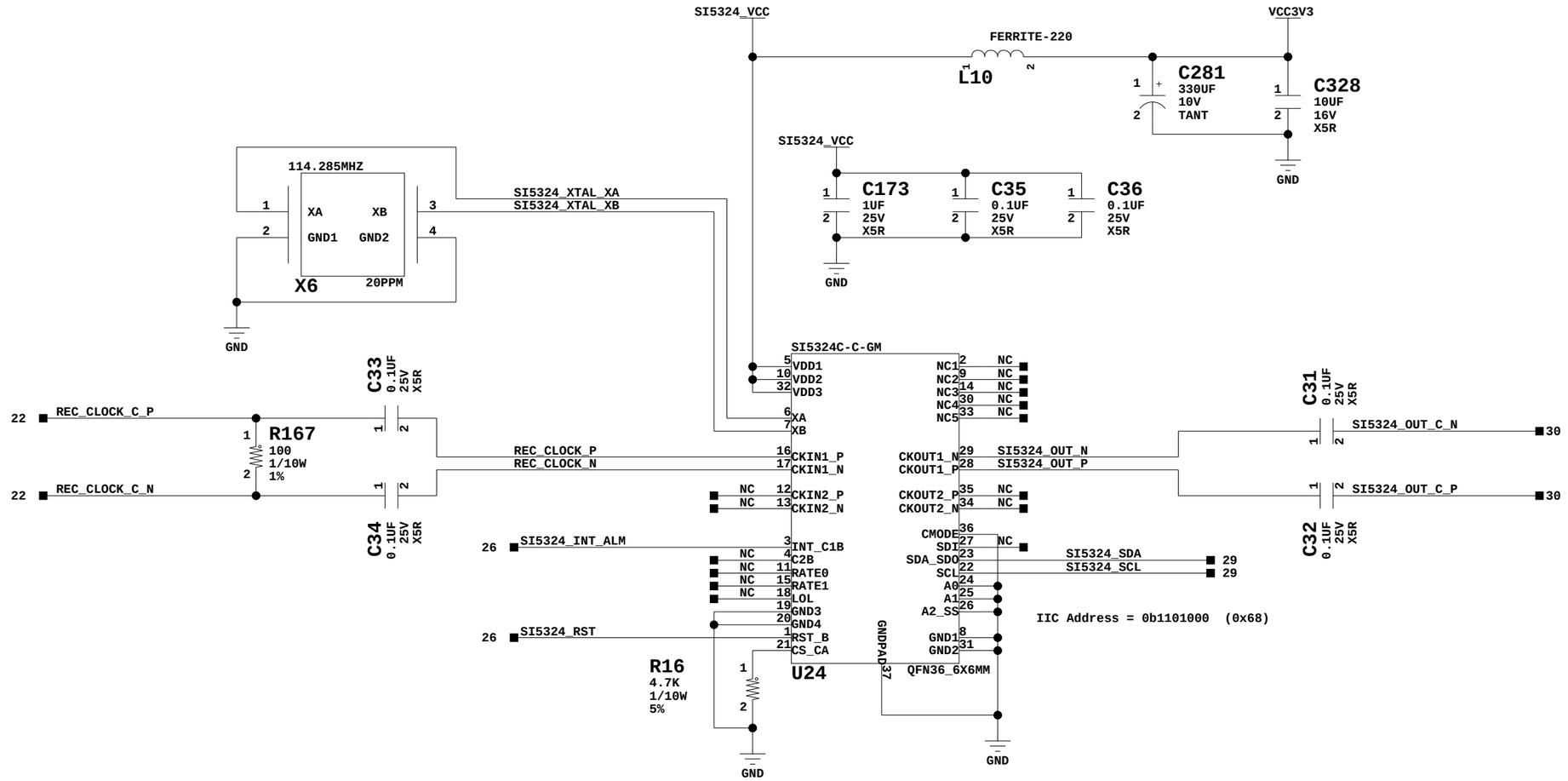

5324 Clock Recovery

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PCB P/N: 1280666
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Title:	5324 Clock Recovery SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-6-2012_11:50	Ver:	1.0
Sheet Size: B		Rev:	01
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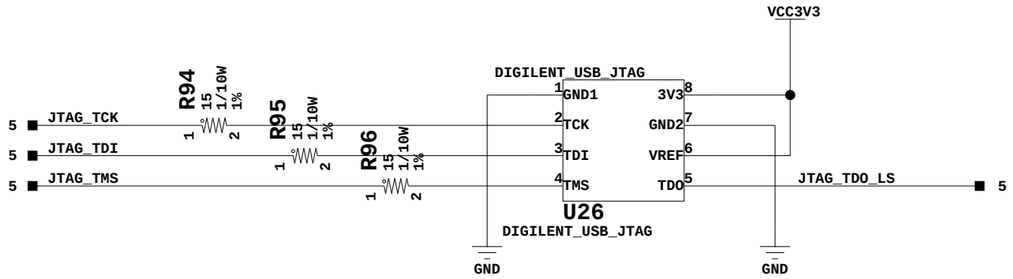

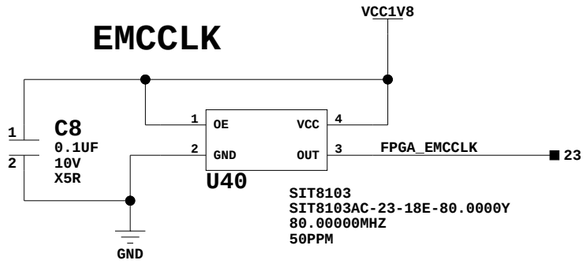

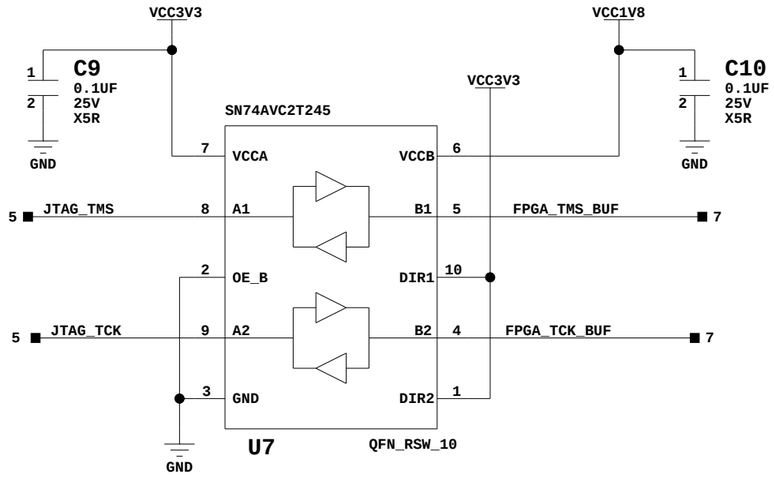

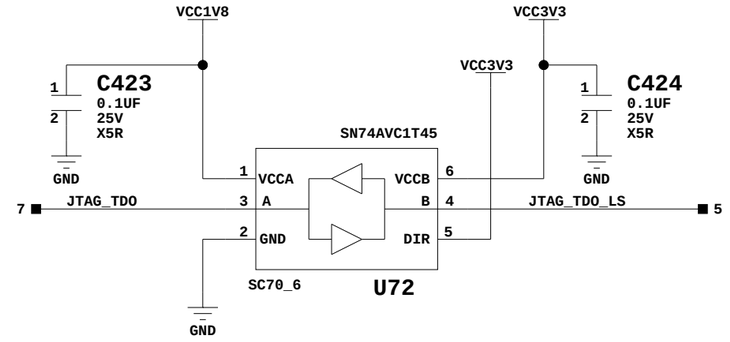

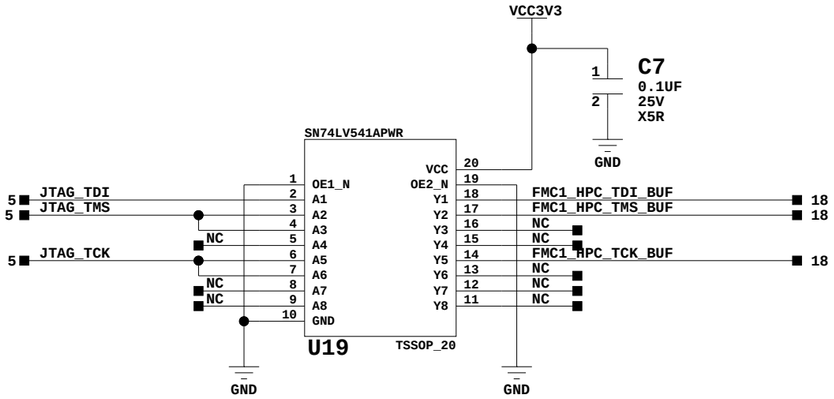

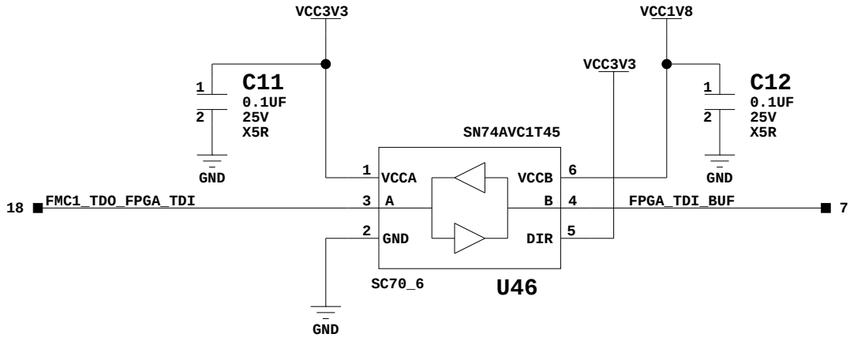

JTAG Buffer, USB JTAG Module, JTAG Hdr

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	JTAG Buffer, USB JTAG Module, JTAG Hdr SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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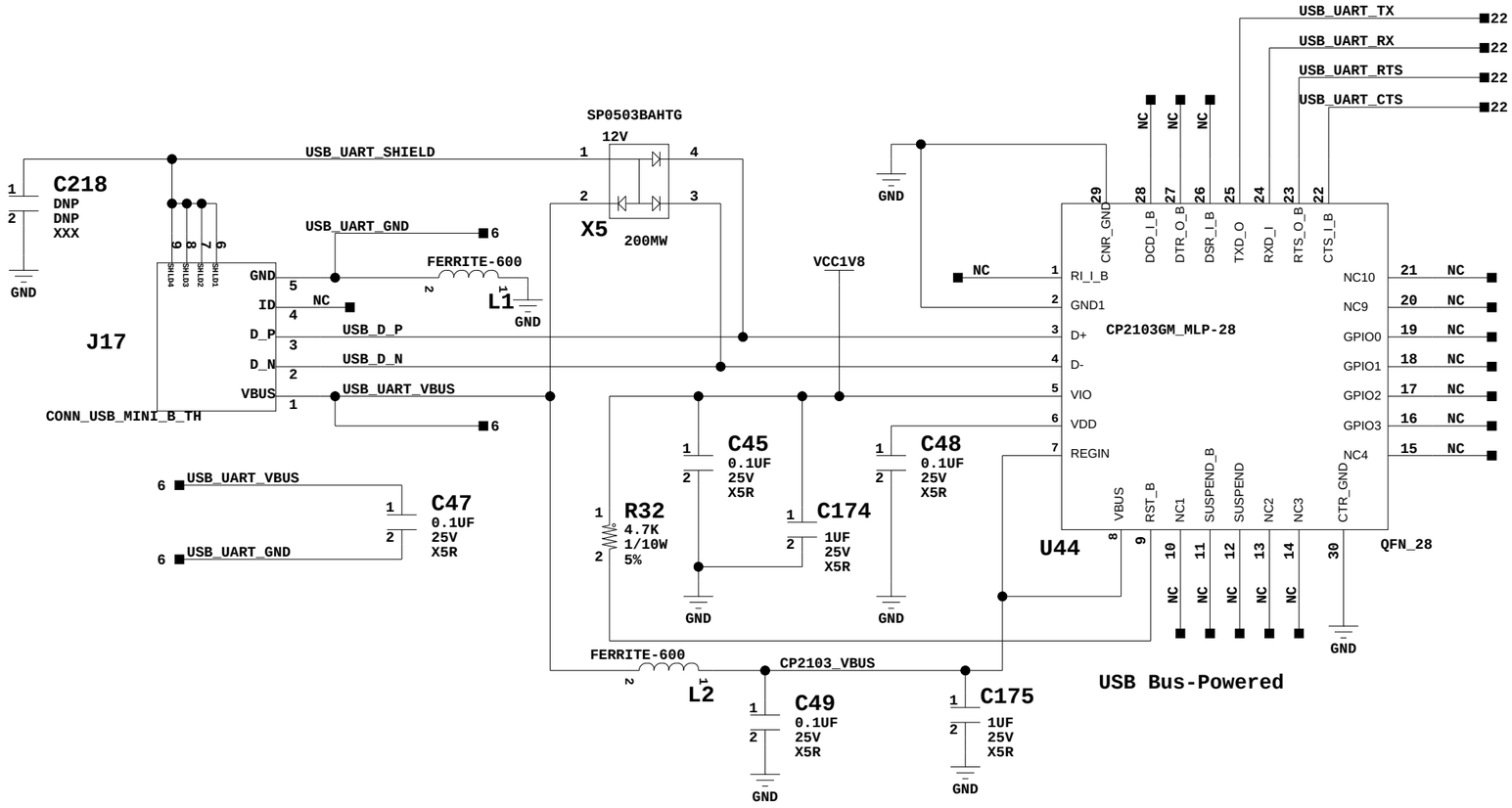

USB UART

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Title:	USB UART, EEPROM, Config DIPs SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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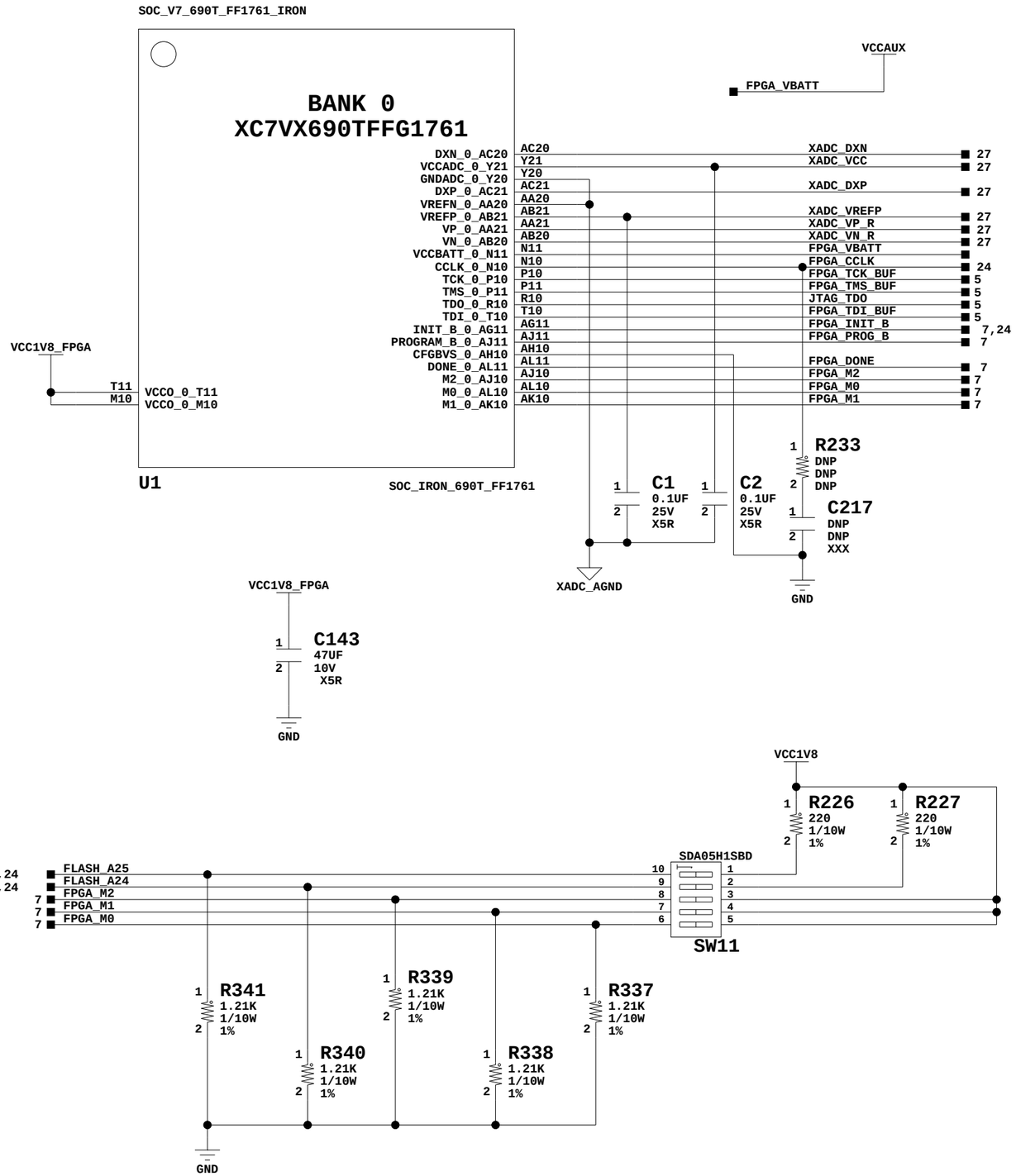

FPGA Banks 0

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ASSY P/N: 0431748
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Title:	FPGA Banks 0,13 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-21-2012_12:08	Ver:	1.0
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SOC_V7_690T_FF1761_IRON

BANK 39
XC7VX690TFFG1761

VTTVREF

C463 0.1UF 25V X5R (1, 2) — C492 0.1UF 25V X5R (1, 2)

GND

IO_0_VRN_39_J16	J16	VRN_39	8
IO_L1P_T0_39_C16	C16	DDR3_A_D30	10
IO_L1N_T0_39_B16	B16	DDR3_A_D26	10
IO_L2P_T0_39_B14	B14	DDR3_A_D24	10
IO_L2N_T0_39_A14	A14	DDR3_A_DM3	10
IO_L3P_T0_DQS_39_C15	C15	DDR3_A_DQS3_P	10
IO_L3N_T0_DQS_39_C14	C14	DDR3_A_DQS3_N	10
IO_L4P_T0_39_D13	D13	DDR3_A_D28	10
IO_L4N_T0_39_C13	C13	DDR3_A_D25	10
IO_L5P_T0_39_D16	D16	DDR3_A_D31	10
IO_L5N_T0_39_D15	D15	DDR3_A_D27	10
IO_L6P_T0_39_E12	E12	DDR3_A_D29	10
IO_L6N_T0_VREF_39_D12	D12		
IO_L7P_T1_39_F16	F16	NC	
IO_L7N_T1_39_E15	E15	DDR3_A_D16	10
IO_L8P_T1_39_E14	E14	DDR3_A_D19	10
IO_L8N_T1_39_E13	E13	DDR3_A_D17	10
IO_L9P_T1_DQS_39_H16	H16	DDR3_A_DQS2_P	10
IO_L9N_T1_DQS_39_G16	G16	DDR3_A_DQS2_N	10
IO_L10P_T1_39_G12	G12	DDR3_A_D21	10
IO_L10N_T1_39_F12	F12	DDR3_A_DM2	10
IO_L11P_T1_SRCC_39_F15	F15	DDR3_A_D18	10
IO_L11N_T1_SRCC_39_F14	F14	DDR3_A_D22	10
IO_L12P_T1_MRCC_39_G14	G14	DDR3_A_D23	10
IO_L12N_T1_MRCC_39_G13	G13	DDR3_A_D20	10
IO_L13P_T2_MRCC_39_H15	H15	NC	
IO_L13N_T2_MRCC_39_H14	H14	DDR3_A_D14	10
IO_L14P_T2_SRCC_39_J13	J13	DDR3_A_D11	10
IO_L14N_T2_SRCC_39_H13	H13	DDR3_A_D10	10
IO_L15P_T2_DQS_39_K12	K12	DDR3_A_DQS1_P	10
IO_L15N_T2_DQS_39_J12	J12	DDR3_A_DQS1_N	10
IO_L16P_T2_39_K15	K15	DDR3_A_DM1	10
IO_L16N_T2_39_J15	J15	DDR3_A_D15	10
IO_L17P_T2_39_K14	K14	DDR3_A_D8	10
IO_L17N_T2_39_K13	K13	DDR3_A_D9	10
IO_L18P_T2_39_L16	L16	DDR3_A_D12	10
IO_L18N_T2_39_L15	L15	DDR3_A_D13	10
IO_L19P_T3_39_L12	L12	DDR3_A_D7	10
IO_L19N_T3_VREF_39_L11	L11		
IO_L20P_T3_39_M14	M14	DDR3_A_D3	10
IO_L20N_T3_39_L14	L14	DDR3_A_D2	10
IO_L21P_T3_DQS_39_N16	N16	DDR3_A_DQS0_P	10
IO_L21N_T3_DQS_39_M16	M16	DDR3_A_DQS0_N	10
IO_L22P_T3_39_N13	N13	DDR3_A_D1	10
IO_L22N_T3_39_M13	M13	DDR3_A_DM0	10
IO_L23P_T3_39_N15	N15	DDR3_A_D5	10
IO_L23N_T3_39_N14	N14	DDR3_A_D0	10
IO_L24P_T3_39_M12	M12	DDR3_A_D4	10
IO_L24N_T3_39_M11	M11	DDR3_A_D6	10
IO_25_VRP_39_J11	J11	VRP_39	8

VCC1V5_FPGA

D14	VCCO_39_D14
G15	VCCO_39_G15
H12	VCCO_39_H12
K16	VCCO_39_K16
L13	VCCO_39_L13
P14	VCCO_39_P14

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 37
XC7VX690TFFG1761

VTTVREF

C461 0.1UF 25V X5R (1, 2) — C490 0.1UF 25V X5R (1, 2)

GND

IO_0_VRN_37_F21	F21	VRN_37	8
IO_L1P_T0_37_A24	A24	DDR3_A_D32	10
IO_L1N_T0_37_A25	A25	DDR3_A_D38	10
IO_L2P_T0_37_B22	B22	DDR3_A_D37	10
IO_L2N_T0_37_A22	A22	DDR3_A_D36	10
IO_L3P_T0_DQS_37_A26	A26	DDR3_A_DQS4_P	10
IO_L3N_T0_DQS_37_A27	A27	DDR3_A_DQS4_N	10
IO_L4P_T0_37_C23	C23	DDR3_A_DM4	10
IO_L4N_T0_37_B23	B23	DDR3_A_D33	10
IO_L5P_T0_37_B26	B26	DDR3_A_D35	10
IO_L5N_T0_37_B27	B27	DDR3_A_D34	10
IO_L6P_T0_37_C24	C24	DDR3_A_D39	10
IO_L6N_T0_VREF_37_B24	B24		
IO_L7P_T1_37_E23	E23	DDR3_A_D44	10
IO_L7N_T1_37_E24	E24	DDR3_A_D40	10
IO_L8P_T1_37_F22	F22	DDR3_A_D46	10
IO_L8N_T1_37_E22	E22	DDR3_A_D47	10
IO_L9P_T1_DQS_37_F25	F25	DDR3_A_DQS5_P	10
IO_L9N_T1_DQS_37_E25	E25	DDR3_A_DQS5_N	10
IO_L10P_T1_37_D22	D22	DDR3_A_D45	10
IO_L10N_T1_37_D23	D23	DDR3_A_D41	10
IO_L11P_T1_SRCC_37_D25	D25	DDR3_A_DM5	10
IO_L11N_T1_SRCC_37_D26	D26	DDR3_A_D42	10
IO_L12P_T1_MRCC_37_C25	C25	DDR3_A_D43	10
IO_L12N_T1_MRCC_37_C26	C26	NC	
IO_L13P_T2_MRCC_37_D27	D27	DDR3_A_D49	10
IO_L13N_T2_MRCC_37_D28	D28	DDR3_A_D52	10
IO_L14P_T2_SRCC_37_C28	C28	DDR3_A_D51	10
IO_L14N_T2_SRCC_37_C29	C29	NC	
IO_L15P_T2_DQS_37_B28	B28	DDR3_A_DQS6_P	10
IO_L15N_T2_DQS_37_B29	B29	DDR3_A_DQS6_N	10
IO_L16P_T2_37_A31	A31	DDR3_A_D54	10
IO_L16N_T2_37_A32	A32	DDR3_A_D55	10
IO_L17P_T2_37_A29	A29	DDR3_A_D50	10
IO_L17N_T2_37_A30	A30	DDR3_A_D48	10
IO_L18P_T2_37_C31	C31	DDR3_A_DM6	10
IO_L18N_T2_37_B31	B31	DDR3_A_D53	10
IO_L19P_T3_37_E30	E30	DDR3_A_D56	10
IO_L19N_T3_VREF_37_D31	D31		
IO_L20P_T3_37_D30	D30	DDR3_A_D63	10
IO_L20N_T3_37_C30	C30	DDR3_A_D60	10
IO_L21P_T3_DQS_37_E27	E27	DDR3_A_DQS7_P	10
IO_L21N_T3_DQS_37_E28	E28	DDR3_A_DQS7_N	10
IO_L22P_T3_37_F29	F29	DDR3_A_D57	10
IO_L22N_T3_37_E29	E29	DDR3_A_D61	10
IO_L23P_T3_37_F26	F26	DDR3_A_D62	10
IO_L23N_T3_37_F27	F27	DDR3_A_D59	10
IO_L24P_T3_37_F30	F30	DDR3_A_D58	10
IO_L24N_T3_37_F31	F31	DDR3_A_DM7	10
IO_25_VRP_37_F24	F24	VRP_37	8

VCC1V5_FPGA

A23	VCCO_37_A23
B30	VCCO_37_B30
C27	VCCO_37_C27
D24	VCCO_37_D24
E21	VCCO_37_E21
F28	VCCO_37_F28

U1 SOC_IRON_690T_FF1761

VCC1V5_FPGA

C160 100UF 6.3 X5R (1, 2)

GND

VCC1V5_FPGA

R163 80.6 1/10W 1% (1, 2) — 8 VRN_39

R164 80.6 1/10W 1% (1, 2) — 8 VRP_39

GND

VCC1V5_FPGA

R160 80.6 1/10W 1% (1, 2) — 8 VRN_37

R159 80.6 1/10W 1% (1, 2) — 8 VRP_37

GND

VCC1V5_FPGA

C161 100UF 6.3 X5R (1, 2)

GND

FPGA Banks 39, 37

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ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA Banks 36, 37 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-21-2012_12:08	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 38
XC7VX690TFFG1761

IO_0_VRN_38_K18	K18	VRN_38	
IO_L1P_T0_38_C19	C19	DDR3_A_A9	9
IO_L1N_T0_38_B19	B19	DDR3_A_A1	10
IO_L2P_T0_38_A16	A16	DDR3_A_A5	10
IO_L2N_T0_38_A15	A15	DDR3_A_A12	10
IO_L3P_T0_DQS_38_A20	A20	DDR3_A_A0	10
IO_L3N_T0_DQS_38_A19	A19	DDR3_A_A3	10
IO_L4P_T0_38_B17	B17	DDR3_A_A11	10
IO_L4N_T0_38_A17	A17	DDR3_A_A4	10
IO_L5P_T0_38_B21	B21	DDR3_A_A10	10
IO_L5N_T0_38_A21	A21	DDR3_A_A13	10
IO_L6P_T0_38_C18	C18	DDR3_A_A7	10
IO_L6N_T0_VREF_38_B18	B18		
IO_L7P_T1_38_D20	D20	DDR3_A_A6	10
IO_L7N_T1_38_C20	C20	DDR3_A_A2	10
IO_L8P_T1_38_F17	F17	DDR3_A_A14	10
IO_L8N_T1_38_E17	E17	DDR3_A_A15	10
IO_L9P_T1_DQS_38_D21	D21	DDR3_A_BA0	10
IO_L9N_T1_DQS_38_C21	C21	DDR3_A_BA1	10
IO_L10P_T1_38_D18	D18	DDR3_A_BA2	10
IO_L10N_T1_38_D17	D17	DDR3_A_A8	10
IO_L11P_T1_SRCC_38_G19	G19	DDR3_A_CLK1_P	10
IO_L11N_T1_SRCC_38_F19	F19	DDR3_A_CLK1_N	10
IO_L12P_T1_MRCC_38_E19	E19	DDR3_A_CLK0_P	10
IO_L12N_T1_MRCC_38_E18	E18	DDR3_A_CLK0_N	10
IO_L13P_T2_MRCC_38_H19	H19	SYSCLK_P	3,9
IO_L13N_T2_MRCC_38_G18	G18	SYSCLK_N	3,9
IO_L14P_T2_SRCC_38_K19	K19	DDR3_A_CKE0	10
IO_L14N_T2_SRCC_38_J18	J18	DDR3_A_CKE1	10
IO_L15P_T2_DQS_38_F20	F20	DDR3_A_WE_B	10
IO_L15N_T2_DQS_38_E20	E20	DDR3_A_RAS_B	10
IO_L16P_T2_38_K17	K17	DDR3_A_CAS_B	10
IO_L16N_T2_38_J17	J17	DDR3_A_S0_B	10
IO_L17P_T2_38_J20	J20	DDR3_A_S1_B	10
IO_L17N_T2_38_H20	H20	DDR3_A_ODT0	10
IO_L18P_T2_38_H18	H18	DDR3_A_ODT1	10
IO_L18N_T2_38_G17	G17	DDR3_A_TEMP_EVENT_B	10
IO_L19P_T3_38_P18	P18	DDR3_A_RESET_B	10
IO_L19N_T3_VREF_38_P17	P17		
IO_L20P_T3_38_M17	M17	NC	
IO_L20N_T3_38_L17	L17	NC	
IO_L21P_T3_DQS_38_N19	N19	NC	
IO_L21N_T3_DQS_38_N18	N18	NC	
IO_L22P_T3_38_M19	M19	NC	
IO_L22N_T3_38_M18	M18	NC	
IO_L23P_T3_38_P20	P20	NC	
IO_L23N_T3_38_N20	N20	NC	
IO_L24P_T3_38_L20	L20	NC	
IO_L24N_T3_38_L19	L19	NC	
IO_25_VRP_38_K20	K20	VRP_38	9

VCC1V5_FPGA	B20	VCCO_38_B20
	C17	VCCO_38_C17
	F18	VCCO_38_F18
	J19	VCCO_38_J19
	M20	VCCO_38_M20
	N17	VCCO_38_N17

U1

SOC_IRON_690T_FF1761

VTTVREF

C462 (1, 2): 0.1UF, 25V, X5R — GND

C491 (1, 2): 0.1UF, 25V, X5R

3,9 SYSCLK_P — R2 (1, 2): DNP, 1/10W, 1% — 3,9 SYSCLK_N

VCC1V5_FPGA

C162 (1, 2): 100UF, 6.3, X5R — GND

VCC1V5_FPGA

R162 (1, 2): 80.6, 1/10W, 1% — 9 VRN_38

9 VRP_38 — R161 (1, 2): 80.6, 1/10W, 1% — GND

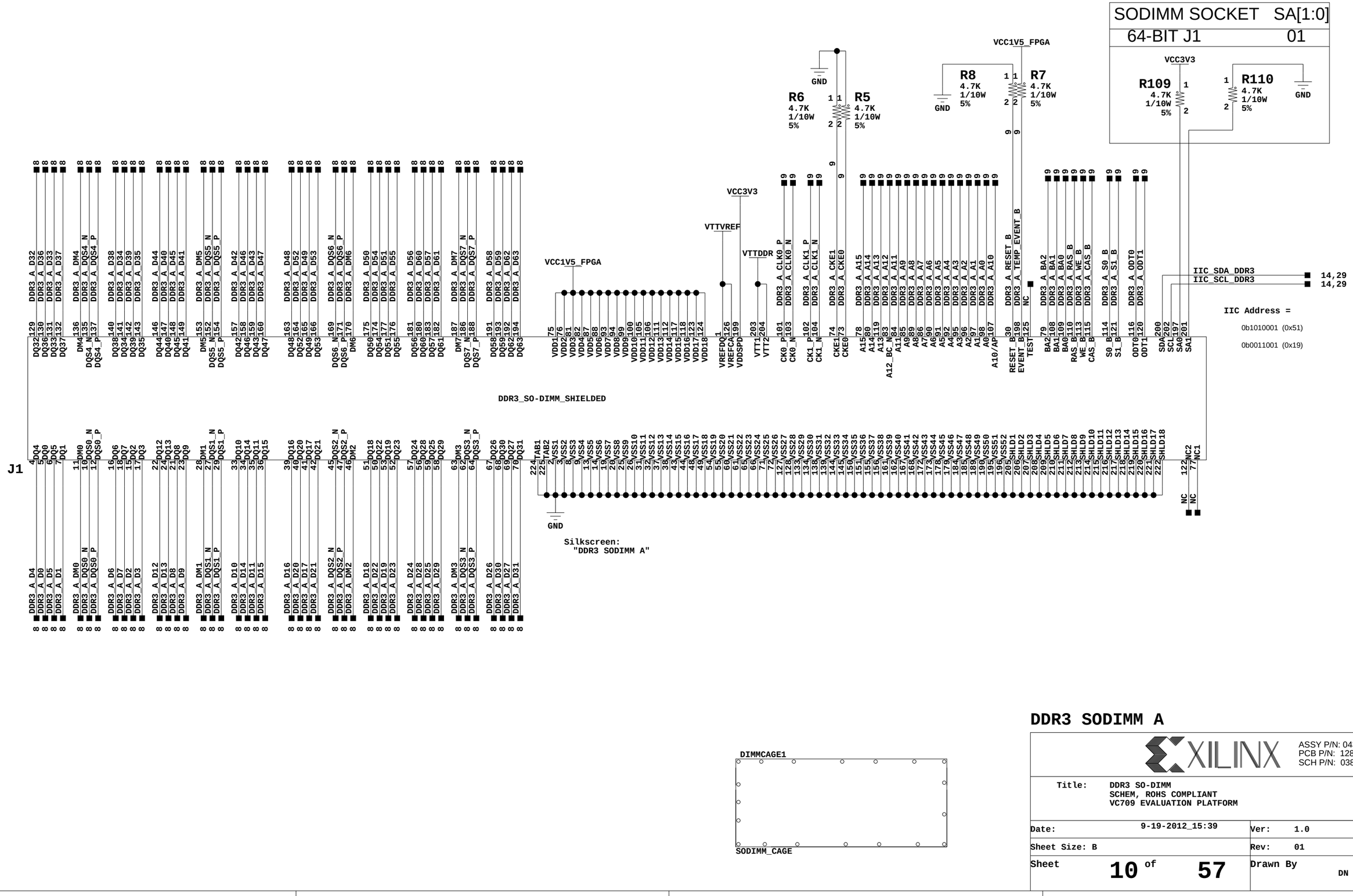
FPGA Banks 38

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Banks 38, 39
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_12:08	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	9 of 57	Drawn By	DN



DDR3 SODIMM A

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	DDR3 SO-DIMM SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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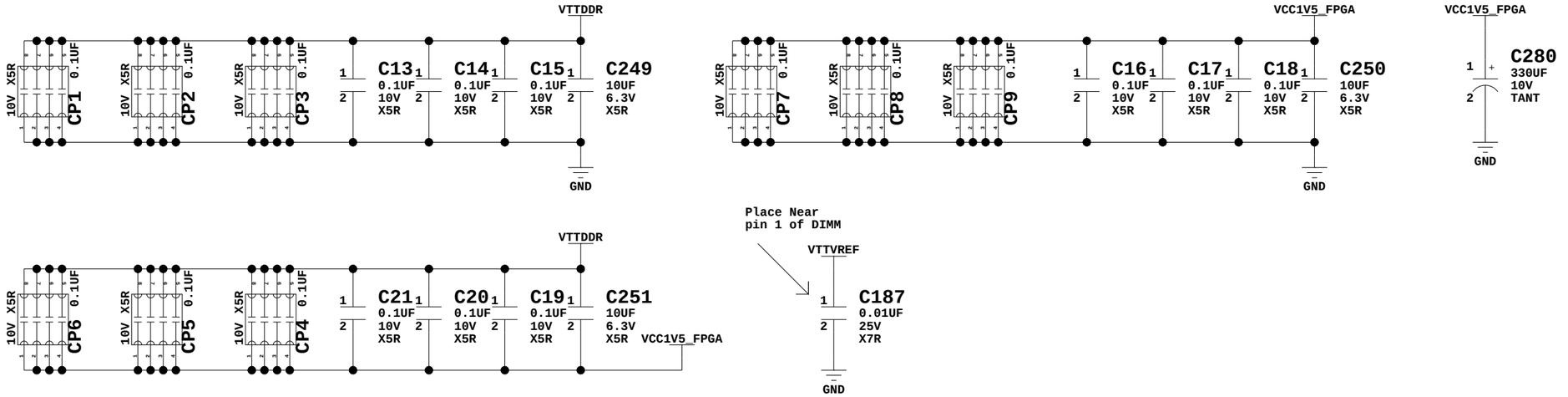

SODIMM A DECOUPLING

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	IIC MUX SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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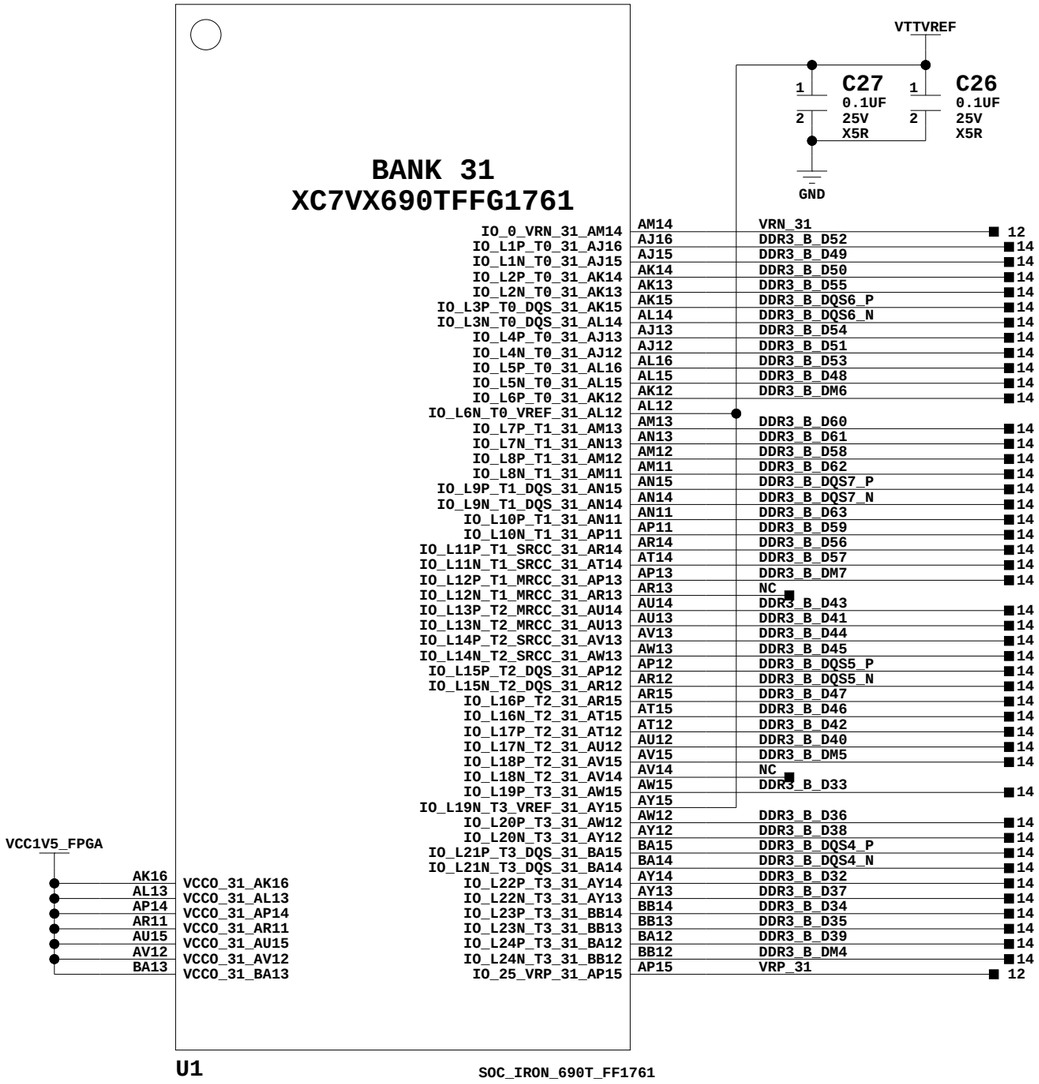
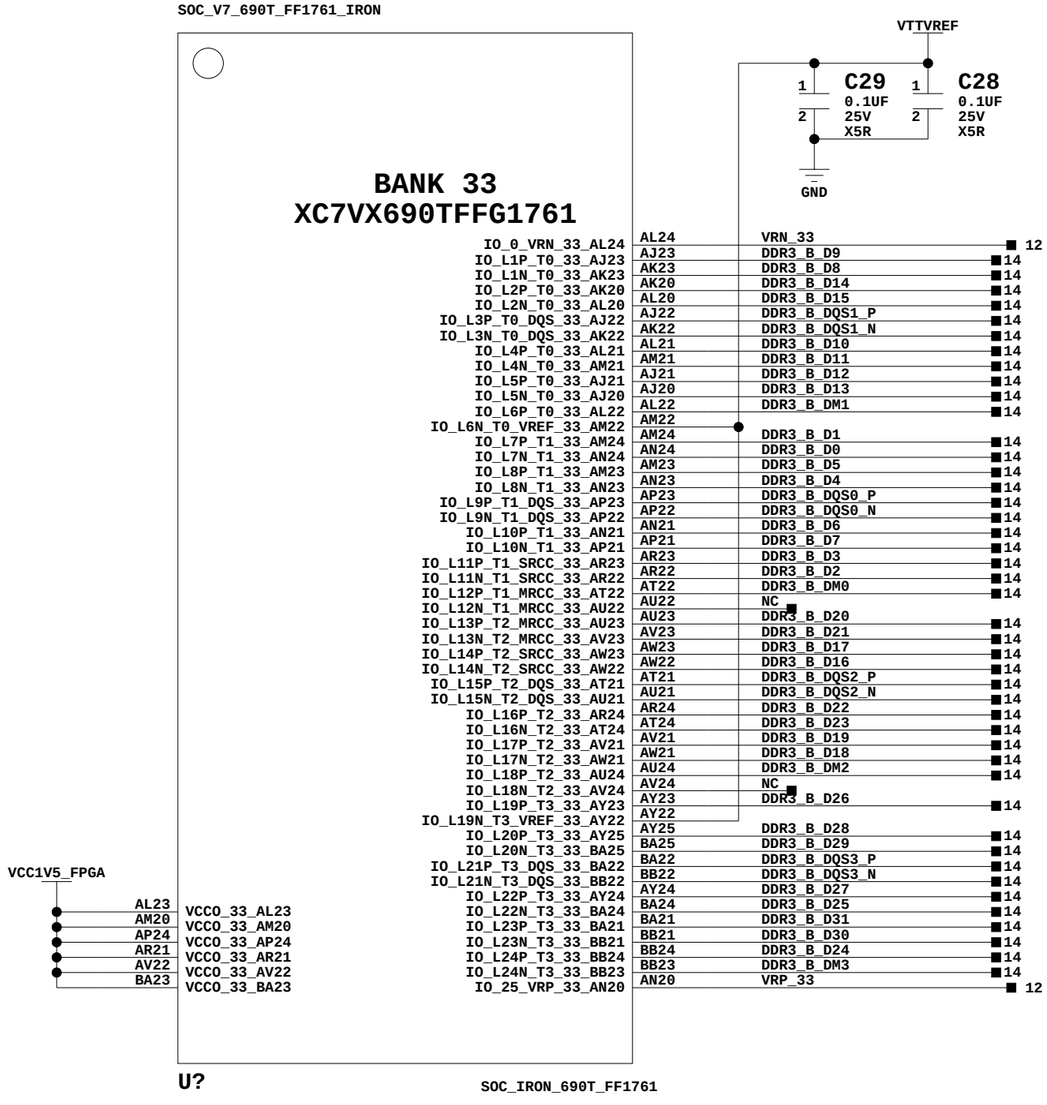
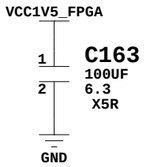
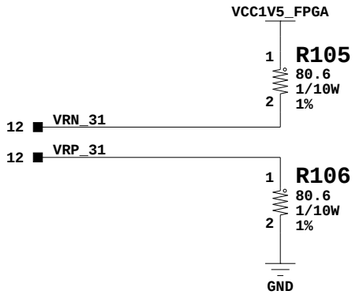
SOC_V7_690T_FF1761_IRON

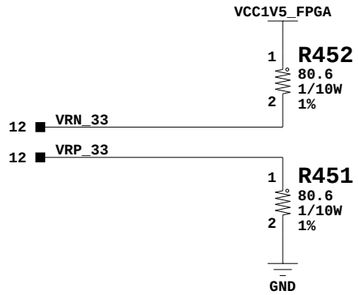


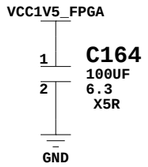
SOC_V7_690T_FF1761_IRON











FPGA BankS 31, 33

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Bank 33
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_12:08	Ver:	1.0
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SOC_V7_690T_FF1761_IRON

BANK 32
XC7VX690TFFG1761

IO_0_VRN_32_AR20	AR20	NC
IO_L1P_T0_32_AL19	AL19	DDR3_B_A15
IO_L1N_T0_32_AM19	AM19	DDR3_B_A14
IO_L2P_T0_32_AK17	AK17	DDR3_B_A13
IO_L2N_T0_32_AL17	AL17	DDR3_B_A12
IO_L3P_T0_DQS_32_AM18	AM18	DDR3_B_A11
IO_L3N_T0_DQS_32_AM17	AM17	DDR3_B_A10
IO_L4P_T0_32_AK19	AK19	DDR3_B_A9
IO_L4N_T0_32_AK18	AK18	DDR3_B_A8
IO_L5P_T0_32_AM16	AM16	DDR3_B_A7
IO_L5N_T0_32_AN16	AN16	DDR3_B_A6
IO_L6P_T0_32_AJ18	AJ18	DDR3_B_A5
IO_L6N_T0_VREF_32_AJ17	AJ17	
IO_L7P_T1_32_AP18	AP18	DDR3_B_A4
IO_L7N_T1_32_AP17	AP17	DDR3_B_A3
IO_L8P_T1_32_AP20	AP20	DDR3_B_A2
IO_L8N_T1_32_AR19	AR19	DDR3_B_A1
IO_L9P_T1_DQS_32_AN19	AN19	DDR3_B_A0
IO_L9N_T1_DQS_32_AN18	AN18	DDR3_B_BA2
IO_L10P_T1_32_AR18	AR18	DDR3_B_BA1
IO_L10N_T1_32_AR17	AR17	DDR3_B_BA0
IO_L11P_T1_SRCC_32_AU18	AU18	DDR3_B_CLK1_P
IO_L11N_T1_SRCC_32_AV18	AV18	DDR3_B_CLK1_N
IO_L12P_T1_MRCC_32_AT17	AT17	DDR3_B_CLK0_P
IO_L12N_T1_MRCC_32_AU17	AU17	DDR3_B_CLK0_N
IO_L13P_T2_MRCC_32_AY18	AY18	SYSCLK_233_P
IO_L13N_T2_MRCC_32_AY17	AY17	SYSCLK_233_N
IO_L14P_T2_SRCC_32_AW18	AW18	DDR3_B_CKE1
IO_L14N_T2_SRCC_32_AW17	AW17	DDR3_B_CKE0
IO_L15P_T2_DQS_32_AU19	AU19	DDR3_B_WE_B
IO_L15N_T2_DQS_32_AV19	AV19	DDR3_B_RAS_B
IO_L16P_T2_32_AT20	AT20	DDR3_B_CAS_B
IO_L16N_T2_32_AT19	AT19	DDR3_B_S1_B
IO_L17P_T2_32_AV16	AV16	DDR3_B_S0_B
IO_L17N_T2_32_AW16	AW16	DDR3_B_ODT1
IO_L18P_T2_32_AT16	AT16	DDR3_B_ODT0
IO_L18N_T2_32_AU16	AU16	DDR3_B_TEMP_EVENT_B
IO_L19P_T3_32_BB19	BB19	DDR3_B_RESET_B
IO_L19N_T3_VREF_32_BB18	BB18	
IO_L20P_T3_32_AV20	AV20	NC
IO_L20N_T3_32_AW20	AW20	NC
IO_L21P_T3_DQS_32_BA17	BA17	NC
IO_L21N_T3_DQS_32_BB17	BB17	NC
IO_L22P_T3_32_AY20	AY20	NC
IO_L22N_T3_32_BA20	BA20	NC
IO_L23P_T3_32_BA16	BA16	NC
IO_L23N_T3_32_BB16	BB16	NC
IO_L24P_T3_32_AY19	AY19	NC
IO_L24N_T3_32_BA19	BA19	NC
IO_25_VRP_32_AP16	AP16	NC

AJ19	VCCO_32_AJ19
AN17	VCCO_32_AN17
AT18	VCCO_32_AT18
AW19	VCCO_32_AW19
AY16	VCCO_32_AY16
BB20	VCCO_32_BB20

U1

SOC_IRON_690T_FF1761

VCC1V5_FPGA

VTTVREF

C53 0.1UF 25V X5R

C54 0.1UF 25V X5R

GND

3,13 SYSCLK_233_P

R43 DNP 1/10W 1%

3,13 SYSCLK_233_N

VCC1V5_FPGA

C165 100UF 6.3 X5R

GND

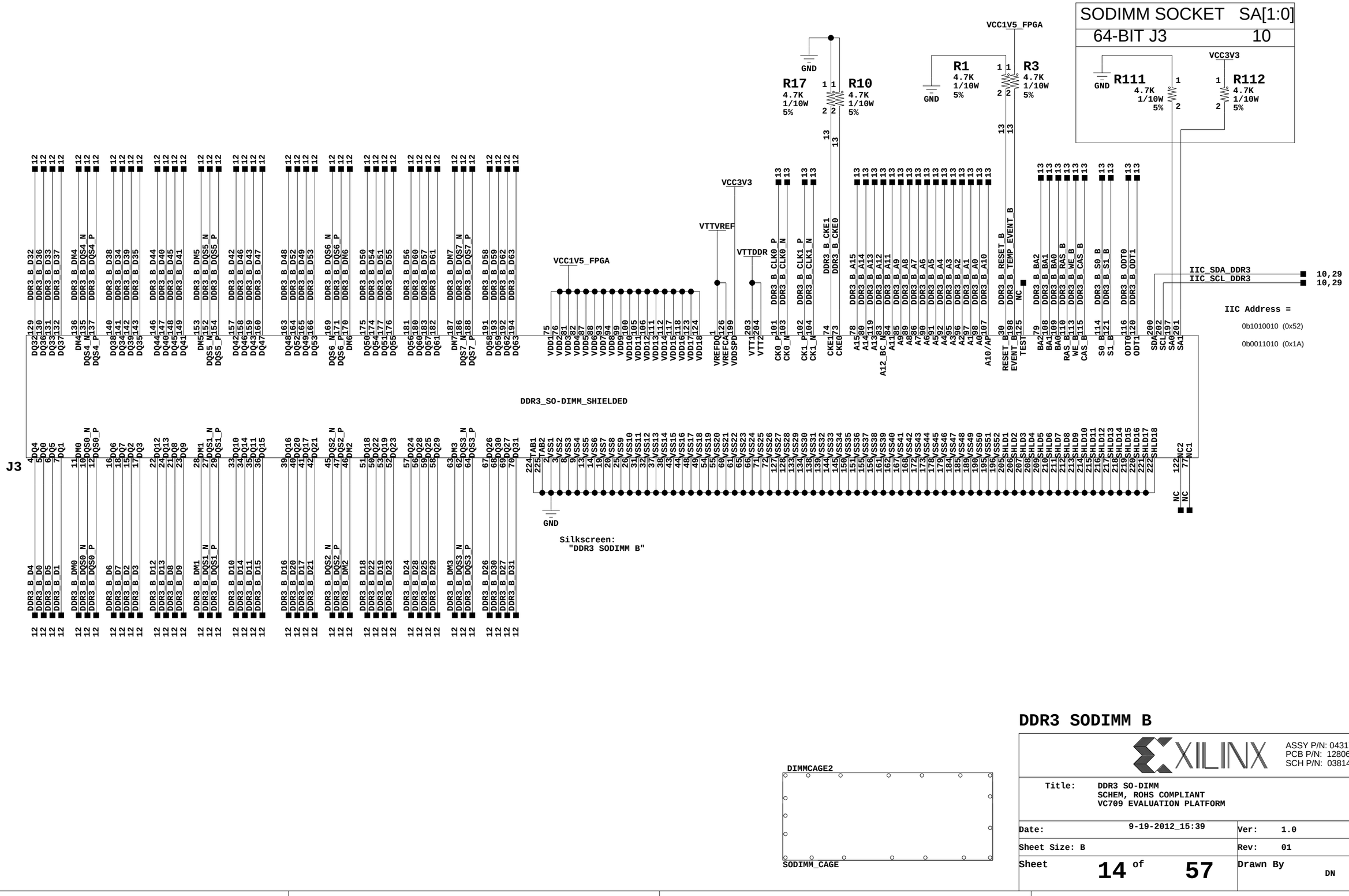
FPGA Banks 32

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Banks 12, 32
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_12:08	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	13 of 57	Drawn By	DN

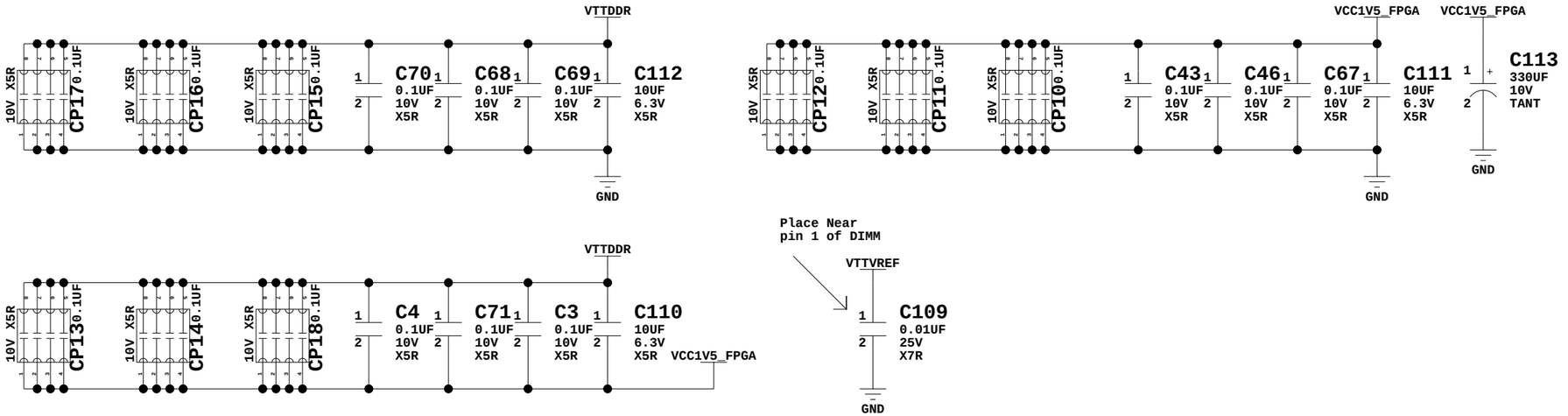


DDR3 SODIMM B

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: DDR3 SO-DIMM SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM	
Date: 9-19-2012_15:39	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 14 of 57	Drawn By DN



SODIMM B DECOUPLING

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 36
XC7VX690TFFG1761

	IO_0_VRN_36_M23	M23	NC
	IO_L1P_T0_36_H24	H24	FMC1_HPC_HB04_P
	IO_L1N_T0_36_G24	G24	FMC1_HPC_HB04_N
	IO_L2P_T0_36_J21	J21	FMC1_HPC_HB14_P
	IO_L2N_T0_36_H21	H21	FMC1_HPC_HB14_N
	IO_L3P_T0_DQS_36_H25	H25	FMC1_HPC_HB08_P
	IO_L3N_T0_DQS_36_H26	H26	FMC1_HPC_HB08_N
	IO_L4P_T0_36_G21	G21	FMC1_HPC_HB18_P
	IO_L4N_T0_36_G22	G22	FMC1_HPC_HB18_N
	IO_L5P_T0_36_G26	G26	FMC1_HPC_HB07_P
	IO_L5N_T0_36_G27	G27	FMC1_HPC_HB07_N
	IO_L6P_T0_36_H23	H23	FMC1_HPC_HB09_P
	IO_L6N_T0_VREF_36_G23	G23	FMC1_HPC_HB09_N
	IO_L7P_T1_36_G28	G28	FMC1_HPC_HB03_P
	IO_L7N_T1_36_G29	G29	FMC1_HPC_HB03_N
	IO_L8P_T1_36_K28	K28	FMC1_HPC_HB02_P
	IO_L8N_T1_36_J28	J28	FMC1_HPC_HB02_N
	IO_L9P_T1_DQS_36_H28	H28	FMC1_HPC_HB01_P
	IO_L9N_T1_DQS_36_H29	H29	FMC1_HPC_HB01_N
	IO_L10P_T1_36_K27	K27	FMC1_HPC_HB05_P
	IO_L10N_T1_36_J27	J27	FMC1_HPC_HB05_N
	IO_L11P_T1_SRCC_36_K24	K24	FMC1_HPC_HB12_P
	IO_L11N_T1_SRCC_36_K25	K25	FMC1_HPC_HB12_N
	IO_L12P_T1_MRCC_36_J25	J25	FMC1_HPC_HB00_CC_P
	IO_L12N_T1_MRCC_36_J26	J26	FMC1_HPC_HB00_CC_N
	IO_L13P_T2_MRCC_36_M24	M24	FMC1_HPC_HB17_CC_P
	IO_L13N_T2_MRCC_36_L24	L24	FMC1_HPC_HB17_CC_N
	IO_L14P_T2_SRCC_36_K23	K23	FMC1_HPC_HB06_CC_P
	IO_L14N_T2_SRCC_36_J23	J23	FMC1_HPC_HB06_CC_N
	IO_L15P_T2_DQS_36_M22	M22	FMC1_HPC_HB10_P
	IO_L15N_T2_DQS_36_L22	L22	FMC1_HPC_HB10_N
	IO_L16P_T2_36_L25	L25	FMC1_HPC_HB19_P
	IO_L16N_T2_36_L26	L26	FMC1_HPC_HB19_N
	IO_L17P_T2_36_K22	K22	FMC1_HPC_HB11_P
	IO_L17N_T2_36_J22	J22	FMC1_HPC_HB11_N
	IO_L18P_T2_36_M21	M21	FMC1_HPC_HB15_P
	IO_L18N_T2_36_L21	L21	FMC1_HPC_HB15_N
	IO_L19P_T3_36_P21	P21	FMC1_HPC_HB20_P
	IO_L19N_T3_VREF_36_N21	N21	FMC1_HPC_HB20_N
	IO_L20P_T3_36_P25	P25	FMC1_HPC_HB13_P
	IO_L20N_T3_36_P26	P26	FMC1_HPC_HB13_N
	IO_L21P_T3_DQS_36_P22	P22	FMC1_HPC_HB21_P
	IO_L21N_T3_DQS_36_P23	P23	FMC1_HPC_HB21_N
	IO_L22P_T3_36_N25	N25	FMC1_HPC_HB16_P
	IO_L22N_T3_36_N26	N26	FMC1_HPC_HB16_N
	IO_L23P_T3_36_N23	N23	NC
	IO_L23N_T3_36_N24	N24	NC
	IO_L24P_T3_36_M27	M27	NC
	IO_L24N_T3_36_L27	L27	NC
	IO_25_VRP_36_M26	M26	NC

FMC1_VIO_B_M2C

G25	VCCO_36_G25	
H22	VCCO_36_H22	
J29	VCCO_36_J29	
K26	VCCO_36_K26	
L23	VCCO_36_L23	
N27	VCCO_36_N27	
P24	VCCO_36_P24	

U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 19
XC7VX690TFFG1761

	IO_0_VRN_19_L36	L36	VRN_19
	IO_L1P_T0_19_E40	E40	NC
	IO_L1N_T0_19_D40	D40	NC
	IO_L2P_T0_19_A40	A40	NC
	IO_L2N_T0_19_A41	A41	NC
	IO_L3P_T0_DQS_19_D41	D41	NC
	IO_L3N_T0_DQS_19_D42	D42	NC
	IO_L4P_T0_19_B41	B41	NC
	IO_L4N_T0_19_B42	B42	NC
	IO_L5P_T0_19_F42	F42	NC
	IO_L5N_T0_19_E42	E42	NC
	IO_L6P_T0_19_C40	C40	NC
	IO_L6N_T0_VREF_19_C41	C41	NC
	IO_L7P_T1_19_H40	H40	FMC1_HPC_LA04_P
	IO_L7N_T1_19_H41	H41	FMC1_HPC_LA04_N
	IO_L8P_T1_19_H39	H39	FMC1_HPC_LA13_P
	IO_L8N_T1_19_G39	G39	FMC1_HPC_LA13_N
	IO_L9P_T1_DQS_19_G41	G41	FMC1_HPC_LA07_P
	IO_L9N_T1_DQS_19_G42	G42	FMC1_HPC_LA07_N
	IO_L10P_T1_19_F40	F40	FMC1_HPC_LA11_P
	IO_L10N_T1_19_F41	F41	FMC1_HPC_LA11_N
	IO_L11P_T1_SRCC_19_J40	J40	FMC1_HPC_LA01_CC_P
	IO_L11N_T1_SRCC_19_J41	J41	FMC1_HPC_LA01_CC_N
	IO_L12P_T1_MRCC_19_K39	K39	FMC1_HPC_LA00_CC_P
	IO_L12N_T1_MRCC_19_K40	K40	FMC1_HPC_LA00_CC_N
	IO_L13P_T2_MRCC_19_L39	L39	FMC1_HPC_CLK0_M2C_P
	IO_L13N_T2_MRCC_19_L40	L40	FMC1_HPC_CLK0_M2C_N
	IO_L14P_T2_SRCC_19_M41	M41	FMC1_HPC_LA05_P
	IO_L14N_T2_SRCC_19_L41	L41	FMC1_HPC_LA05_N
	IO_L15P_T2_DQS_19_K42	K42	FMC1_HPC_LA06_P
	IO_L15N_T2_DQS_19_J42	J42	FMC1_HPC_LA06_N
	IO_L16P_T2_19_M42	M42	FMC1_HPC_LA03_P
	IO_L16N_T2_19_L42	L42	FMC1_HPC_LA03_N
	IO_L17P_T2_19_K37	K37	FMC1_HPC_LA16_P
	IO_L17N_T2_19_K38	K38	FMC1_HPC_LA16_N
	IO_L18P_T2_19_M36	M36	FMC1_HPC_LA15_P
	IO_L18N_T2_19_L37	L37	FMC1_HPC_LA15_N
	IO_L19P_T3_19_P41	P41	FMC1_HPC_LA02_P
	IO_L19N_T3_VREF_19_N41	N41	FMC1_HPC_LA02_N
	IO_L20P_T3_19_M37	M37	FMC1_HPC_LA08_P
	IO_L20N_T3_19_M38	M38	FMC1_HPC_LA08_N
	IO_L21P_T3_DQS_19_R42	R42	FMC1_HPC_LA09_P
	IO_L21N_T3_DQS_19_P42	P42	FMC1_HPC_LA09_N
	IO_L22P_T3_19_N38	N38	FMC1_HPC_LA10_P
	IO_L22N_T3_19_M39	M39	FMC1_HPC_LA10_N
	IO_L23P_T3_19_R40	R40	FMC1_HPC_LA12_P
	IO_L23N_T3_19_P40	P40	FMC1_HPC_LA12_N
	IO_L24P_T3_19_N39	N39	FMC1_HPC_LA14_P
	IO_L24N_T3_19_N40	N40	FMC1_HPC_LA14_N
	IO_25_VRP_19_N36	N36	VRP_19

VCC1V8_FPGA

B40	VCCO_19_B40	
E41	VCCO_19_E41	
H42	VCCO_19_H42	
J39	VCCO_19_J39	
M40	VCCO_19_M40	
N37	VCCO_19_N37	
R41	VCCO_19_R41	

U1

SOC_IRON_690T_FF1761

FMC1_VIO_B_M2C

C404
100UF
6.3
X5R
1
2
GND

VCC1V8_FPGA

R450
100
1/10W
1%
1
2
16 VRN_19

R449
100
1/10W
1%
1
2
16 VRP_19
GND

VCC1V8_FPGA

C156
100UF
6.3
X5R
1
2
GND

FPGA Banks 36, 19

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Banks 18, 19
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	16 of 57	Drawn By	DN

SOC_V7_690T_FF1761_IRON

BANK 34
XC7VX690TFFG1761

IO_0_VRN_34_R29	R29	VRN_34	17
IO_L1P_T0_34_K35	K35	NC	
IO_L1N_T0_34_J35	J35	NC	
IO_L2P_T0_34_J32	J32	NC	
IO_L2N_T0_34_J33	J33	NC	
IO_L3P_T0_DQS_34_K33	K33	NC	
IO_L3N_T0_DQS_34_K34	K34	NC	
IO_L4P_T0_34_L34	L34	NC	
IO_L4N_T0_34_L35	L35	NC	
IO_L5P_T0_34_M33	M33	NC	
IO_L5N_T0_34_M34	M34	NC	
IO_L6P_T0_34_H34	H34	NC	
IO_L6N_T0_VREF_34_H35	H35	NC	
IO_L7P_T1_34_K29	K29	FMC1_HPC_LA25_P	19
IO_L7N_T1_34_K30	K30	FMC1_HPC_LA25_N	19
IO_L8P_T1_34_J30	J30	FMC1_HPC_LA26_P	18
IO_L8N_T1_34_H30	H30	FMC1_HPC_LA26_N	18
IO_L9P_T1_DQS_34_L29	L29	FMC1_HPC_LA28_P	20
IO_L9N_T1_DQS_34_L30	L30	FMC1_HPC_LA28_N	20
IO_L10P_T1_34_J31	J31	FMC1_HPC_LA27_P	18
IO_L10N_T1_34_H31	H31	FMC1_HPC_LA27_N	18
IO_L11P_T1_SRCC_34_M32	M32	FMC1_HPC_LA18_CC_P	18
IO_L11N_T1_SRCC_34_L32	L32	FMC1_HPC_LA18_CC_N	18
IO_L12P_T1_MRCC_34_L31	L31	FMC1_HPC_LA17_CC_P	18
IO_L12N_T1_MRCC_34_K32	K32	FMC1_HPC_LA17_CC_N	18
IO_L13P_T2_MRCC_34_N30	N30	FMC1_HPC_CLK1_M2C_P	19
IO_L13N_T2_MRCC_34_M31	M31	FMC1_HPC_CLK1_M2C_N	19
IO_L14P_T2_SRCC_34_P30	P30	FMC1_HPC_LA23_P	19
IO_L14N_T2_SRCC_34_N31	N31	FMC1_HPC_LA23_N	18
IO_L15P_T2_DQS_34_M28	M28	FMC1_HPC_LA31_P	18
IO_L15N_T2_DQS_34_M29	M29	FMC1_HPC_LA31_N	19
IO_L16P_T2_34_R28	R28	FMC1_HPC_LA22_P	19
IO_L16N_T2_34_P28	P28	FMC1_HPC_LA22_N	19
IO_L17P_T2_34_N28	N28	FMC1_HPC_LA21_P	19
IO_L17N_T2_34_N29	N29	FMC1_HPC_LA21_N	20
IO_L18P_T2_34_R30	R30	FMC1_HPC_LA24_P	20
IO_L18N_T2_34_P31	P31	FMC1_HPC_LA24_N	20
IO_L19P_T3_34_U31	U31	FMC1_HPC_LA33_P	19
IO_L19N_T3_VREF_34_T31	T31	FMC1_HPC_LA33_N	19
IO_L20P_T3_34_V30	V30	FMC1_HPC_LA30_P	19
IO_L20N_T3_34_V31	V31	FMC1_HPC_LA30_N	20
IO_L21P_T3_DQS_34_T29	T29	FMC1_HPC_LA29_P	20
IO_L21N_T3_DQS_34_T30	T30	FMC1_HPC_LA29_N	19
IO_L22P_T3_34_W30	W30	FMC1_HPC_LA19_P	19
IO_L22N_T3_34_W31	W31	FMC1_HPC_LA19_N	20
IO_L23P_T3_34_V29	V29	FMC1_HPC_LA32_P	20
IO_L23N_T3_34_U29	U29	FMC1_HPC_LA32_N	20
IO_L24P_T3_34_Y29	Y29	FMC1_HPC_LA20_P	20
IO_L24N_T3_34_Y30	Y30	FMC1_HPC_LA20_N	19
IO_25_VRP_34_U28	U28	VRP_34	19
			17

VCC1V8_FPGA

H32	VCCO_34_H32
L33	VCCO_34_L33
M30	VCCO_34_M30
R31	VCCO_34_R31
T28	VCCO_34_T28
W29	VCCO_34_W29

U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 35
XC7VX690TFFG1761

IO_0_VRN_35_G31	G31	NC	
IO_L1P_T0_AD4P_35_B36	B36	FMC1_HPC_HA13_P	19
IO_L1N_T0_AD4N_35_A37	A37	FMC1_HPC_HA13_N	19
IO_L2P_T0_AD12P_35_B34	B34	FMC1_HPC_HA20_P	19
IO_L2N_T0_AD12N_35_A34	A34	FMC1_HPC_HA20_N	19
IO_L3P_T0_DQS_AD5P_35_B39	B39	FMC1_HPC_HA16_P	19
IO_L3N_T0_DQS_AD5N_35_A39	A39	FMC1_HPC_HA16_N	19
IO_L4P_T0_35_A35	A35	FMC1_HPC_HA23_P	20
IO_L4N_T0_35_A36	A36	FMC1_HPC_HA23_N	20
IO_L5P_T0_AD13P_35_C38	C38	FMC1_HPC_HA07_P	20
IO_L5N_T0_AD13N_35_C39	C39	FMC1_HPC_HA07_N	20
IO_L6P_T0_35_B37	B37	FMC1_HPC_HA12_P	19
IO_L6N_T0_VREF_35_B38	B38	FMC1_HPC_HA12_N	19
IO_L7P_T1_AD6P_35_E32	E32	FMC1_HPC_HA09_P	19
IO_L7N_T1_AD6N_35_D32	D32	FMC1_HPC_HA09_N	19
IO_L8P_T1_AD14P_35_B32	B32	FMC1_HPC_HA19_P	19
IO_L8N_T1_AD14N_35_B33	B33	FMC1_HPC_HA19_N	19
IO_L9P_T1_DQS_AD7P_35_E33	E33	FMC1_HPC_HA02_P	20
IO_L9N_T1_DQS_AD7N_35_D33	D33	FMC1_HPC_HA02_N	20
IO_L10P_T1_AD15P_35_C33	C33	FMC1_HPC_HA15_P	19
IO_L10N_T1_AD15N_35_C34	C34	FMC1_HPC_HA15_N	19
IO_L11P_T1_SRCC_35_D35	D35	FMC1_HPC_HA01_CC_P	19
IO_L11N_T1_SRCC_35_D36	D36	FMC1_HPC_HA01_CC_N	19
IO_L12P_T1_MRCC_35_C35	C35	FMC1_HPC_HA17_CC_P	20
IO_L12N_T1_MRCC_35_C36	C36	FMC1_HPC_HA17_CC_N	20
IO_L13P_T2_MRCC_35_E34	E34	FMC1_HPC_HA00_CC_P	19
IO_L13N_T2_MRCC_35_E35	E35	FMC1_HPC_HA00_CC_N	19
IO_L14P_T2_SRCC_35_D37	D37	FMC1_HPC_HA21_P	19
IO_L14N_T2_SRCC_35_D38	D38	FMC1_HPC_HA21_N	20
IO_L15P_T2_DQS_35_G32	G32	FMC1_HPC_HA05_P	20
IO_L15N_T2_DQS_35_F32	F32	FMC1_HPC_HA05_N	19
IO_L16P_T2_35_F36	F36	FMC1_HPC_HA22_P	19
IO_L16N_T2_35_F37	F37	FMC1_HPC_HA22_N	20
IO_L17P_T2_35_F34	F34	FMC1_HPC_HA04_P	20
IO_L17N_T2_35_F35	F35	FMC1_HPC_HA04_N	19
IO_L18P_T2_35_H33	H33	FMC1_HPC_HA03_P	19
IO_L18N_T2_35_G33	G33	FMC1_HPC_HA03_N	20
IO_L19P_T3_35_E37	E37	FMC1_HPC_HA14_P	20
IO_L19N_T3_VREF_35_E38	E38	FMC1_HPC_HA14_N	20
IO_L20P_T3_35_G36	G36	FMC1_HPC_HA06_P	20
IO_L20N_T3_35_G37	G37	FMC1_HPC_HA06_N	20
IO_L21P_T3_DQS_35_F39	F39	FMC1_HPC_HA18_P	20
IO_L21N_T3_DQS_35_E39	E39	FMC1_HPC_HA18_N	20
IO_L22P_T3_35_J37	J37	FMC1_HPC_HA11_P	20
IO_L22N_T3_35_J38	J38	FMC1_HPC_HA11_N	20
IO_L23P_T3_35_H38	H38	FMC1_HPC_HA10_P	20
IO_L23N_T3_35_G38	G38	FMC1_HPC_HA10_N	20
IO_L24P_T3_35_J36	J36	FMC1_HPC_HA08_P	19
IO_L24N_T3_35_H36	H36	FMC1_HPC_HA08_N	19
IO_25_VRP_35_G34	G34	NC	

VCC1V8_FPGA

A33	VCCO_35_A33
C37	VCCO_35_C37
D34	VCCO_35_D34
E31	VCCO_35_E31
F38	VCCO_35_F38
G35	VCCO_35_G35
K36	VCCO_35_K36

U1

SOC_IRON_690T_FF1761

VCC1V8_FPGA

C157
100UF
6.3
X5R

GND

VCC1V8_FPGA

R454
100
1/10W
1%

17 VRN_34

17 VRP_34

R453
100
1/10W
1%

GND

VCC1V8_FPGA

C158
100UF
6.3
X5R

GND

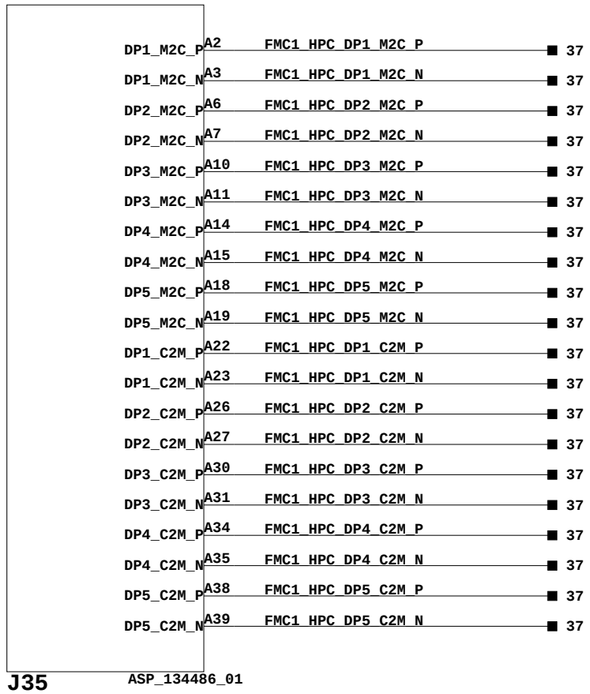
FPGA Banks 34,35 FMC1

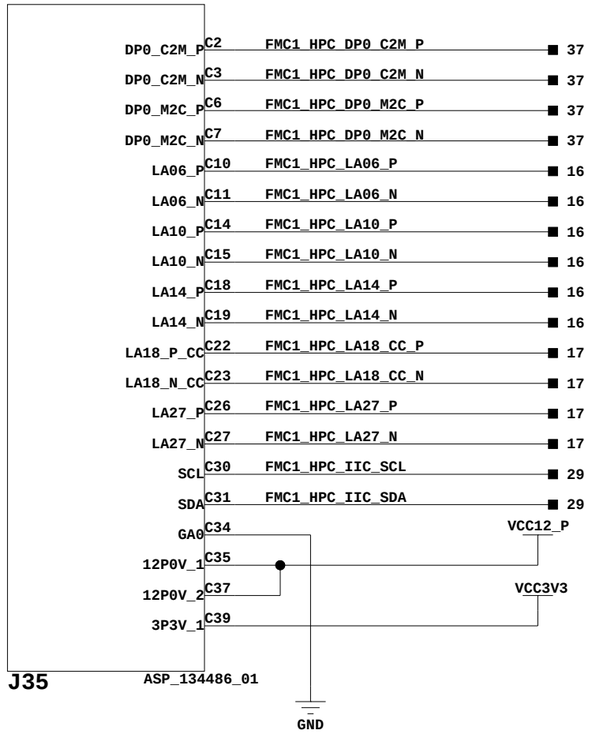
XILINX

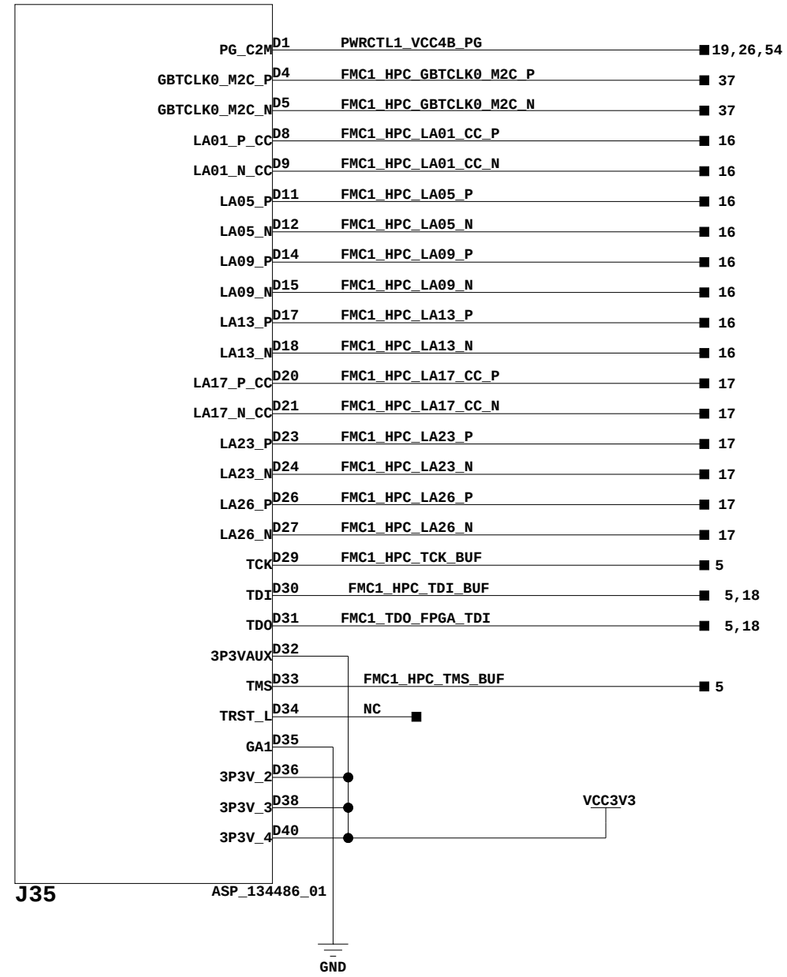
ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

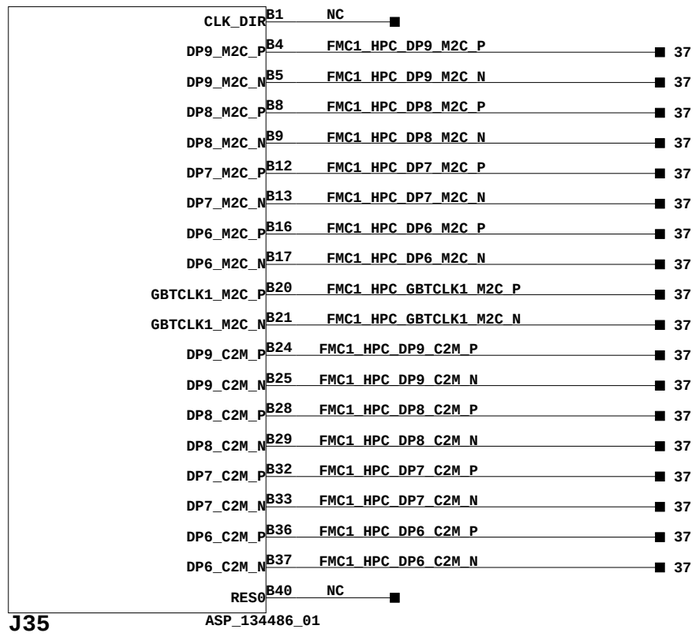
Title: FPGA Banks 34, 35
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

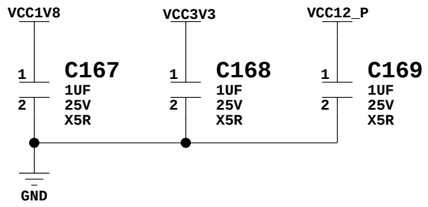
Date:	12-21-2012_12:08	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	17 of 57	Drawn By	DN

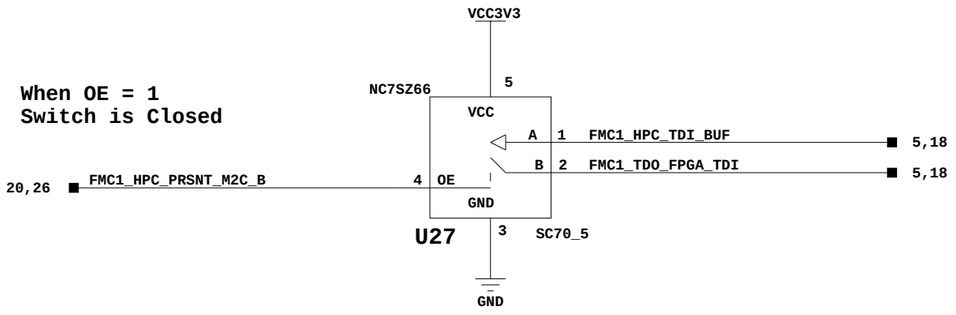










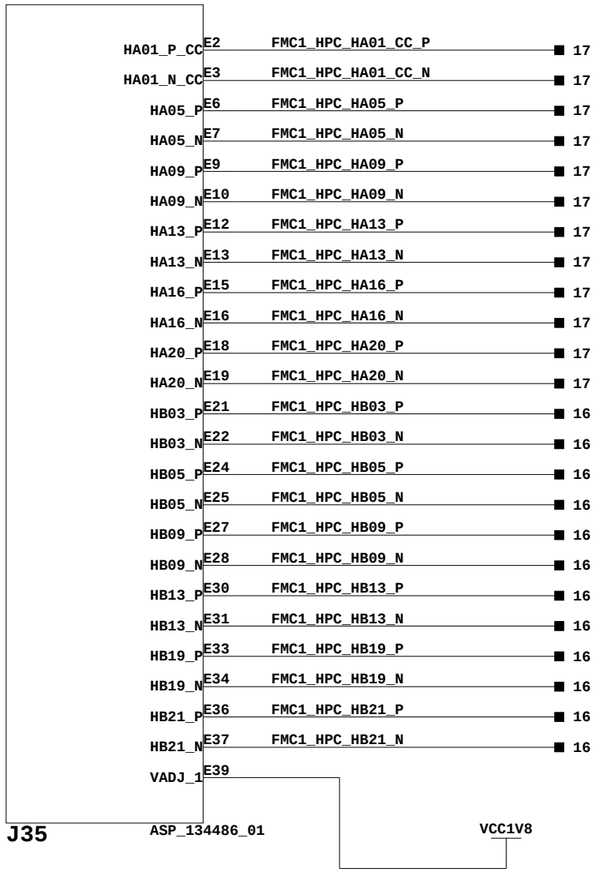


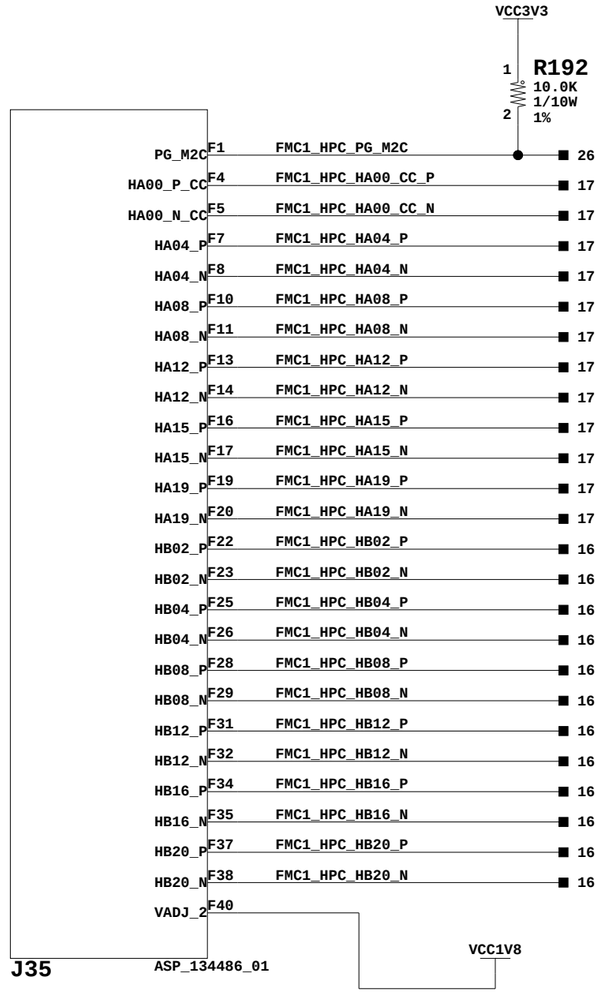
ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows A, B, C, D

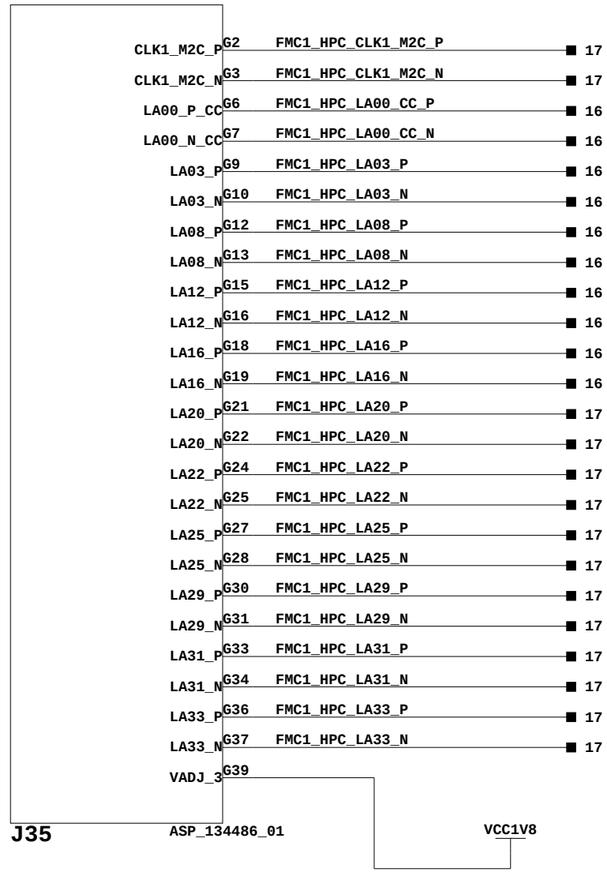
XILINX

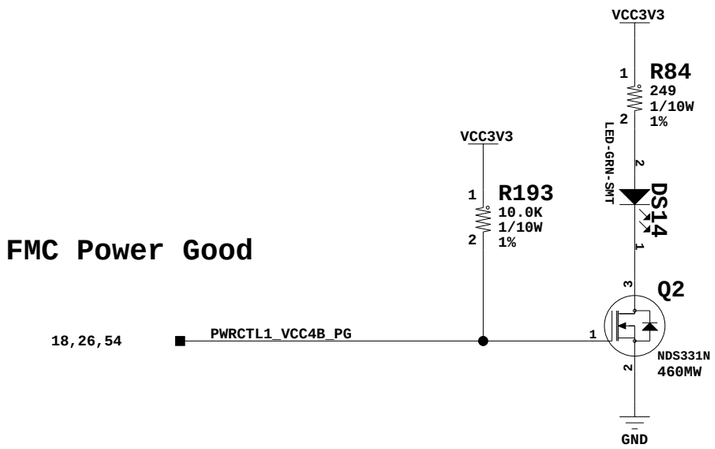
ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FMC 1 HPC Header, Rows A, B, C, D SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	18 of 57	Drawn By	DN









ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows E, F, G

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FMC 1 HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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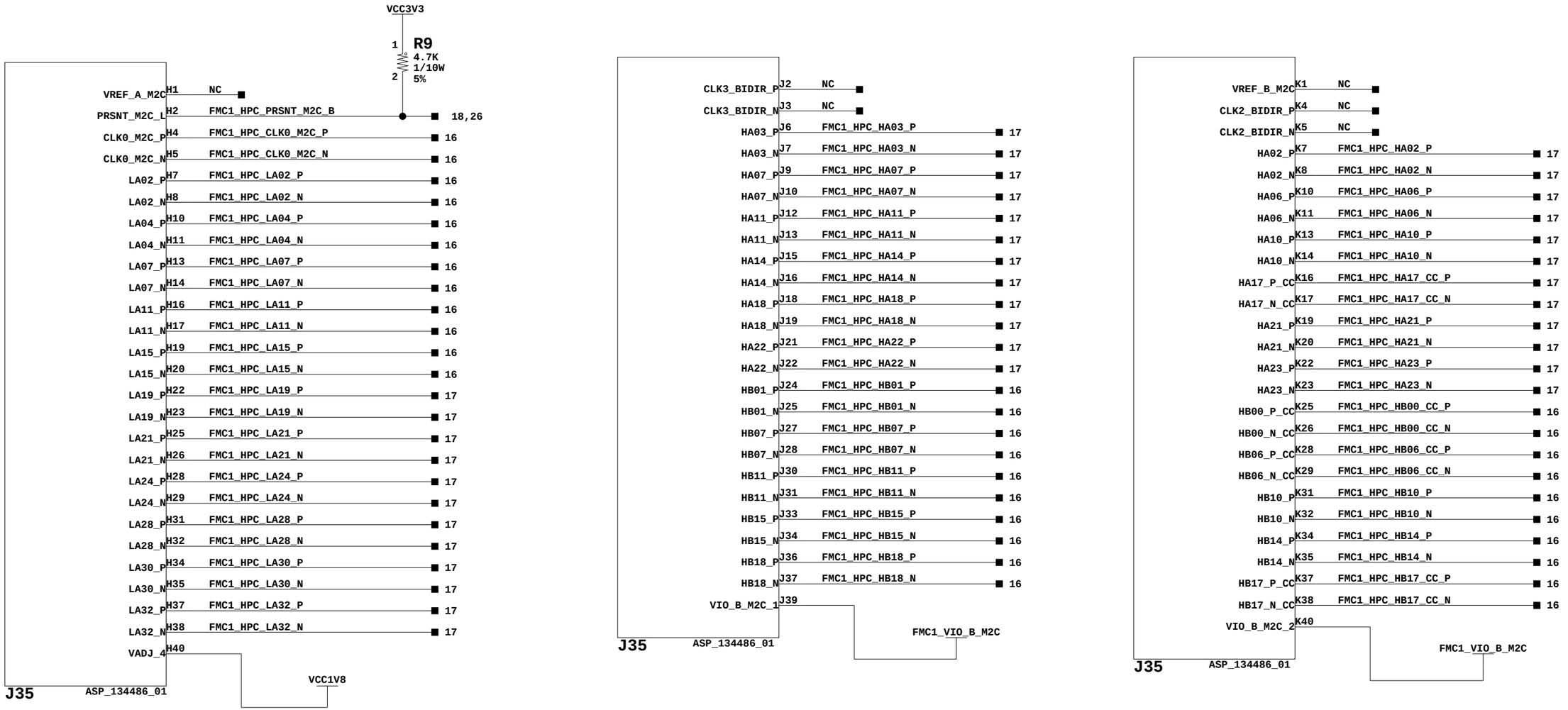

ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows H, J, K

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FMC 1 HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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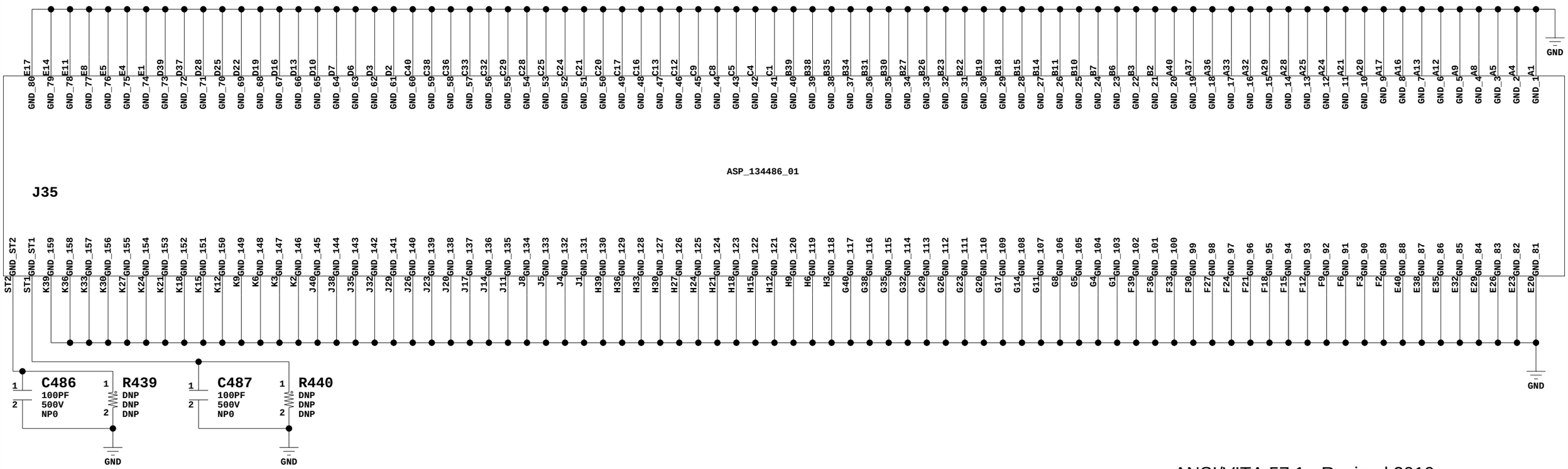

ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, GND

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FMC 1 HPC Header, GND SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 13
XC7VX690TFFG1761

IO_0_VRN_13_AR35	AR35	GPIO_LED_4_LS	26
IO_L1P_T0_13_AY34	AY34	NC	
IO_L1N_T0_13_BA35	BA35	NC	
IO_L2P_T0_13_AV36	AV36	NC	
IO_L2N_T0_13_AW36	AW36	NC	
IO_L3P_T0_DQS_13_BA34	BA34	NC	
IO_L3N_T0_DQS_13_BB34	BB34	NC	
IO_L4P_T0_13_BA36	BA36	NC	
IO_L4N_T0_13_BB36	BB36	NC	
IO_L5P_T0_13_BB32	BB32	NC	
IO_L5N_T0_13_BB33	BB33	NC	
IO_L6P_T0_13_AW35	AW35	NC	
IO_L6N_T0_VREF_13_AY35	AY35	NC	
IO_L7P_T1_13_AT34	AT34	NC	
IO_L7N_T1_13_AU34	AU34	SI5324_INT_ALM_LS	26
IO_L8P_T1_13_AT36	AT36	SI5324_RST_LS	26
IO_L8N_T1_13_AU36	AU36	USB_UART_RX	6
IO_L9P_T1_DQS_13_AT32	AT32	USB_UART_RTS	6
IO_L9N_T1_DQS_13_AU33	AU33	USB_UART_TX	6
IO_L10P_T1_13_AR34	AR34	USB_UART_CTS	6
IO_L10N_T1_13_AT35	AT35	IIC_SCL_MAIN_LS	29
IO_L11P_T1_SRCC_13_AU32	AU32	IIC_SDA_MAIN_LS	29
IO_L11N_T1_SRCC_13_AV33	AV33	PCIE_WAKE_B_LS	26
IO_L12P_T1_MRCC_13_AW32	AW32	REC_CLOCK_C_P	4
IO_L12N_T1_MRCC_13_AW33	AW33	REC_CLOCK_C_N	4
IO_L13P_T2_MRCC_13_AV34	AV34	NC	
IO_L13N_T2_MRCC_13_AV35	AV35	PCIE_PERST_LS	26
IO_L14P_T2_SRCC_13_AY32	AY32	NC	
IO_L14N_T2_SRCC_13_AY33	AY33	GPIO_DIP_SW1	25
IO_L15P_T2_DQS_13_BA31	BA31	GPIO_DIP_SW2	25
IO_L15N_T2_DQS_13_BA32	BA32	GPIO_DIP_SW3	25
IO_L16P_T2_13_AW30	AW30	GPIO_DIP_SW4	25
IO_L16N_T2_13_AY30	AY30	GPIO_DIP_SW5	25
IO_L17P_T2_13_BA30	BA30	GPIO_DIP_SW6	25
IO_L17N_T2_13_BB31	BB31	GPIO_DIP_SW7	25
IO_L18P_T2_13_AV30	AV30	GPIO_DIP_SW0	25
IO_L18N_T2_13_AW31	AW31	NC	
IO_L19P_T3_13_AR30	AR30	NC	
IO_L19N_T3_VREF_13_AT30	AT30	NC	
IO_L20P_T3_13_AU31	AU31	NC	
IO_L20N_T3_13_AV31	AV31	NC	
IO_L21P_T3_DQS_13_AN30	AN30	NC	
IO_L21N_T3_DQS_13_AP30	AP30	NC	
IO_L22P_T3_13_AP32	AP32	NC	
IO_L22N_T3_13_AR32	AR32	NC	
IO_L23P_T3_13_AN31	AN31	NC	
IO_L23N_T3_13_AP31	AP31	NC	
IO_L24P_T3_13_AP33	AP33	NC	
IO_L24N_T3_13_AR33	AR33	NC	
IO_25_VRP_13_AT31	AT31	NC	

VCC1V8_FPGA

AP34	VCCO_13_AP34
AR31	VCCO_13_AR31
AU35	VCCO_13_AU35
AV32	VCCO_13_AV32
AY36	VCCO_13_AY36
BA33	VCCO_13_BA33
BB30	VCCO_13_BB30

U1

SOC_IRON_690T_FF1761

VCC1V8_FPGA

C159
100UF
6.3
X5R
1
2
GND

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: USER IO
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_12:08	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 14
XC7VX690TFFG1761

IO_0_VRN_14_AH35	AH35	NC
IO_L1P_T0_D00_MOSI_14_AM36	AM36	FLASH_D0 24
IO_L1N_T0_D01_DIN_14_AN36	AN36	FLASH_D1 24
IO_L2P_T0_D02_14_AJ36	AJ36	FLASH_D2 24
IO_L2N_T0_D03_14_AJ37	AJ37	FLASH_D3 24
IO_L3P_T0_DQS_PUDC_B_14_AP36	AP36	
IO_L3N_T0_DQS_EMCCLK_14_AP37	AP37	FPGA_EMCCLK 5
IO_L4P_T0_D04_14_AK37	AK37	FLASH_D4 24
IO_L4N_T0_D05_14_AL37	AL37	FLASH_D5 24
IO_L5P_T0_D06_14_AN35	AN35	FLASH_D6 24
IO_L5N_T0_D07_14_AP35	AP35	FLASH_D7 24
IO_L6P_T0_FCS_B_14_AL36	AL36	FLASH_CE_B 24
IO_L6N_T0_D08_VREF_14_AM37	AM37	FLASH_D8 24
IO_L7P_T1_D09_14_AG33	AG33	FLASH_D9 24
IO_L7N_T1_D10_14_AH33	AH33	FLASH_D10 24
IO_L8P_T1_D11_14_AK35	AK35	FLASH_D11 24
IO_L8N_T1_D12_14_AL35	AL35	FLASH_D12 24
IO_L9P_T1_DQS_14_AH31	AH31	NC
IO_L9N_T1_DQS_D13_14_AJ31	AJ31	FLASH_D13
IO_L10P_T1_D14_14_AH34	AH34	FLASH_D14 24
IO_L10N_T1_D15_14_AJ35	AJ35	FLASH_D15 24
IO_L11P_T1_SRCC_14_AJ33	AJ33	NC
IO_L11N_T1_SRCC_14_AK33	AK33	NC
IO_L12P_T1_MRCC_14_AK34	AK34	USER_CLOCK_P 3
IO_L12N_T1_MRCC_14_AL34	AL34	USER_CLOCK_N 3
IO_L13P_T2_MRCC_14_AJ32	AJ32	USER_SMA_CLOCK_P 3
IO_L13N_T2_MRCC_14_AK32	AK32	USER_SMA_CLOCK_N 3
IO_L14P_T2_SRCC_14_AL31	AL31	NC
IO_L14N_T2_SRCC_14_AL32	AL32	FMC_C2M_PG_LS 26
IO_L15P_T2_DQS_RDWR_B_14_AM34	AM34	FLASH_WAIT 24
IO_L15N_T2_DQSDOUT_CSO_B_14_AN34	AN34	FMC1_HPC_PG_M2C_LS 26
IO_L16P_T2_CSI_B_14_AM31	AM31	FMC1_HPC_PRSNT_M2C_B_LS 26
IO_L16N_T2_A15_D31_14_AM32	AM32	FLASH_A15 24
IO_L17P_T2_A14_D30_14_AM33	AM33	FLASH_A14 24
IO_L17N_T2_A13_D29_14_AN33	AN33	FLASH_A13 24
IO_L18P_T2_A12_D28_14_AL29	AL29	FLASH_A12 24
IO_L18N_T2_A11_D27_14_AL30	AL30	FLASH_A11 24
IO_L19P_T3_A10_D26_14_AH29	AH29	FLASH_A10 24
IO_L19N_T3A09D25_VREF_14_AH30	AH30	FLASH_A9 24
IO_L20P_T3_A08_D24_14_AJ30	AJ30	FLASH_A8 24
IO_L20N_T3_A07_D23_14_AK30	AK30	FLASH_A7 24
IO_L21P_T3_DQS_14_AF29	AF29	NC
IO_L21N_T3_DQS_A06_D22_14_AG29	AG29	FLASH_A6 24
IO_L22P_T3_A05_D21_14_AK28	AK28	FLASH_A5 24
IO_L22N_T3_A04_D20_14_AK29	AK29	FLASH_A4 24
IO_L23P_T3_A03_D19_14_AF30	AF30	FLASH_A3 24
IO_L23N_T3_A02_D18_14_AG31	AG31	FLASH_A2 24
IO_L24P_T3_A01_D17_14_AH28	AH28	FLASH_A1 24
IO_L24N_T3_A00_D16_14_AJ28	AJ28	FLASH_A0 24
IO_25_VRP_14_AG32	AG32	NC

VCC1V8_FPGA

AF28	VCCO_14_AF28
AH32	VCCO_14_AH32
AJ29	VCCO_14_AJ29
AK36	VCCO_14_AK36
AL33	VCCO_14_AL33
AM30	VCCO_14_AM30
AN37	VCCO_14_AN37

R276 1.00K 1/16W 1% — 1 — 2 — GND

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 15
XC7VX690TFFG1761

IO_0_VRN_15_AM38	AM38	VRN_15 23
IO_L1P_T0_AD0P_15_AN38	AN38	XADC_VAUX0P_R 27
IO_L1N_T0_AD0N_15_AP38	AP38	XADC_VAUX0N_R 27
IO_L2P_T0_AD8P_15_AM41	AM41	XADC_VAUX8P_R 27
IO_L2N_T0_AD8N_15_AM42	AM42	XADC_VAUX8N_R 27
IO_L3P_T0_DQS_AD1P_15_AR38	AR38	XADC_GPIO_0 27
IO_L3N_T0_DQS_AD1N_15_AR39	AR39	XADC_GPIO_1 27
IO_L4P_T0_15_AN40	AN40	XADC_GPIO_2 27
IO_L4N_T0_15_AN41	AN41	XADC_GPIO_3 27
IO_L5P_T0_AD9P_15_AR37	AR37	GPIO_LED_2_LS 26
IO_L5N_T0_AD9N_15_AT37	AT37	GPIO_LED_3_LS 26
IO_L6P_T0_15_AM39	AM39	GPIO_LED_0_LS 26
IO_L6N_T0_VREF_15_AN39	AN39	GPIO_LED_1_LS 26
IO_L7P_T1_AD2P_15_AP40	AP40	GPIO_SW_S 25
IO_L7N_T1_AD2N_15_AR40	AR40	GPIO_SW_N 25
IO_L8P_T1_AD10P_15_AP41	AP41	GPIO_LED_5_LS 26
IO_L8N_T1_AD10N_15_AP42	AP42	GPIO_LED_6_LS 26
IO_L9P_T1_DQS_AD3P_15_AT39	AT39	NC
IO_L9N_T1_DQS_AD3N_15_AT40	AT40	NC
IO_L10P_T1_AD11P_15_AR42	AR42	NC
IO_L10N_T1_AD11N_15_AT42	AT42	NC
IO_L11P_T1_SRCC_15_AU39	AU39	GPIO_LED_7_LS 26
IO_L11N_T1_SRCC_15_AV39	AV39	GPIO_SW_C 25
IO_L12P_T1_MRCC_15_AU38	AU38	GPIO_SW_E 25
IO_L12N_T1_MRCC_15_AV38	AV38	PMBUS_ALERT_LS 46
IO_L13P_T2_MRCC_15_AV40	AV40	CPU_RESET 25
IO_L13N_T2_MRCC_15_AW40	AW40	GPIO_SW_W 25
IO_L14P_T2_SRCC_15_AY39	AY39	PMBUS_DATA_LS 46
IO_L14N_T2_SRCC_15_AY40	AY40	NC
IO_L15P_T2_DQS_15_AW37	AW37	PMBUS_CLK_LS
IO_L15N_T2_DQS_ADV_B_15_AY37	AY37	FLASH_ADV_B 46
IO_L16P_T2_A28_15_BA37	BA37	SM_FAN_PWM 24
IO_L16N_T2_A27_15_BB37	BB37	SM_FAN_TACH 46
IO_L17P_T2_A26_15_AW38	AW38	NC
IO_L17N_T2_A25_15_AY38	AY38	NC
IO_L18P_T2_A24_15_BB38	BB38	NC
IO_L18N_T2_A23_15_BB39	BB39	FLASH_A23
IO_L19P_T3_A22_15_BA39	BA39	FLASH_A22 24
IO_L19N_T3_A21_VREF_15_BA40	BA40	FLASH_A21 24
IO_L20P_T3_A20_15_AT41	AT41	FLASH_A20 24
IO_L20N_T3_A19_15_AU42	AU42	FLASH_A19 24
IO_L21P_T3_DQS_15_AY42	AY42	IIC_MUX_RESET_B_LS 24
IO_L21N_T3_DQS_A18_15_BA42	BA42	FLASH_A18 26
IO_L22P_T3_A17_15_AU41	AU41	FLASH_A17 24
IO_L22N_T3_A16_15_AV41	AV41	FLASH_A16 24
IO_L23P_T3_FOE_B_15_BA41	BA41	FLASH_OE_B 24
IO_L23N_T3_FWE_B_15_BB41	BB41	FLASH_FWE_B 24
IO_L24P_T3_RS1_15_AW41	AW41	FLASH_A25 7,24
IO_L24N_T3_RS0_15_AW42	AW42	FLASH_A24 7,24
IO_25_VRP_15_AU37	AU37	VRP_15 23

VCC1V8_FPGA

AM40	VCCO_15_AM40
AR41	VCCO_15_AR41
AT38	VCCO_15_AT38
AV42	VCCO_15_AV42
AW39	VCCO_15_AW39
BB40	VCCO_15_BB40

U1 SOC_IRON_690T_FF1761

VCC1V8_FPGA — C400 100UF 6.3 X5R — 1 — 2 — GND

VCC1V8_FPGA — R419 100 1/10W 1% — 1 — 2 — VRN_15 (23)

VRP_15 (23) — R420 100 1/10W 1% — 1 — 2 — GND

VCC1V8_FPGA — C401 100UF 6.3 X5R — 1 — 2 — GND

FPGA Banks 14, 15

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Banks 14, 15
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_12:08	Ver:	1.0
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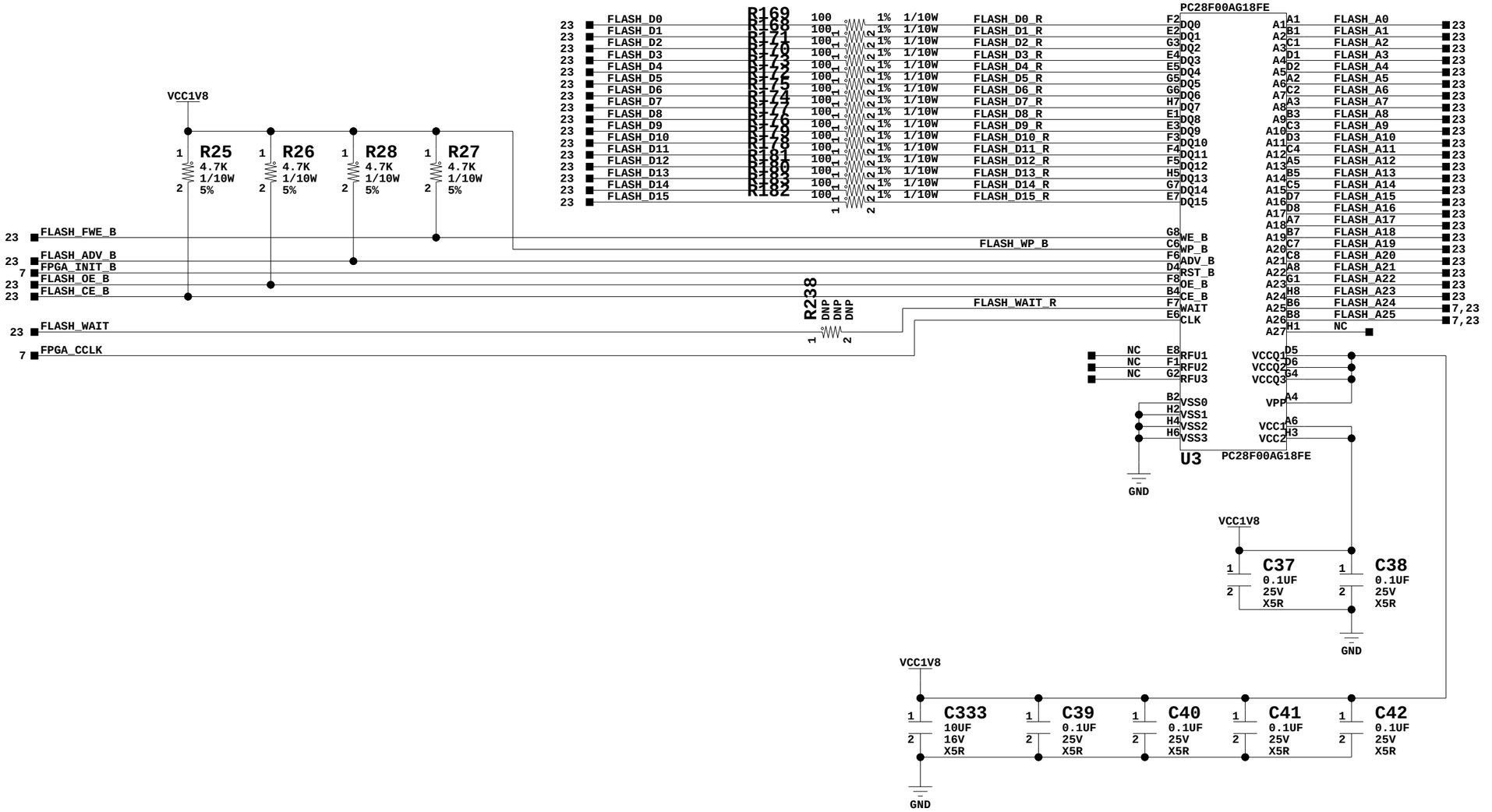

BPI FLASH

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	BPI FLASH SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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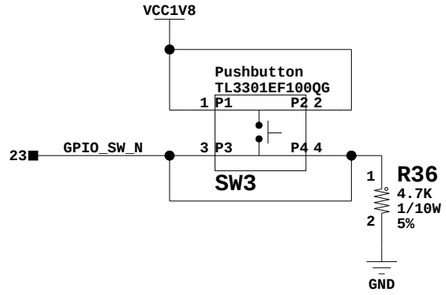
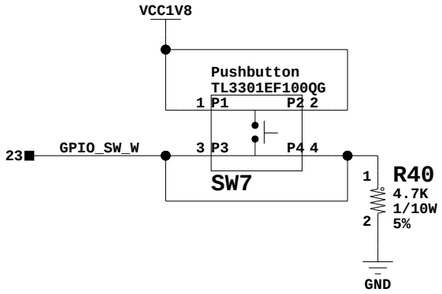
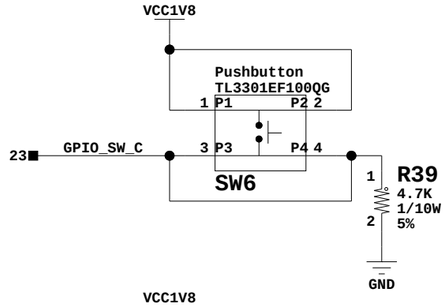
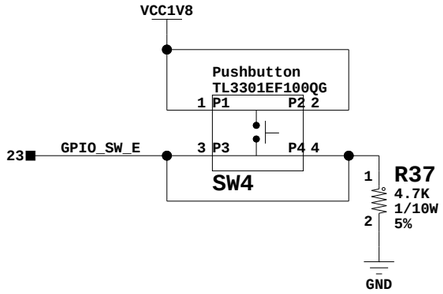
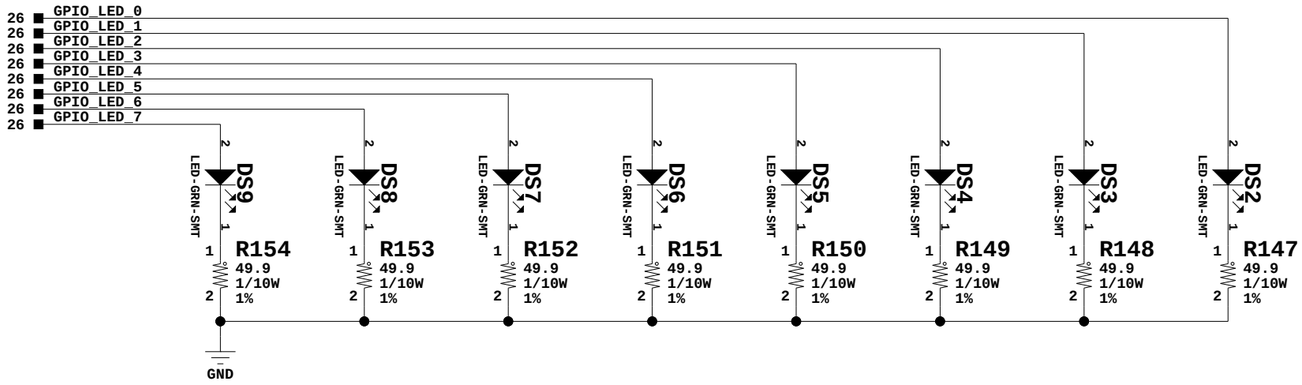


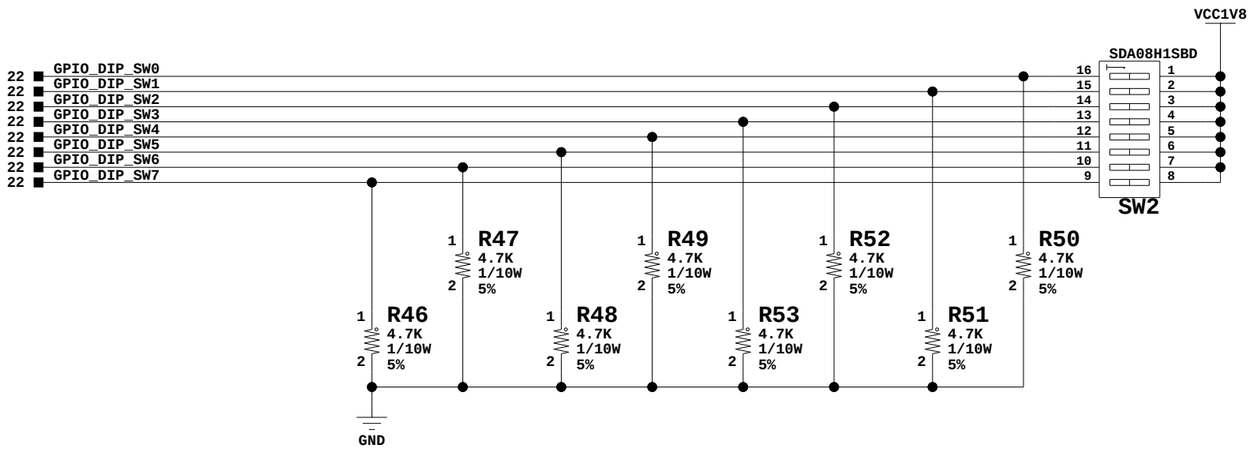


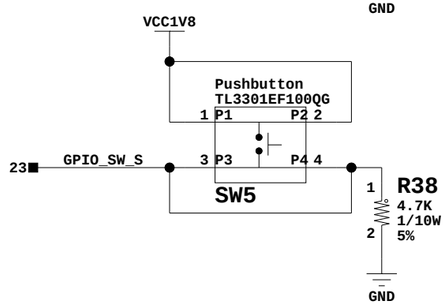


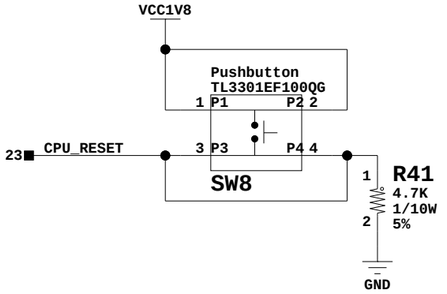


LEDs near top edge









Buttons, Switches, LEDs

XILINX		ASSY P/N: 0431748 PCB P/N: 1280666 SCH P/N: 0381499	
Title:	Buttons, Switches, LEDs, Rotary Encoder **SCHEM, ROHS COMPLIANT** **VC709 EVALUATION PLATFORM**		
Date:	9-19-2012_15:39	Ver:	1.0
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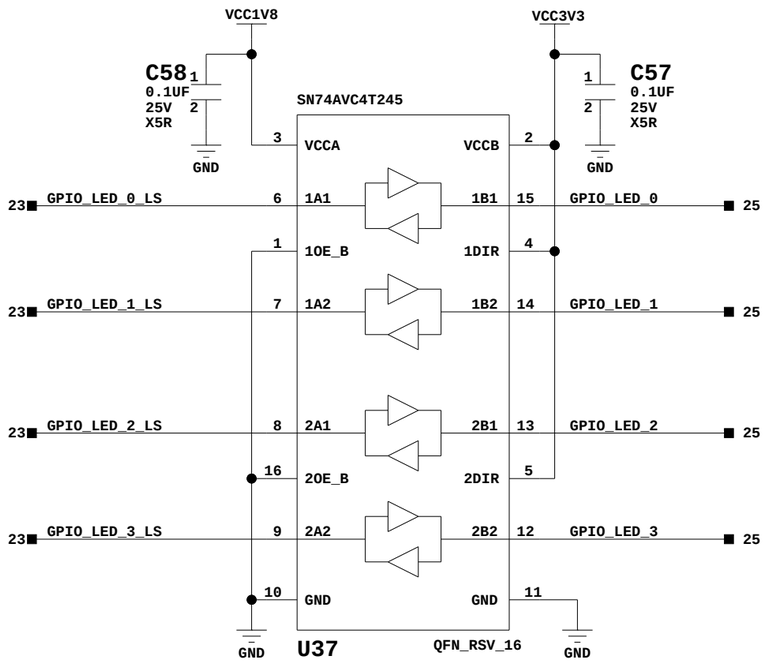

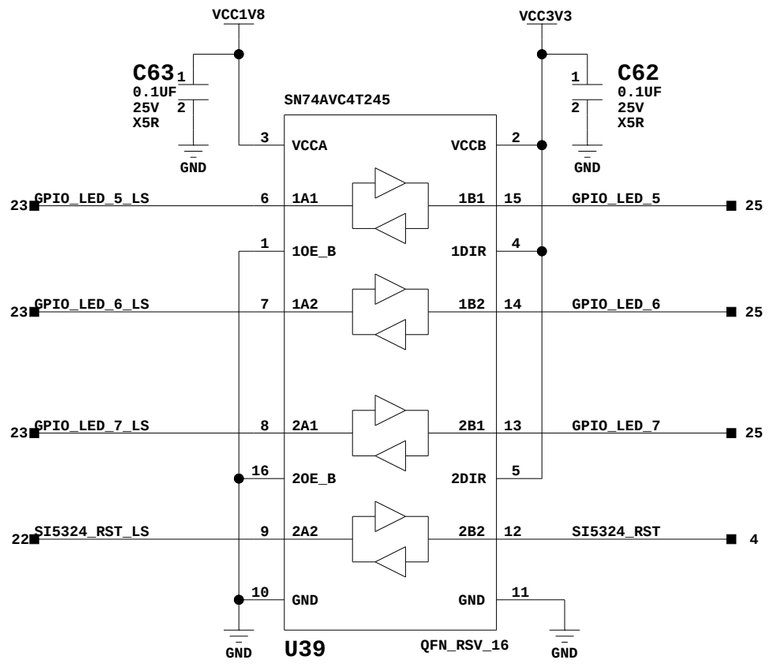

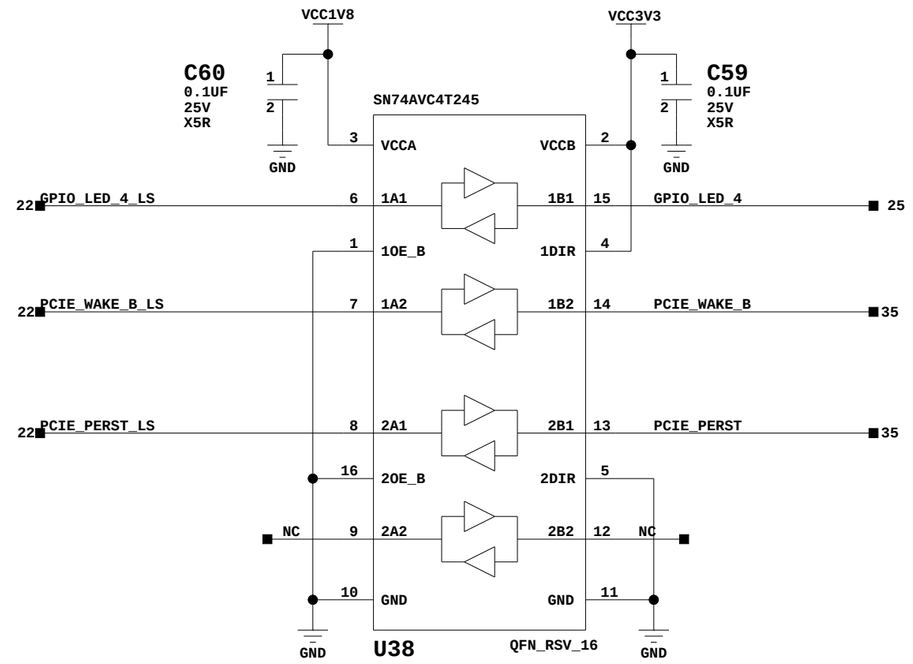

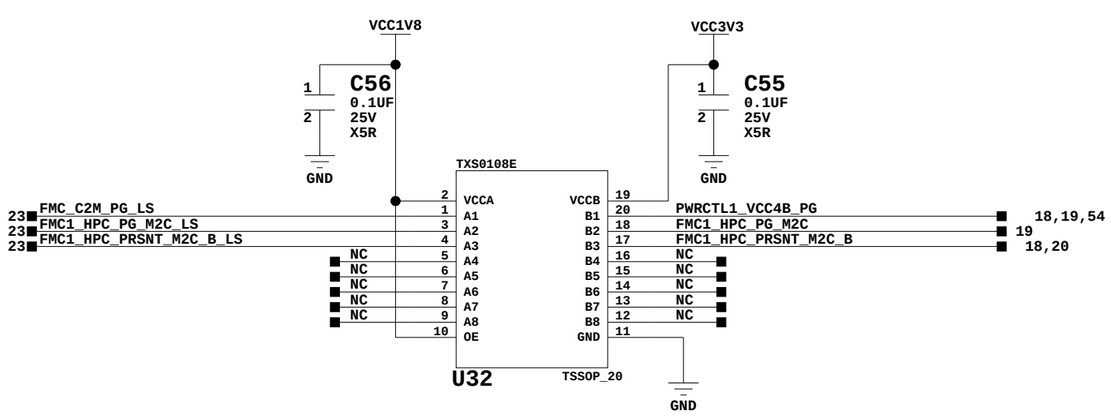

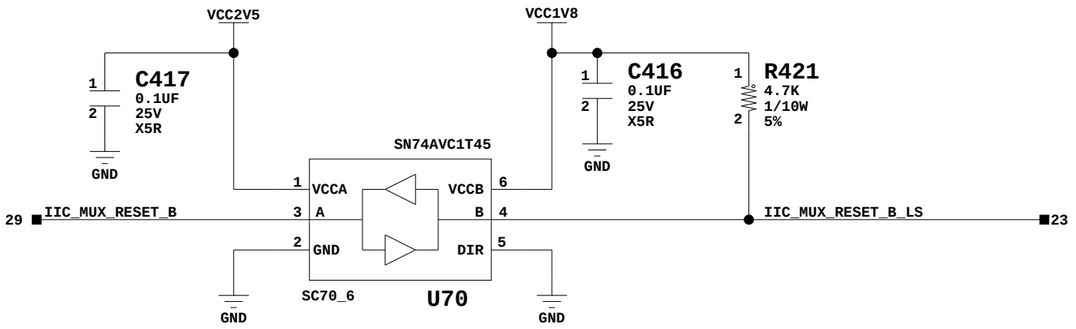

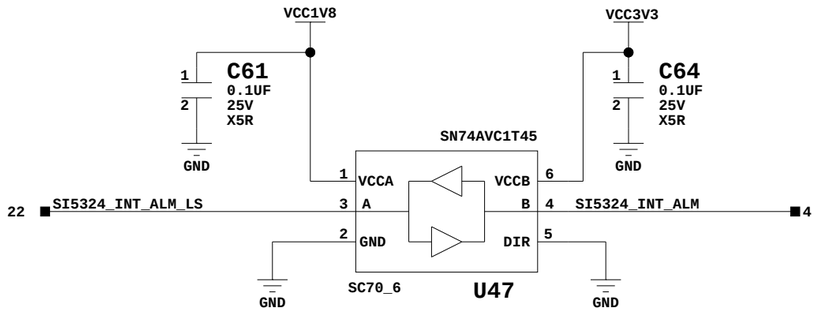

LCD, Level Shifters

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	LCD, Level Shifters SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-6-2012_11:50	Ver:	1.0
Sheet Size: B		Rev:	01
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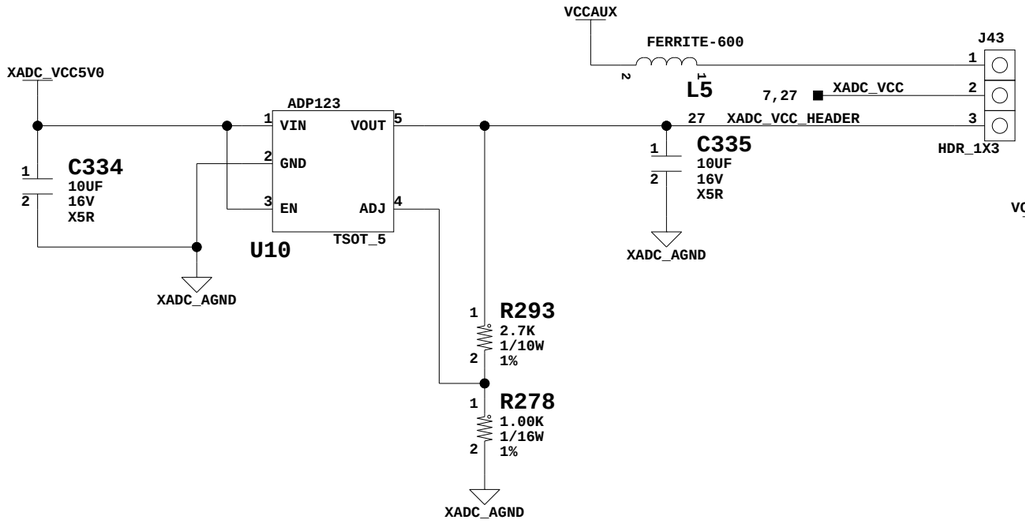

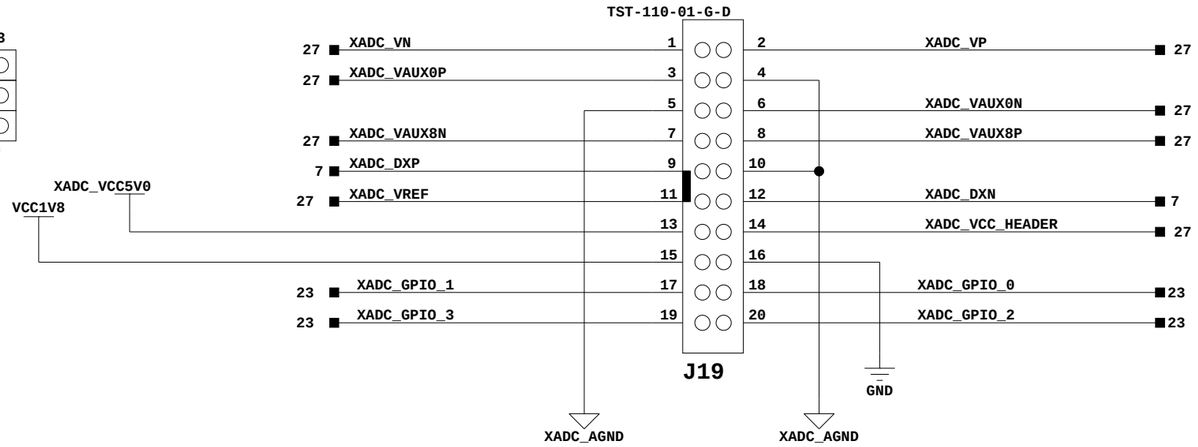

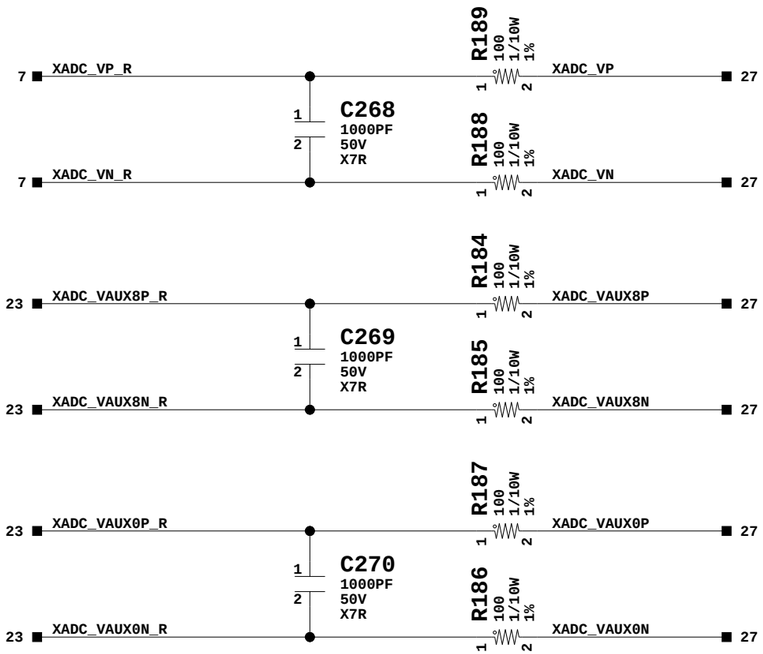

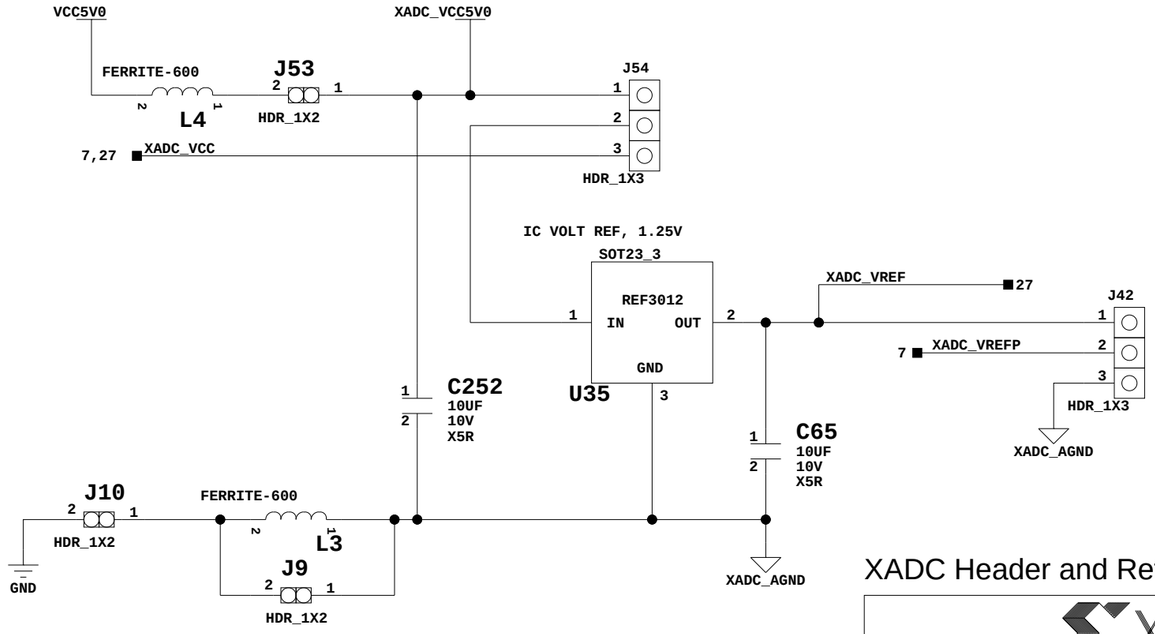

XADC Header and Reference

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	XADC Header and Reference SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-6-2012_11:50	Ver:	1.0
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XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Blank SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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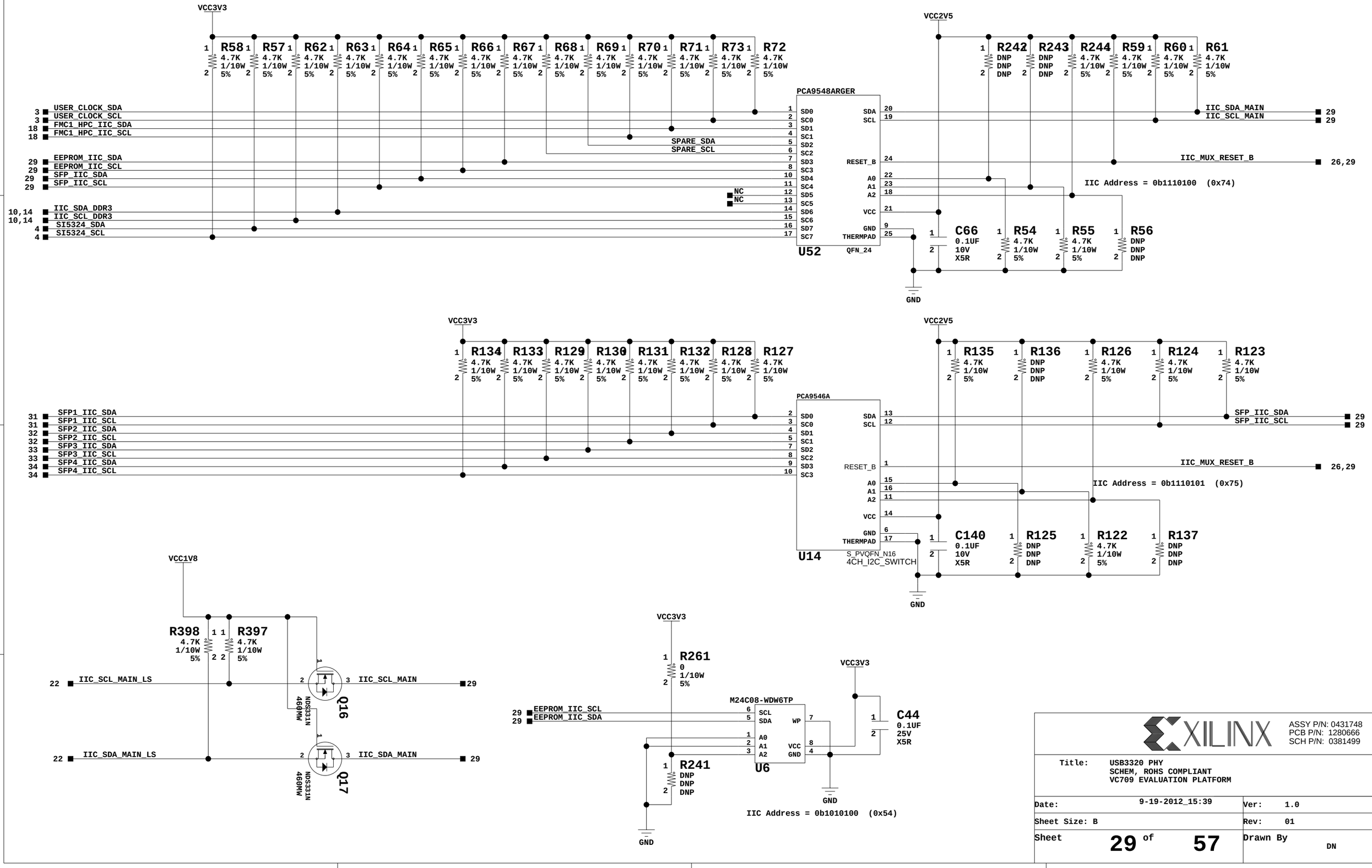

ASSY P/N:	0431748
PCB P/N:	1280666
SCH P/N:	0381499
Title:	USB3320 PHY SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM
Date:	9-19-2012_15:39
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Sheet Size:	B
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SOC_V7_690T_FF1761_IRON

BANK 17
XC7VX690TFFG1761

IO_0_VRN_17_Y38	Y38	SFP1_TX_FAULT_LS
IO_L1P_T0_17_AB41	AB41	SFP1_TX_DISABLE_LS_B
IO_L1N_T0_17_AB42	AB42	SFP1_MOD_DETECT_LS
IO_L2P_T0_17_W40	W40	SFP1_RS0_LS
IO_L2N_T0_17_Y40	Y40	SFP1_RS1_LS
IO_L3P_T0_DQS_17_Y39	Y39	SFP1_LOS_LS
IO_L3N_T0_DQS_17_AA39	AA39	SFP2_TX_FAULT_LS
IO_L4P_T0_17_Y42	Y42	SFP2_TX_DISABLE_LS_B
IO_L4N_T0_17_AA42	AA42	SFP2_MOD_DETECT_LS
IO_L5P_T0_17_AB38	AB38	SFP2_RS0_LS
IO_L5N_T0_17_AB39	AB39	SFP2_RS1_LS
IO_L6P_T0_17_AA40	AA40	SFP2_LOS_LS
IO_L6N_T0_VREF_17_AA41	AA41	SFP3_TX_FAULT_LS
IO_L7P_T1_17_AC38	AC38	SFP3_TX_DISABLE_LS_B
IO_L7N_T1_17_AC39	AC39	SFP3_MOD_DETECT_LS
IO_L8P_T1_17_AD42	AD42	SFP3_RS0_LS
IO_L8N_T1_17_AE42	AE42	SFP3_RS1_LS
IO_L9P_T1_DQS_17_AD38	AD38	SFP3_LOS_LS
IO_L9N_T1_DQS_17_AE38	AE38	SFP4_TX_FAULT_LS
IO_L10P_T1_17_AC40	AC40	SFP4_TX_DISABLE_LS_B
IO_L10N_T1_17_AC41	AC41	SFP4_MOD_DETECT_LS
IO_L11P_T1_SRCC_17_AE39	AE39	SFP4_RS0_LS
IO_L11N_T1_SRCC_17_AE40	AE40	SFP4_RS1_LS
IO_L12P_T1_MRCC_17_AD40	AD40	SFP4_LOS_LS
IO_L12N_T1_MRCC_17_AD41	AD41	NC
IO_L13P_T2_MRCC_17_AF39	AF39	NC
IO_L13N_T2_MRCC_17_AF40	AF40	NC
IO_L14P_T2_SRCC_17_AF41	AF41	NC
IO_L14N_T2_SRCC_17_AG41	AG41	NC
IO_L15P_T2_DQS_17_AG39	AG39	NC
IO_L15N_T2_DQS_17_AH39	AH39	NC
IO_L16P_T2_17_AF42	AF42	NC
IO_L16N_T2_17_AG42	AG42	NC
IO_L17P_T2_17_AG38	AG38	NC
IO_L17N_T2_17_AH38	AH38	NC
IO_L18P_T2_17_AJ38	AJ38	NC
IO_L18N_T2_17_AK38	AK38	NC
IO_L19P_T3_17_AK40	AK40	NC
IO_L19N_T3_VREF_17_AL40	AL40	NC
IO_L20P_T3_17_AH40	AH40	NC
IO_L20N_T3_17_AH41	AH41	NC
IO_L21P_T3_DQS_17_AL41	AL41	NC
IO_L21N_T3_DQS_17_AL42	AL42	NC
IO_L22P_T3_17_AJ40	AJ40	NC
IO_L22N_T3_17_AJ41	AJ41	NC
IO_L23P_T3_17_AK39	AK39	NC
IO_L23N_T3_17_AL39	AL39	NC
IO_L24P_T3_17_AJ42	AJ42	NC
IO_L24N_T3_17_AK42	AK42	NC
IO_25_VRP_17_AG37	AG37	NC

VCC1V8_FPGA		
AB40	VCCO_17_AB40	
AC37	VCCO_17_AC37	
AE41	VCCO_17_AE41	
AF38	VCCO_17_AF38	
AH42	VCCO_17_AH42	
AJ39	VCCO_17_AJ39	

U1 SOC_IRON_690T_FF1761

Note: SFPx_TX_DISABLE_LS_B is not named correctly, SFP TX is disabled when HIGH

SOC_V7_690T_FF1761_IRON

BANK 113
XC7VX690TFFG1761

MGTHTXP0_113_AP4	AP4	SFP1_TX_P
MGTHTXN0_113_AP3	AP3	SFP1_TX_N
MGTHRXP0_113_AN6	AN6	SFP1_RX_P
MGTHRXN0_113_AN5	AN5	SFP1_RX_N
MGTHTXP1_113_AN2	AN2	SFP2_TX_P
MGTHTXN1_113_AN1	AN1	SFP2_TX_N
MGTHRXP1_113_AM8	AM8	SFP2_RX_P
MGTHRXN1_113_AM7	AM7	SFP2_RX_N
MGTHTXP2_113_AM4	AM4	SFP3_TX_P
MGTHTXN2_113_AM3	AM3	SFP3_TX_N
MGTHRXP2_113_AL6	AL6	SFP3_RX_P
MGTHRXN2_113_AL5	AL5	SFP3_RX_N
MGTHTXP3_113_AL2	AL2	SFP4_TX_P
MGTHTXN3_113_AL1	AL1	SFP4_TX_N
MGTHRXP3_113_AJ6	AJ6	SFP4_RX_P
MGTHRXN3_113_AJ5	AJ5	SFP4_RX_N
MGTREFCLK0P_113_AH8	AH8	SI5324_OUT_C_P
MGTREFCLK0N_113_AH7	AH7	SI5324_OUT_C_N
MGTREFCLK1P_113_AK8	AK8	SMA_MGT_REFCLK_P
MGTREFCLK1N_113_AK7	AK7	SMA_MGT_REFCLK_N

U1 SOC_IRON_690T_FF1761

J25: GND1 (2), GND2 (3), SIG (1) SMA_MGT_REFCLK_C_P, GND3 (4), GND4 (5) — 32K10K-400L5

C25 0.1UF 25V X5R: SMA_MGT_REFCLK_C_P → SMA_MGT_REFCLK_P → 30

J26: GND1 (2), GND2 (3), SIG (1) SMA_MGT_REFCLK_C_N, GND3 (4), GND4 (5) — 32K10K-400L5

C24 0.1UF 25V X5R: SMA_MGT_REFCLK_C_N → SMA_MGT_REFCLK_N → 30

GND

VCC1V8_FPGA

C402 100UF 6.3 X5R

GND

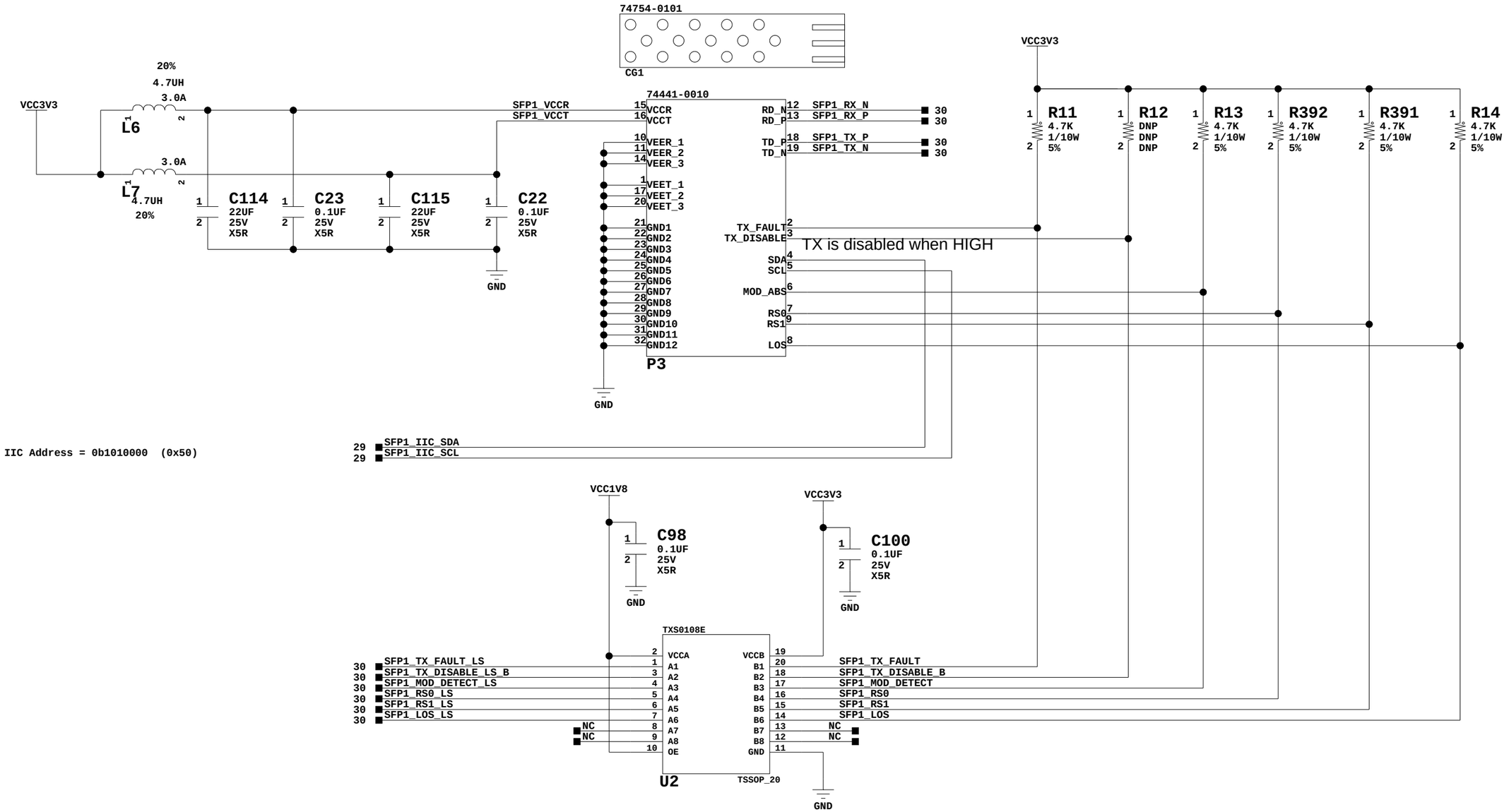
FPGA Bank 17

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: DISCLAIMER
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	30 of 57	Drawn By	DN



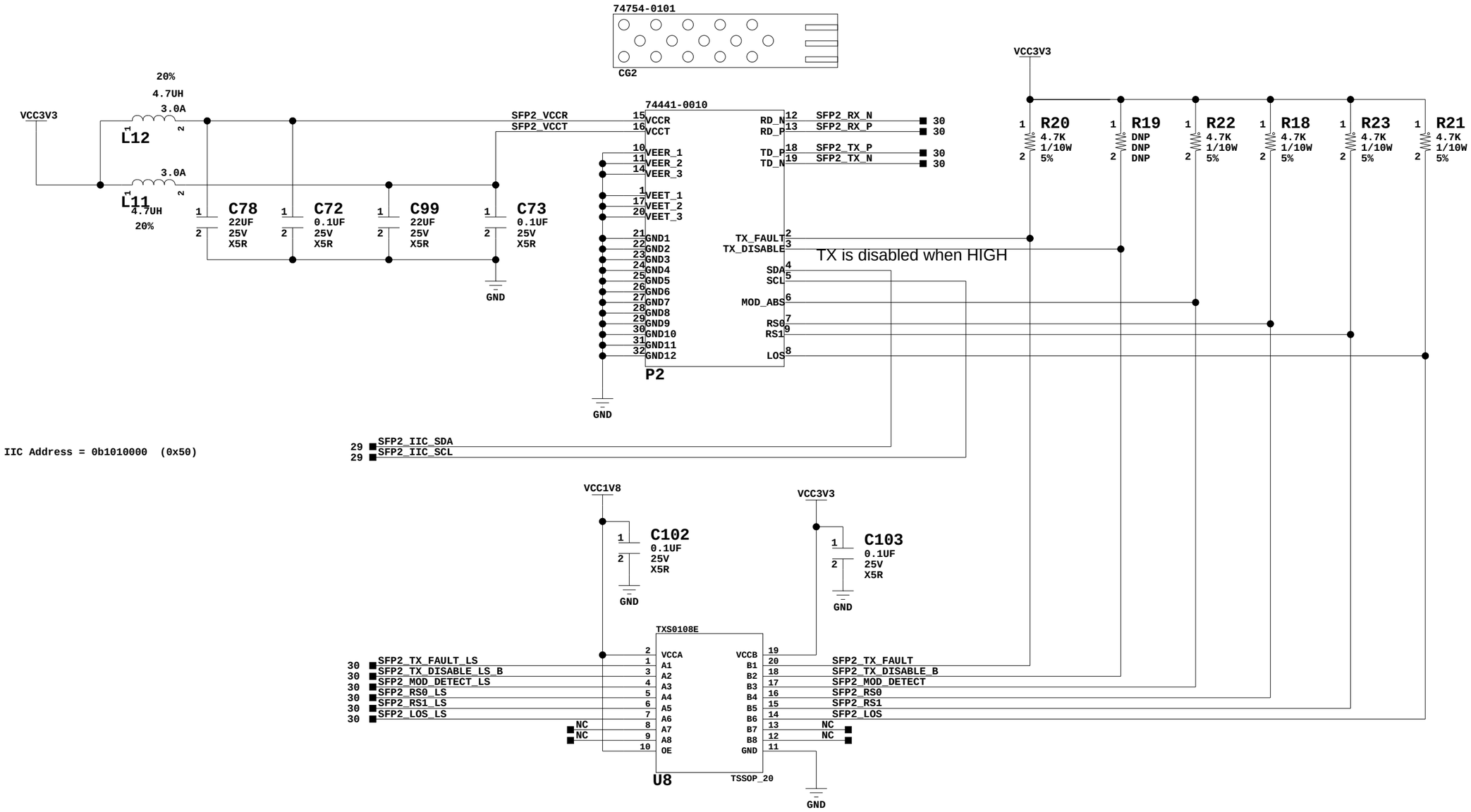
SFP+ Connector#1 and Cage

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: SFP+ Connector and Cage
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-6-2012_11:50	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	31 of 57	Drawn By	DN

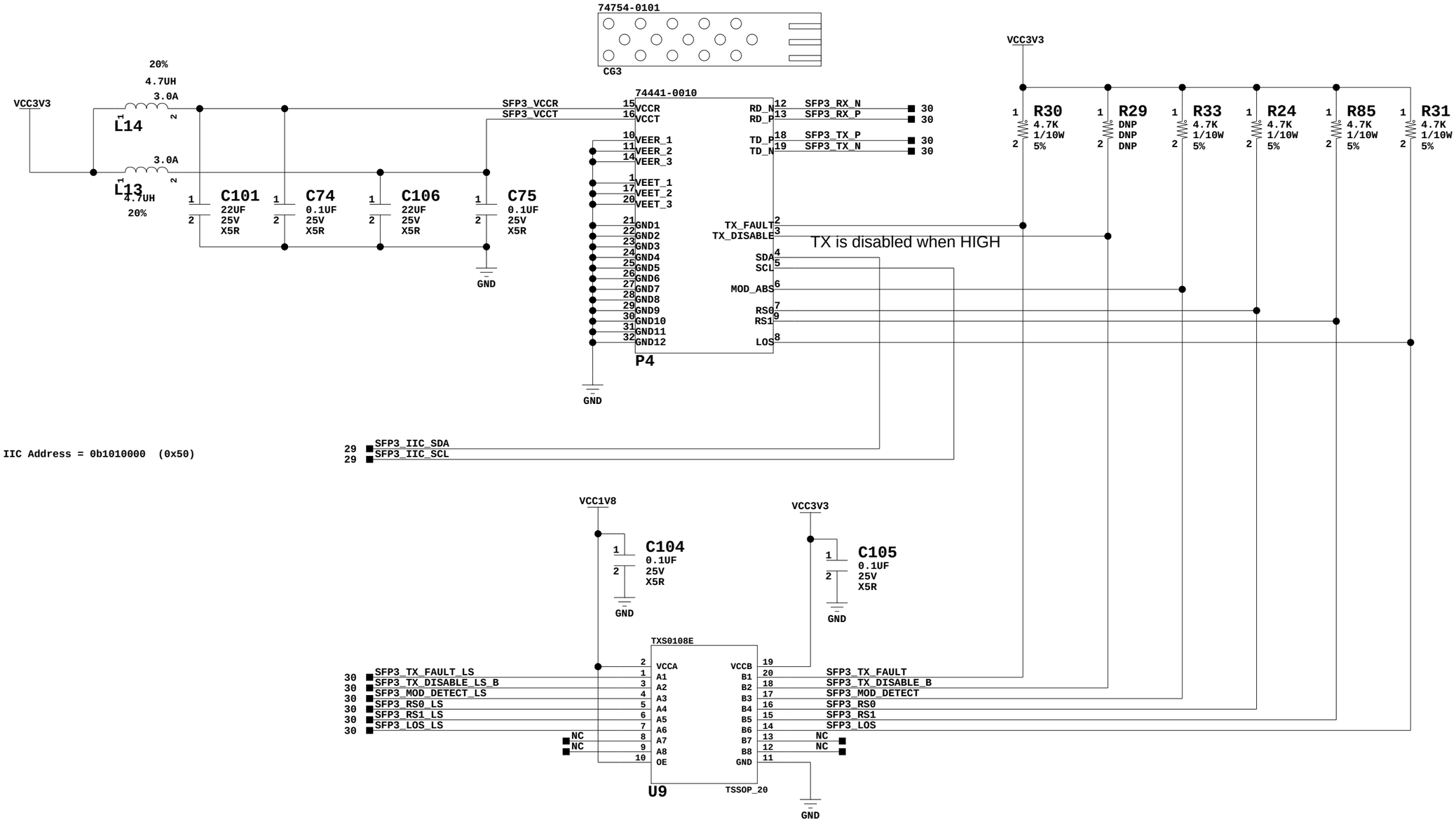


SFP+ Connector#2 and Cage

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FMC 2 HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-6-2012_11:50	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	32 of 57	Drawn By	DN



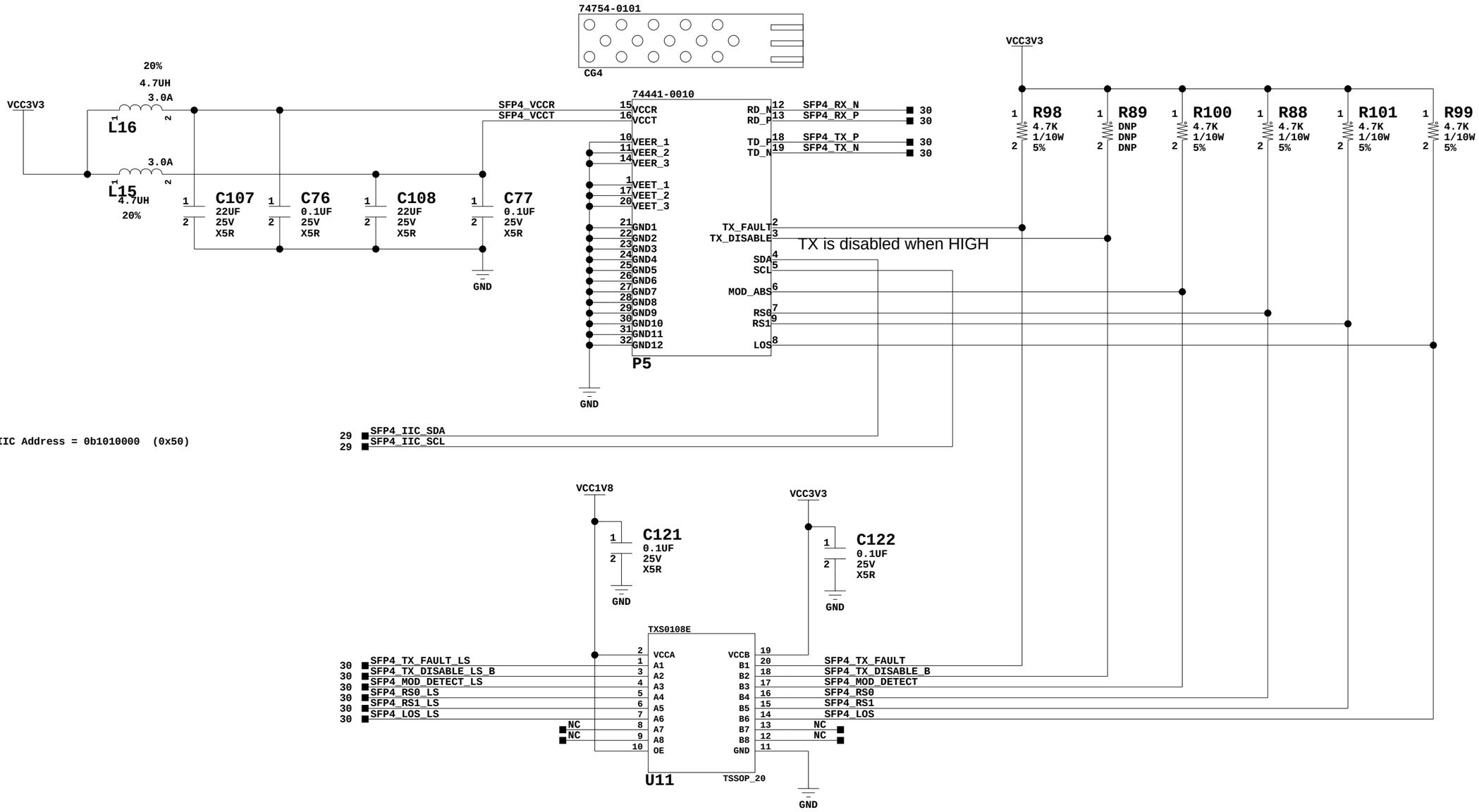
SFP+ Connector#3 and Cage

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

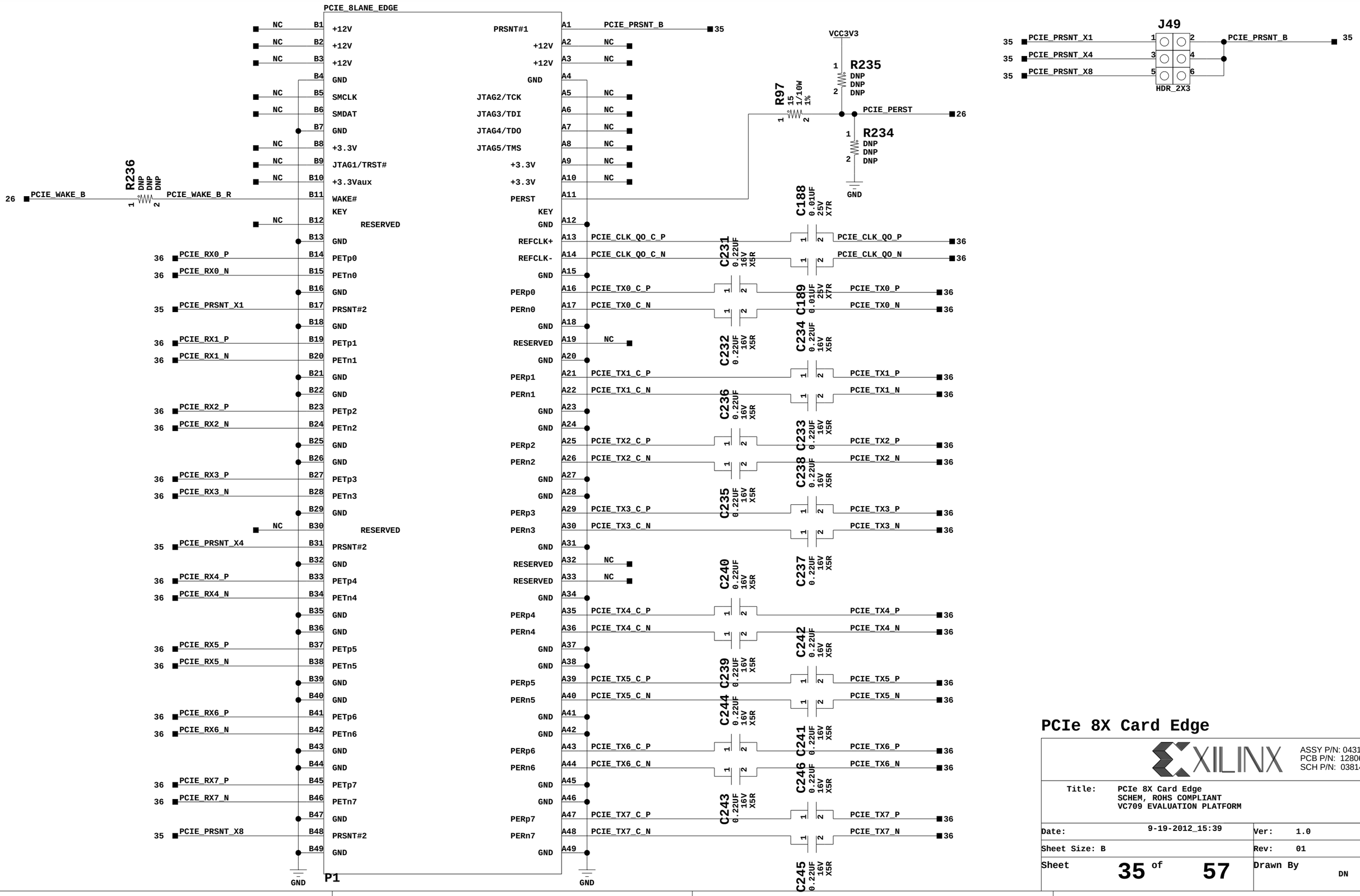
Title: FMC 2 HPC Header, Rows H, J, K
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-6-2012_11:50	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	33 of 57	Drawn By	DN



SFP+ Connector#4 and Cage

XILINX	ASSY P/N: 0431748 PCB P/N: 1280666 SCH P/N: 0381499
Title:	FMC 2 HPC Header, GND SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM
Date: 12-6-2012_11:50	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 34 of 57	Drawn By DN



PCIe 8X Card Edge

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	PCIe 8X Card Edge SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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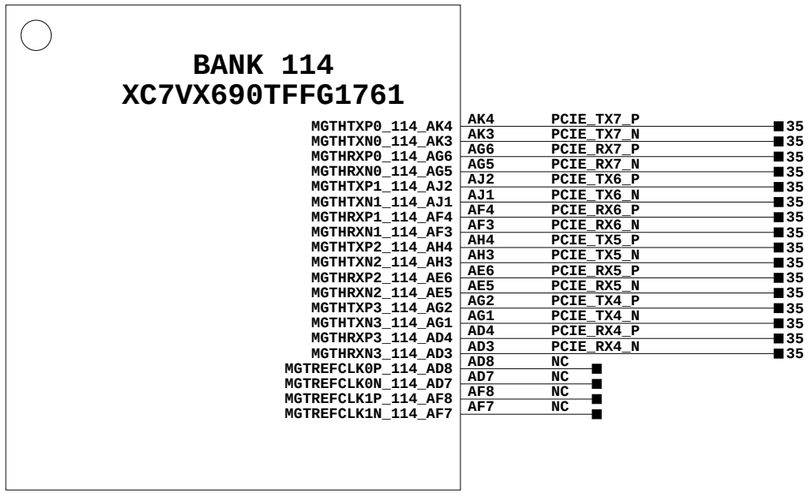
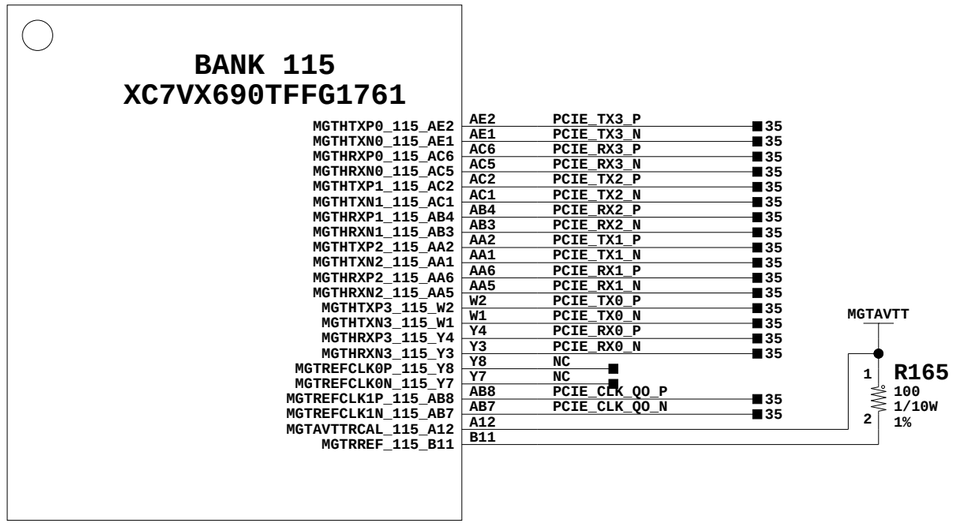
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

FPGA GT Banks 113, 114

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA GT Banks 113, 114 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 118
XC7VX690TFFG1761

MGTHTXP0_118_J2	J2	FMC1_HPC_DP4_C2M_P	18
MGTHTXN0_118_J1	J1	FMC1_HPC_DP4_C2M_N	18
MGTHRXP0_118_H8	H8	FMC1_HPC_DP4_M2C_P	18
MGTHRXN0_118_H7	H7	FMC1_HPC_DP4_M2C_N	18
MGTHTXP1_118_H4	H4	FMC1_HPC_DP5_C2M_P	18
MGTHTXN1_118_H3	H3	FMC1_HPC_DP5_C2M_N	18
MGTHRXP1_118_G6	G6	FMC1_HPC_DP5_M2C_P	18
MGTHRXN1_118_G5	G5	FMC1_HPC_DP5_M2C_N	18
MGTHTXP2_118_G2	G2	FMC1_HPC_DP6_C2M_P	18
MGTHTXN2_118_G1	G1	FMC1_HPC_DP6_C2M_N	18
MGTHRXP2_118_F8	F8	FMC1_HPC_DP6_M2C_P	18
MGTHRXN2_118_F7	F7	FMC1_HPC_DP6_M2C_N	18
MGTHTXP3_118_F4	F4	FMC1_HPC_DP7_C2M_P	18
MGTHTXN3_118_F3	F3	FMC1_HPC_DP7_C2M_N	18
MGTHRXP3_118_E6	E6	FMC1_HPC_DP7_M2C_P	18
MGTHRXN3_118_E5	E5	FMC1_HPC_DP7_M2C_N	18
MGTREFCLK0P_118_E10	E10	FMC1_HPC_GBTCLK1_M2C_C_P	37
MGTREFCLK0N_118_E9	E9	FMC1_HPC_GBTCLK1_M2C_C_N	37
MGTREFCLK1P_118_G10	G10	FMC1_HPC_GBTCLK0_M2C_C_P	37
MGTREFCLK1N_118_G9	G9	FMC1_HPC_GBTCLK0_M2C_C_N	37

U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 119
XC7VX690TFFG1761

MGTHTXP0_119_E2	E2	FMC1_HPC_DP0_C2M_P	18
MGTHTXN0_119_E1	E1	FMC1_HPC_DP0_C2M_N	18
MGTHRXP0_119_D8	D8	FMC1_HPC_DP0_M2C_P	18
MGTHRXN0_119_D7	D7	FMC1_HPC_DP0_M2C_N	18
MGTHTXP1_119_D4	D4	FMC1_HPC_DP1_C2M_P	18
MGTHTXN1_119_D3	D3	FMC1_HPC_DP1_C2M_N	18
MGTHRXP1_119_C6	C6	FMC1_HPC_DP1_M2C_P	18
MGTHRXN1_119_C5	C5	FMC1_HPC_DP1_M2C_N	18
MGTHTXP2_119_C2	C2	FMC1_HPC_DP2_C2M_P	18
MGTHTXN2_119_C1	C1	FMC1_HPC_DP2_C2M_N	18
MGTHRXP2_119_B8	B8	FMC1_HPC_DP2_M2C_P	18
MGTHRXN2_119_B7	B7	FMC1_HPC_DP2_M2C_N	18
MGTHTXP3_119_B4	B4	FMC1_HPC_DP3_C2M_P	18
MGTHTXN3_119_B3	B3	FMC1_HPC_DP3_C2M_N	18
MGTHRXP3_119_A6	A6	FMC1_HPC_DP3_M2C_P	18
MGTHRXN3_119_A5	A5	FMC1_HPC_DP3_M2C_N	18
MGTREFCLK0P_119_A10	A10	NC	
MGTREFCLK0N_119_A9	A9	NC	
MGTREFCLK1P_119_C10	C10	NC	
MGTREFCLK1N_119_C9	C9	NC	

U1

SOC_IRON_690T_FF1761

C393 0.1UF 25V X5R

18 FMC1_HPC_GBTCLK1_M2C_P — FMC1_HPC_GBTCLK1_M2C_C_P 37

18 FMC1_HPC_GBTCLK1_M2C_N — FMC1_HPC_GBTCLK1_M2C_C_N 37

C394 0.1UF 25V X5R

C6 0.1UF 25V X5R

18 FMC1_HPC_GBTCLK0_M2C_P — FMC1_HPC_GBTCLK0_M2C_C_P 37

18 FMC1_HPC_GBTCLK0_M2C_N — FMC1_HPC_GBTCLK0_M2C_C_N 37

C5 0.1UF 25V X5R

SOC_V7_690T_FF1761_IRON

BANK 117
XC7VX690TFFG1761

MGTHTXP0_117_N2	N2	FMC1_HPC_DP8_C2M_P	18
MGTHTXN0_117_N1	N1	FMC1_HPC_DP8_C2M_N	18
MGTHRXP0_117_P8	P8	FMC1_HPC_DP8_M2C_P	18
MGTHRXN0_117_P7	P7	FMC1_HPC_DP8_M2C_N	18
MGTHTXP1_117_M4	M4	FMC1_HPC_DP9_C2M_P	18
MGTHTXN1_117_M3	M3	FMC1_HPC_DP9_C2M_N	18
MGTHRXP1_117_N6	N6	FMC1_HPC_DP9_M2C_P	18
MGTHRXN1_117_N5	N5	FMC1_HPC_DP9_M2C_N	18
MGTHTXP2_117_L2	L2	NC	
MGTHTXN2_117_L1	L1	NC	
MGTHRXP2_117_L6	L6	NC	
MGTHRXN2_117_L5	L5	NC	
MGTHTXP3_117_K4	K4	NC	
MGTHTXN3_117_K3	K3	NC	
MGTHRXP3_117_J6	J6	NC	
MGTHRXN3_117_J5	J5	NC	
MGTREFCLK0P_117_K8	K8	NC	
MGTREFCLK0N_117_K7	K7	NC	
MGTREFCLK1P_117_M8	M8	NC	
MGTREFCLK1N_117_M7	M7	NC	

U1

SOC_IRON_690T_FF1761

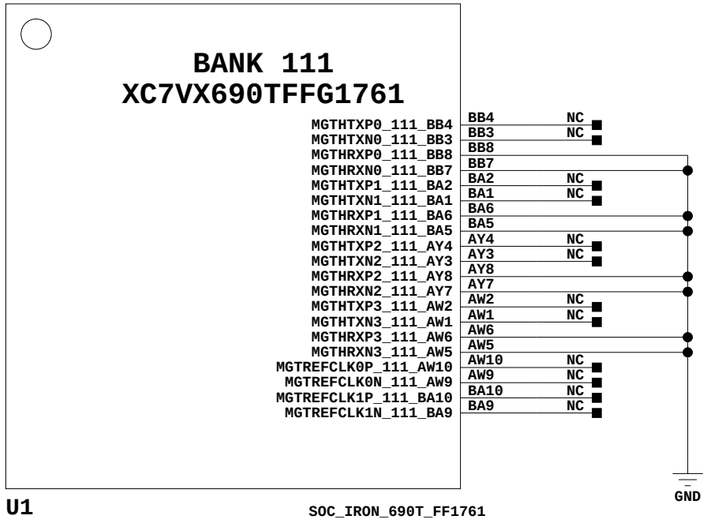
FPGA GT Banks 117, 118, 119

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA GT Banks 117, 118, 119 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	37 of 57	Drawn By	DN

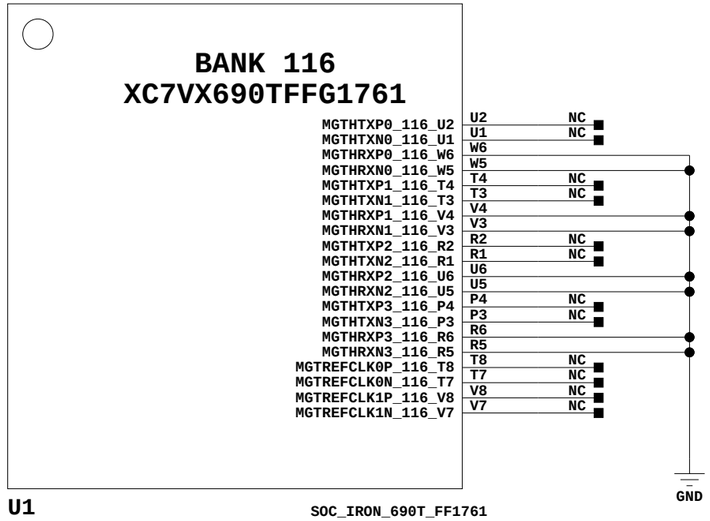
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

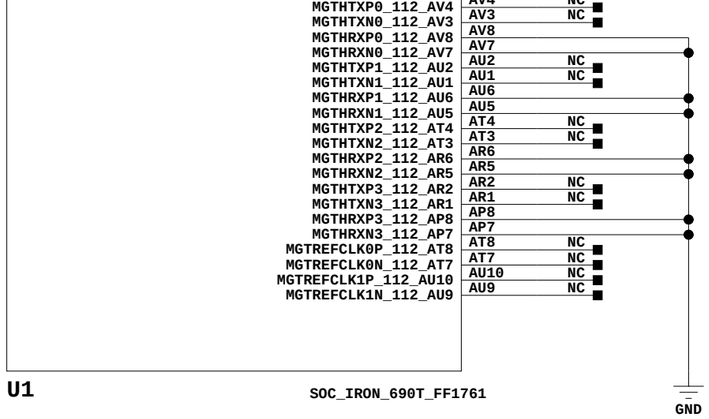
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

FPGA Bank 31, GT Banks 111, 112

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA Bank 31, GT Banks 111, 112 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
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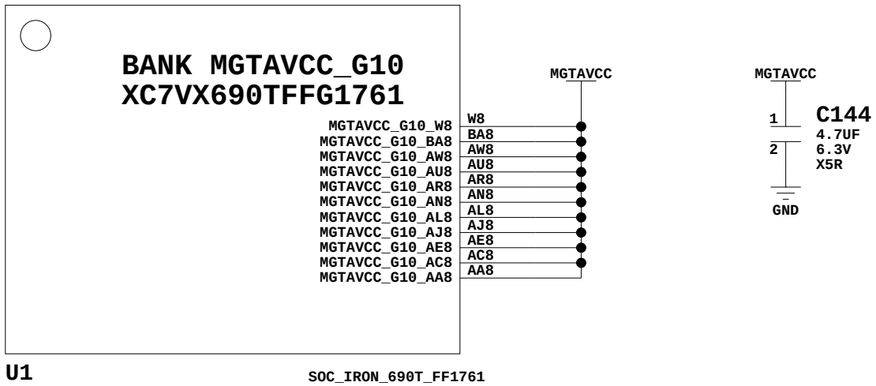
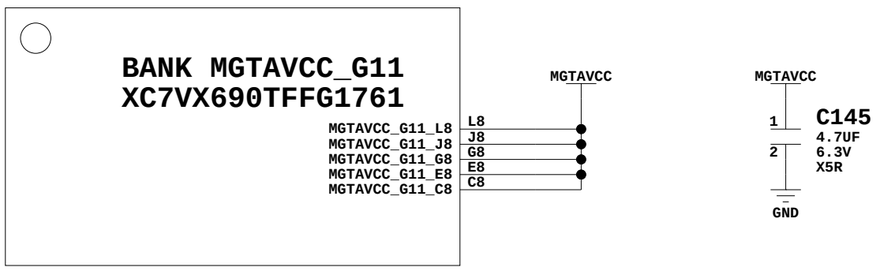
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

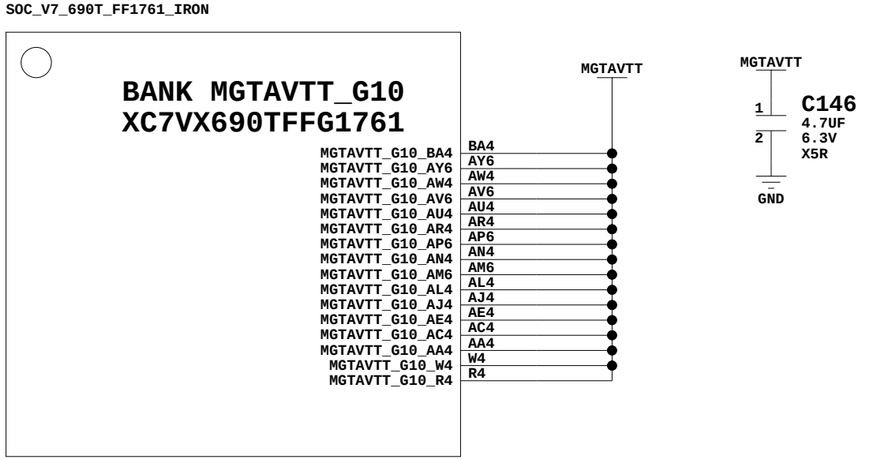
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

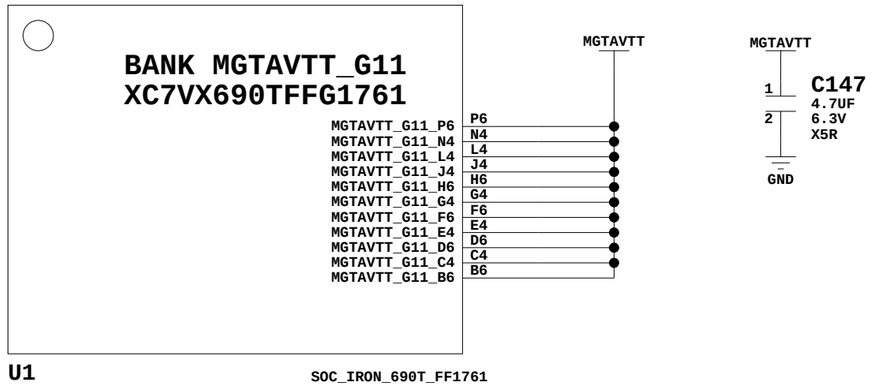
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

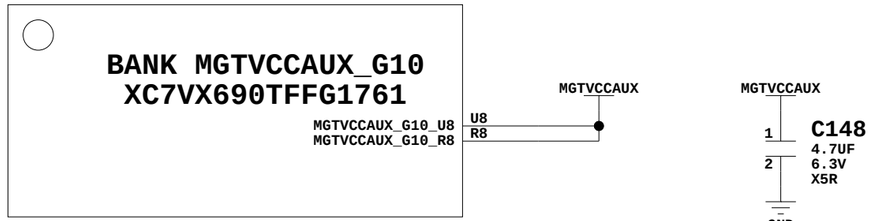
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

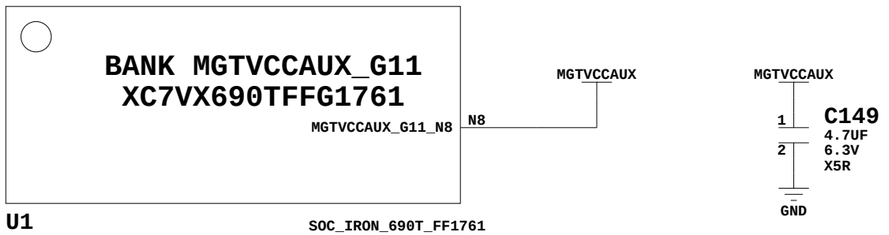
SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON



U1

SOC_IRON_690T_FF1761

FPGA Power Pins

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Power Pins
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	12-21-2012_13:14	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_V7_690T_FF1761_IRON

BANK 12
XC7VX690TFFG1761

IO_0_VRN_12_AN29	AN29	NC
IO_L1P_T0_12_AY27	AY27	NC
IO_L1N_T0_12_AY28	AY28	NC
IO_L2P_T0_12_AU29	AU29	NC
IO_L2N_T0_12_AV29	AV29	NC
IO_L3P_T0_DQS_12_BA26	BA26	NC
IO_L3N_T0_DQS_12_BA27	BA27	NC
IO_L4P_T0_12_BB28	BB28	NC
IO_L4N_T0_12_BB29	BB29	NC
IO_L5P_T0_12_BB26	BB26	NC
IO_L5N_T0_12_BB27	BB27	NC
IO_L6P_T0_12_AY29	AY29	NC
IO_L6N_T0_VREF_12_BA29	BA29	NC
IO_L7P_T1_12_AW25	AW25	NC
IO_L7N_T1_12_AW26	AW26	NC
IO_L8P_T1_12_AR29	AR29	NC
IO_L8N_T1_12_AT29	AT29	NC
IO_L9P_T1_DQS_12_AV25	AV25	NC
IO_L9N_T1_DQS_12_AV26	AV26	NC
IO_L10P_T1_12_AW27	AW27	NC
IO_L10N_T1_12_AW28	AW28	NC
IO_L11P_T1_SRCC_12_AU28	AU28	NC
IO_L11N_T1_SRCC_12_AV28	AV28	NC
IO_L12P_T1_MRCC_12_AU26	AU26	NC
IO_L12N_T1_MRCC_12_AU27	AU27	NC
IO_L13P_T2_MRCC_12_AR27	AR27	NC
IO_L13N_T2_MRCC_12_AT27	AT27	NC
IO_L14P_T2_SRCC_12_AP27	AP27	NC
IO_L14N_T2_SRCC_12_AR28	AR28	NC
IO_L15P_T2_DQS_12_AN28	AN28	NC
IO_L15N_T2_DQS_12_AP28	AP28	NC
IO_L16P_T2_12_AT25	AT25	NC
IO_L16N_T2_12_AT26	AT26	NC
IO_L17P_T2_12_AP25	AP25	NC
IO_L17N_T2_12_AR25	AR25	NC
IO_L18P_T2_12_AN25	AN25	NC
IO_L18N_T2_12_AN26	AN26	NC
IO_L19P_T3_12_AM28	AM28	NC
IO_L19N_T3_VREF_12_AM29	AM29	NC
IO_L20P_T3_12_AK27	AK27	NC
IO_L20N_T3_12_AL27	AL27	NC
IO_L21P_T3_DQS_12_AM26	AM26	NC
IO_L21N_T3_DQS_12_AM27	AM27	NC
IO_L22P_T3_12_AK24	AK24	NC
IO_L22N_T3_12_AK25	AK25	NC
IO_L23P_T3_12_AL25	AL25	NC
IO_L23N_T3_12_AL26	AL26	NC
IO_L24P_T3_12_AJ25	AJ25	NC
IO_L24N_T3_12_AJ26	AJ26	NC
IO_25_VRP_12_AP26	AP26	NC

VCC1V8_FPGA

AK26	VCCO_12_AK26
AN27	VCCO_12_AN27
AT28	VCCO_12_AT28
AU25	VCCO_12_AU25
AW29	VCCO_12_AW29
AY26	VCCO_12_AY26

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK 16
XC7VX690TFFG1761

IO_0_VRN_16_Y34	Y34	NC
IO_L1P_T0_16_AF35	AF35	NC
IO_L1N_T0_16_AF36	AF36	NC
IO_L2P_T0_16_AE37	AE37	NC
IO_L2N_T0_16_AF37	AF37	NC
IO_L3P_T0_DQS_16_AF34	AF34	NC
IO_L3N_T0_DQS_16_AG34	AG34	NC
IO_L4P_T0_16_AD36	AD36	NC
IO_L4N_T0_16_AD37	AD37	NC
IO_L5P_T0_16_AC35	AC35	NC
IO_L5N_T0_16_AC36	AC36	NC
IO_L6P_T0_16_AG36	AG36	NC
IO_L6N_T0_VREF_16_AH36	AH36	NC
IO_L7P_T1_16_Y37	Y37	NC
IO_L7N_T1_16_AA37	AA37	NC
IO_L8P_T1_16_Y35	Y35	NC
IO_L8N_T1_16_AA36	AA36	NC
IO_L9P_T1_DQS_16_AB36	AB36	NC
IO_L9N_T1_DQS_16_AB37	AB37	NC
IO_L10P_T1_16_AA34	AA34	NC
IO_L10N_T1_16_AA35	AA35	NC
IO_L11P_T1_SRCC_16_AB31	AB31	NC
IO_L11N_T1_SRCC_16_AB32	AB32	NC
IO_L12P_T1_MRCC_16_AB33	AB33	NC
IO_L12N_T1_MRCC_16_AC33	AC33	NC
IO_L13P_T2_MRCC_16_AD32	AD32	NC
IO_L13N_T2_MRCC_16_AD33	AD33	NC
IO_L14P_T2_SRCC_16_AC34	AC34	NC
IO_L14N_T2_SRCC_16_AD35	AD35	NC
IO_L15P_T2_DQS_16_AE32	AE32	NC
IO_L15N_T2_DQS_16_AE33	AE33	NC
IO_L16P_T2_16_AF31	AF31	NC
IO_L16N_T2_16_AF32	AF32	NC
IO_L17P_T2_16_AE34	AE34	NC
IO_L17N_T2_16_AE35	AE35	NC
IO_L18P_T2_16_AE29	AE29	NC
IO_L18N_T2_16_AE30	AE30	NC
IO_L19P_T3_16_Y32	Y32	NC
IO_L19N_T3_VREF_16_Y33	Y33	NC
IO_L20P_T3_16_AC31	AC31	NC
IO_L20N_T3_16_AD31	AD31	NC
IO_L21P_T3_DQS_16_AA31	AA31	NC
IO_L21N_T3_DQS_16_AA32	AA32	NC
IO_L22P_T3_16_AC30	AC30	NC
IO_L22N_T3_16_AD30	AD30	NC
IO_L23P_T3_16_AA29	AA29	NC
IO_L23N_T3_16_AA30	AA30	NC
IO_L24P_T3_16_AB29	AB29	NC
IO_L24N_T3_16_AC29	AC29	NC
IO_25_VRP_16_AB34	AB34	NC

VCC1V8_FPGA

AA33	VCCO_16_AA33
AB30	VCCO_16_AB30
AD34	VCCO_16_AD34
AE31	VCCO_16_AE31
AG35	VCCO_16_AG35
Y36	VCCO_16_Y36

U1 SOC_IRON_690T_FF1761

FPGA Banks 12, 16

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: HDMI CONNECTOR
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

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SOC_V7_690T_FF1761_IRON

BANK 18
XC7VX690TFFG1761

IO_0_VRN_18_N35	N35	NC
IO_L1P_T0_18_T34	T34	NC
IO_L1N_T0_18_R35	R35	NC
IO_L2P_T0_18_N33	N33	NC
IO_L2N_T0_18_N34	N34	NC
IO_L3P_T0_DQS_18_R33	R33	NC
IO_L3N_T0_DQS_18_R34	R34	NC
IO_L4P_T0_18_P35	P35	NC
IO_L4N_T0_18_P36	P36	NC
IO_L5P_T0_18_T32	T32	NC
IO_L5N_T0_18_R32	R32	NC
IO_L6P_T0_18_P32	P32	NC
IO_L6N_T0_VREF_18_P33	P33	NC
IO_L7P_T1_18_T36	T36	NC
IO_L7N_T1_18_R37	R37	NC
IO_L8P_T1_18_P37	P37	NC
IO_L8N_T1_18_P38	P38	NC
IO_L9P_T1_DQS_18_U34	U34	NC
IO_L9N_T1_DQS_18_T35	T35	NC
IO_L10P_T1_18_R38	R38	NC
IO_L10N_T1_18_R39	R39	NC
IO_L11P_T1_SRCC_18_U37	U37	NC
IO_L11N_T1_SRCC_18_U38	U38	NC
IO_L12P_T1_MRCC_18_U39	U39	NC
IO_L12N_T1_MRCC_18_T39	T39	NC
IO_L13P_T2_MRCC_18_U36	U36	NC
IO_L13N_T2_MRCC_18_T37	T37	NC
IO_L14P_T2_SRCC_18_V35	V35	NC
IO_L14N_T2_SRCC_18_V36	V36	NC
IO_L15P_T2_DQS_18_V33	V33	NC
IO_L15N_T2_DQS_18_V34	V34	NC
IO_L16P_T2_18_W36	W36	NC
IO_L16N_T2_18_W37	W37	NC
IO_L17P_T2_18_U32	U32	NC
IO_L17N_T2_18_U33	U33	NC
IO_L18P_T2_18_W32	W32	NC
IO_L18N_T2_18_W33	W33	NC
IO_L19P_T3_18_V39	V39	NC
IO_L19N_T3_VREF_18_V40	V40	NC
IO_L20P_T3_18_T40	T40	NC
IO_L20N_T3_18_T41	T41	NC
IO_L21P_T3_DQS_18_W41	W41	NC
IO_L21N_T3_DQS_18_W42	W42	NC
IO_L22P_T3_18_U41	U41	NC
IO_L22N_T3_18_T42	T42	NC
IO_L23P_T3_18_W38	W38	NC
IO_L23N_T3_18_V38	V38	NC
IO_L24P_T3_18_V41	V41	NC
IO_L24N_T3_18_U42	U42	NC
IO_25_VRP_18_W35	W35	NC

VCC1V8_FPGA

P34	VCCO_18_P34
T38	VCCO_18_T38
U35	VCCO_18_U35
V32	VCCO_18_V32
V42	VCCO_18_V42
W39	VCCO_18_W39

U1

SOC_IRON_690T_FF1761

FPGA Bank 18

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Banks 16, 17
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

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SOC_V7_690T_FF1761_IRON

BANK VCCINT
XC7VX690TFFG1761

VCCINT_FPGA

VCCINT_Y27	Y27
VCCINT_Y23	Y23
VCCINT_Y19	Y19
VCCINT_Y15	Y15
VCCINT_Y13	Y13
VCCINT_Y11	Y11
VCCINT_W28	W28
VCCINT_W24	W24
VCCINT_W20	W20
VCCINT_W16	W16
VCCINT_W14	W14
VCCINT_W12	W12
VCCINT_V27	V27
VCCINT_V23	V23
VCCINT_V21	V21
VCCINT_V19	V19
VCCINT_V15	V15
VCCINT_V13	V13
VCCINT_V11	V11
VCCINT_U24	U24
VCCINT_U20	U20
VCCINT_U16	U16
VCCINT_U14	U14
VCCINT_U12	U12
VCCINT_T27	T27
VCCINT_T23	T23
VCCINT_T21	T21
VCCINT_T15	T15
VCCINT_T13	T13
VCCINT_R24	R24
VCCINT_R20	R20
VCCINT_R16	R16
VCCINT_R14	R14
VCCINT_R12	R12
VCCINT_P27	P27
VCCINT_P15	P15
VCCINT_P13	P13
VCCINT_AH27	AH27
VCCINT_AH23	AH23
VCCINT_AH19	AH19
VCCINT_AH15	AH15
VCCINT_AH13	AH13
VCCINT_AH11	AH11
VCCINT_AG28	AG28
VCCINT_AG24	AG24
VCCINT_AG20	AG20
VCCINT_AG16	AG16
VCCINT_AG14	AG14
VCCINT_AG12	AG12
VCCINT_AF27	AF27
VCCINT_AF23	AF23
VCCINT_AF21	AF21
VCCINT_AF15	AF15
VCCINT_AF13	AF13
VCCINT_AF11	AF11
VCCINT_AE28	AE28
VCCINT_AE24	AE24
VCCINT_AE20	AE20
VCCINT_AE16	AE16
VCCINT_AE14	AE14
VCCINT_AE12	AE12
VCCINT_AE10	AE10
VCCINT_AD27	AD27
VCCINT_AD23	AD23
VCCINT_AD21	AD21
VCCINT_AD19	AD19
VCCINT_AD15	AD15
VCCINT_AD13	AD13
VCCINT_AD11	AD11
VCCINT_AC28	AC28
VCCINT_AC24	AC24
VCCINT_AC16	AC16
VCCINT_AC14	AC14
VCCINT_AC12	AC12
VCCINT_AB27	AB27
VCCINT_AB23	AB23
VCCINT_AB19	AB19
VCCINT_AB15	AB15
VCCINT_AB13	AB13
VCCINT_AB11	AB11
VCCINT_AA28	AA28
VCCINT_AA24	AA24
VCCINT_AA16	AA16
VCCINT_AA14	AA14
VCCINT_AA12	AA12
VCCINT_AA10	AA10

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX
XC7VX690TFFG1761

VCCAUX

VCCAUX_Y17	Y17
VCCAUX_W26	W26
VCCAUX_V17	V17
VCCAUX_U26	U26
VCCAUX_T17	T17
VCCAUX_AG26	AG26
VCCAUX_AF17	AF17
VCCAUX_AE26	AE26
VCCAUX_AD17	AD17
VCCAUX_AC26	AC26
VCCAUX_AB17	AB17
VCCAUX_AA26	AA26

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G0
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G0_AF25	AF25
VCCAUX_IO_G0_AH25	AH25

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G1
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G1_Y25	Y25
VCCAUX_IO_G1_AB25	AB25
VCCAUX_IO_G1_AD25	AD25

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G2
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G2_R26	R26
VCCAUX_IO_G2_T25	T25
VCCAUX_IO_G2_V25	V25

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCBRAM
XC7VX690TFFG1761

VCCINT_FPGA

VCCBRAM_W22	W22
VCCBRAM_U22	U22
VCCBRAM_R22	R22
VCCBRAM_AH21	AH21
VCCBRAM_AG22	AG22
VCCBRAM_AE22	AE22
VCCBRAM_AC22	AC22
VCCBRAM_AA22	AA22

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G3
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G3_AE18	AE18
VCCAUX_IO_G3_AF19	AF19
VCCAUX_IO_G3_AG18	AG18

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G4
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G4_W18	W18
VCCAUX_IO_G4_AA18	AA18
VCCAUX_IO_G4_AC18	AC18

U1 SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK VCCAUX_IO_G5
XC7VX690TFFG1761

VCCAUX_IO

VCCAUX_IO_G5_R18	R18
VCCAUX_IO_G5_T19	T19
VCCAUX_IO_G5_U18	U18

U1 SOC_IRON_690T_FF1761

FPGA Power Pins

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Power Pins
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

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SOC_V7_690T_FF1761_IRON

BANK GND2
XC7VX690TFFG1761

Y41	GND_Y41	GND_M15	M15
Y31	GND_Y31	GND_M9	M9
Y28	GND_Y28	GND_M6	M6
Y26	GND_Y26	GND_M5	M5
Y24	GND_Y24	GND_M2	M2
Y22	GND_Y22	GND_M1	M1
Y18	GND_Y18	GND_L38	L38
Y16	GND_Y16	GND_L28	L28
Y14	GND_Y14	GND_L18	L18
Y12	GND_Y12	GND_L10	L10
Y10	GND_Y10	GND_L9	L9
Y9	GND_Y9	GND_L7	L7
Y6	GND_Y6	GND_L3	L3
Y5	GND_Y5	GND_K41	K41
Y2	GND_Y2	GND_K31	K31
Y1	GND_Y1	GND_K21	K21
W34	GND_W34	GND_K11	K11
W27	GND_W27	GND_K10	K10
W25	GND_W25	GND_K9	K9
W23	GND_W23	GND_K6	K6
W21	GND_W21	GND_K5	K5
W19	GND_W19	GND_K2	K2
W17	GND_W17	GND_K1	K1
W15	GND_W15	GND_J34	J34
W13	GND_W13	GND_J24	J24
W11	GND_W11	GND_J14	J14
W7	GND_W7	GND_J10	J10
W3	GND_W3	GND_J9	J9
V37	GND_V37	GND_J7	J7
V28	GND_V28	GND_J3	J3
V26	GND_V26	GND_H37	H37
V24	GND_V24	GND_H27	H27
V22	GND_V22	GND_H17	H17
V20	GND_V20	GND_H11	H11
V18	GND_V18	GND_H10	H10
V16	GND_V16	GND_H9	H9
V14	GND_V14	GND_H5	H5
V12	GND_V12	GND_H2	H2
V10	GND_V10	GND_H1	H1
V9	GND_V9	GND_G40	G40
V6	GND_V6	GND_G30	G30
V5	GND_V5	GND_G20	G20
V2	GND_V2	GND_G11	G11
V1	GND_V1	GND_G7	G7
U40	GND_U40	GND_G3	G3
U30	GND_U30	GND_F33	F33
U27	GND_U27	GND_F23	F23
U25	GND_U25	GND_F13	F13
U23	GND_U23	GND_F11	F11
U21	GND_U21	GND_F10	F10
U19	GND_U19	GND_F9	F9
U17	GND_U17	GND_F5	F5
U15	GND_U15	GND_F2	F2
U13	GND_U13	GND_F1	F1
U11	GND_U11	GND_E36	E36
U10	GND_U10	GND_E26	E26
U9	GND_U9	GND_E16	E16
U7	GND_U7	GND_E11	E11
U4	GND_U4	GND_E7	E7
U3	GND_U3	GND_E3	E3
T33	GND_T33	GND_D39	D39
T26	GND_T26	GND_D29	D29
T24	GND_T24	GND_D19	D19
T22	GND_T22	GND_D11	D11
T20	GND_T20	GND_D10	D10
T18	GND_T18	GND_D9	D9
T16	GND_T16	GND_D5	D5
T14	GND_T14	GND_D2	D2
T12	GND_T12	GND_D1	D1
T9	GND_T9	GND_C42	C42
T6	GND_T6	GND_C32	C32
T5	GND_T5	GND_C22	C22
T2	GND_T2	GND_C12	C12
T1	GND_T1	GND_C11	C11
R36	GND_R36	GND_C7	C7
R27	GND_R27	GND_C3	C3
R25	GND_R25	GND_BB35	BB35
R23	GND_R23	GND_BB25	BB25
R21	GND_R21	GND_BB15	BB15
R19	GND_R19	GND_BB11	BB11
R17	GND_R17	GND_BB10	BB10
R15	GND_R15	GND_BB9	BB9
R13	GND_R13	GND_BB6	BB6
R11	GND_R11	GND_BB5	BB5
R9	GND_R9	GND_BB2	BB2
R7	GND_R7	GND_BA38	BA38
R3	GND_R3	GND_BA28	BA28
P39	GND_P39	GND_BA18	BA18
P29	GND_P29	GND_BA11	BA11
P19	GND_P19	GND_BA7	BA7
P16	GND_P16	GND_BA3	BA3
P12	GND_P12	GND_B35	B35
P9	GND_P9	GND_B25	B25
P5	GND_P5	GND_B15	B15
P2	GND_P2	GND_B13	B13
P1	GND_P1	GND_B12	B12
N42	GND_N42	GND_B10	B10
N32	GND_N32	GND_B9	B9
N22	GND_N22	GND_B5	B5
N12	GND_N12	GND_B2	B2
N9	GND_N9	GND_B1	B1
N7	GND_N7	GND_AY41	AY41
N3	GND_N3	GND_AY31	AY31
M35	GND_M35	GND_AY21	AY21
M25	GND_M25	GND_AY11	AY11
		GND_AY10	AY10
		GND_AY9	AY9

GND

GND

U1

SOC_IRON_690T_FF1761

SOC_V7_690T_FF1761_IRON

BANK GND1
XC7VX690TFFG1761

AY5	GND_AY5	GND_AG25	AG25
AY2	GND_AY2	GND_AG23	AG23
AY1	GND_AY1	GND_AG21	AG21
AW34	GND_AW34	GND_AG19	AG19
AW24	GND_AW24	GND_AG17	AG17
AW14	GND_AW14	GND_AG15	AG15
AW11	GND_AW11	GND_AG13	AG13
AW7	GND_AW7	GND_AG10	AG10
AW3	GND_AW3	GND_AG9	AG9
AV37	GND_AV37	GND_AG8	AG8
AV27	GND_AV27	GND_AG7	AG7
AV17	GND_AV17	GND_AG4	AG4
AV11	GND_AV11	GND_AG3	AG3
AV10	GND_AV10	GND_AF33	AF33
AV9	GND_AV9	GND_AF26	AF26
AV5	GND_AV5	GND_AF24	AF24
AV2	GND_AV2	GND_AF22	AF22
AV1	GND_AV1	GND_AF20	AF20
AU40	GND_AU40	GND_AF18	AF18
AU30	GND_AU30	GND_AF16	AF16
AU20	GND_AU20	GND_AF14	AF14
AU11	GND_AU11	GND_AF12	AF12
AU7	GND_AU7	GND_AF10	AF10
AU3	GND_AU3	GND_AF9	AF9
AT33	GND_AT33	GND_AF6	AF6
AT23	GND_AT23	GND_AF5	AF5
AT13	GND_AT13	GND_AF2	AF2
AT11	GND_AT11	GND_AF1	AF1
AT10	GND_AT10	GND_AE36	AE36
AT9	GND_AT9	GND_AE27	AE27
AT6	GND_AT6	GND_AE25	AE25
AT5	GND_AT5	GND_AE23	AE23
AT2	GND_AT2	GND_AE21	AE21
AT1	GND_AT1	GND_AE19	AE19
AR36	GND_AR36	GND_AE17	AE17
AR26	GND_AR26	GND_AE15	AE15
AR16	GND_AR16	GND_AE13	AE13
AR10	GND_AR10	GND_AE11	AE11
AR9	GND_AR9	GND_AE9	AE9
AR7	GND_AR7	GND_AE7	AE7
AR3	GND_AR3	GND_AE3	AE3
AP39	GND_AP39	GND_AD39	AD39
AP29	GND_AP29	GND_AD29	AD29
AP19	GND_AP19	GND_AD28	AD28
AP10	GND_AP10	GND_AD26	AD26
AP9	GND_AP9	GND_AD24	AD24
AP5	GND_AP5	GND_AD22	AD22
AP2	GND_AP2	GND_AD20	AD20
AP1	GND_AP1	GND_AD18	AD18
AN42	GND_AN42	GND_AD16	AD16
AN32	GND_AN32	GND_AD14	AD14
AN22	GND_AN22	GND_AD12	AD12
AN12	GND_AN12	GND_AD10	AD10
AN10	GND_AN10	GND_AD9	AD9
AN9	GND_AN9	GND_AD6	AD6
AN7	GND_AN7	GND_AD5	AD5
AN3	GND_AN3	GND_AD2	AD2
AM35	GND_AM35	GND_AD1	AD1
AM25	GND_AM25	GND_AC42	AC42
AM15	GND_AM15	GND_AC32	AC32
AM10	GND_AM10	GND_AC27	AC27
AM9	GND_AM9	GND_AC25	AC25
AM5	GND_AM5	GND_AC23	AC23
AM2	GND_AM2	GND_AC19	AC19
AM1	GND_AM1	GND_AC17	AC17
AL38	GND_AL38	GND_AC15	AC15
AL28	GND_AL28	GND_AC13	AC13
AL18	GND_AL18	GND_AC11	AC11
AL9	GND_AL9	GND_AC7	AC7
AL7	GND_AL7	GND_AC3	AC3
AL3	GND_AL3	GND_AB35	AB35
AK41	GND_AK41	GND_AB28	AB28
AK31	GND_AK31	GND_AB26	AB26
AK21	GND_AK21	GND_AB24	AB24
AK11	GND_AK11	GND_AB22	AB22
AK9	GND_AK9	GND_AB18	AB18
AK6	GND_AK6	GND_AB16	AB16
AK5	GND_AK5	GND_AB14	AB14
AK2	GND_AK2	GND_AB12	AB12
AK1	GND_AK1	GND_AB10	AB10
AJ34	GND_AJ34	GND_AB9	AB9
AJ27	GND_AJ27	GND_AB6	AB6
AJ24	GND_AJ24	GND_AB5	AB5
AJ14	GND_AJ14	GND_AB2	AB2
AJ9	GND_AJ9	GND_AB1	AB1
AJ7	GND_AJ7	GND_AA38	AA38
AJ3	GND_AJ3	GND_AA27	AA27
AH37	GND_AH37	GND_AA25	AA25
AH26	GND_AH26	GND_AA23	AA23
AH24	GND_AH24	GND_AA19	AA19
AH22	GND_AH22	GND_AA17	AA17
AH20	GND_AH20	GND_AA15	AA15
AH18	GND_AH18	GND_AA13	AA13
AH17	GND_AH17	GND_AA11	AA11
AH16	GND_AH16	GND_AA9	AA9
AH14	GND_AH14	GND_AA7	AA7
AH12	GND_AH12	GND_AA3	AA3
AH9	GND_AH9	GND_A38	A38
AH6	GND_AH6	GND_A28	A28
AH5	GND_AH5	GND_A18	A18
AH2	GND_AH2	GND_A13	A13
AH1	GND_AH1	GND_A11	A11
AG40	GND_AG40	GND_A8	A8
AG30	GND_AG30	GND_A7	A7
AG27	GND_AG27	GND_A4	A4
		GND_A3	A3
		GND_A2	A2

GND

GND

U1

SOC_IRON_690T_FF1761

FPGA GND

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA GND
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date: 12-21-2012_13:14

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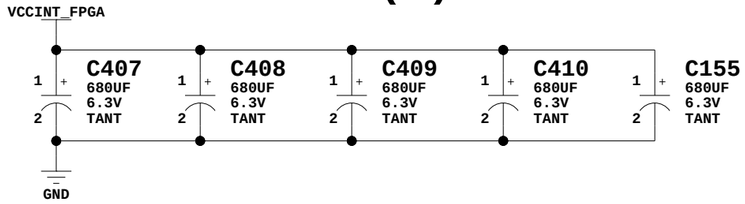
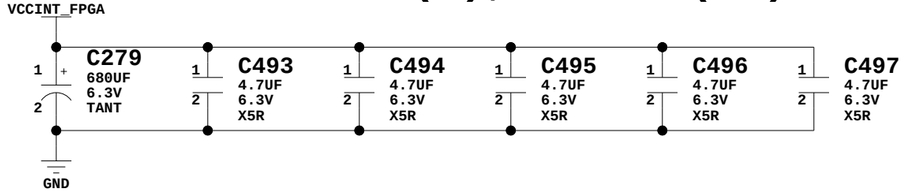
Rev: 01

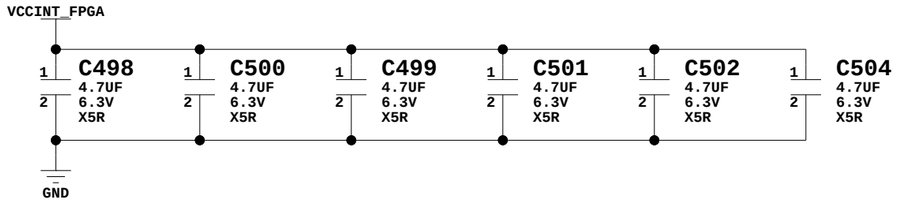
Drawn By DN

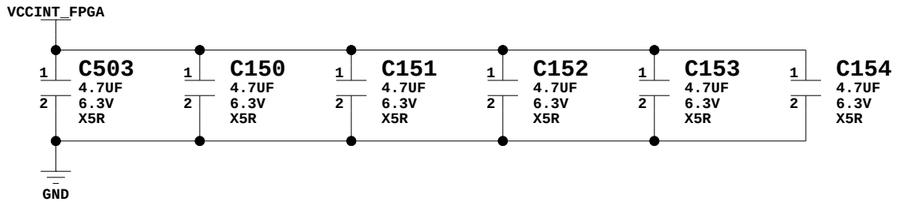
VCCINT 680uF (5)



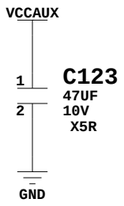
VCCBRAM 660uF (1), 4.7uF (17)



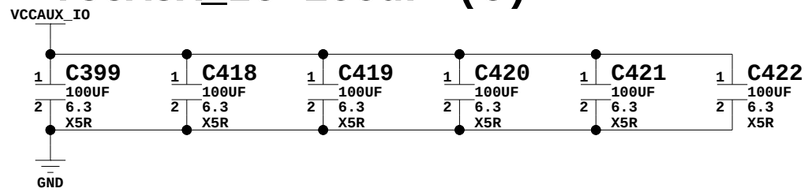




VCCAUX 47uF (1)



VCCAUX_IO 100uF (6)



FPGA Bypass Capacitors

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: FPGA Bypass Capacitors
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

Date:	9-19-2012_15:39	Ver:	1.0
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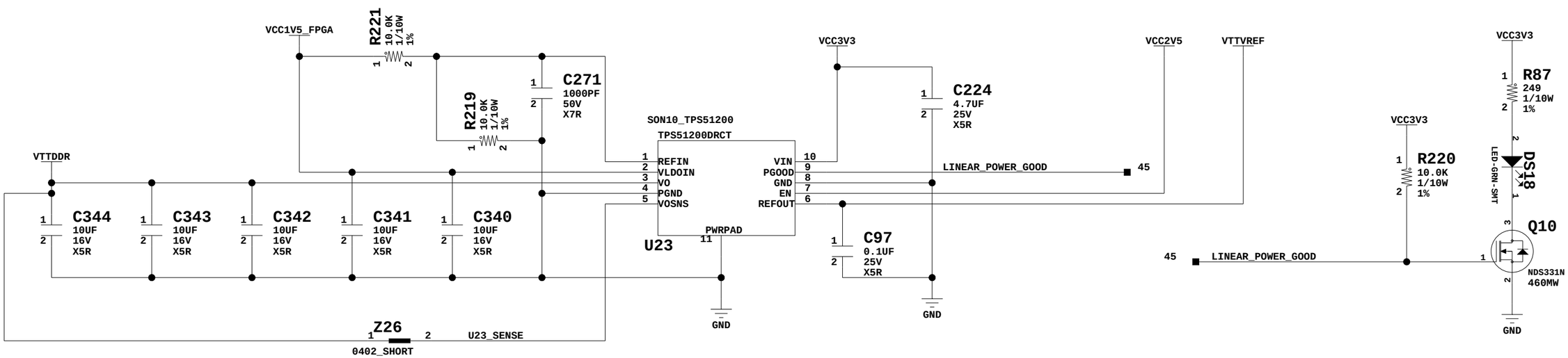

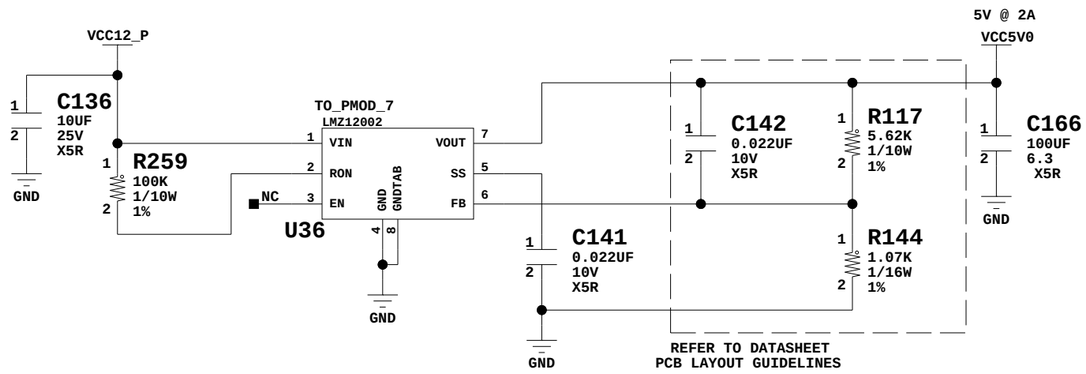

Linear Power Supplies

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Linear Power Supplies SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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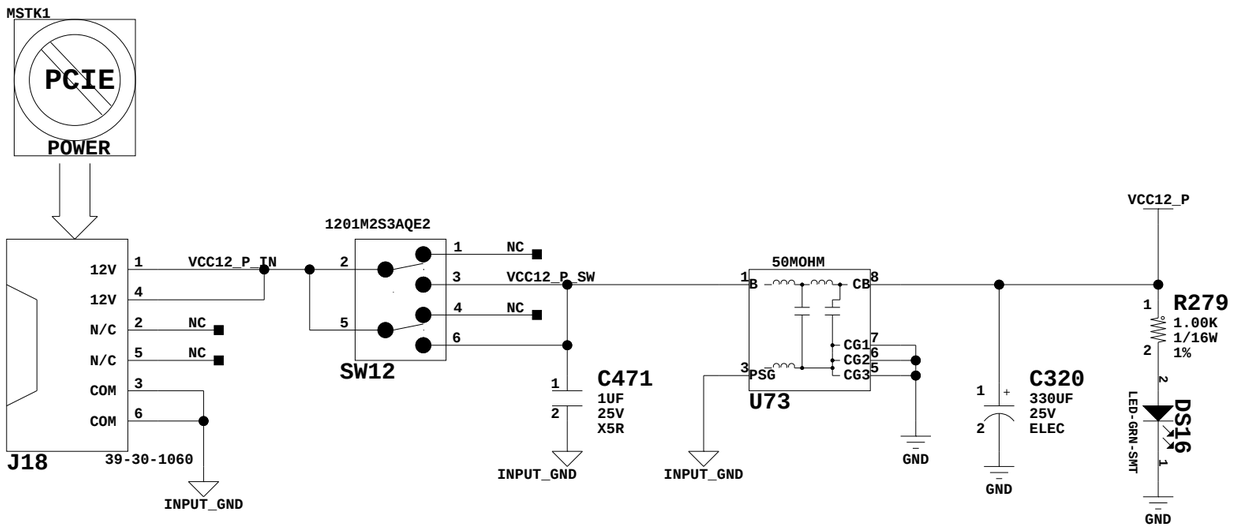

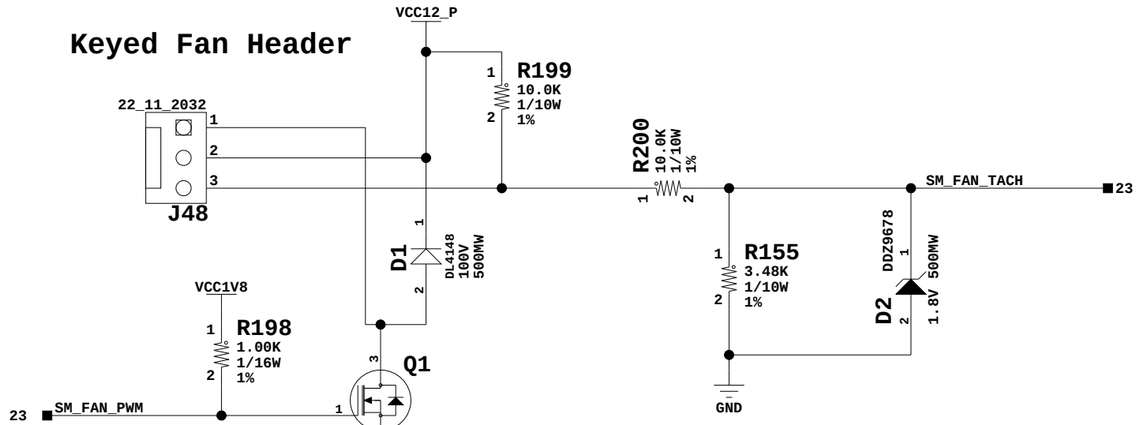

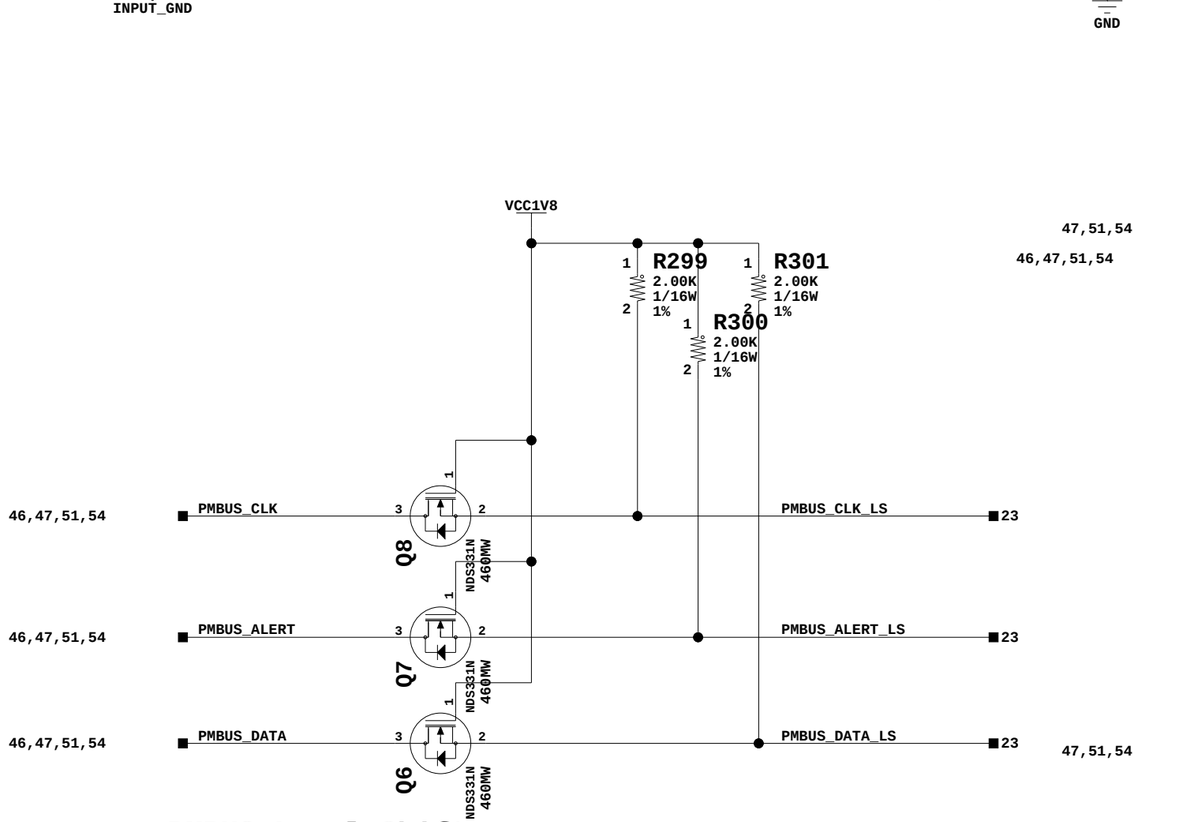

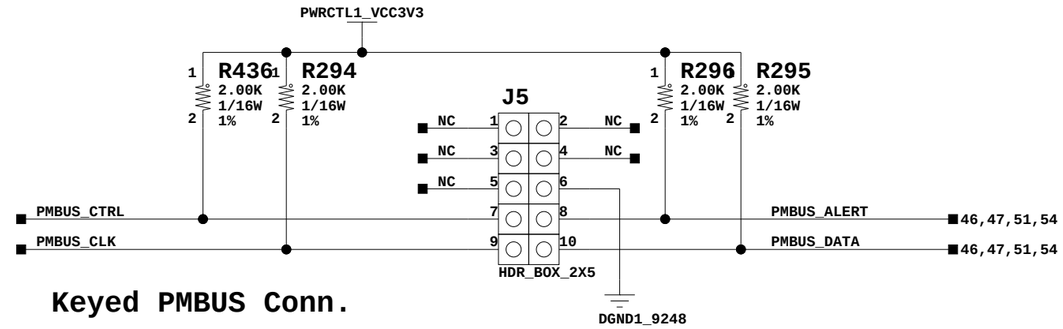

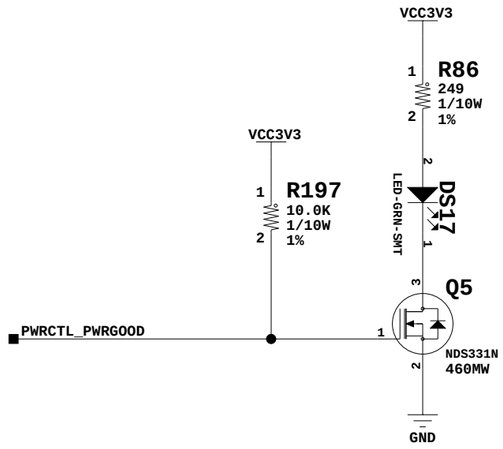

Power Connector and switch, PMBus Header

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Power Connector and switch, PMBus Header SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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FPGA UCD9240 PMBus Controller #1

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA UCD9240 PMBus Controller #1 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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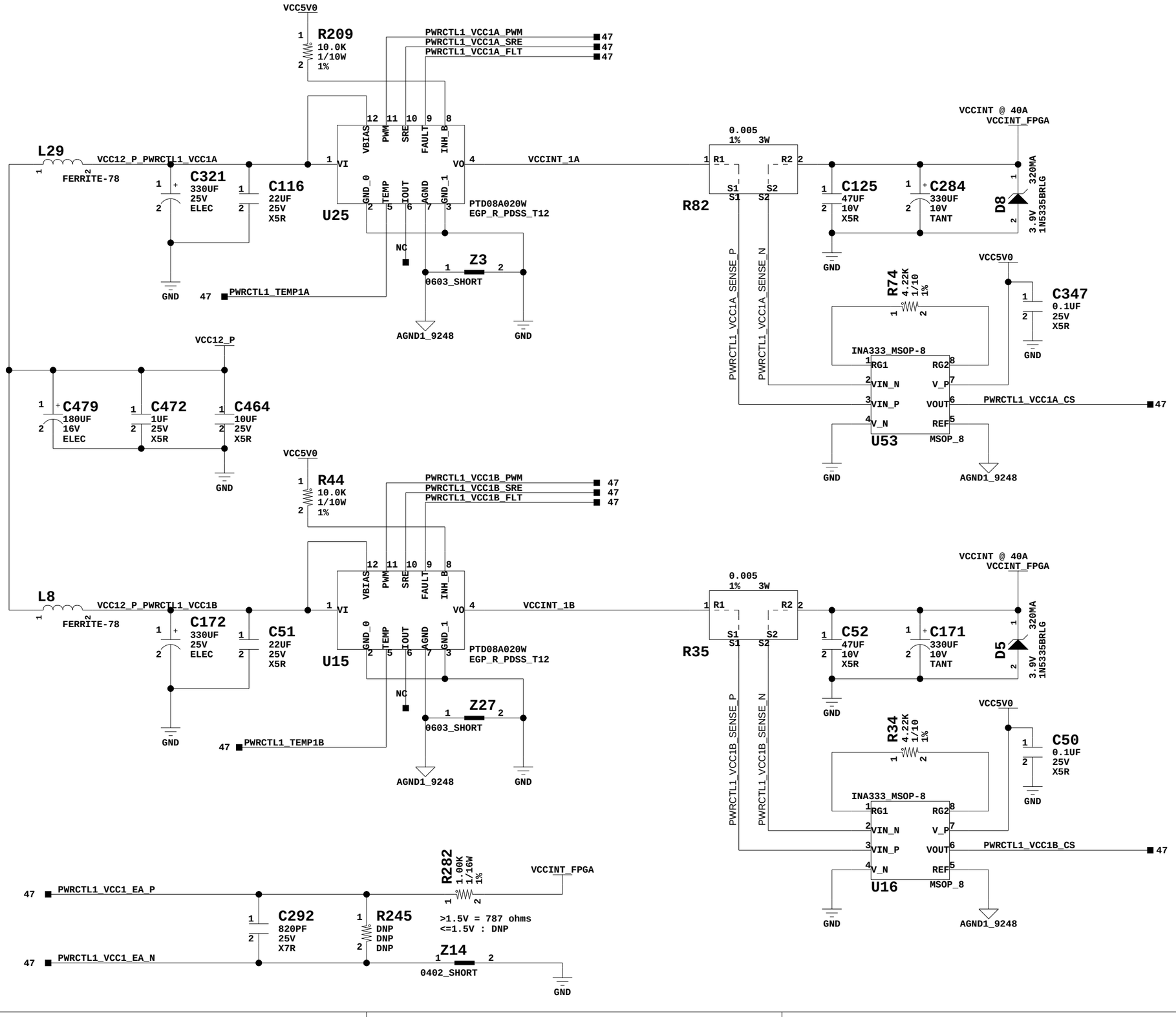
PMBUS Addr = 52



2XPTD08A020W 40A Max. Power Channel

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	PTD08A010W 20A Max. Power Channel SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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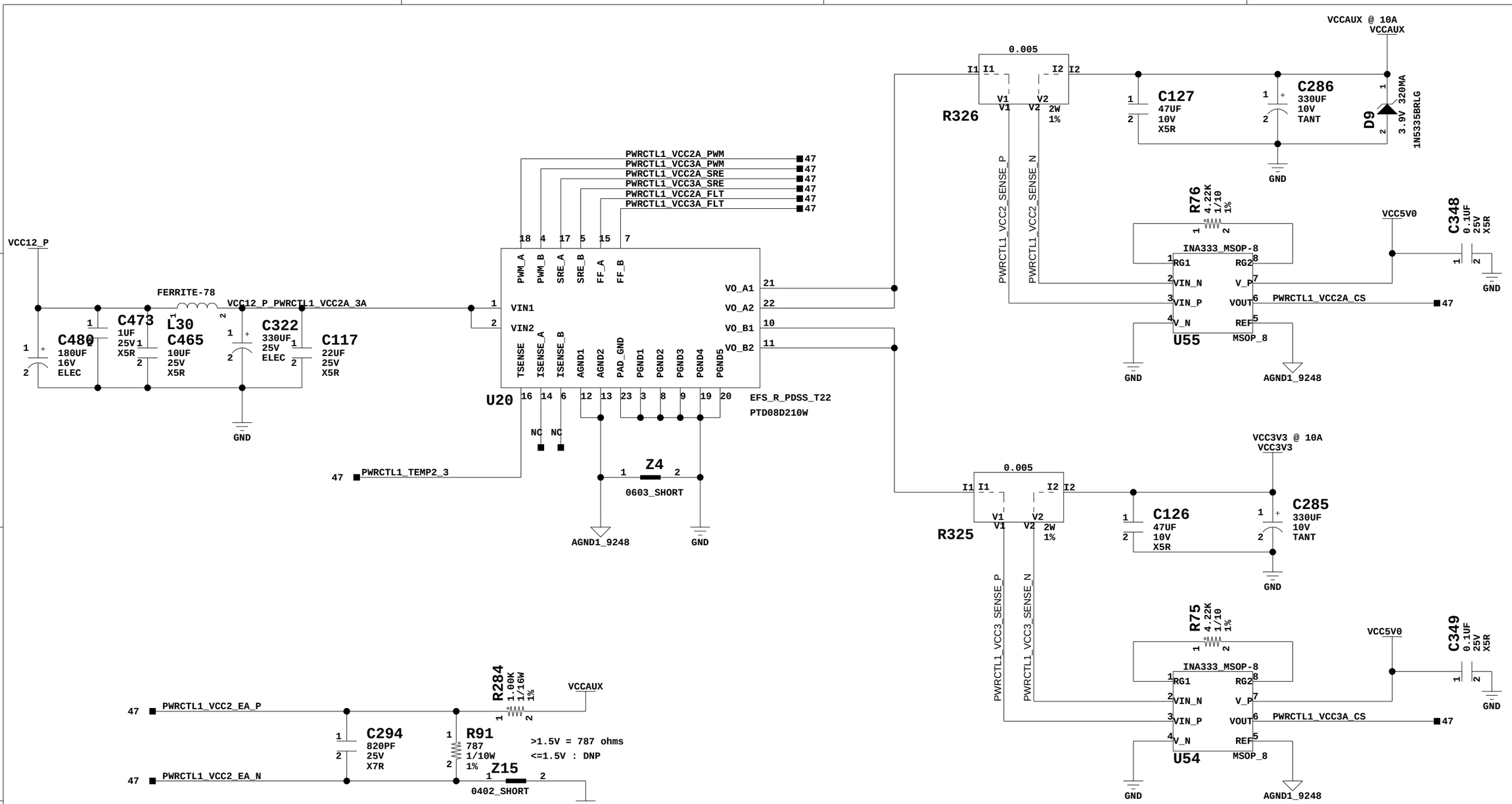

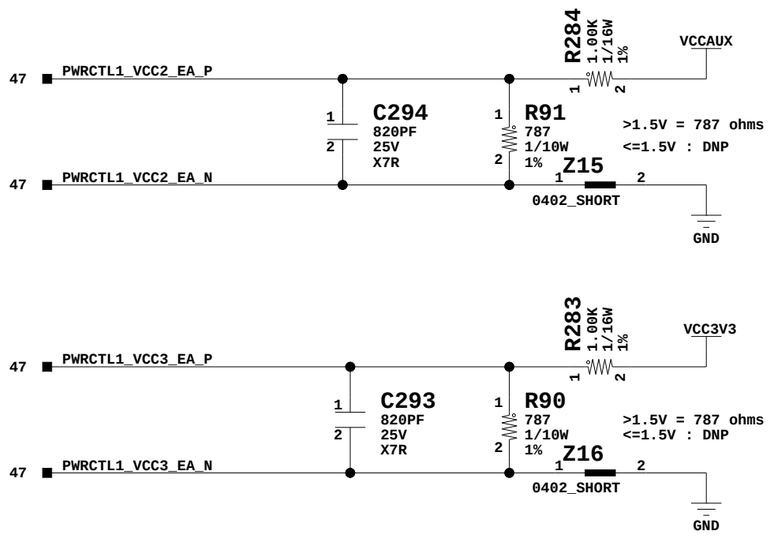

Dual 10A Max. Power Channels

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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PLACEHOLDER PAGE TO RETAIN NET NAMES

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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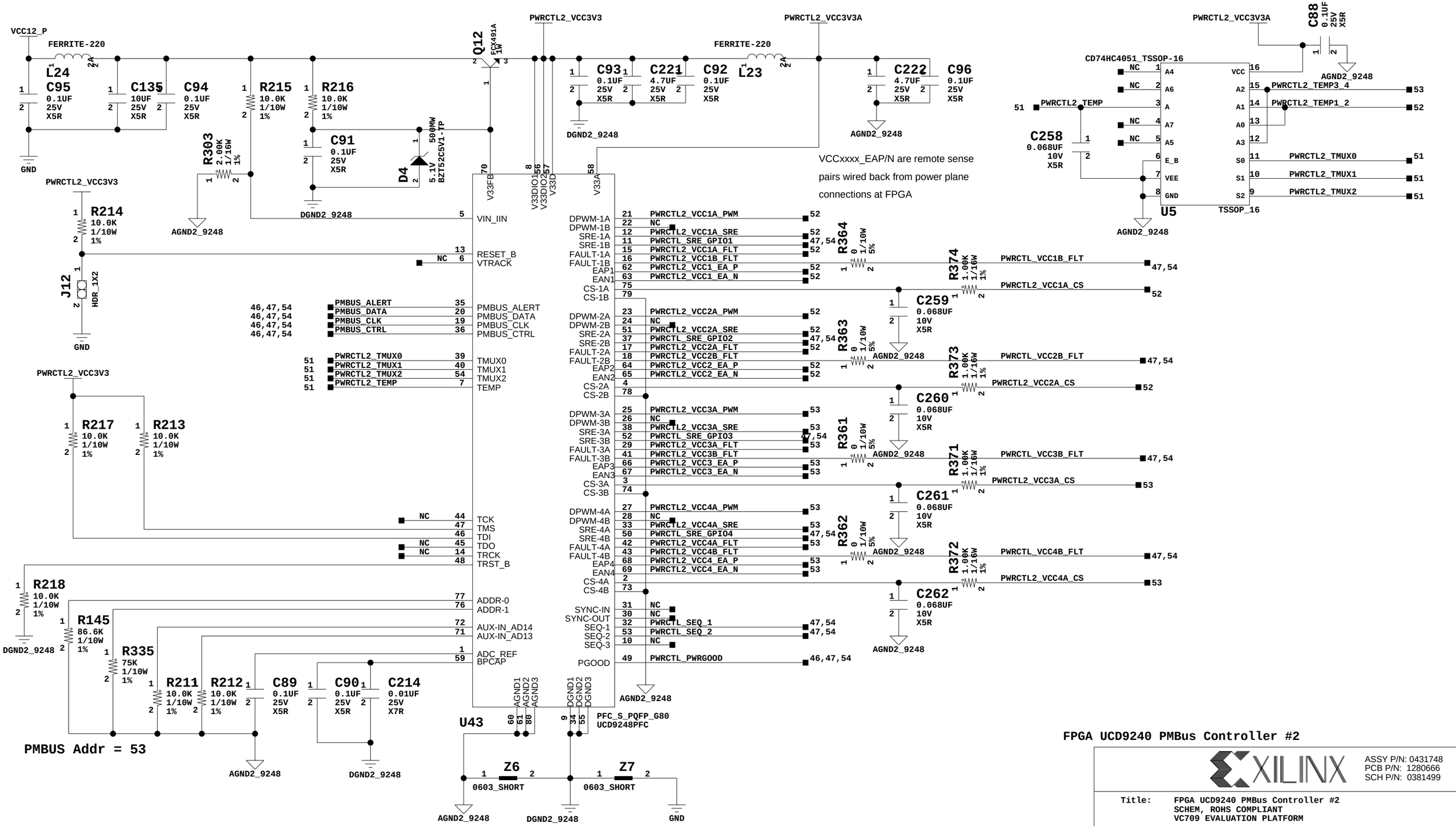

FPGA UCD9240 PMBus Controller #2

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA UCD9240 PMBus Controller #2 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
Sheet Size: B		Rev:	01
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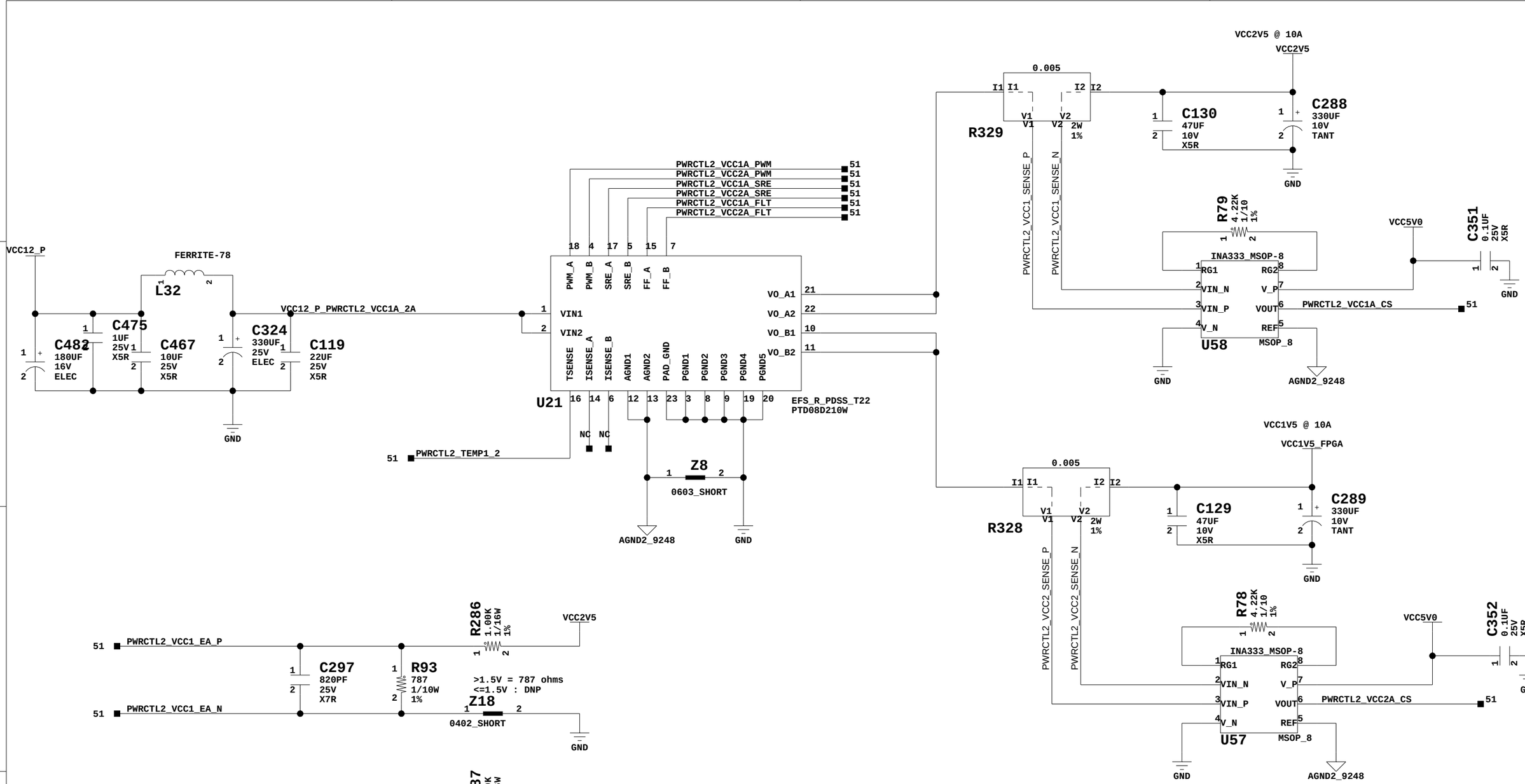

Dual 10A Max. Power Channels

XILINX	ASSY P/N: 0431748 PCB P/N: 1280666 SCH P/N: 0381499
Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM
Date: 9-19-2012_15:39	Ver: 1.0
Sheet Size: B	Rev: 01
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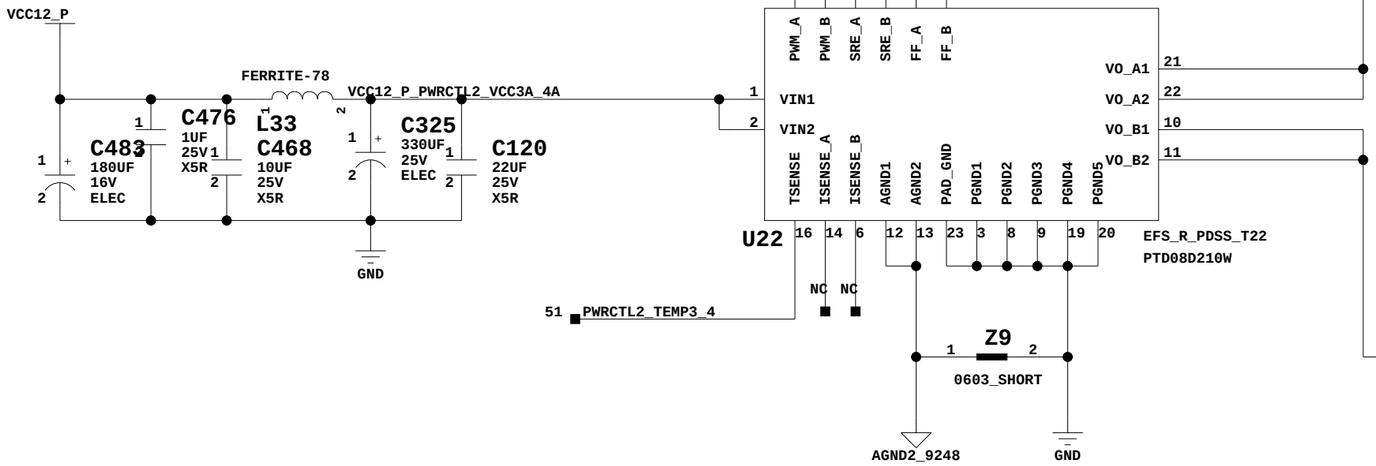

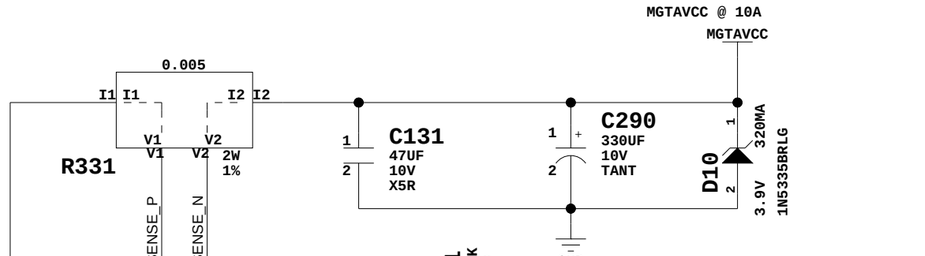

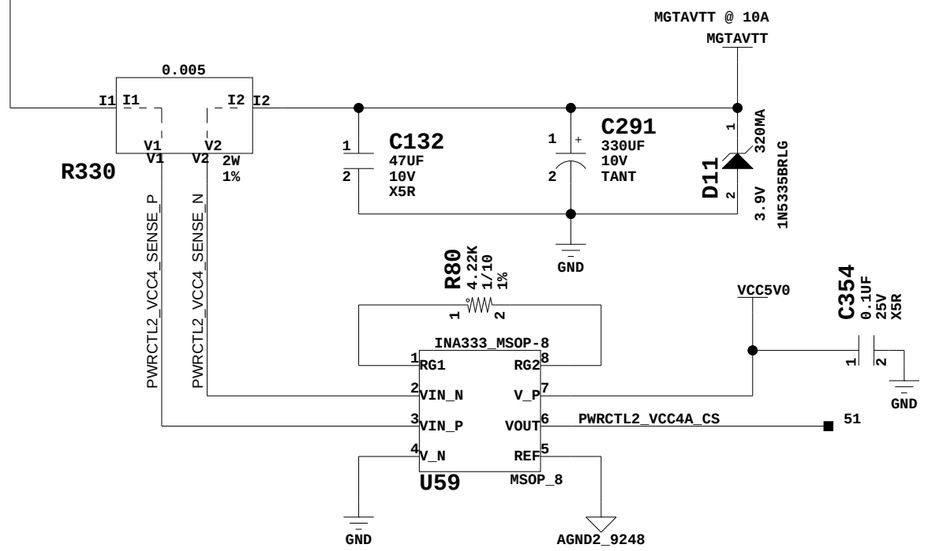

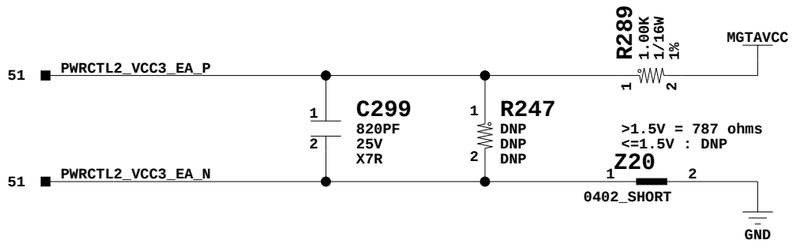

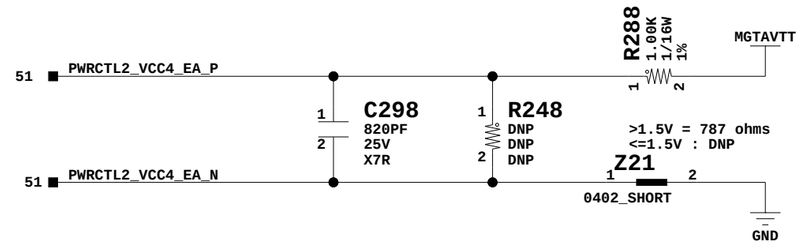

Dual 10A Max. Power Channels

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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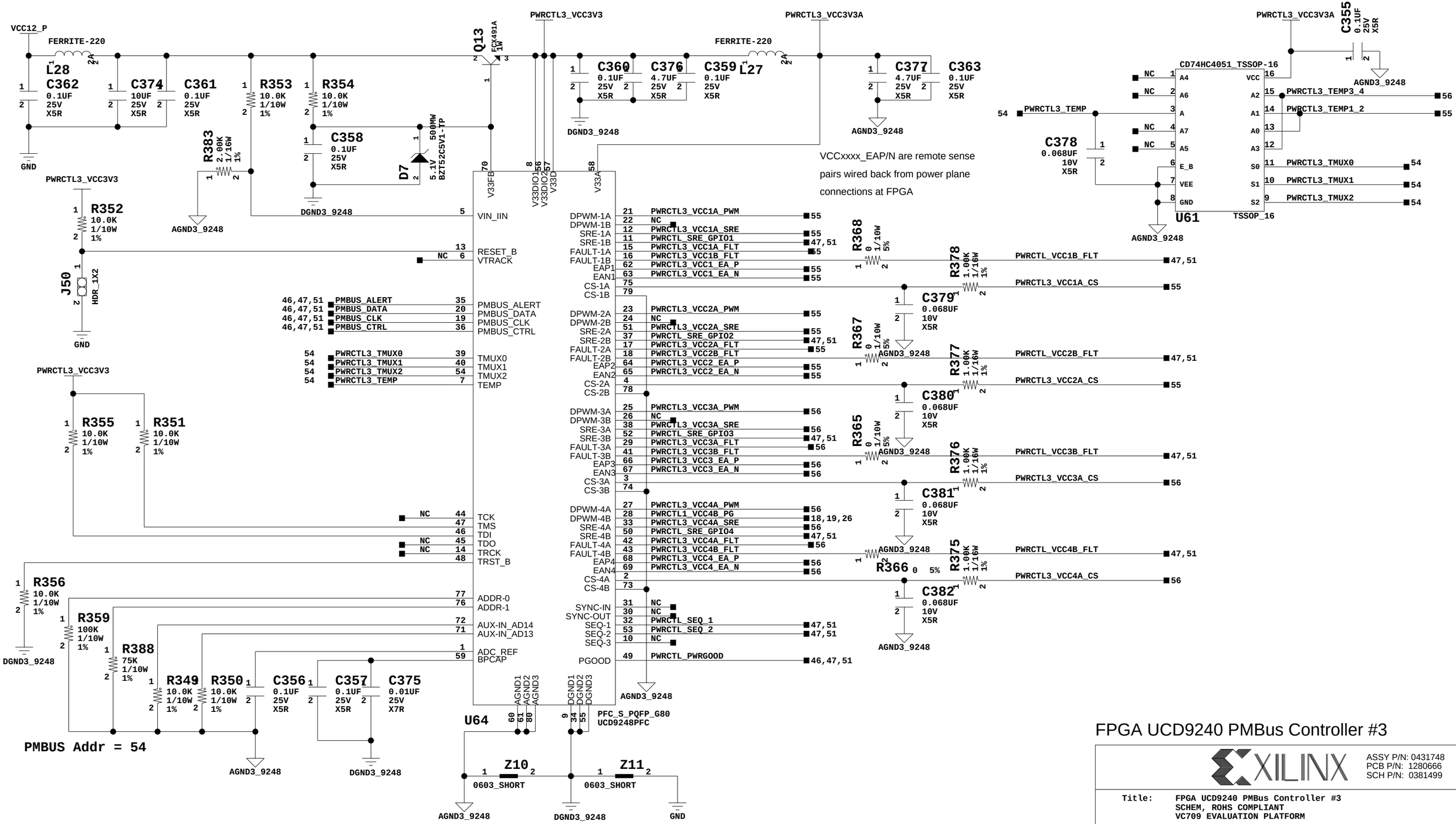

FPGA UCD9240 PMBus Controller #3

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	FPGA UCD9240 PMBus Controller #3 SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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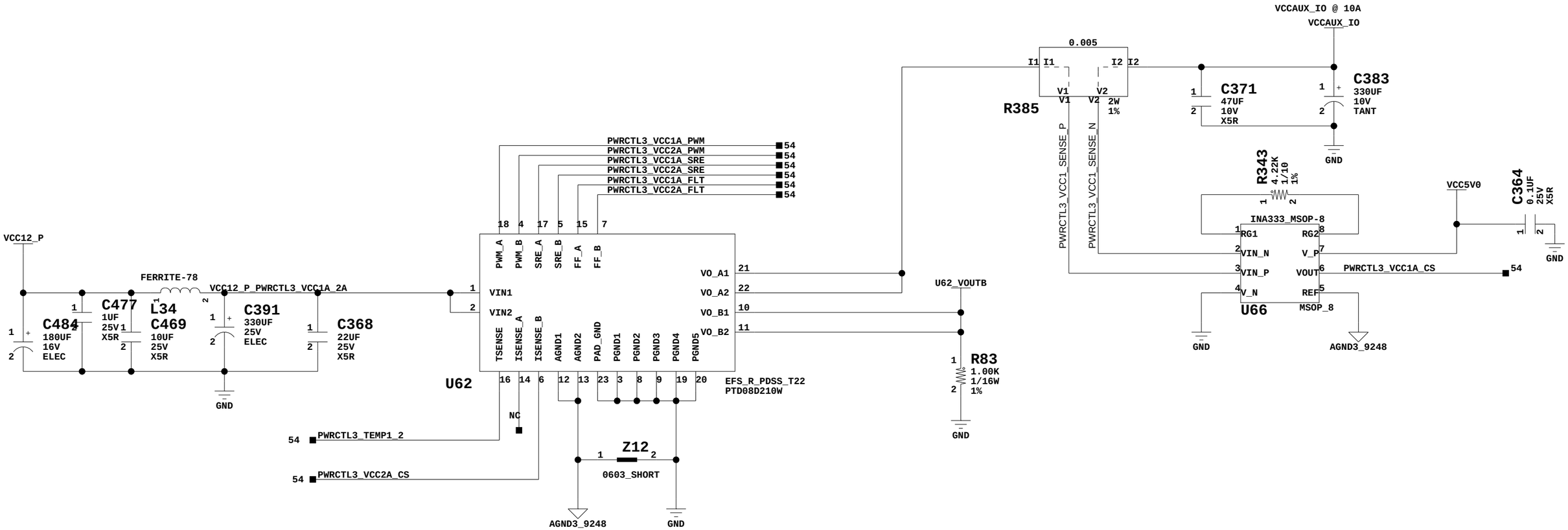

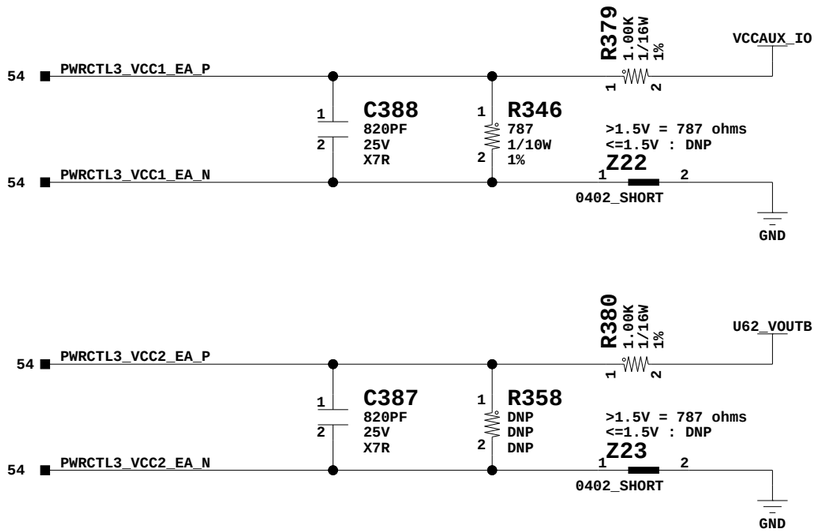

Dual 10A Max. Power Channels

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
Date:	9-19-2012_15:39	Ver:	1.0
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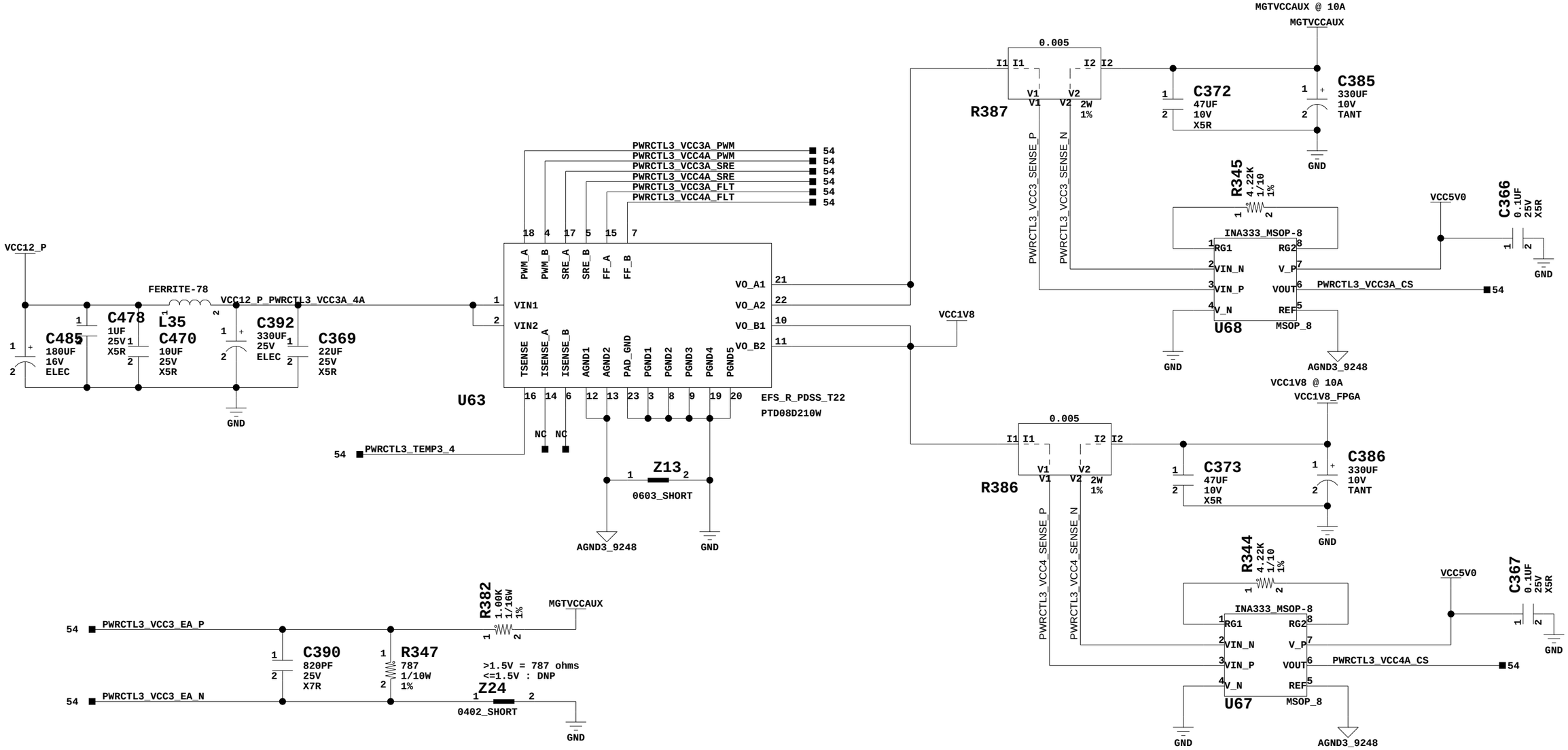

Dual 10A Max. Power Channels

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC709 EVALUATION PLATFORM		
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CBL1

4-Pin ATX Power — 6-Pin Molex Mini-fit Jr.

PCIe Adapter Cable

PCIE_ADAPTER_CABLE

CBL2

110V Prong — IEC320-C13

Power Cord

PC_POWER_CABLE

PB1 PWR_BRICK_12V

12v Power Brick

12V Fan Assembly, w/TACH Output

PL1

VC709_PCIE_PLATE
MANF=PURCELL
MANF_P/N=SK01451

MSTK1 "No PCIe Power" sticker is on PG.46

MMD1 DDR3_SODIMM_4GB

MT8KTF51264HZ-1G9

MMD2 DDR3_SODIMM_4GB

MT8KTF51264HZ-1G9

HS1

12V Fan / Heatsink

12VDC

CBL3

USB A — USB Mini-B

USB_MINIB_CABLE

USB Mini-B Cable

CBL4

USB A — USB Mini-B

USB Micro-B Cable

MS1 — MACHINE_SCREW_4-40

MH_125_250 1 — MH1 — GND

MS01 — STANDOFF_0P375

MRB1 — RUBBER_BUMPER

MS12 — MACHINE_SCREW_4-40

MS2 — MACHINE_SCREW_4-40

MH_125_250 1 — MH2 — GND

MS02 — STANDOFF_0P375

MRB2 — RUBBER_BUMPER

MS13 — MACHINE_SCREW_4-40

MS3 — MACHINE_SCREW_4-40

MH_125_250 1 — MH3 — GND

MS03 — STANDOFF_0P375

MRB3 — RUBBER_BUMPER

MS14 — MACHINE_SCREW_4-40

MS4 — MACHINE_SCREW_4-40

MH_125_250 1 — MH5 — GND

MS04 — STANDOFF_0P375

MRB4 — RUBBER_BUMPER

MS15 — MACHINE_SCREW_4-40

MS5 — MACHINE_SCREW_4-40

MH_125_250 1 — MH6 — GND

MS05 — STANDOFF_0P375

MRB5 — RUBBER_BUMPER

MS16 — MACHINE_SCREW_4-40

FIDCUT 1 NC — FID1

FIDCUT 1 NC — FID2

FIDCUT 1 NC — FID3

FIDCUT 1 NC — FID4

FIDCUT 1 NC — FID5

FIDCUT 1 NC — FID6

MJB1 J49 5-6 — JUMPER_BLOCK_2-PIN

MJB2 J42 1-2 — JUMPER_BLOCK_2-PIN

MJB3 J10 1-2 — JUMPER_BLOCK_2-PIN

MJB4 J53 1-2 — JUMPER_BLOCK_2-PIN

MJB5 J43 1-2 — JUMPER_BLOCK_2-PIN

MJB6 J54 1-2 — JUMPER_BLOCK_2-PIN

MJB7 J51 1-2 — JUMPER_BLOCK_2-PIN

Mechanical Components

XILINX

ASSY P/N: 0431748
PCB P/N: 1280666
SCH P/N: 0381499

Title: Mechanical Components
SCHEM, ROHS COMPLIANT
VC709 EVALUATION PLATFORM

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