



# VC707 PCIe Design Creation

April 2015

XTP207

# Revision History

Date	Version	Description
04/30/14	12.0	Recompiled for 2015.1.
11/24/14	11.0	Recompiled for 2014.4.
10/08/14	10.0	Recompiled for 2014.3.
06/09/14	9.0	Recompiled for 2014.2. AR54939 fixed.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Added AR54939.
06/19/13	5.0	Recompiled for 2013.2. AR55494 fixed.
04/03/13	4.0	Recompiled for 2013.1. Added AR55494.
12/18/12	3.0	Recompiled for 2012.4.
10/23/12	2.0	Recompiled for 2012.3.
09/20/12	1.1	Minor updates.
08/20/12	1.0	Initial version for 2012.2.

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# Overview

➤ **Virtex-7 PCIe x8 Gen 2 Capability**

➤ **Xilinx VC707 Board**

➤ **Software Requirements**

➤ **VC707 Setup**

➤ **Generate x8 Gen 2 PCIe Core**

- Modify PCIe Core
- Compile Example Design
- Generate PCIe MCS File
- Program BPI Flash with PCIe Design

➤ **Running the PCIe x8 Gen 2 Design**

➤ **References**

# Virtex-7 PCIe x8 Gen 2 Capability

## ➤ VC707 Supports PCIe Gen 1 and Gen 2 Capability

- x8, x4, x2, or x1 Gen 2 lane width

## ➤ LogiCORE PIO Example Design

- VC707 PCIe Design Files (2015.1 C) ZIP file
- Available through <http://www.xilinx.com/vc707>

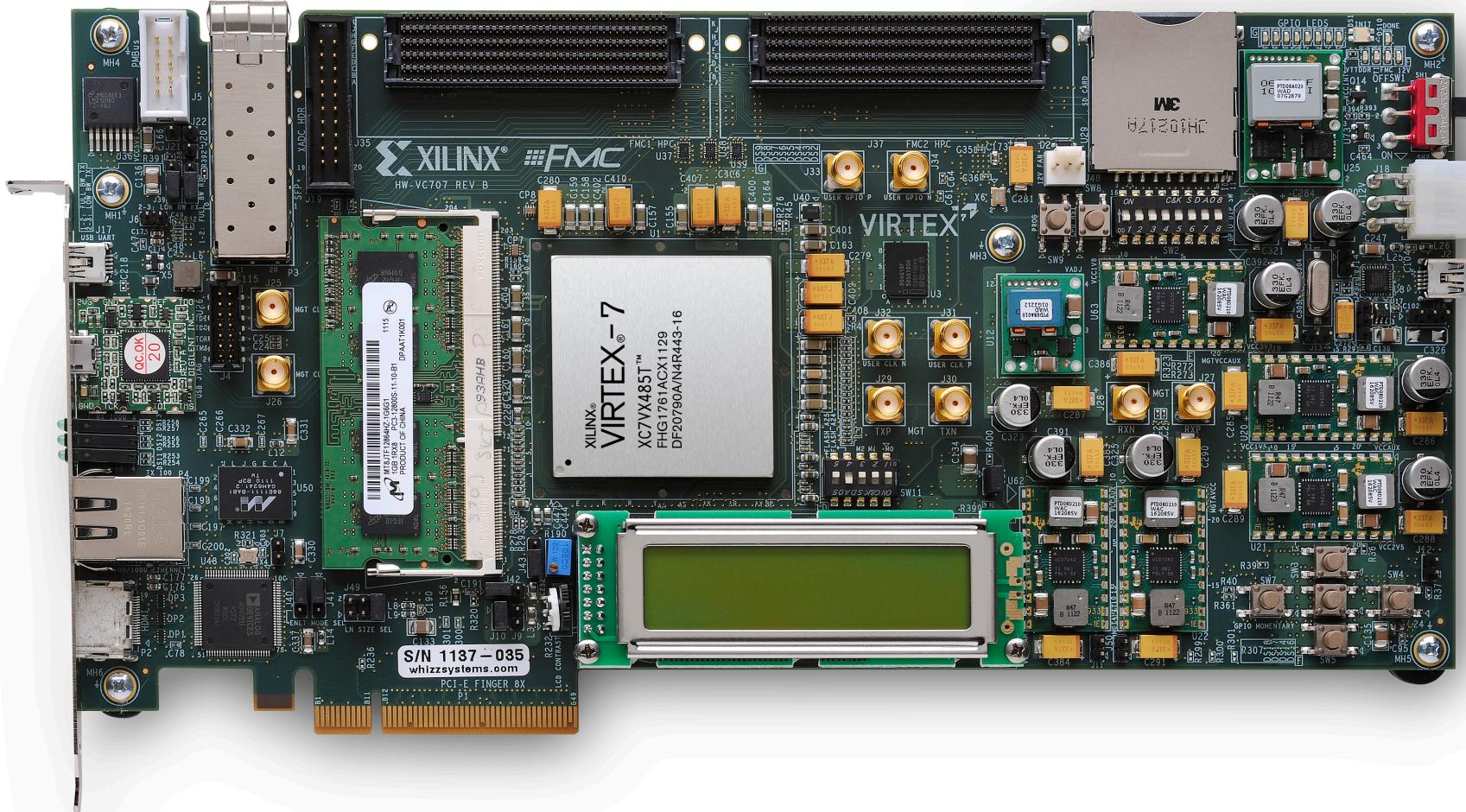
## ➤ 7 Series Integrated Block for PCI Express

- See [PG054](#) for details

# Virtex-7 PCIe x8 Gen 2 Capability

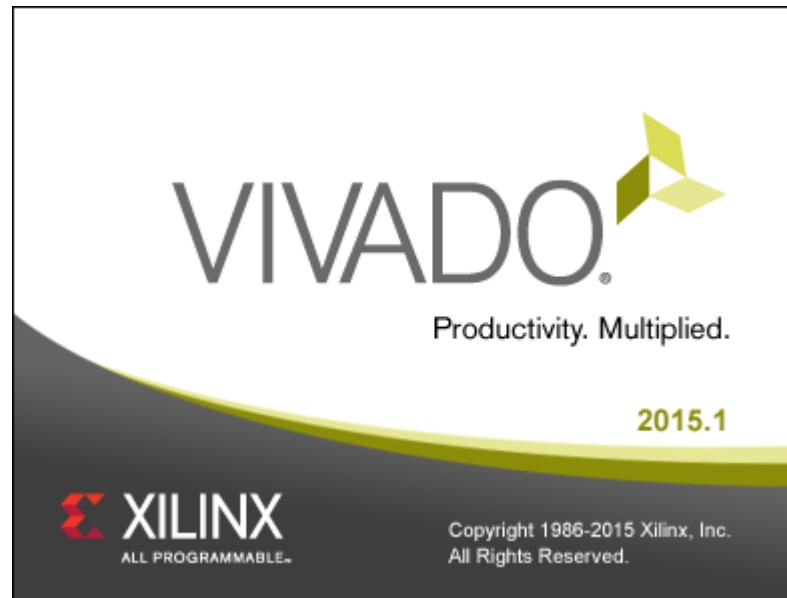
- **Integrated Block for PCI Express**
  - PCI Express Base 2.0 Specification
- **Configurable for Endpoint or Root Port Applications**
  - VC707 configured for Endpoint Applications
- **GTX Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering
- **Management and Statistics Interface**

# Xilinx VC707 Board



# Vivado Software Requirements

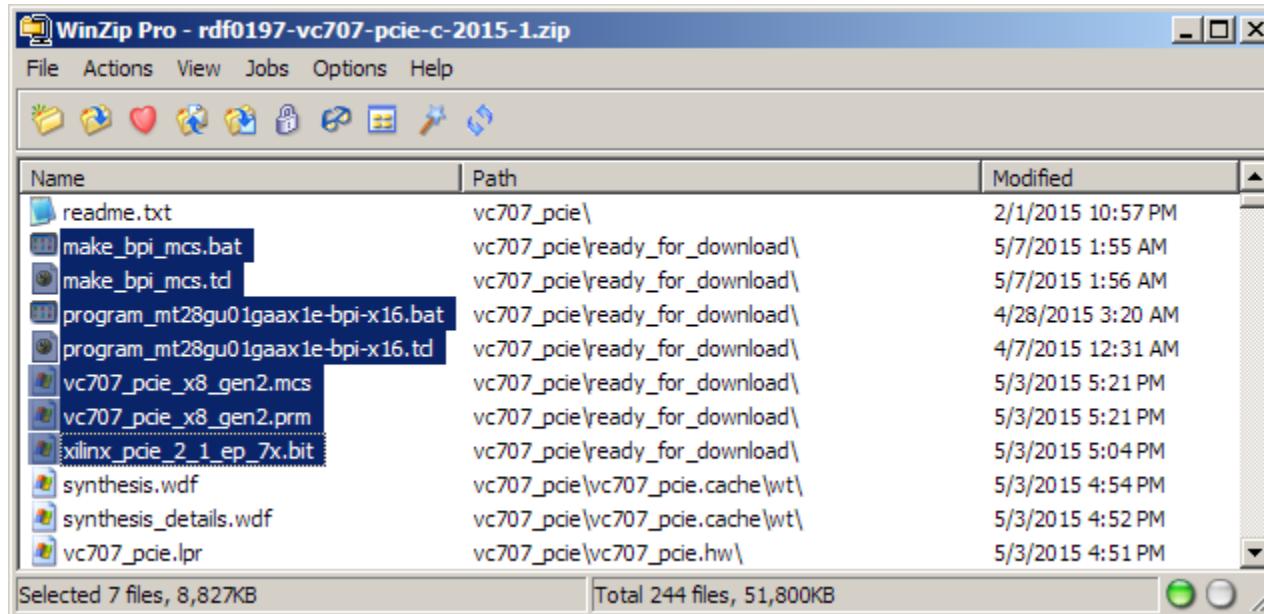
- Xilinx Vivado Design Suite 2015.1, Design Edition



# Setup for the VC707 PCIe Design

► Open the VC707 PCIe Design Files (2015.1 C) ZIP file, and extract these files to your C:\ drive:

- vc707\_PCIE\ready\_for\_download\\*
- Available through <http://www.xilinx.com/vc707>



# PciTree Software Requirement

## ► PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to  
C:\WINDOWS\system32\drivers  
directory



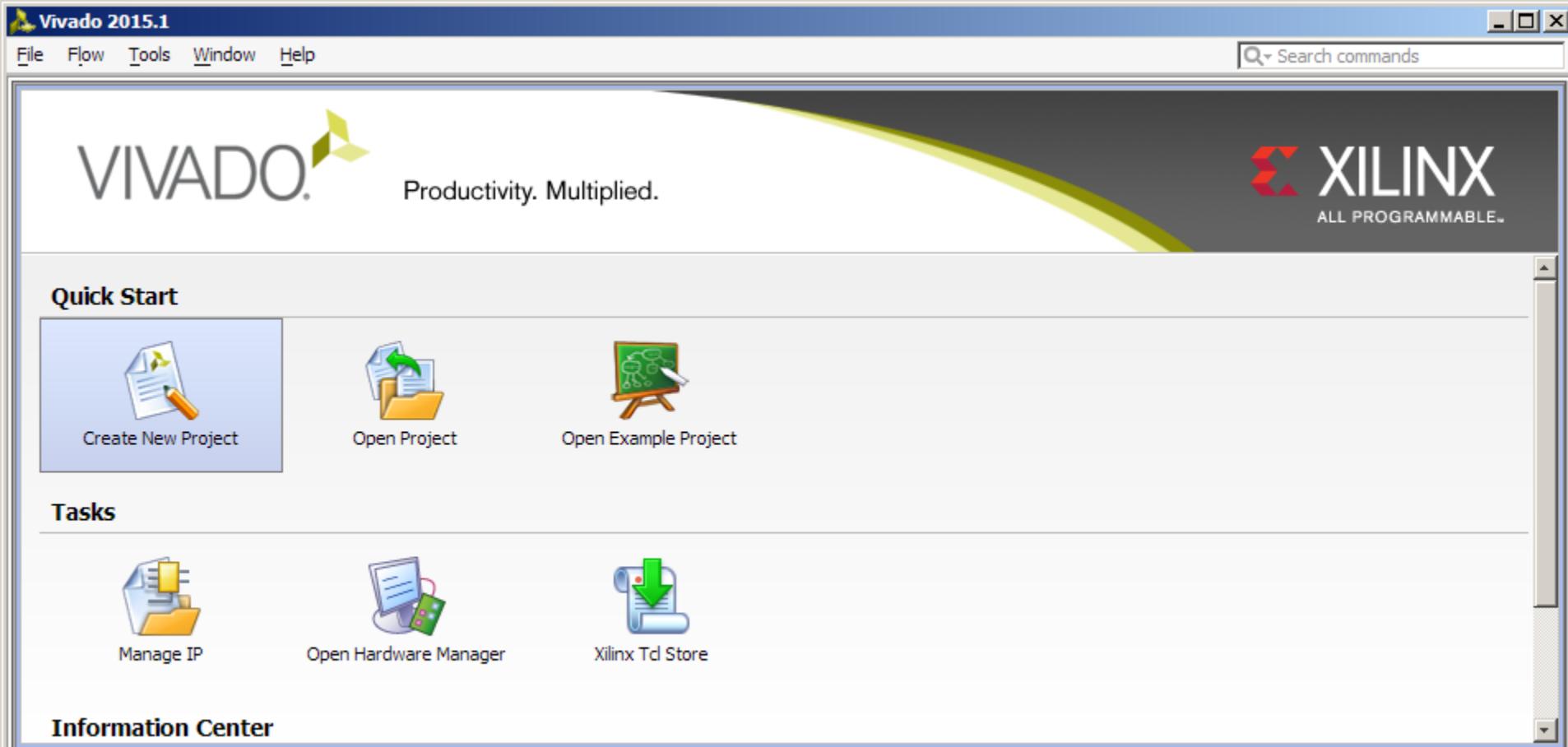
# **Generate x8 Gen 2 PCIe Core**

# Generate x8 Gen 2 PCIe Core

## ► Open Vivado

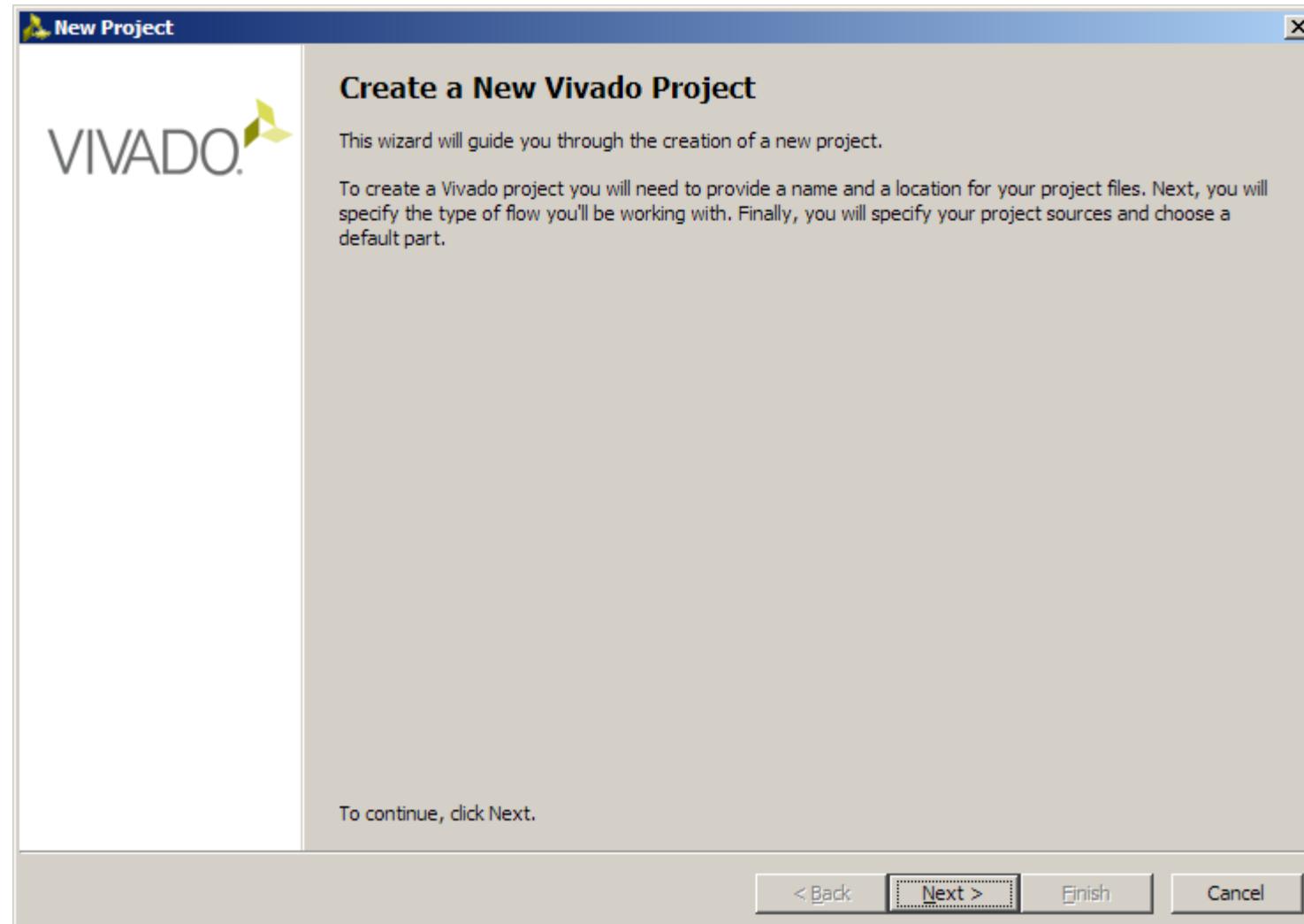
Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

## ► Select Create New Project



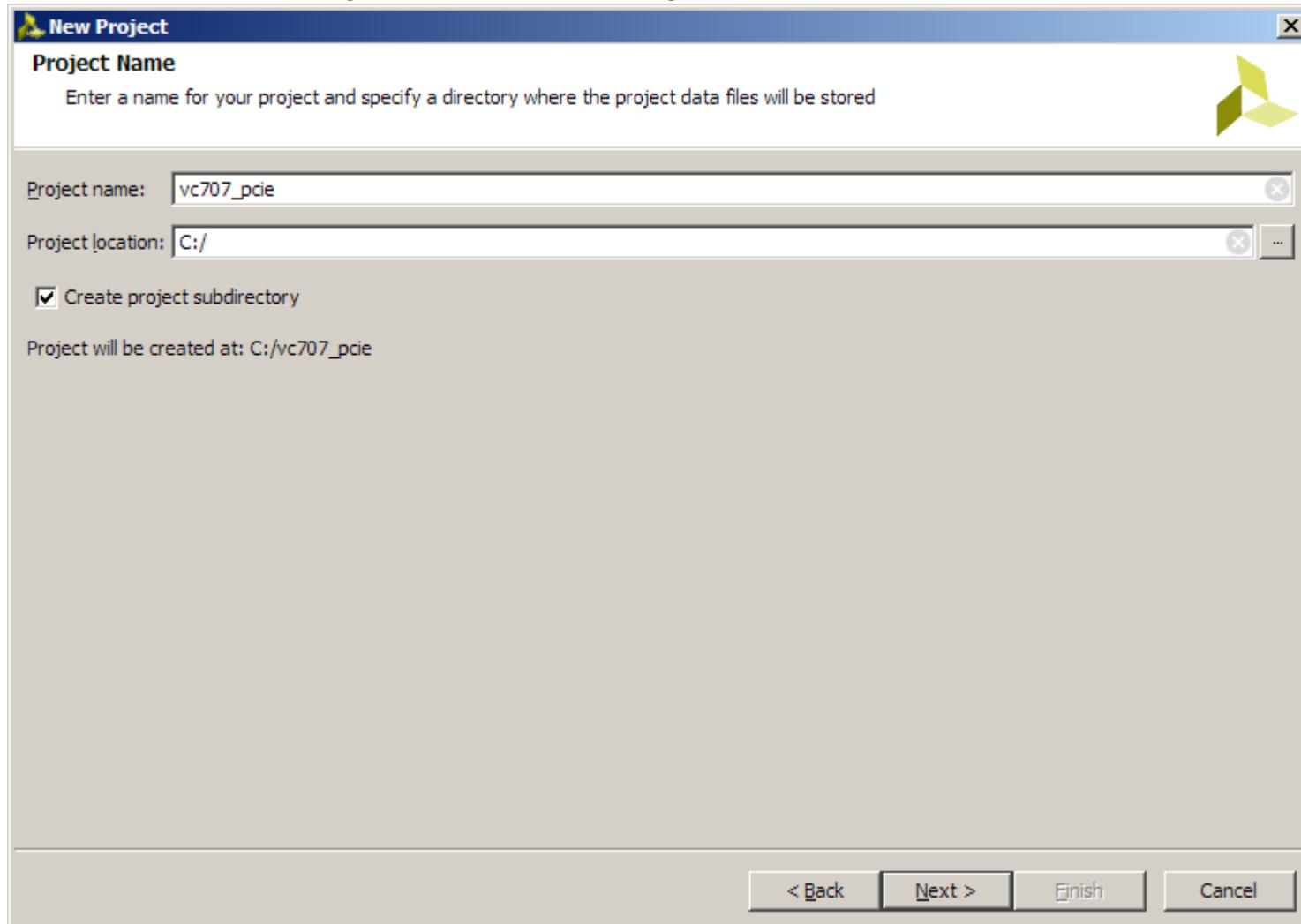
# Generate x8 Gen 2 PCIe Core

► Click Next



# Generate x8 Gen 2 PCIe Core

- Set the Project name and location to vc707\_pcnie and C:/
  - Check Create project subdirectory



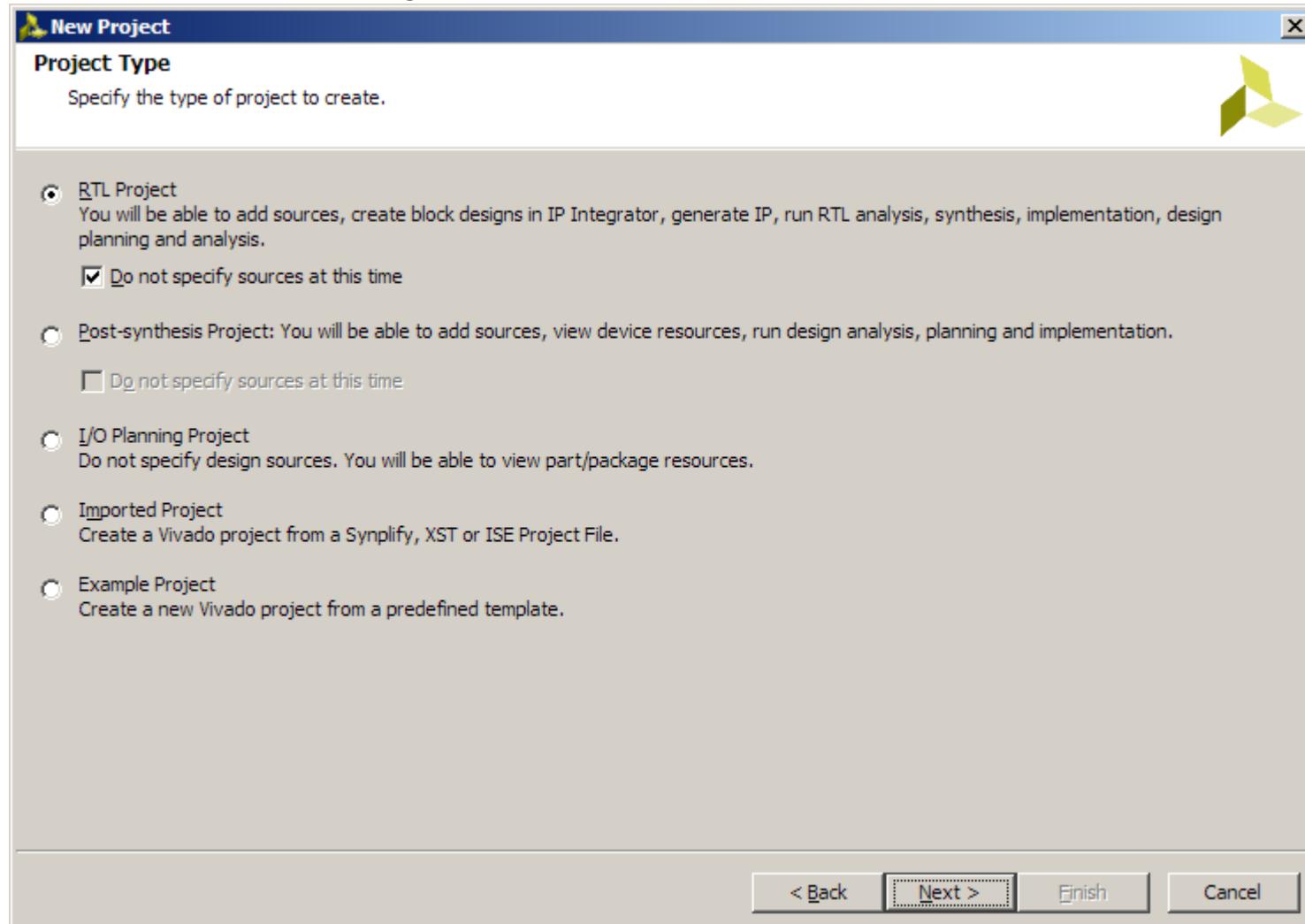
Note: Vivado generally requires forward slashes in paths

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# Generate x8 Gen 2 PCIe Core

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Generate x8 Gen 2 PCIe Core

## ► Select the VC707 Board

The screenshot shows the 'New Project' dialog with the title 'Default Part'. The instructions say 'Choose a default Xilinx part or board for your project. This can be changed later.' Below this, there are two tabs: 'Parts' (selected) and 'Boards'. A 'Filter' section contains dropdown menus for 'Vendor' (All), 'Display Name' (All), and 'Board Rev' (Latest). A 'Reset All Filters' button is also present. A search bar with a magnifying glass icon is below the filters. The main area is a table listing various Xilinx boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfgb676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e	1,156	1.0	520
<b>Virtex-7 VC707 Evaluation Platform</b>	xilinx.com	<b>1.1</b>	<b>xc7vx485tffg1761-2</b>	<b>1,761</b>	<b>1.2</b>	<b>700</b>
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045tffg900-2	900	1.2	362

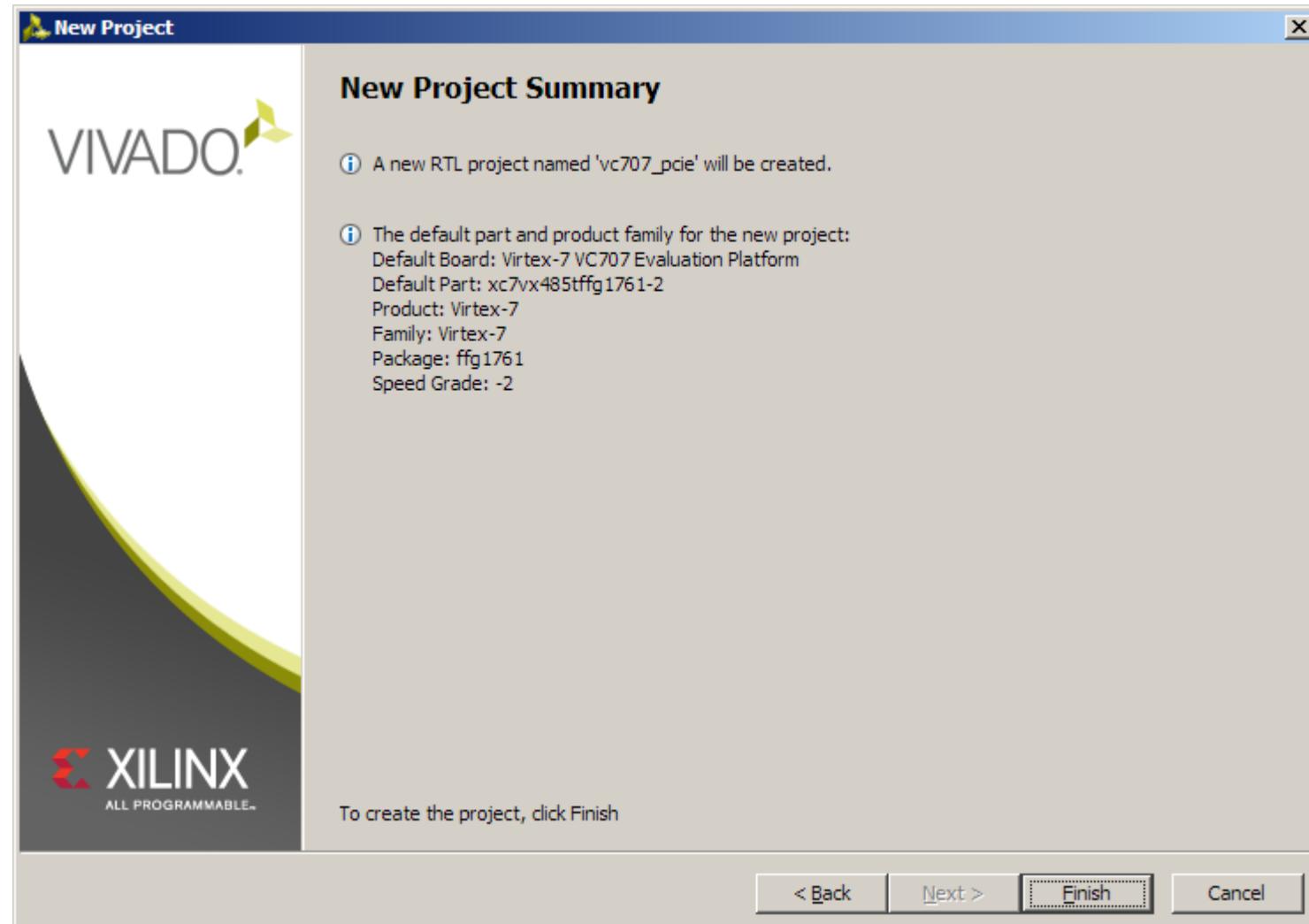
At the bottom are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

Note: Presentation applies to the VC707

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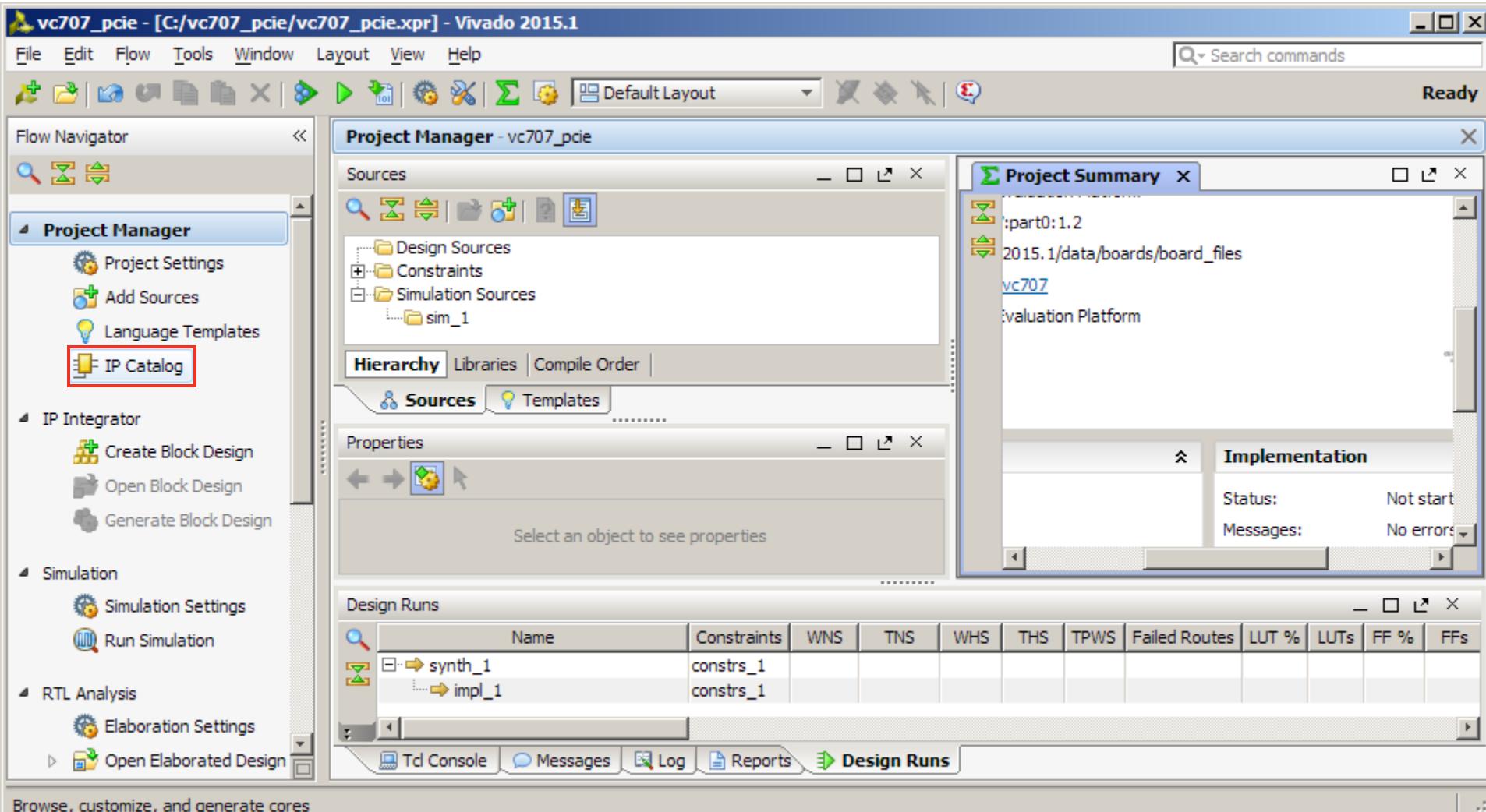
# Generate x8 Gen 2 PCIe Core

► Click Finish



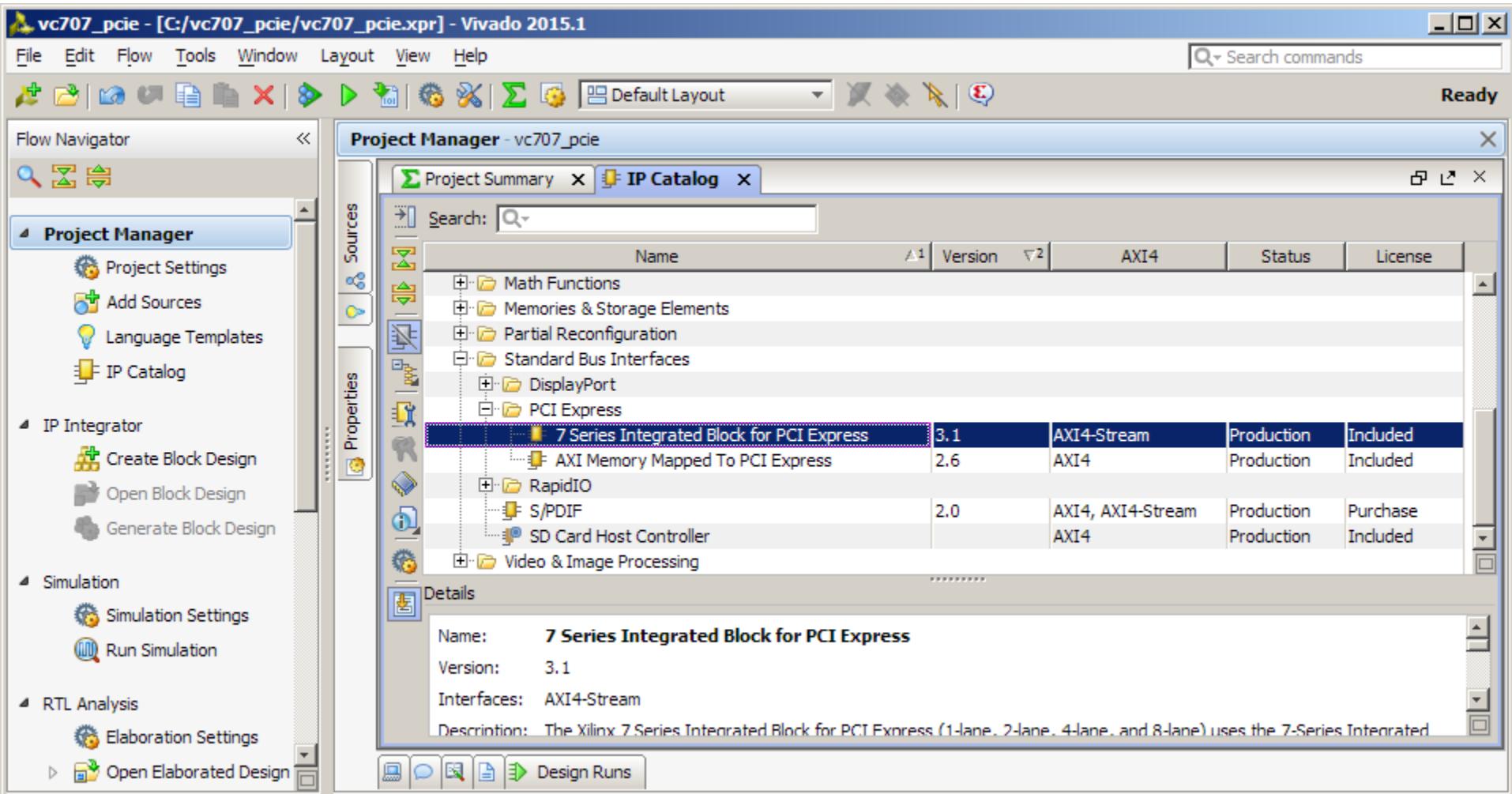
# Generate x8 Gen 2 PCIe Core

► Click on IP Catalog



# Generate x8 Gen 2 PCIe Core

- Select 7 Series Integrated Block for PCI Express, v3.1 under Standard Bus Interfaces



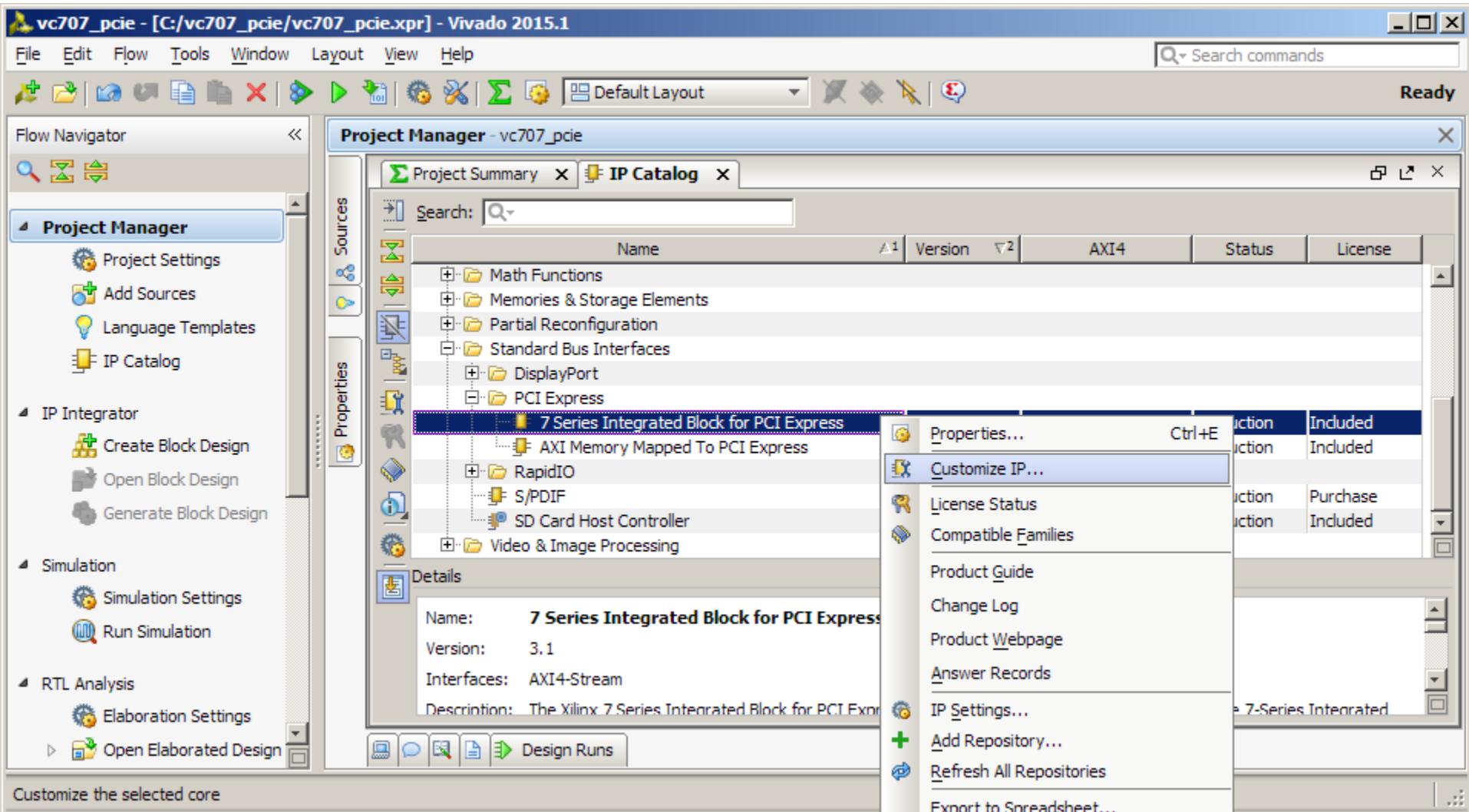
IP: 7 Series Integrated Block for PCI Express

Note: Presentation applies to the VC707

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# Generate x8 Gen 2 PCIe Core

- Right click on 7 Series Integrated Block for PCI Express
  - Select Customize IP

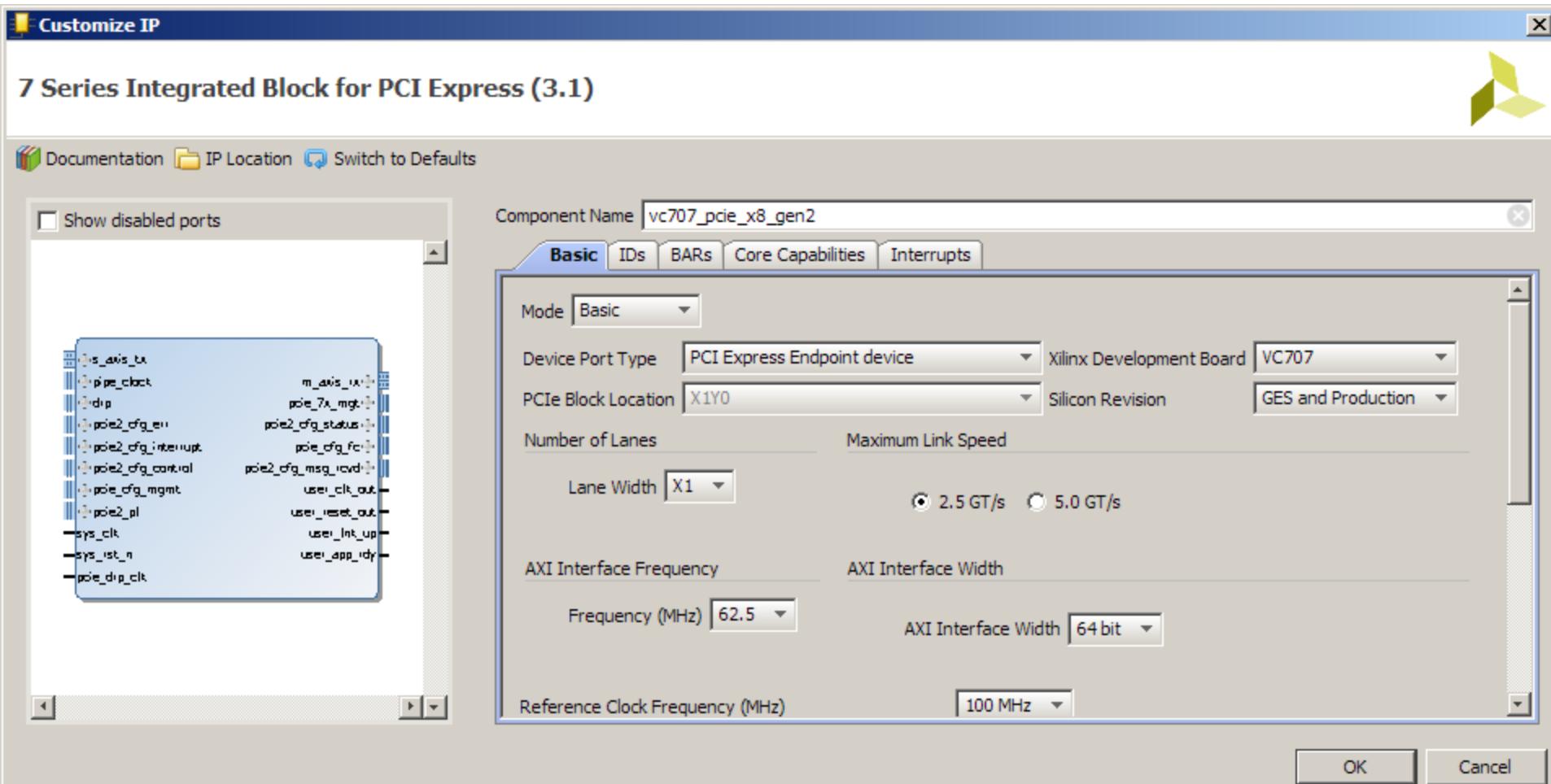


Note: Presentation applies to the VC707

# Generate x8 Gen 2 PCIe Core

► Under the Basic tab,

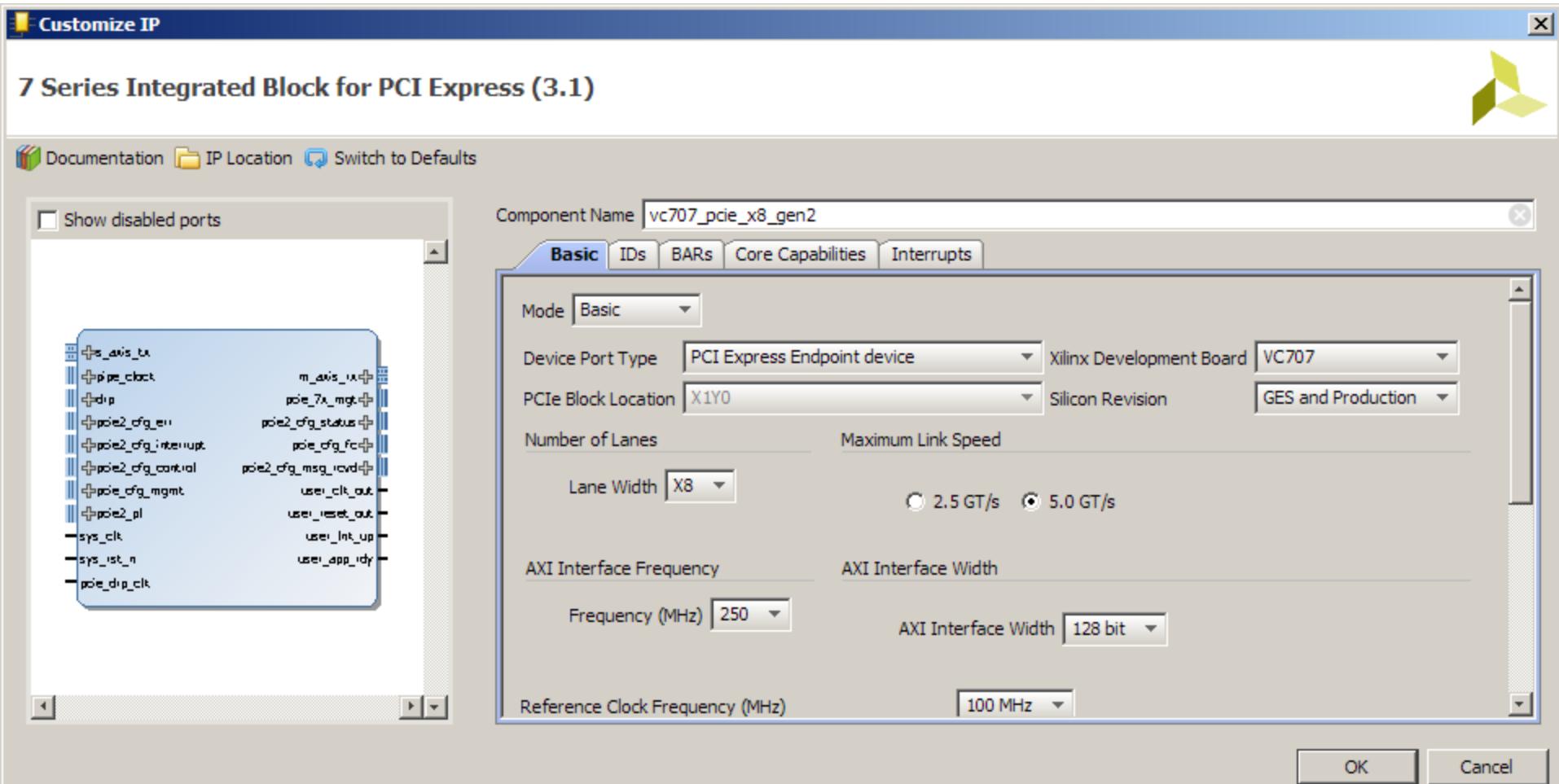
- Set Component name to **vc707\_pcie\_x8\_gen2**
- Set Development Board to **VC707**
- Set Silicon to **GES and Production**



# Generate x8 Gen 2 PCIe Core

## ► Under the Basic tab,

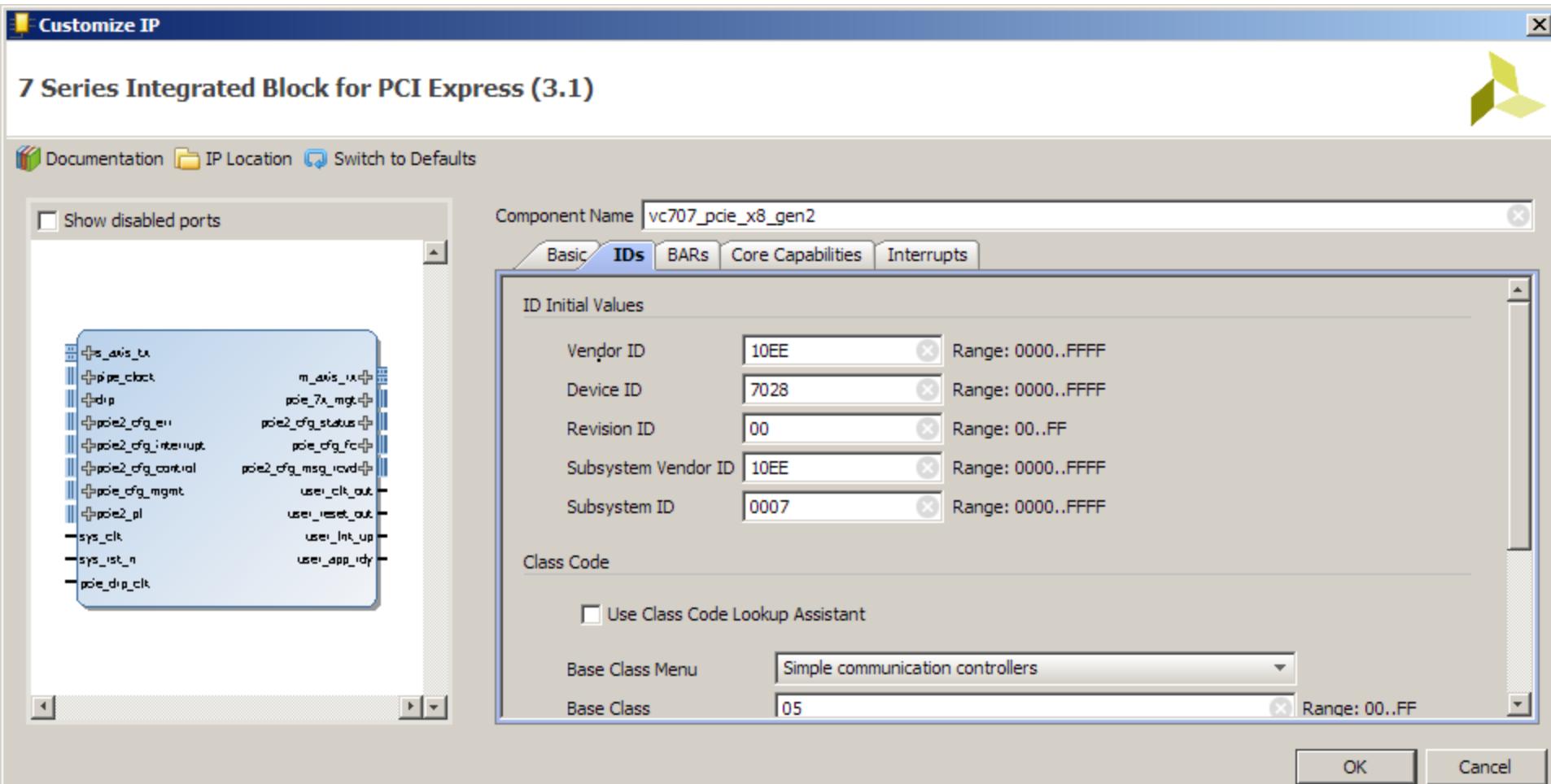
- Set the Lane Width to **X8**
- Set the Max Link Speed to **5 GT/s**
- Set the Ref Clock to **100 MHz**



# Generate x8 Gen 2 PCIe Core

## ► Under the IDs tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **7028**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**

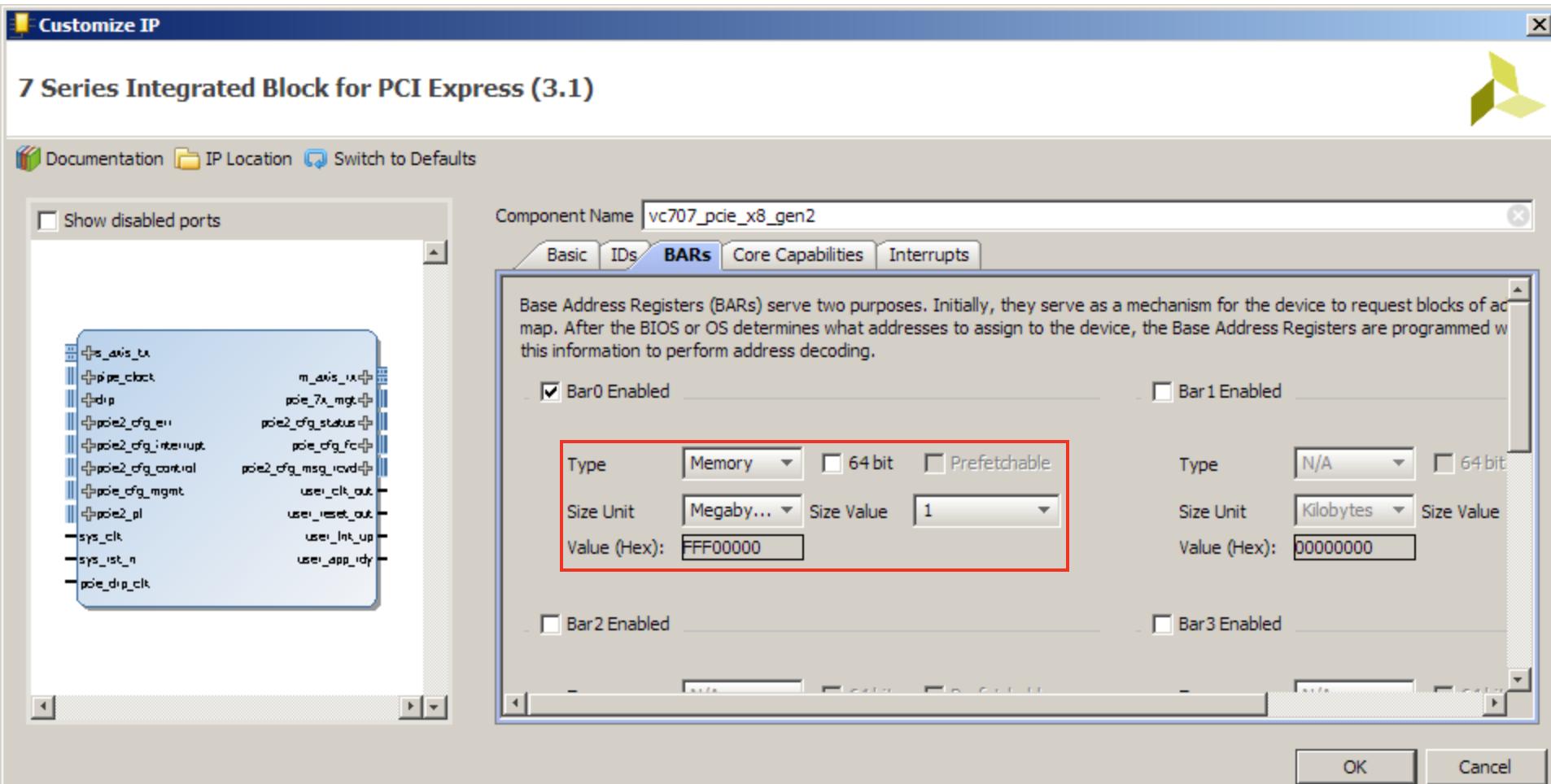


# Generate x8 Gen 2 PCIe Core

► Under the BARs tab, set BAR 0

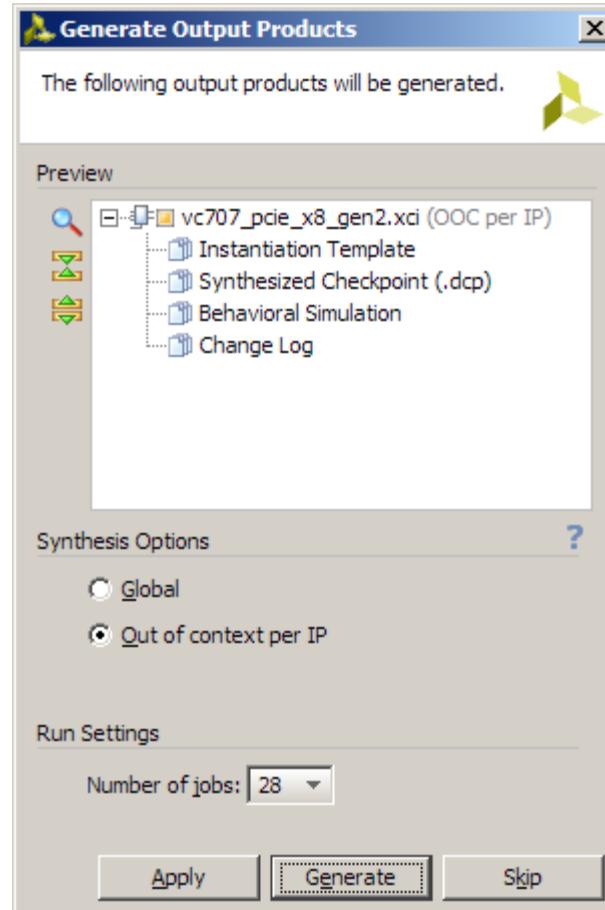
- Set to 1 Megabytes

► Click OK



# Generate x8 Gen 2 PCIe Core

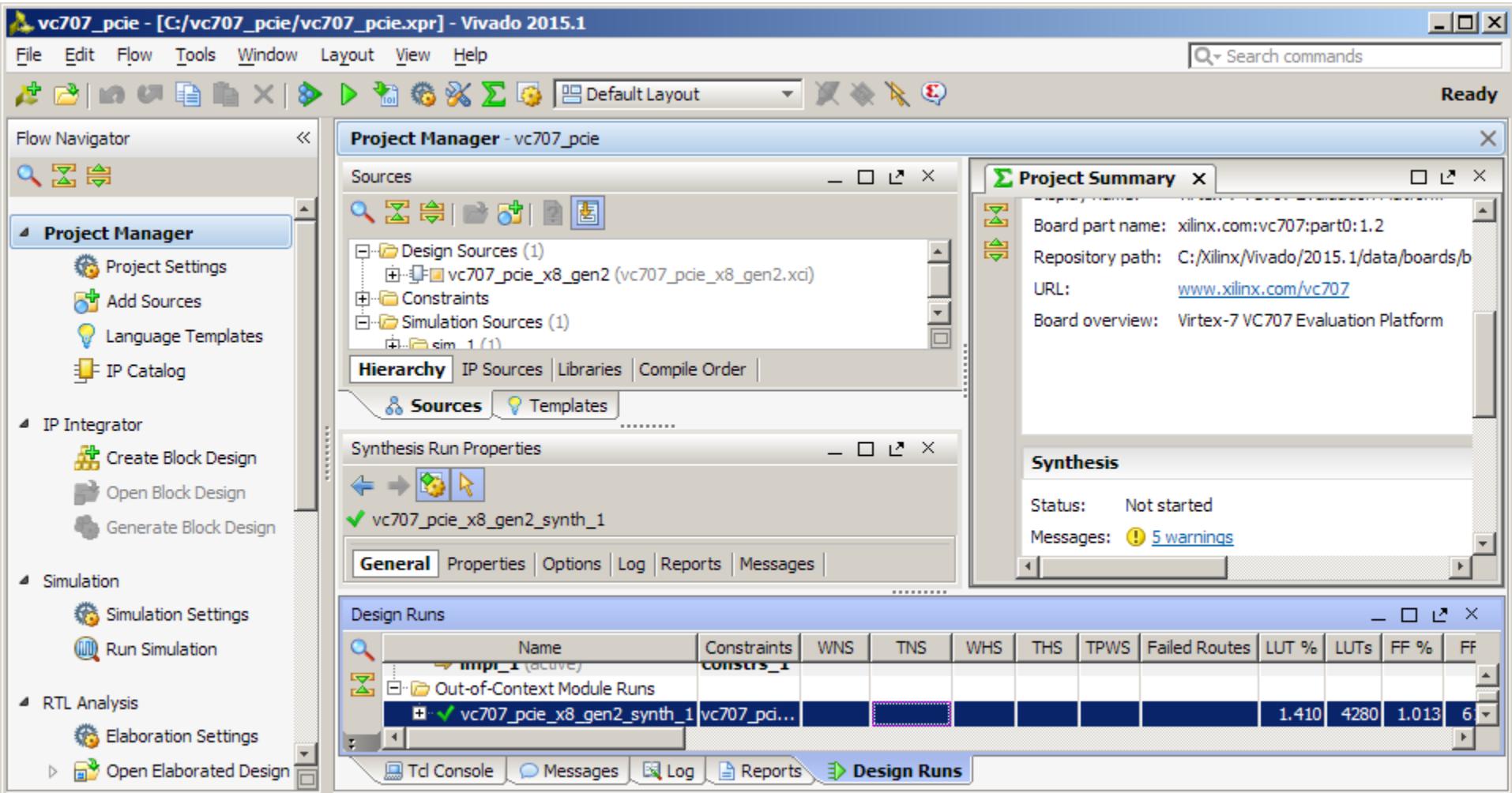
► Click Generate



# Generate x8 Gen 2 PCIe Core

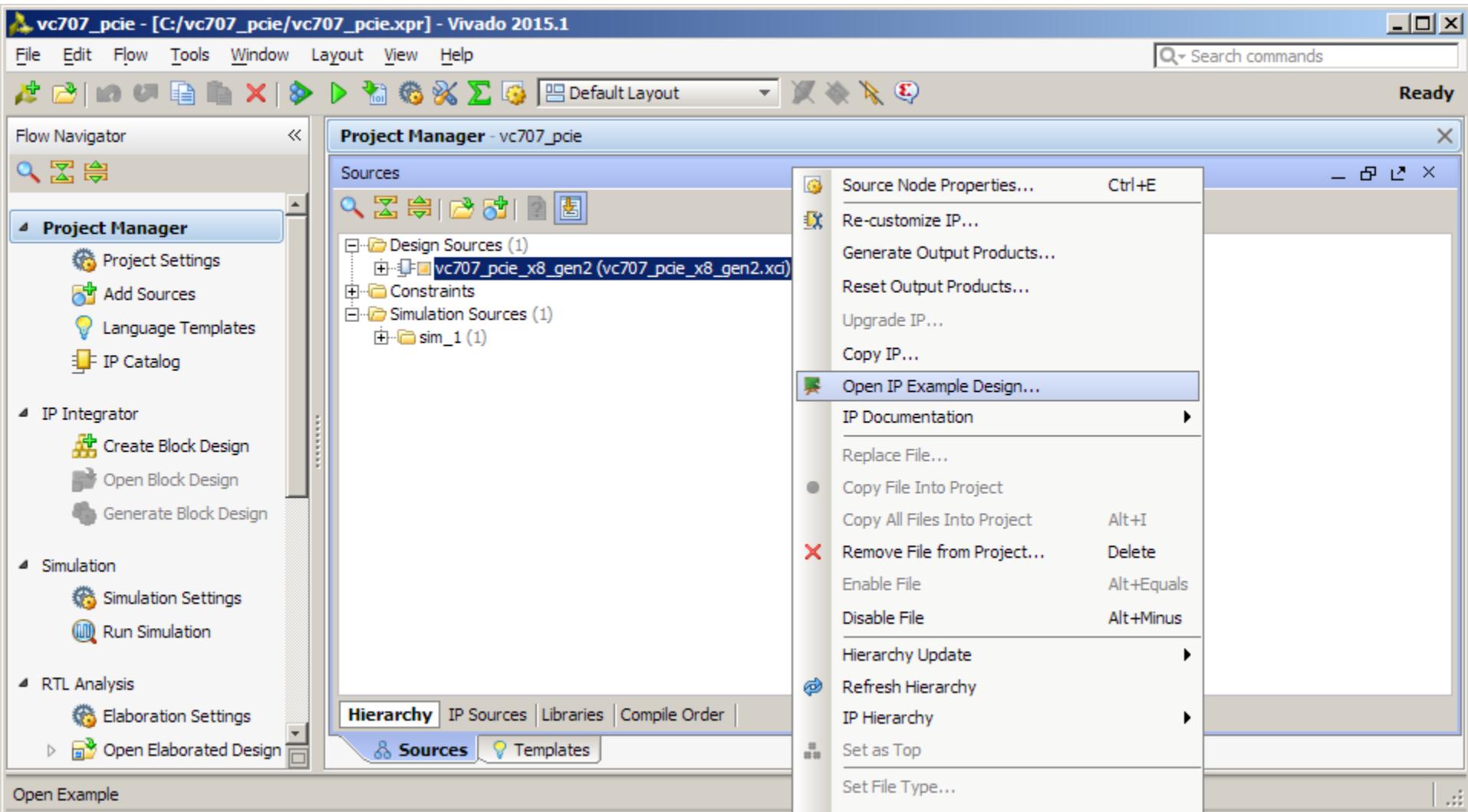
## ► PCIe design appears in Design Sources

- Wait until checkmark appears on vc707\_PCIE\_x8\_gen2\_synth\_1



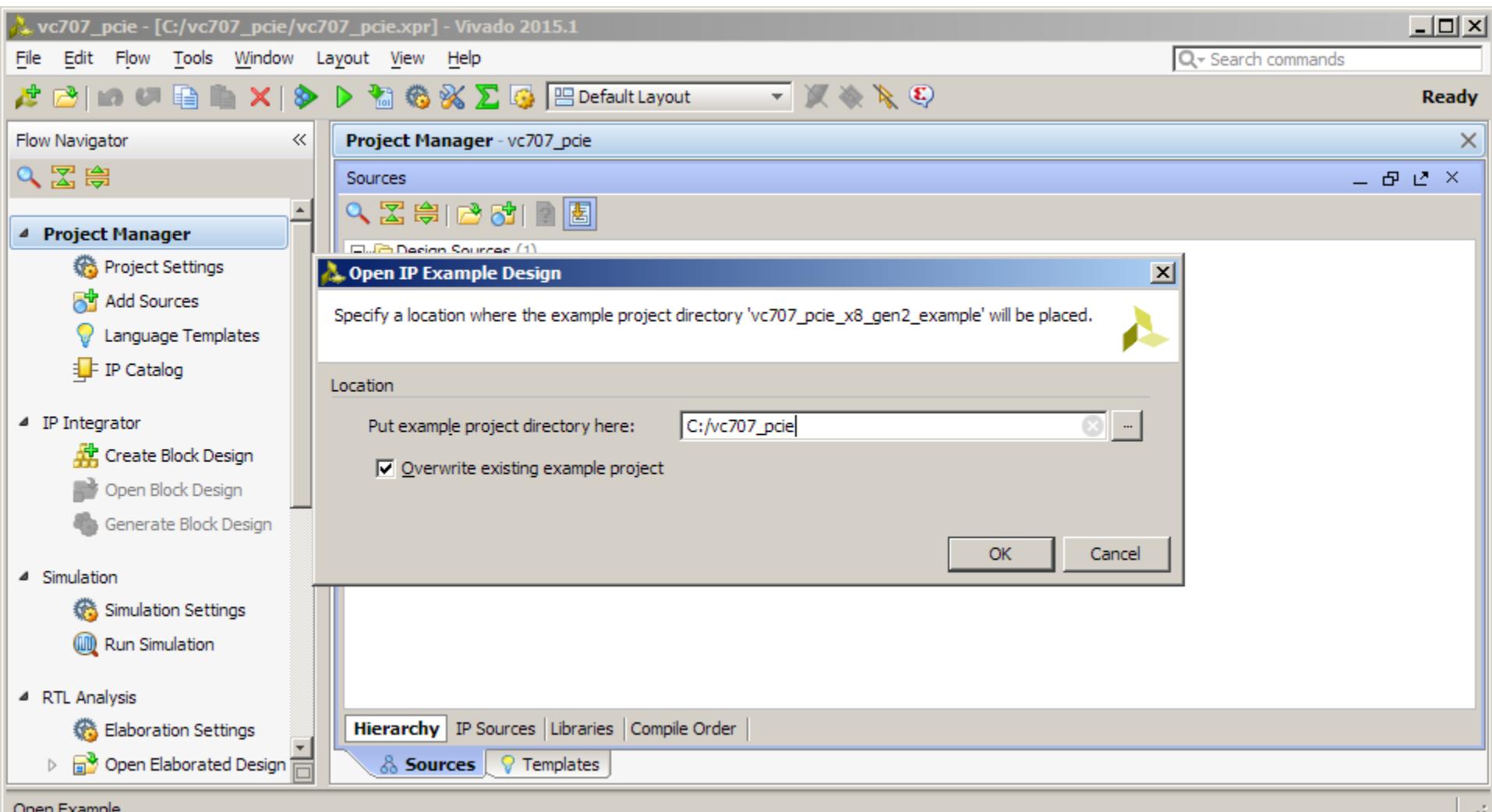
# Generate x8 Gen 2 PCIe Core

- Right-click on vc707\_pcie\_x8\_gen2 and select Open IP Example Design...



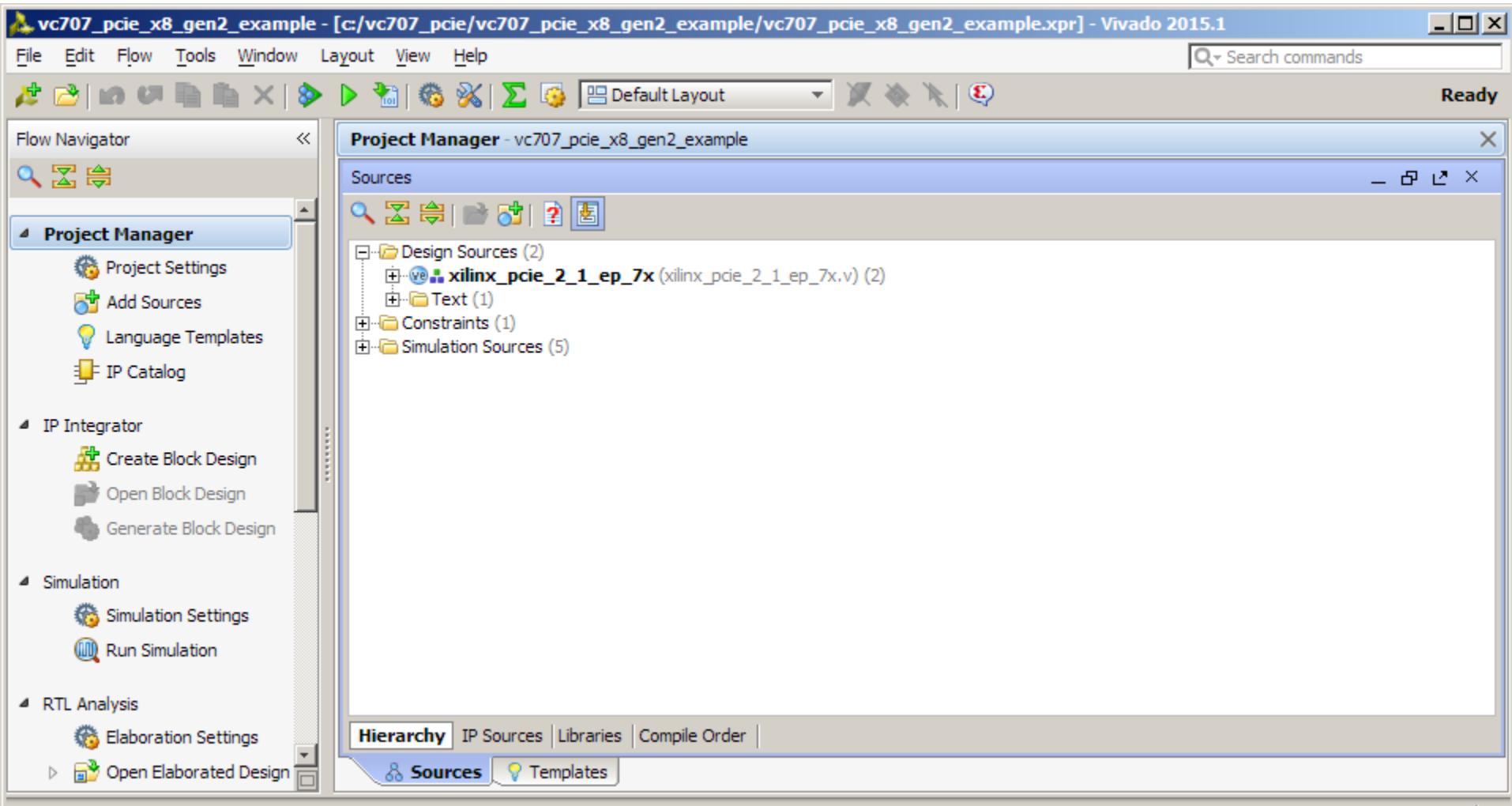
# Generate x8 Gen 2 PCIe Core

► Set the location to C:/vc707\_pcnie and click OK



# Generate x8 Gen 2 PCIe Core

- A new project is created



Note: The original project window can be closed

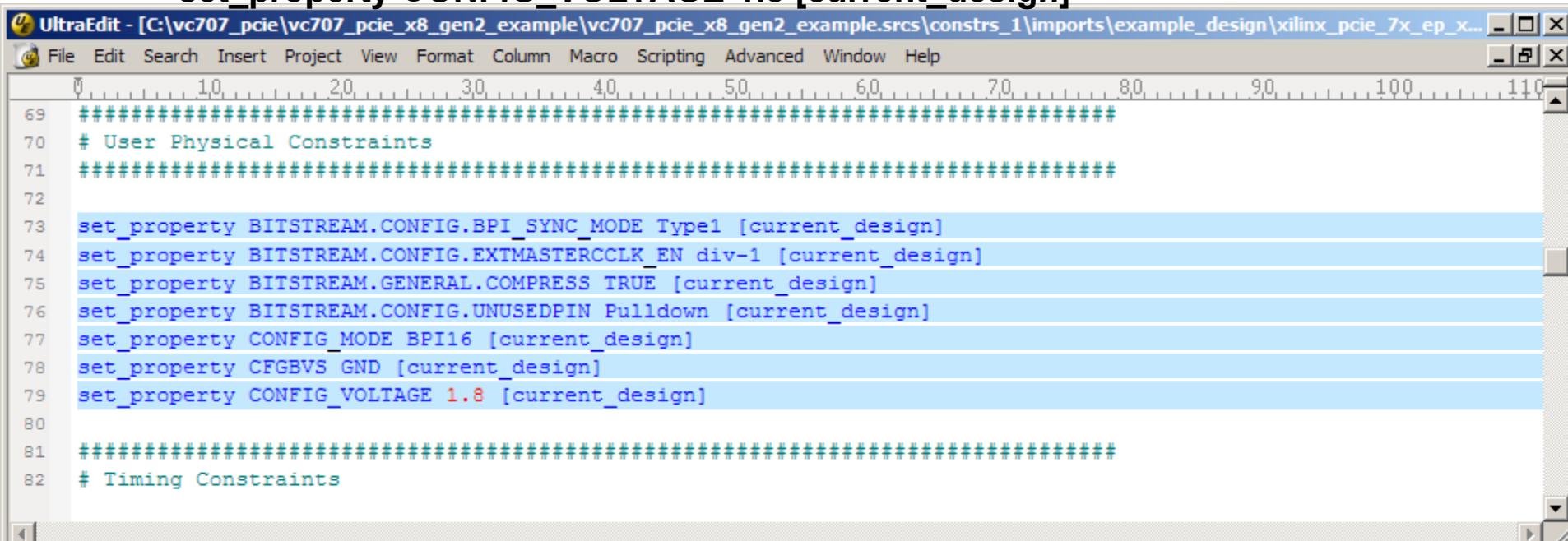
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# Modify PCIe Core

► As per [UG470](#), [UG899](#), [UG908](#), and [G18 Flash](#) specifications

- In the XDC file, `xilinx_pcie_7x_ep_x8g2_VC707.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
```



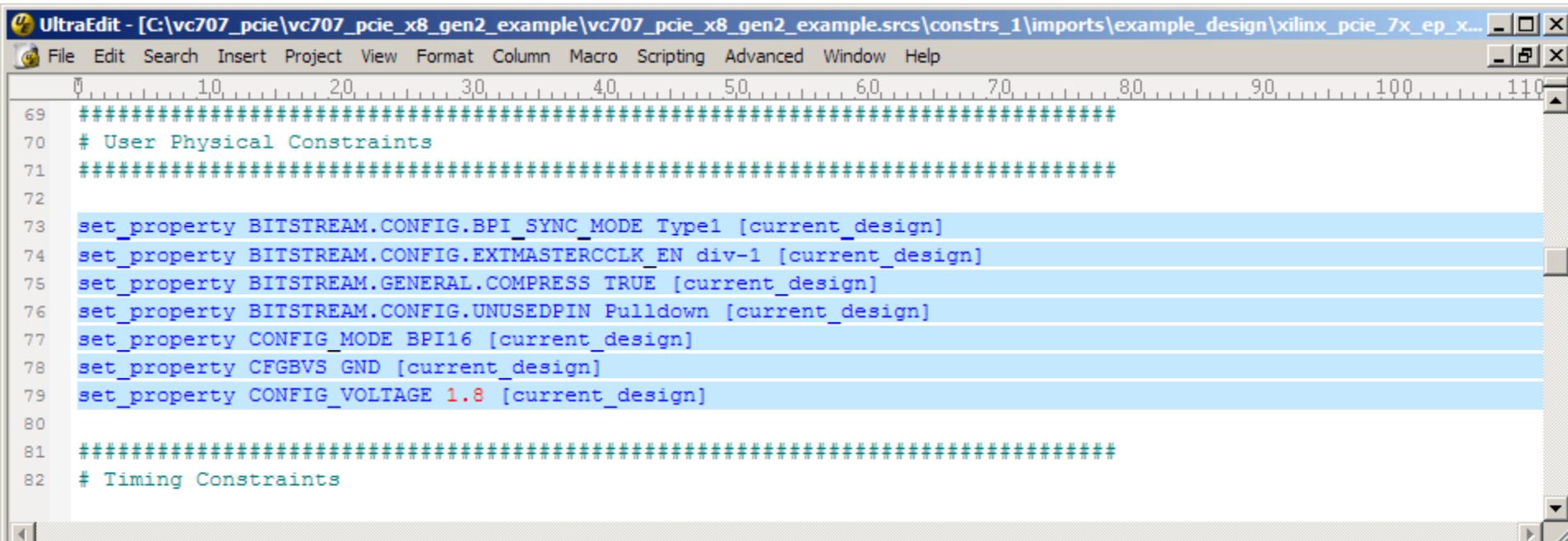
The screenshot shows the UltraEdit text editor displaying an XDC file. The file contains comments for user physical constraints and timing constraints, along with the specified property additions.

```
UltraEdit - [C:\vc707_PCIE\vc707_PCIE_X8_Gen2_Example\vc707_PCIE_X8_Gen2_Example.sr...]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
69 #####
70 # User Physical Constraints
71 #####
72
73 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
74 set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
75 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
76 set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
77 set_property CONFIG_MODE BPI16 [current_design]
78 set_property CFGBVS GND [current_design]
79 set_property CONFIG_VOLTAGE 1.8 [current_design]
80
81 #####
82 # Timing Constraints
```

# Modify PCIe Core

## ► Details on the XDC constraints:

- G18 Maximum Frequency: 108 MHz; VC707 EMCCLK Frequency: 80 MHz
- **BITSTREAM.CONFIG.BPI\_SYNC\_MODE Type1**: For Numonyx G18 Family
- **BITSTREAM.CONFIG.EXTMMASTERCCLK\_EN div-1**: Sets the EMCCLK in the FPGA to divide by 1, which meets the G18 Maximum Frequency specification
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream



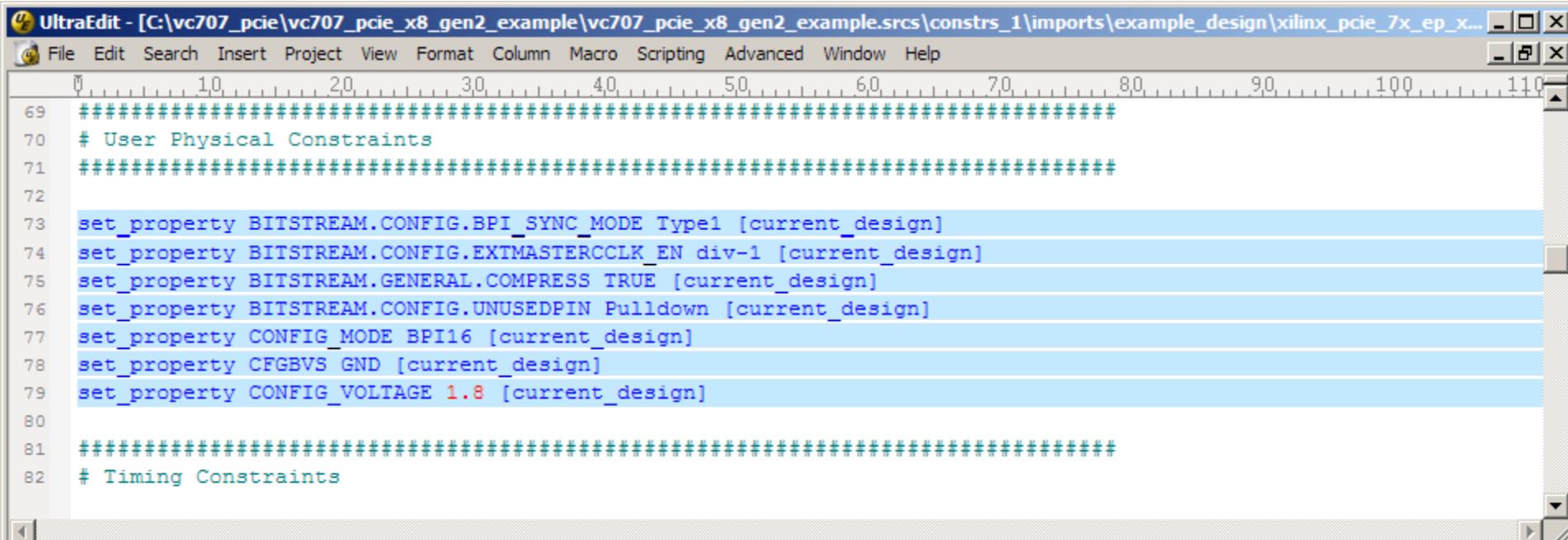
The screenshot shows a Windows application window titled "UltraEdit - [C:\vc707\_pcnie\vc707\_pcnie\_x8\_gen2\_example\vc707\_pcnie\_x8\_gen2\_example.srcts\constrs\_1\imports\example\_design\xilinx\_pcnie\_7x\_ep\_x...]" with a file size of 110 KB. The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The status bar at the bottom shows line numbers from 69 to 82. The code area contains XDC constraint properties:

```
# User Physical Constraints
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
# Timing Constraints
```

# Modify PCIe Core

## ► Details on the XDC constraints:

- **BITSTREAM.CONFIG.UNUSEDPIN Pullup**: Sets unused pins to be pulled up
- **CONFIG\_MODE BPI16**: The BPI is 16 bits wide
- **CFGVBVS GND**: Set to GND when CONFIG\_VOLTAGE is either 1.5 or 1.8 V
- **CONFIG\_VOLTAGE 1.8**: The KC705 Configuration Bank (Bank 0) voltage is connected to 1.8 V

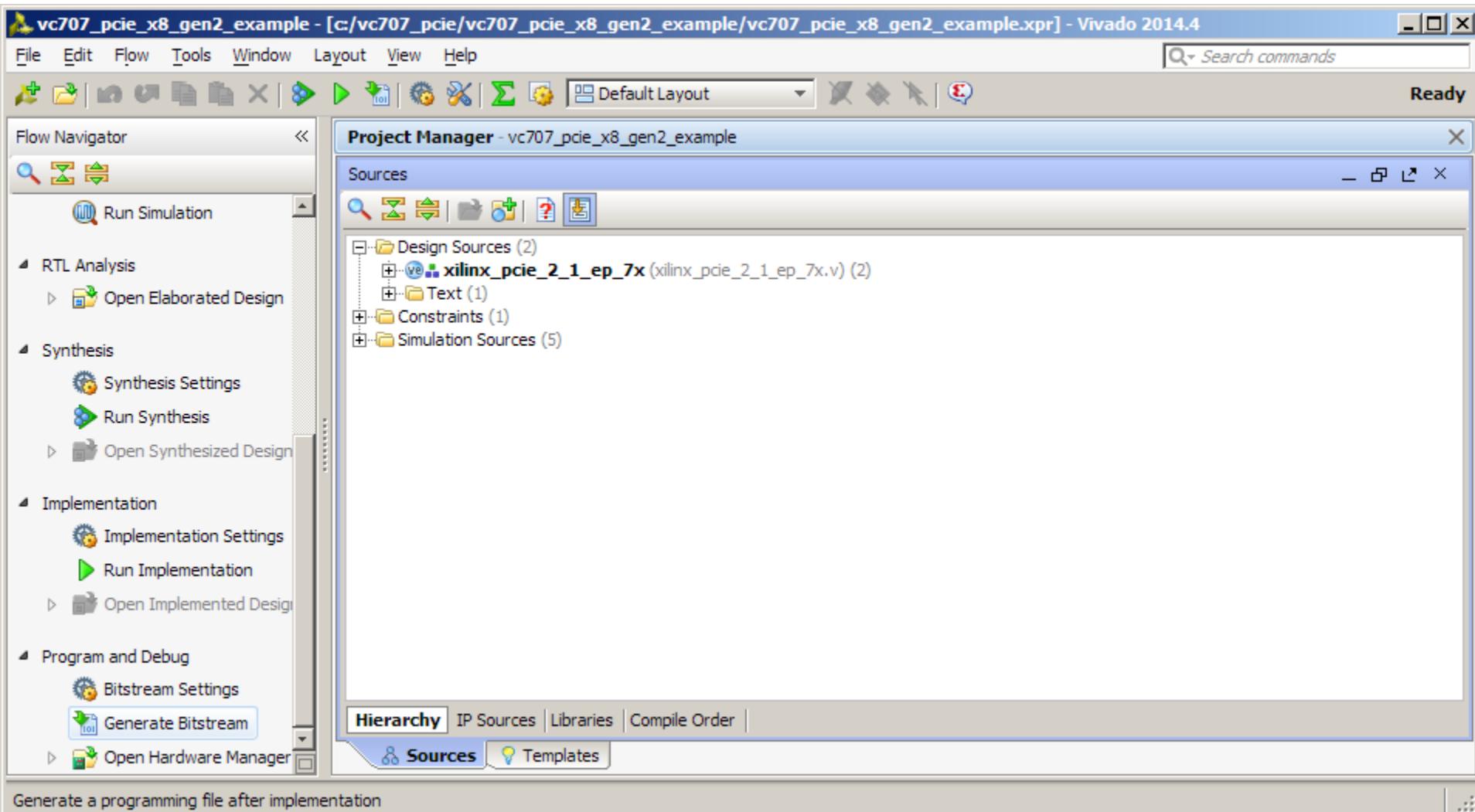


The screenshot shows a Windows application window titled "UltraEdit - [C:\vc707\_pcie\vc707\_pcie\_x8\_gen2\_example\vc707\_pcie\_x8\_gen2\_example.srcs\constrs\_1\imports\example\_design\xilinx\_pcie\_7x\_ep\_x...]" with a status bar indicating "Line 110". The main area displays XDC constraint code. The code includes sections for User Physical Constraints and Timing Constraints, defining properties for bitstream configuration and timing.

```
UltraEdit - [C:\vc707_pcie\vc707_pcie_x8_gen2_example\vc707_pcie_x8_gen2_example.srcs\constrs_1\imports\example_design\xilinx_pcie_7x_ep_x...
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
10 20 30 40 50 60 70 80 90 100 110
69 ######
70 # User Physical Constraints
71 #####
72
73 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
74 set_property BITSTREAM.CONFIG.EXTMASTERCLK_EN div-1 [current_design]
75 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
76 set_property BITSTREAM.CONFIG.UNUSEDPIN Pulldown [current_design]
77 set_property CONFIG_MODE BPI16 [current_design]
78 set_property CFGVBVS GND [current_design]
79 set_property CONFIG_VOLTAGE 1.8 [current_design]
80
81 #####
82 # Timing Constraints
```

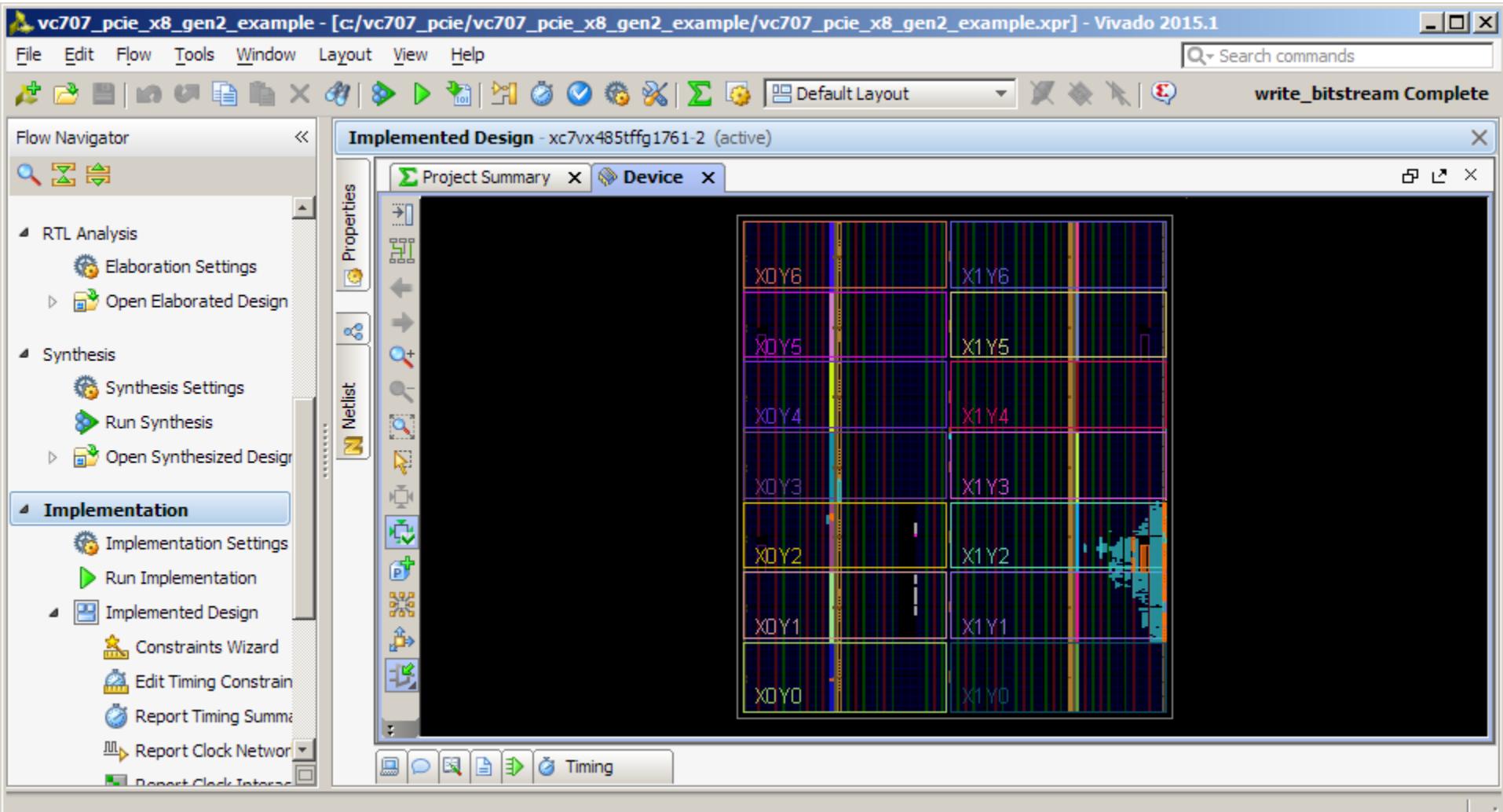
# Compile Example Design

► Click on Generate Bitstream



# Compile Example Design

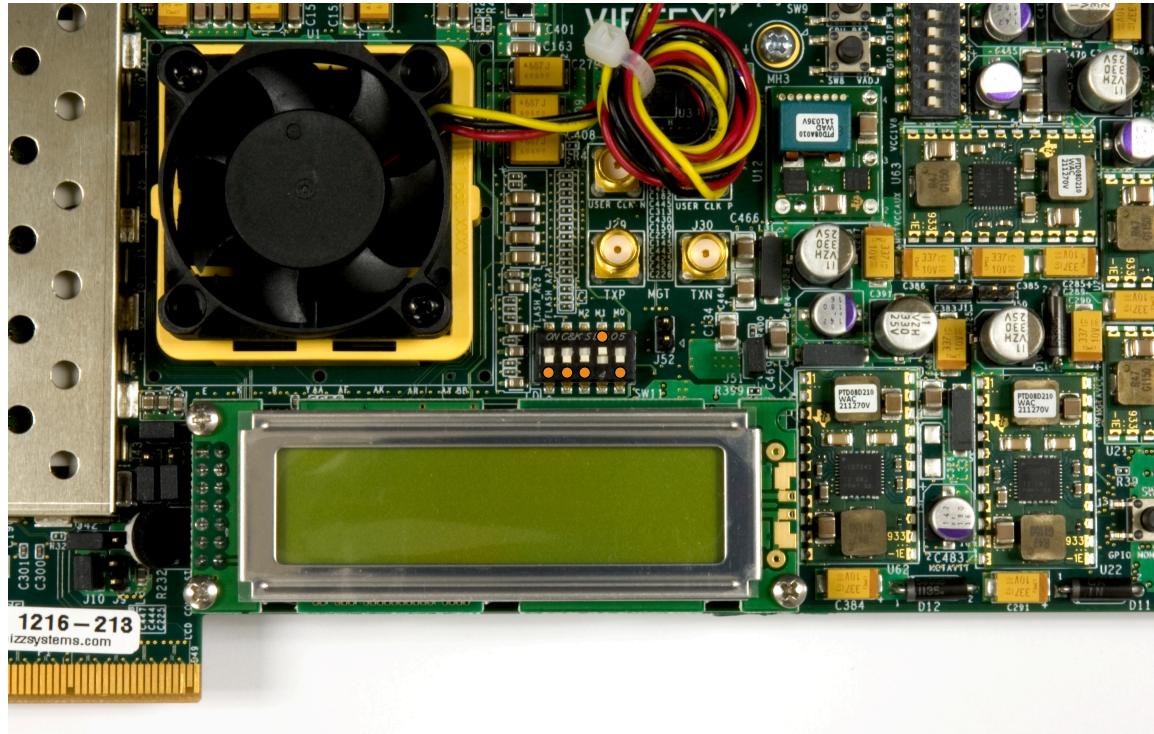
► Open and view the Implemented Design



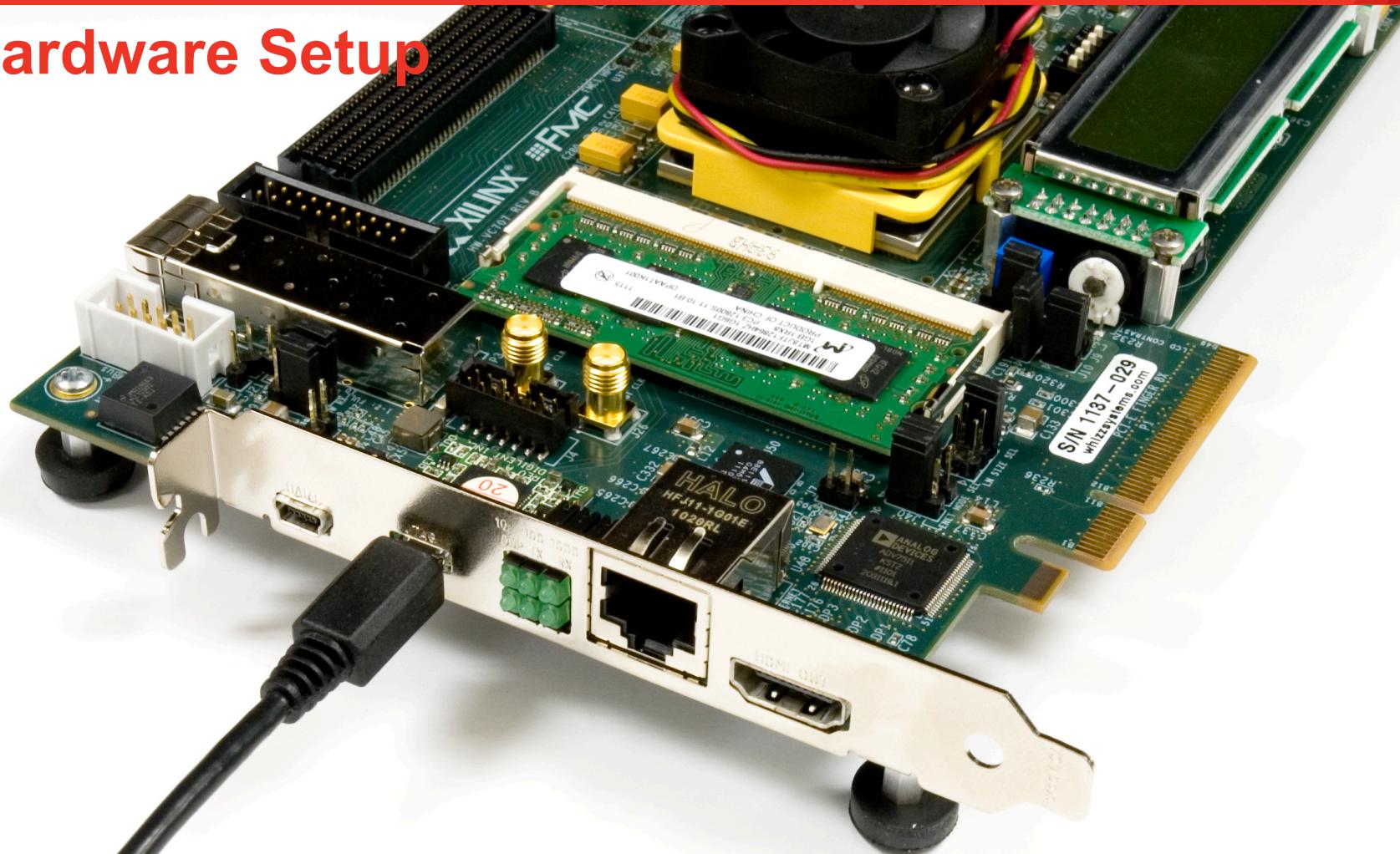
# Hardware Setup

## ► Set SW11 to 00010 (1 = on, Position 1 → Position 5, left to right)

- This enables Master BPI configuration from the Linear Flash
  - Flash A25, A24 = 00
  - FPGA mode pins M[2:0] = 010



# Hardware Setup

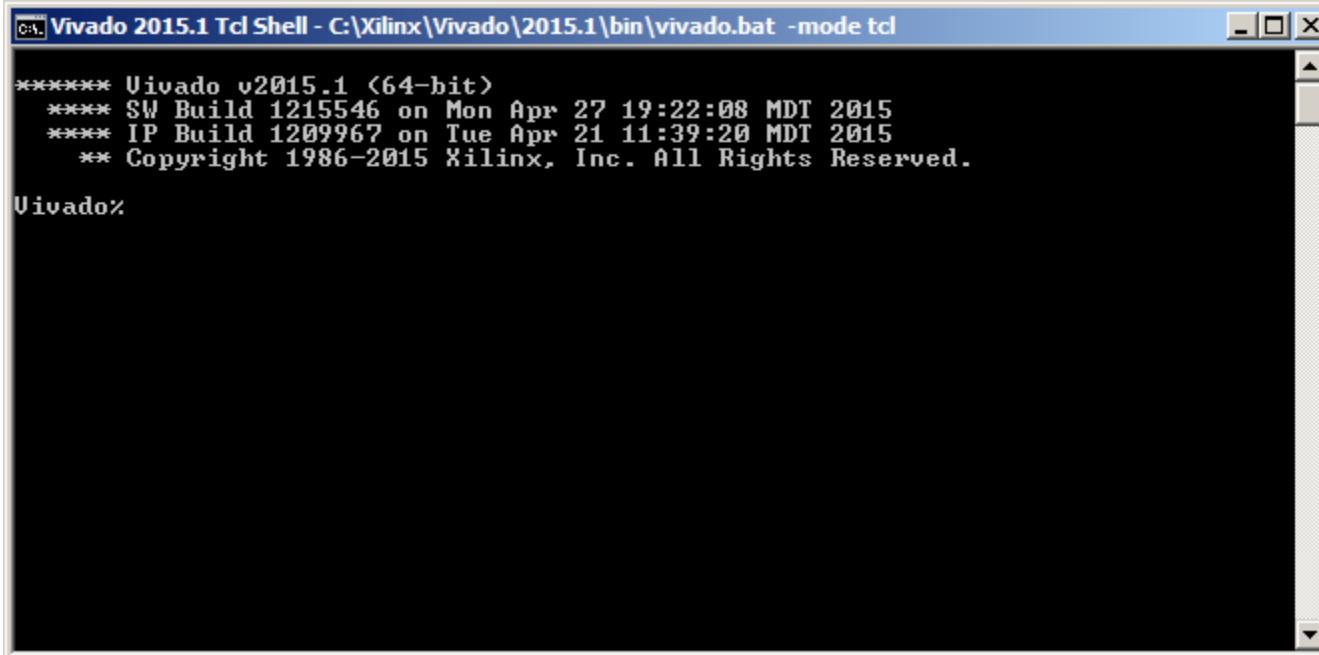


- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC707 board**
  - Connect this cable to your PC
  - Power on the VC707 board

# Generate PCIe MCS File

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2015.1 →  
Vivado 2015.1 Tcl Shell**



The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following startup text:

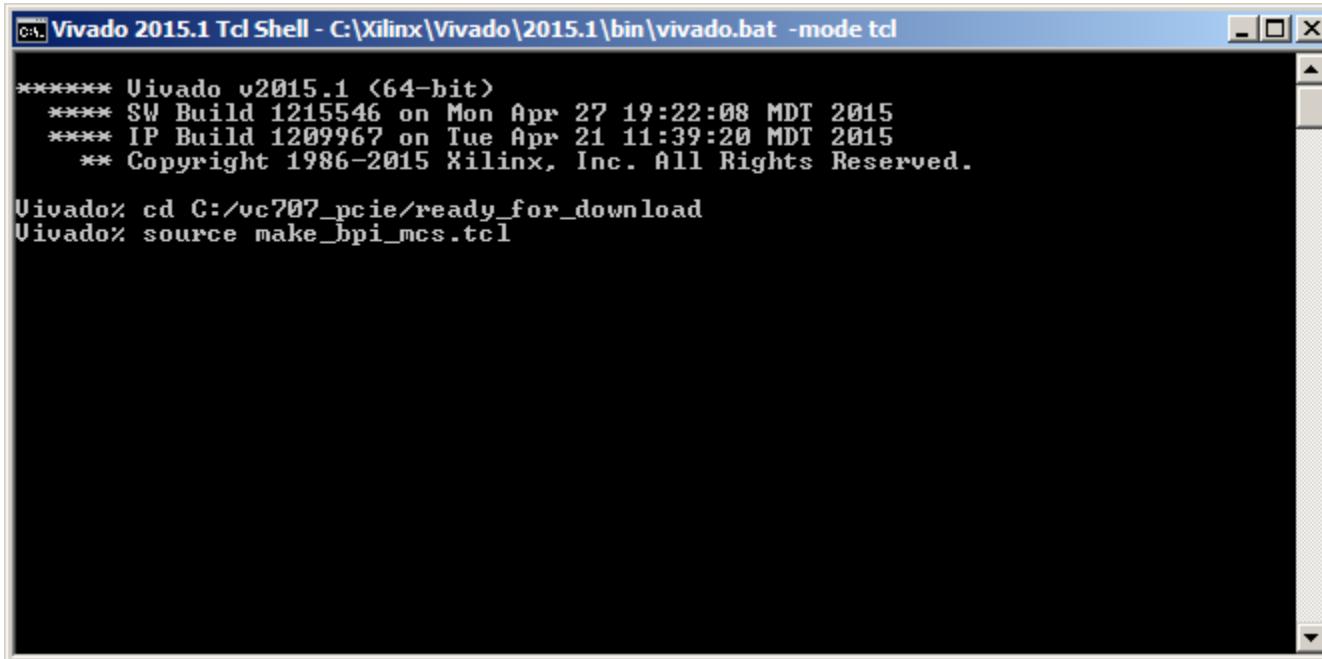
```
***** Vivado v2015.1 (64-bit)
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.
```

The prompt "Vivado%" is visible at the bottom of the window.

# Generate PCIe MCS File

- In the Vivado Tcl Shell type:

```
cd C:/vc707_pcie/ready_for_download  
source make_bpi_mcs.tcl
```



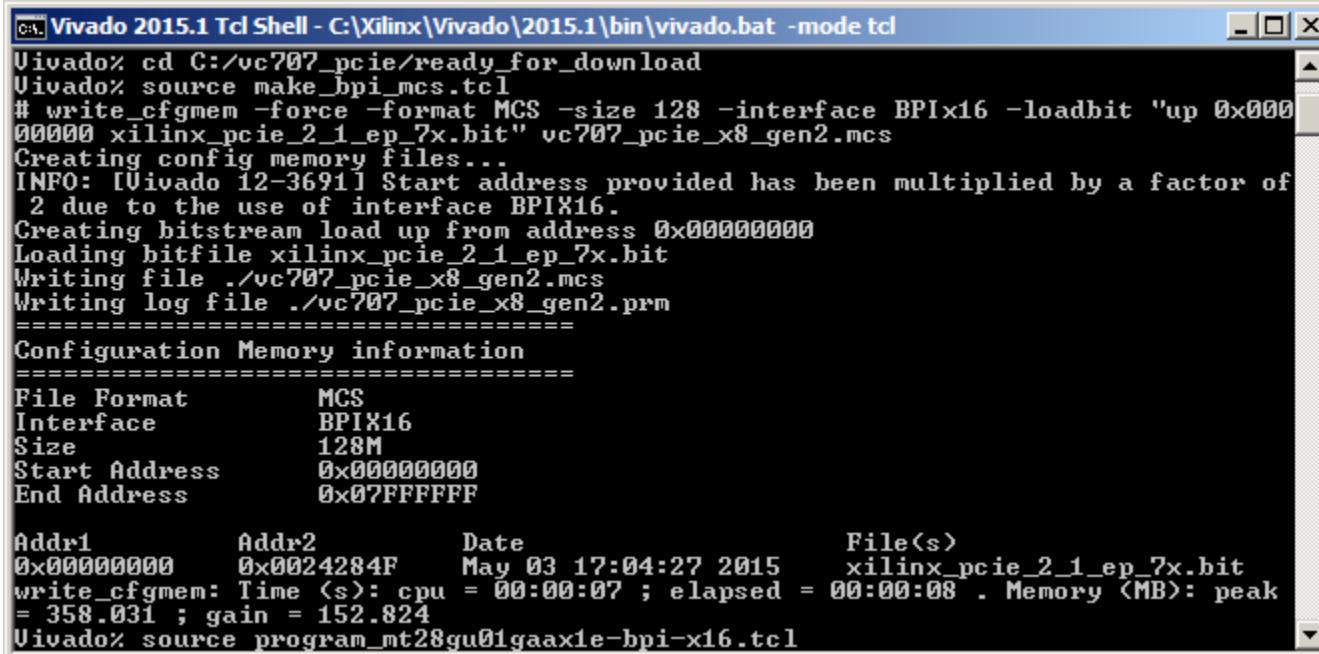
The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vc707_pcie/ready_for_download  
Vivado> source make_bpi_mcs.tcl
```

# Program BPI Flash with PCIe Design

- In the Vivado Tcl Shell type:

```
source program_mt28gu01gaax1e-bpi-x16.tcl
```



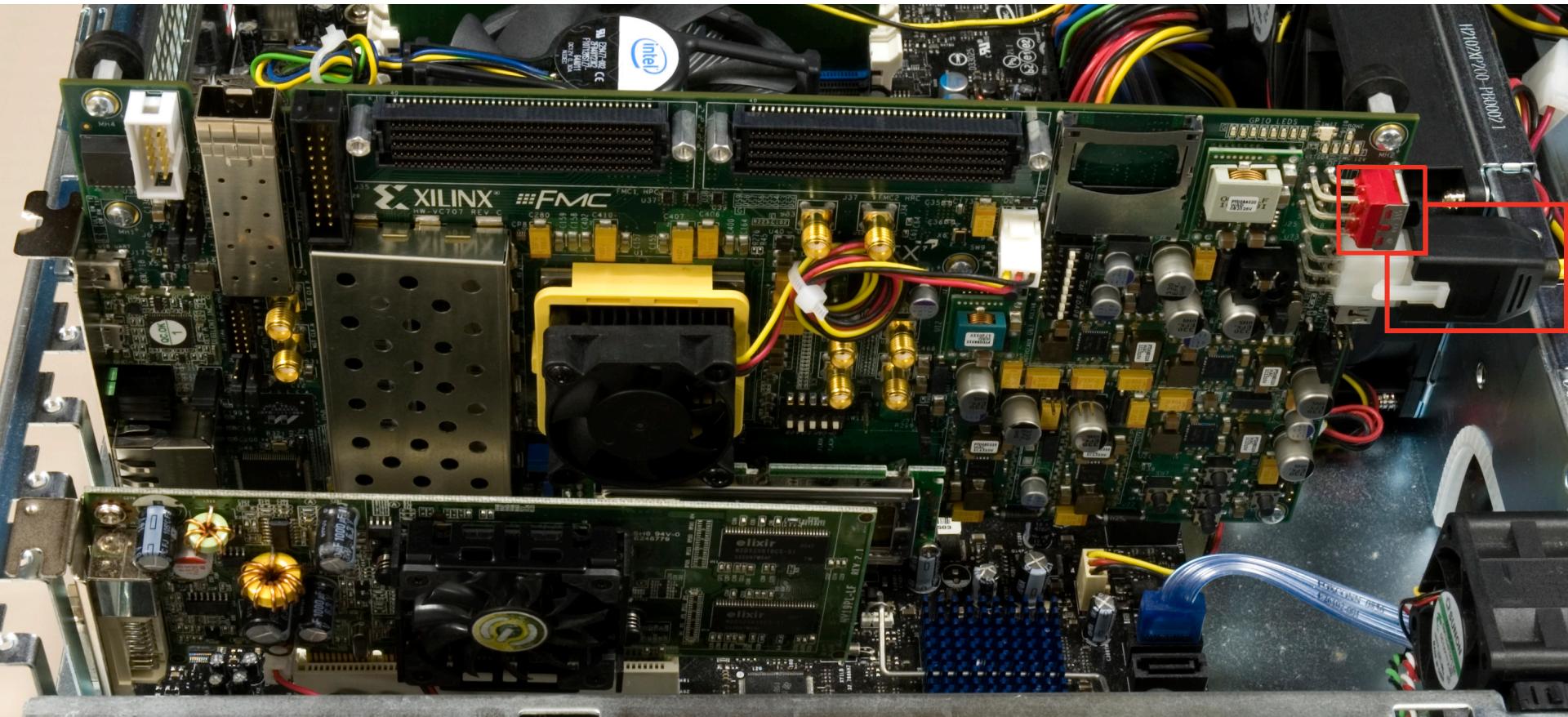
```
Vivado% cd C:/vc707_pcie/ready_for_download
Vivado% source make_bpi_mcs.tcl
# write_cfmem -force -format MCS -size 128 -interface BPIx16 -loadbit "up 0x00000000 xilinx_pcie_2_1_ep_7x.bit" vc707_pcie_x8_gen2.mcs
Creating config memory files...
INFO: [Vivado 12-3691] Start address provided has been multiplied by a factor of 2 due to the use of interface BPIX16.
Creating bitstream load up from address 0x00000000
Loading bitfile xilinx_pcie_2_1_ep_7x.bit
Writing file ./vc707_pcie_x8_gen2.mcs
Writing log file ./vc707_pcie_x8_gen2.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        BPIX16
Size            128M
Start Address   0x00000000
End Address     0x07FFFFFF

Addr1      Addr2      Date           File(s)
0x00000000  0x0024284F  May 03 17:04:27 2015  xilinx_pcie_2_1_ep_7x.bit
write_cfmem: Time <s>: cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 358.031 ; gain = 152.824
Vivado% source program_mt28gu01gaax1e-bpi-x16.tcl
```

# Hardware Setup

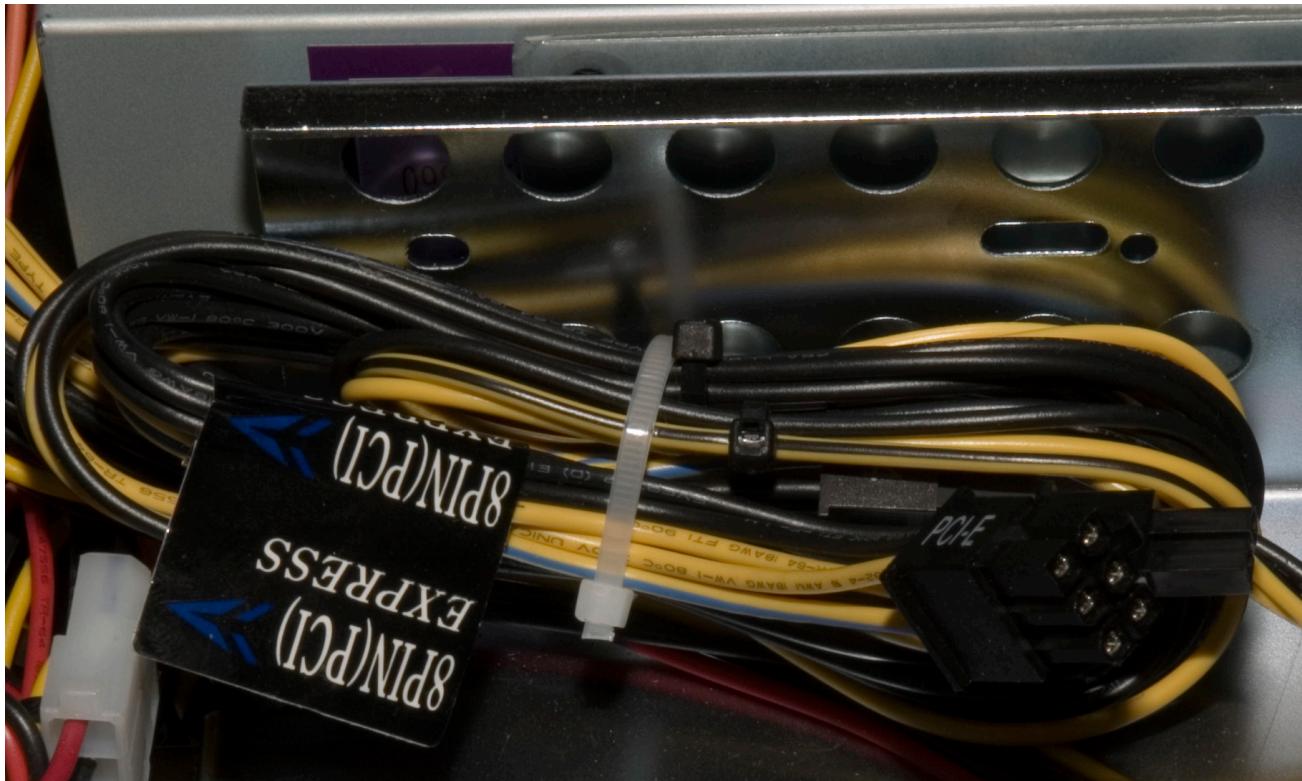
## ► Insert the VC707 Board into a PCIe slot

- Use the included PC Power adapter; turn on Power Switch



# Hardware Setup

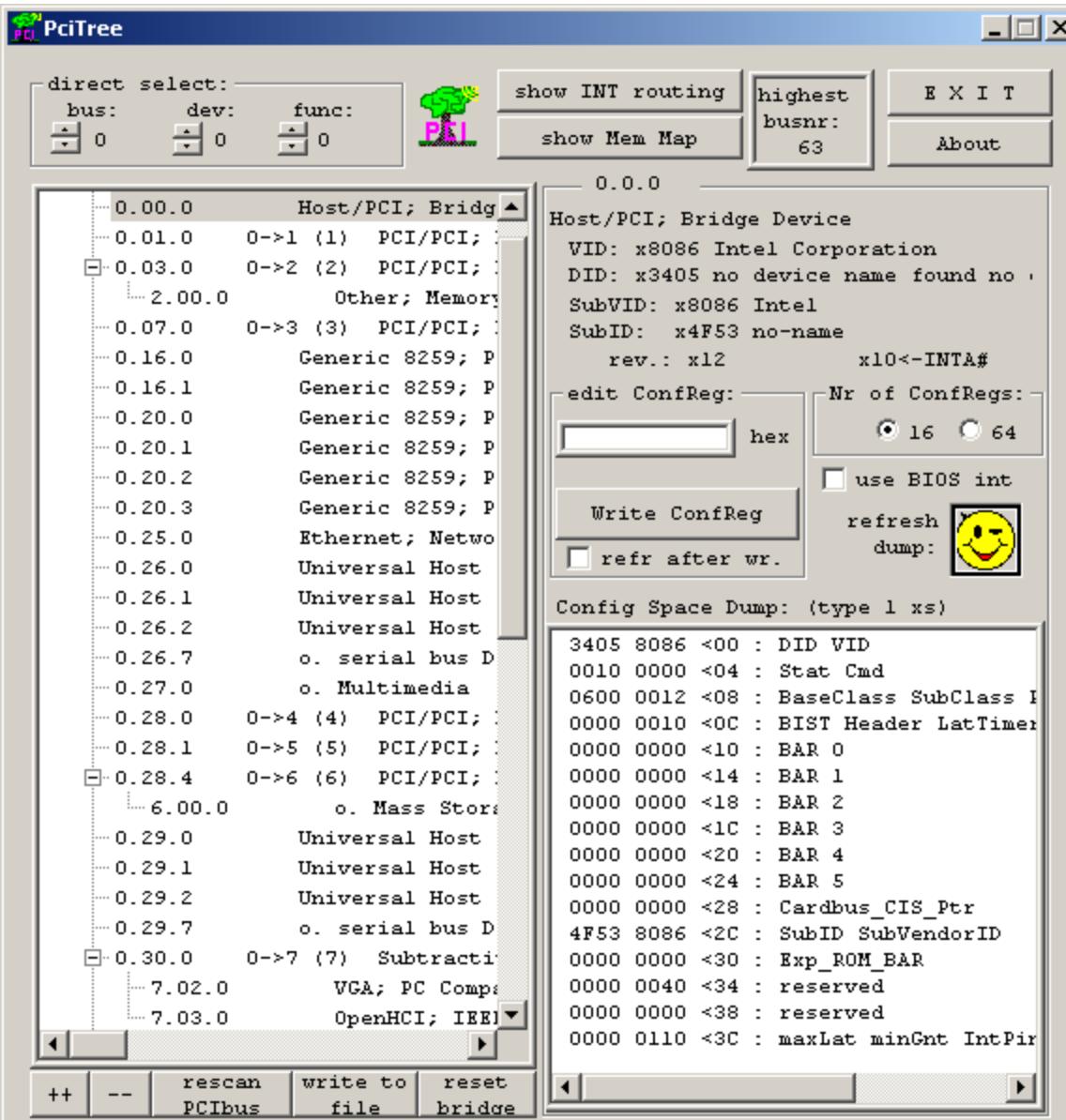
- Do not use the PCIe connector from the PC power supply



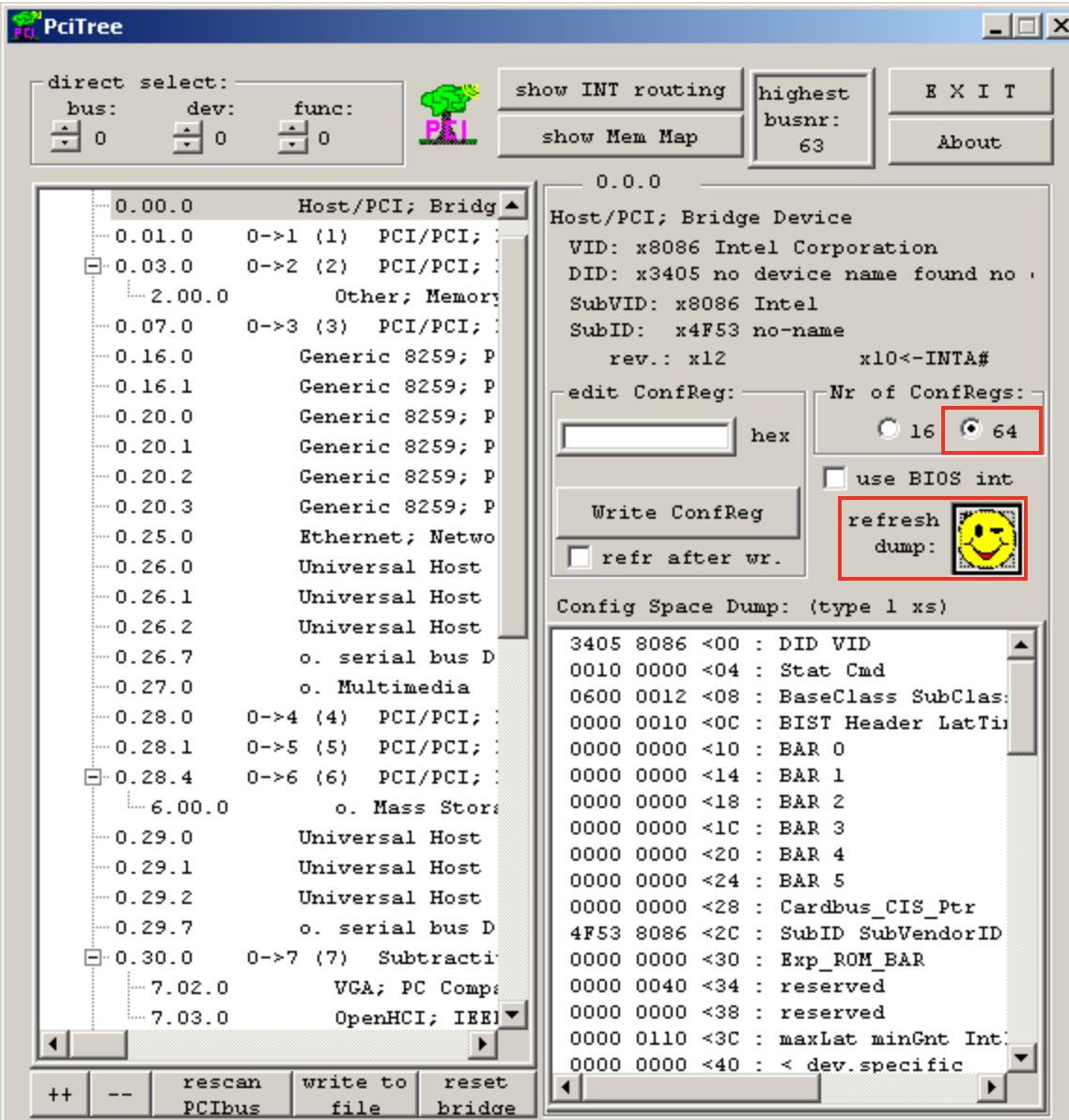
# Running the PCIe x8 Gen 2 Design

► Power on the PC

► Start PciTree



# Running the PCIe x8 Gen 2 Design

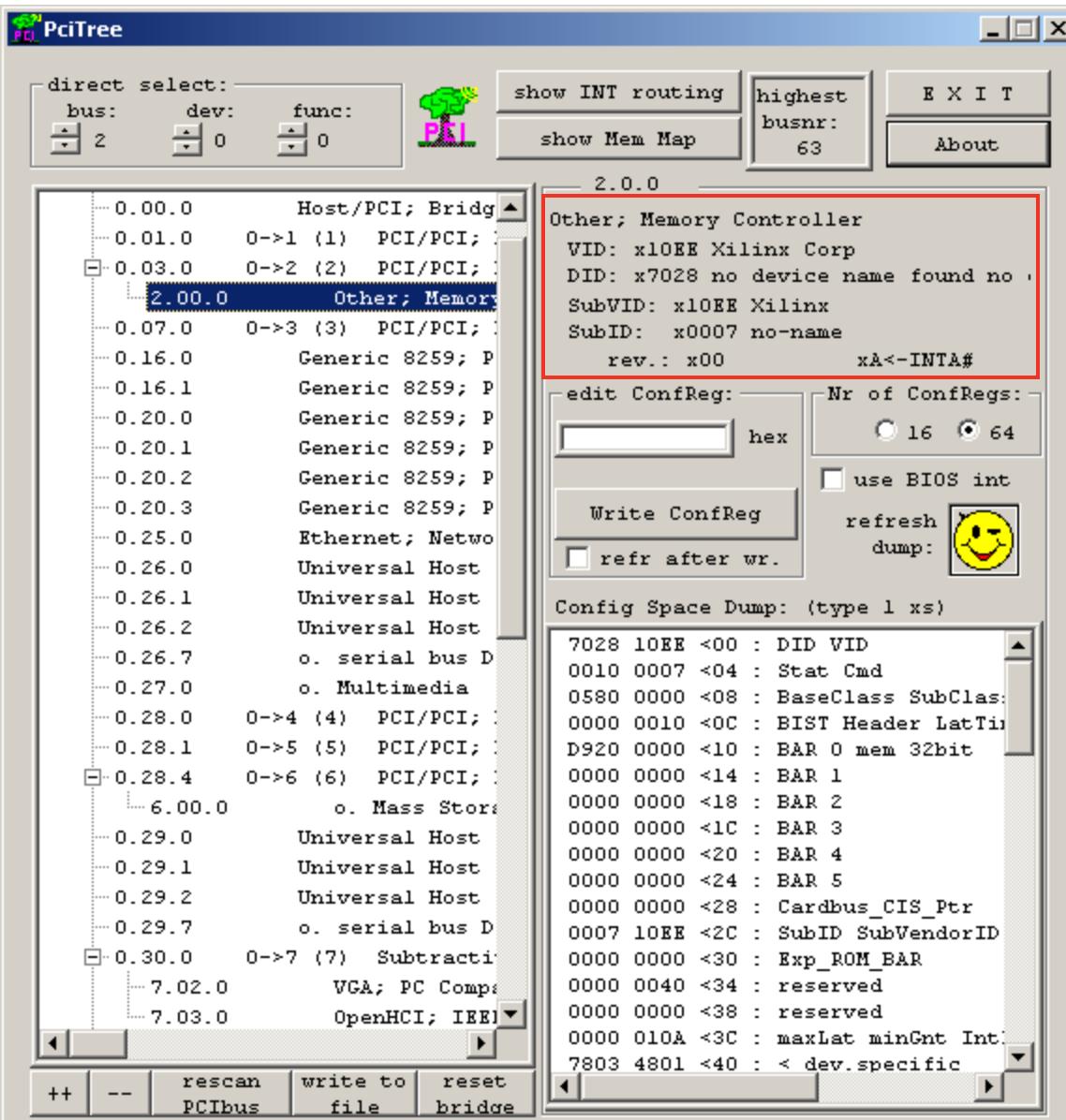


- Set Number of Configuration Registers to 64
- Click on Refresh dump

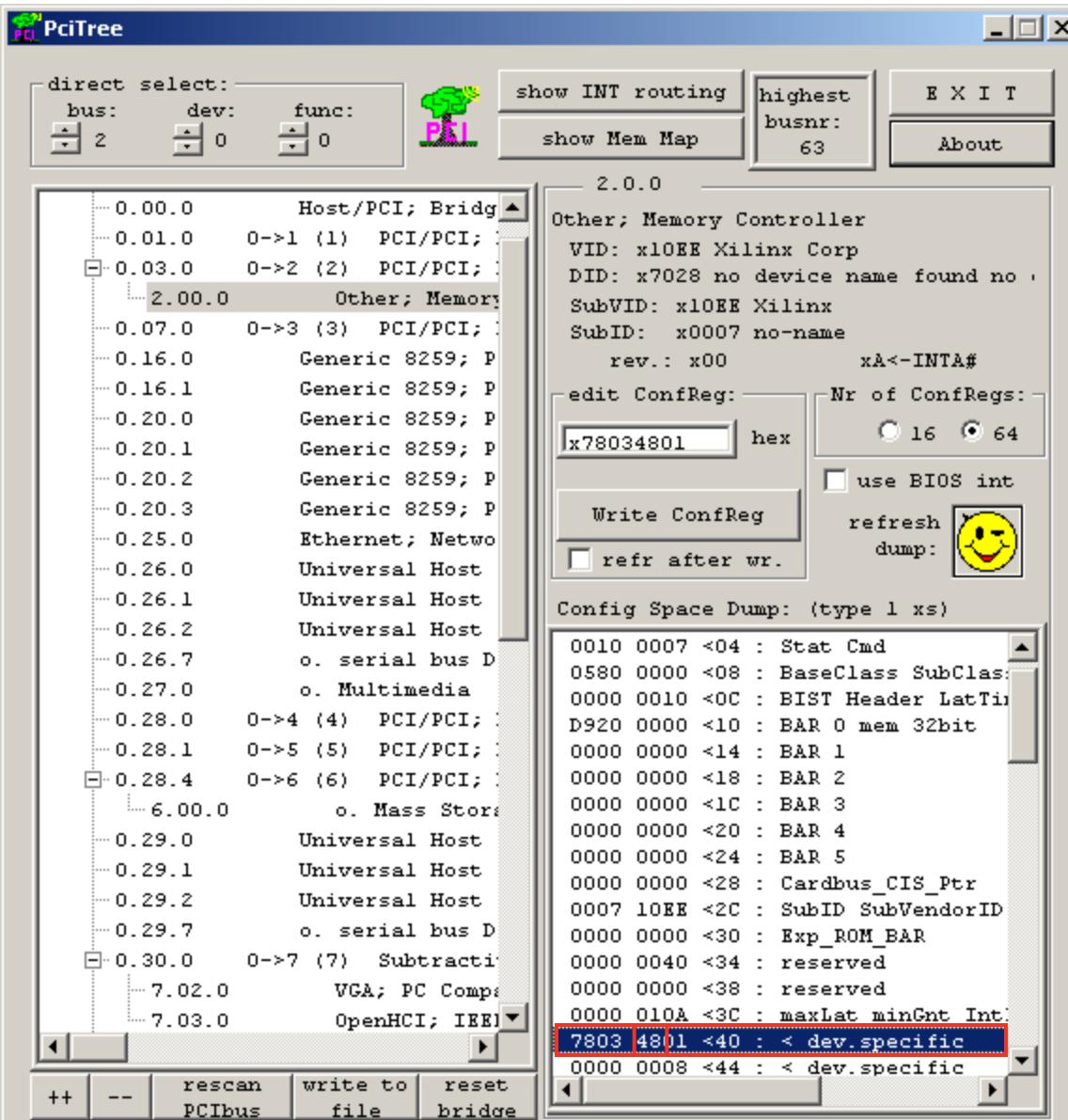
# Running the PCIe x8 Gen 2 Design

## ► Locate the Xilinx Device

- Vendor ID is 0x10EE
- The x8 Gen 2 configuration will have a Device ID of 0x7028



# Running the PCIe x8 Gen 2 Design



➤ Navigate the linked list in configuration space to locate the PCIe Capabilities Structure

- See [PG054](#) for details

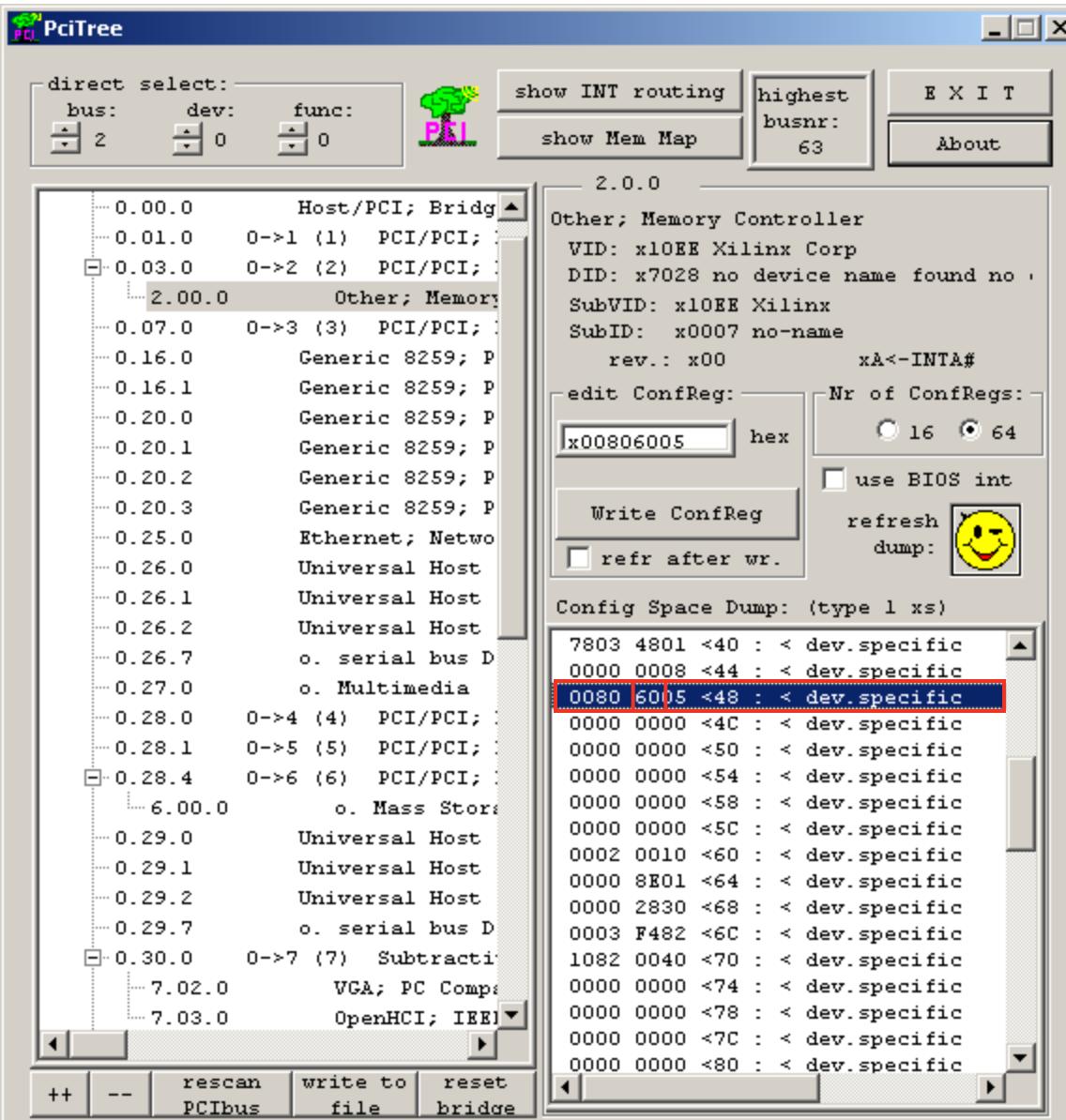
➤ With the Xilinx device selected, select Register 0x40

- Register 0x40 points to the next structure
- 0x48 is the address of the next structure

# Running the PCIe x8 Gen 2 Design

## ► Select Register 0x48

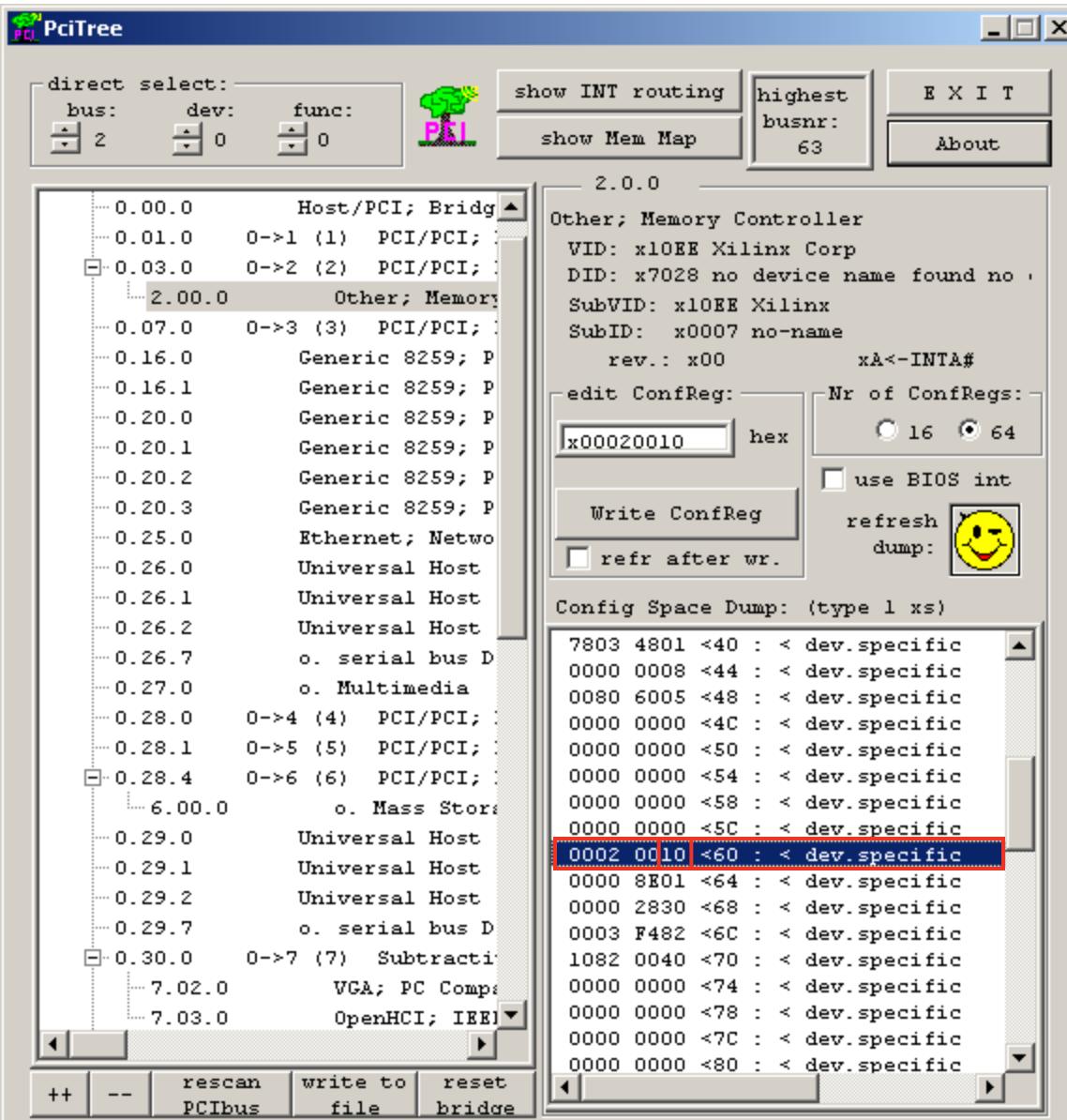
- Register 0x48 points to the next structure
- 0x60 is the address of the next structure



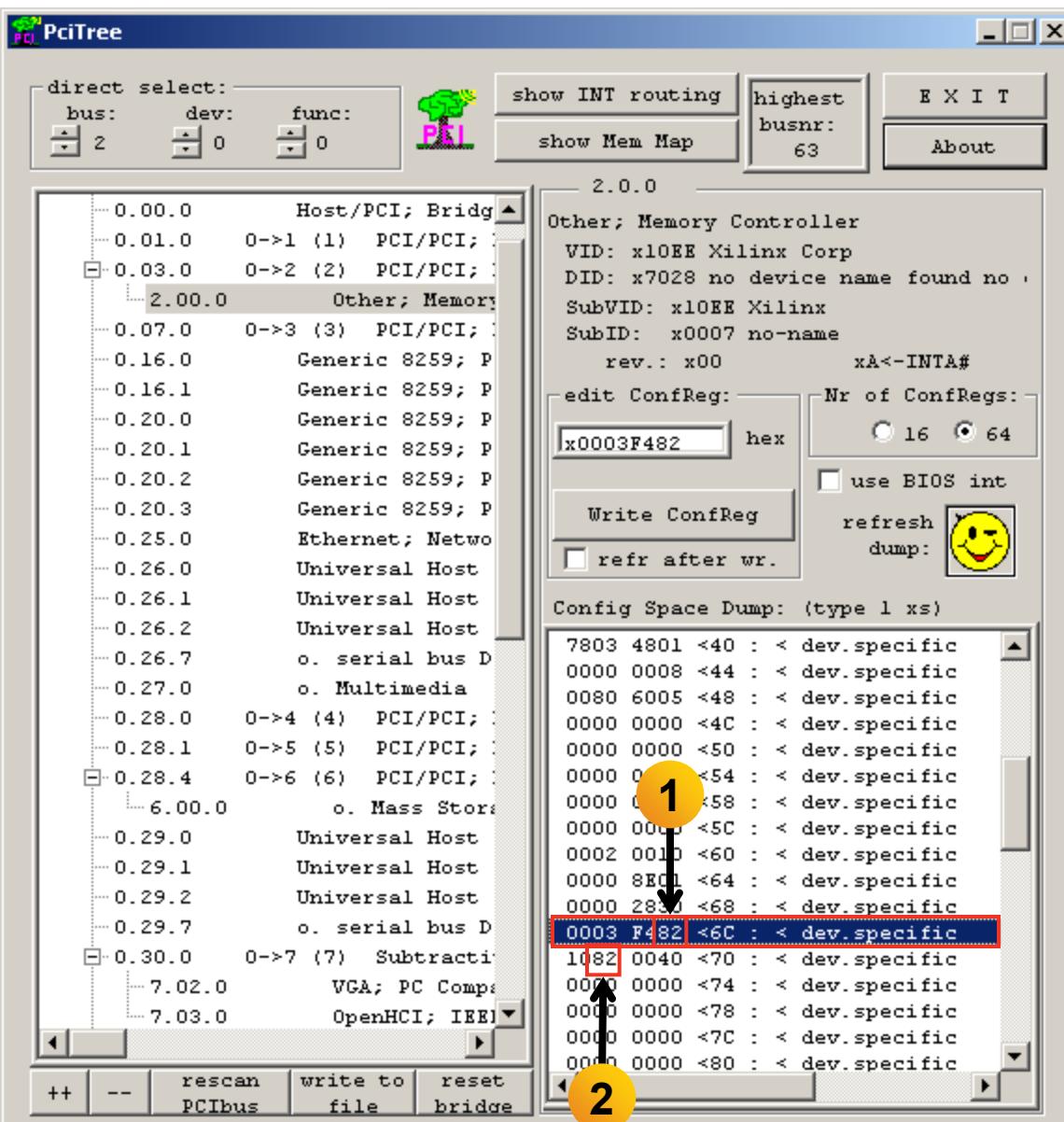
# Running the PCIe x8 Gen 2 Design

## ► Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure



# Running the PCIe x8 Gen 2 Design



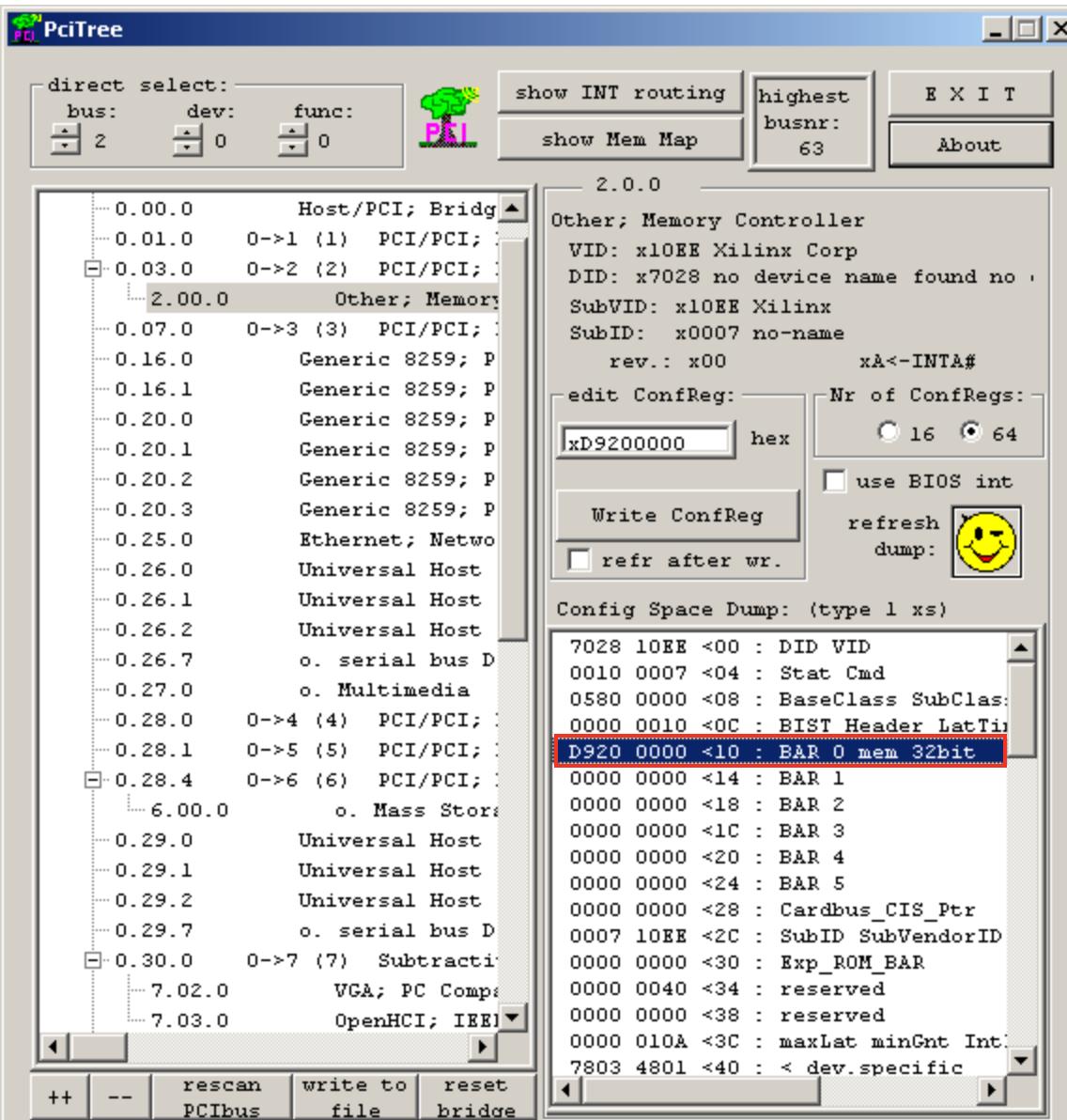
## ➤ Register 0x6C

- Link Capabilities Register
  - Indicates the maximum number of lanes and speed (Gen 1, Gen 2) for device
  - The value 0x82 shows this is an x8 Gen 2 device (1)

# Link Status Register

- 0x70
  - Shows the current link status
  - This design, in a Gen 2 chassis, trained to x8 Gen 2 (2)

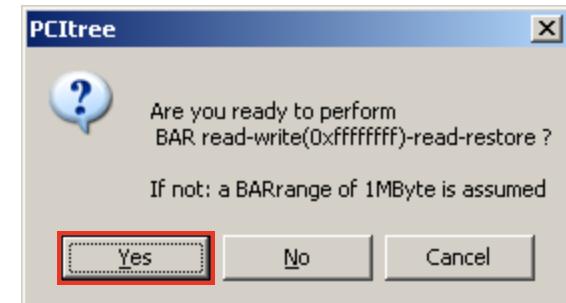
# Running the PCIe x8 Gen 2 Design



## ► Double-click on BAR 0

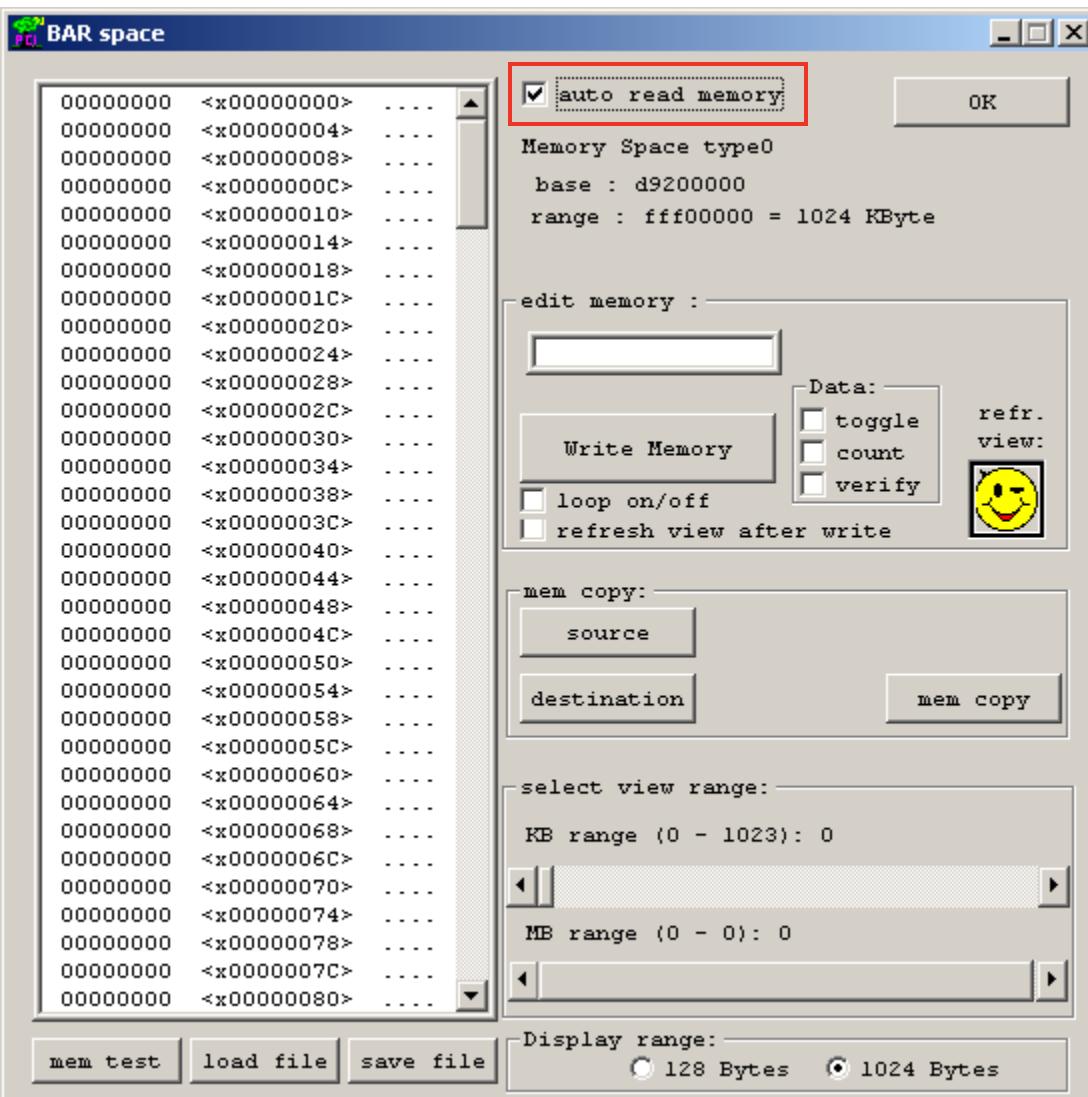
- BAR 0 Address is machine dependent

## ► Click Yes on the Dialog box seen below



# Running the PCIe x8 Gen 2 Design

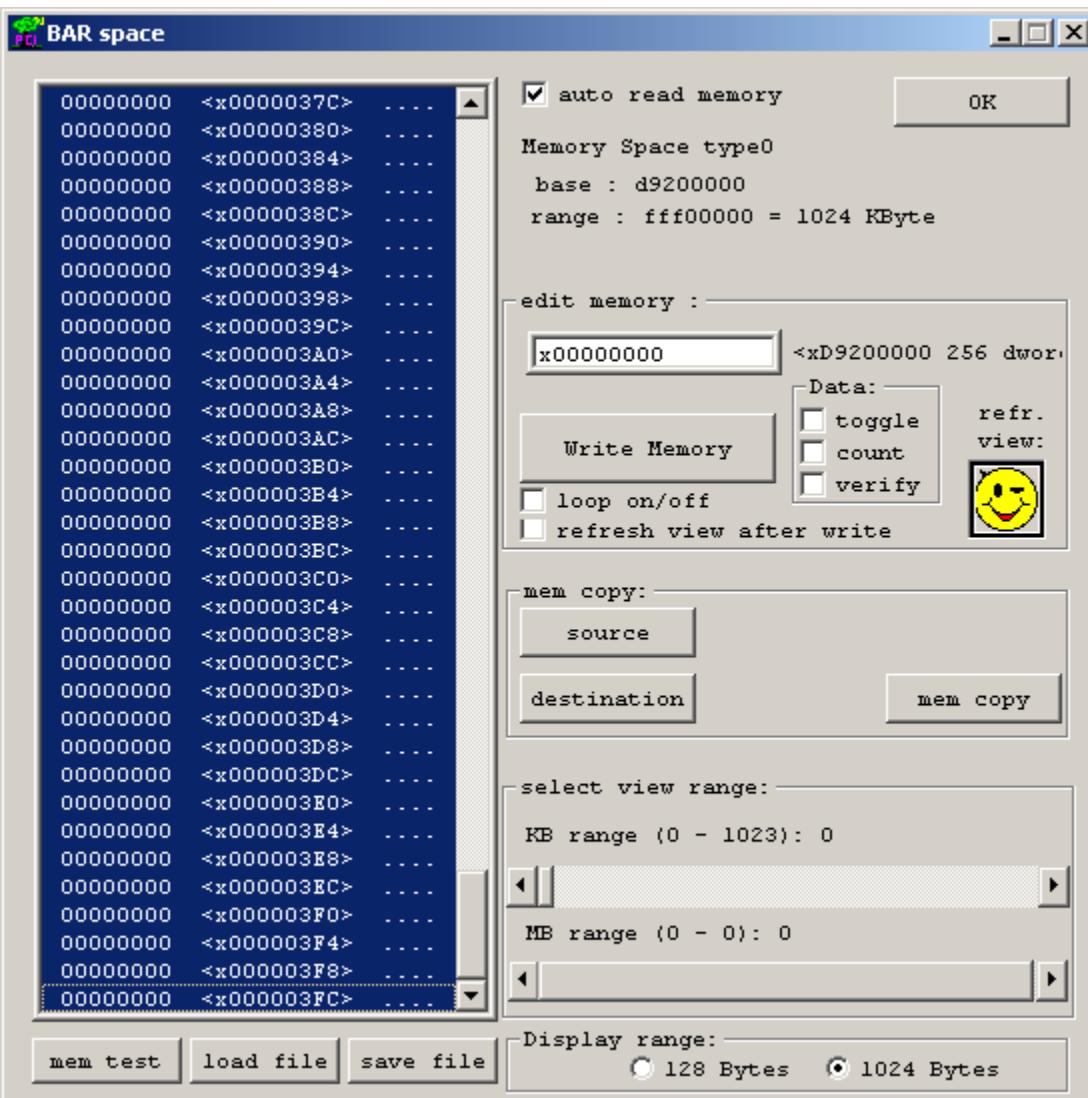
► Select auto read memory



# Running the PCIe x8 Gen 2 Design

► Click on the first memory location

- Type <Shift-End> to select 1024 Bytes

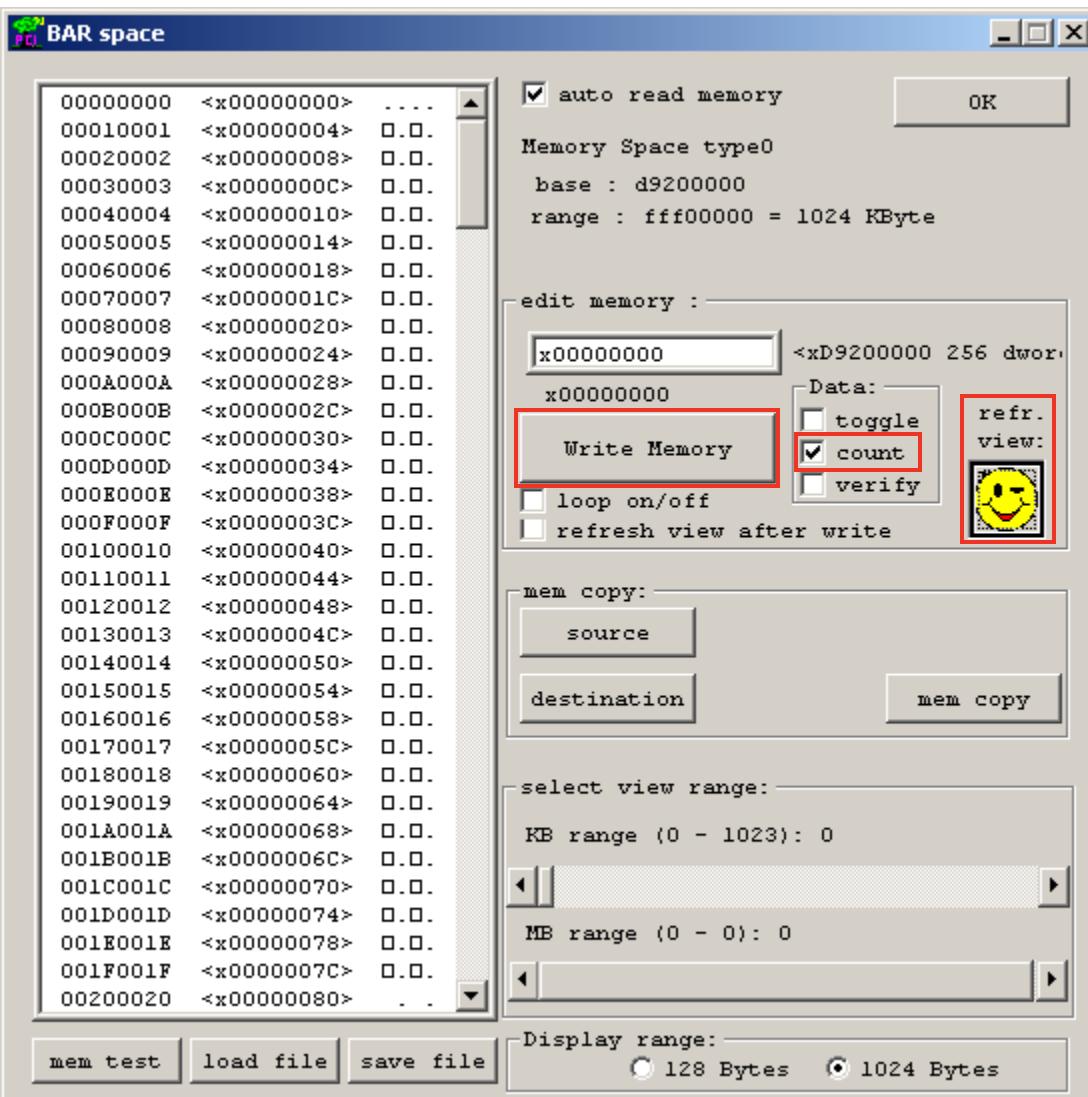


# Running the PCIe x8 Gen 2 Design

## ➤ Write Memory

- Select count
- Click Write Memory
- Click refr view

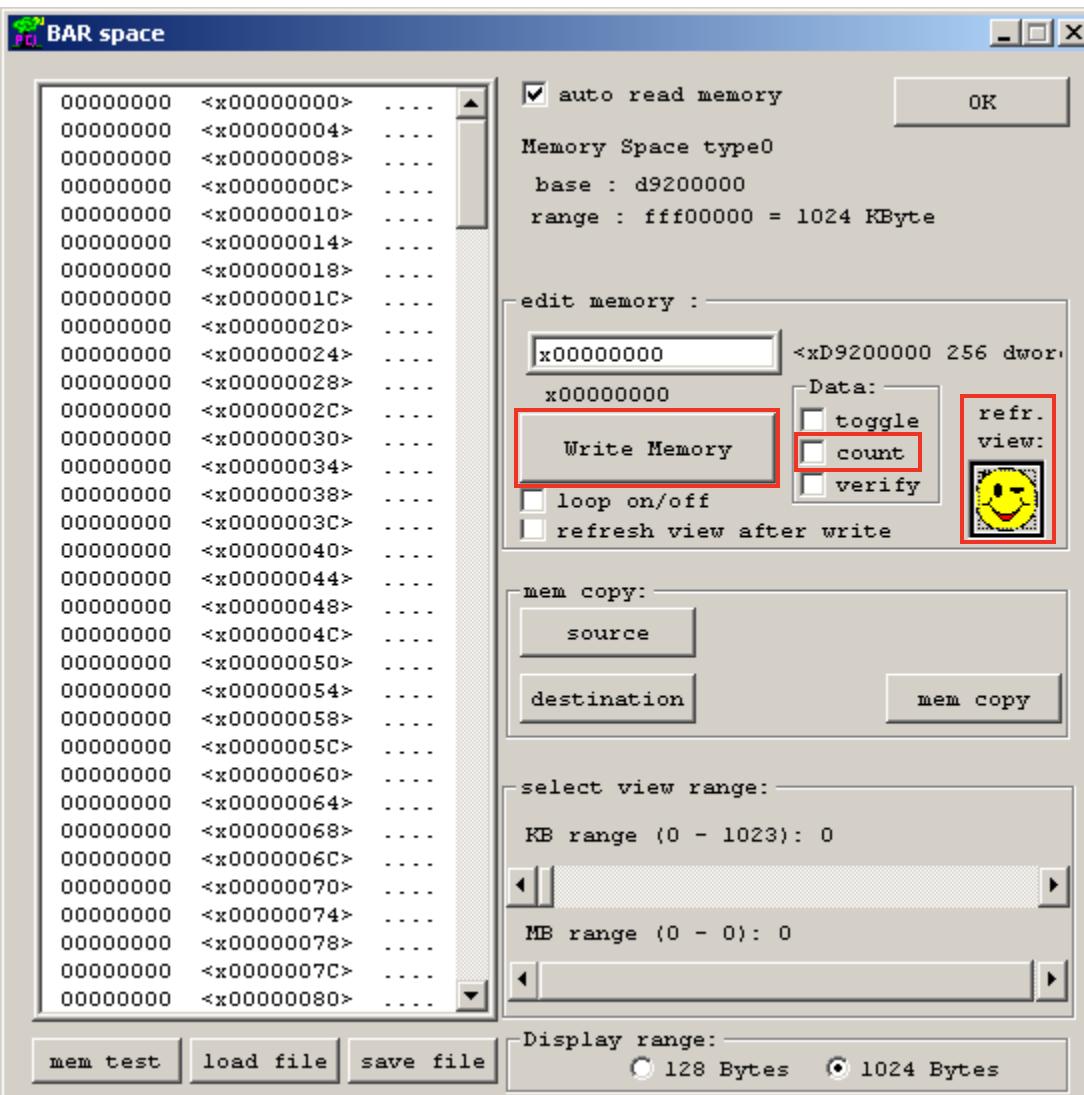
## ➤ View results – counting up to FF



Note: Presentation applies to the VC707

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# Running the PCIe x8 Gen 2 Design



## ➤ Restore Memory

- Deselect count
- Click Write Memory
- Click refr view

## ➤ Memory is reset to zeros

## ➤ Turn off PCIe chassis and remove VC707 board

## References

# References

## ► PCIe Base Specification

- PCI SIG Web Site
  - <http://www.pcisig.com/home>

## ► Xilinx PCI Express

- Xilinx PCI Express Overview
  - <http://www.xilinx.com/products/technology/pci-express.html>
- 7 Series Integrated Block for PCI Express Product Page
  - [http://www.xilinx.com/products/intellectual-property/7\\_series\\_pci\\_express\\_block.html](http://www.xilinx.com/products/intellectual-property/7_series_pci_express_block.html)
- 7 Series Integrated Block for PCI Express Product Guide – PG054
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_7x/v3\\_1/pg054-7series-pcie.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_1/pg054-7series-pcie.pdf)
- 7 Series Integrated Block for PCI Express – Release Notes
  - <http://www.xilinx.com/support/answers/54643.htm>

# References

## ► Micron NOR Flash

- Micron G18 Flash
  - <http://www.micron.com/partsnor-flash/parallel-nor-flash/mt28gu256aaa1egc-0sit>
- Datasheet
  - [http://www.micron.com/~media/documents/products/data-sheet/nor-flash/serial-nor/n25q/n25q\\_256mb\\_3v\\_65nm.pdf](http://www.micron.com/~media/documents/products/data-sheet/nor-flash/serial-nor/n25q/n25q_256mb_3v_65nm.pdf)

## ► Xilinx Generation 7 Configuration with BPI Flash

- 7 Series FPGAs Configuration User Guide – UG470
  - [http://www.xilinx.com/support/documentation/user\\_guides/ug470\\_7Series\\_Config.pdf](http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf)
- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf)
- BPI Fast Configuration with 7 Series FPGAs – XAPP587
  - [http://www.xilinx.com/support/documentation/application\\_notes/xapp587-bpi-fast-configuration.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp587-bpi-fast-configuration.pdf)

# Documentation

# Documentation

## ➤ Virtex-7

- Virtex-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/virtex-7/index.htm>
- Design Advisory Master Answer Record for Virtex-7 FPGAs
  - <http://www.xilinx.com/support/answers/42944.htm>

## ➤ VC707 Documentation

- Virtex-7 FPGA VC707 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html>
- VC707 Getting Started Guide – UG848
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ vc707/ug848-VC707-getting-started-guide.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug848-VC707-getting-started-guide.pdf)
- VC707 User Guide – UG885
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ vc707/ug885\\_VC707\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug885_VC707_Eval_Bd.pdf)