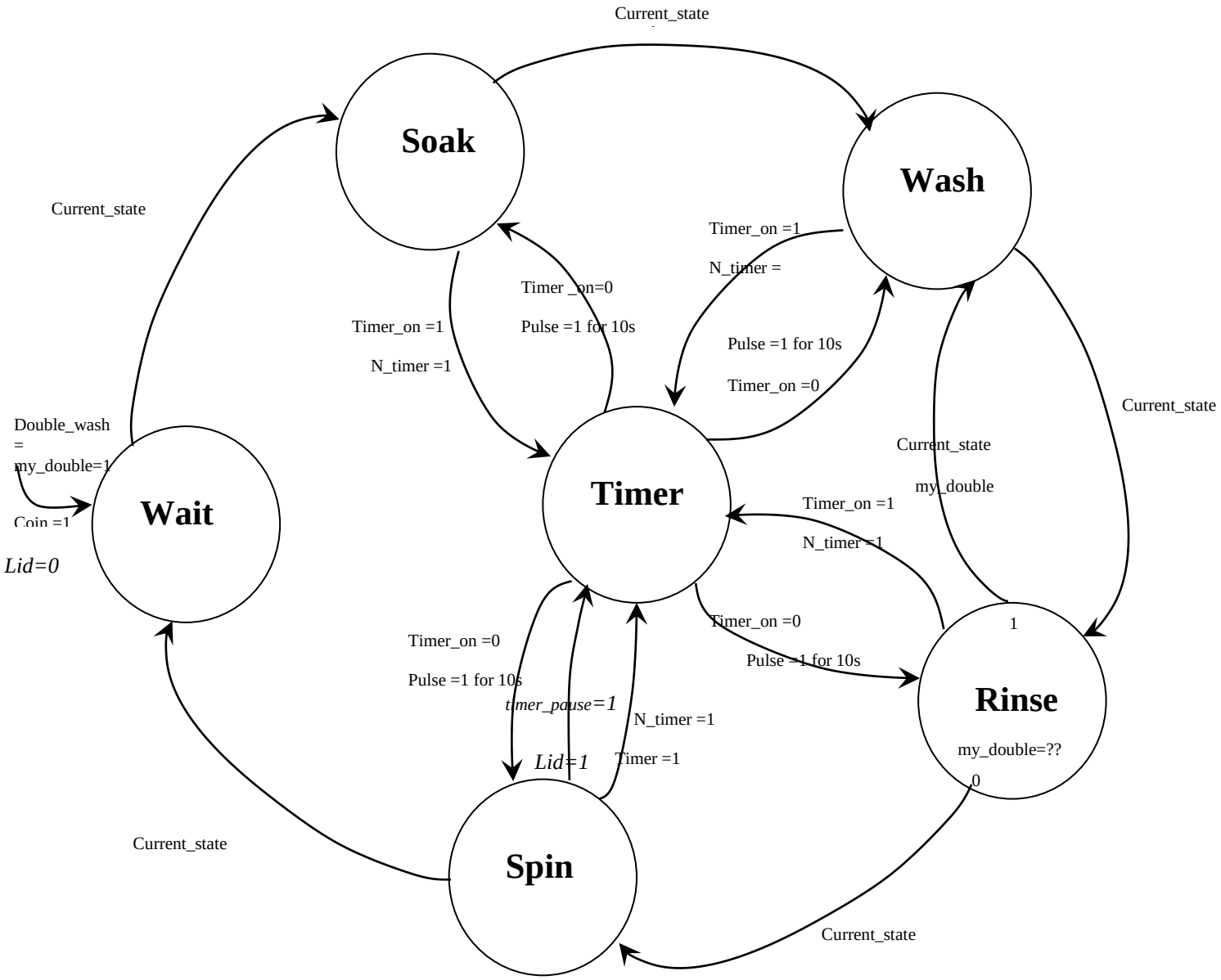
# Project

**Consider the operation of the embedded controller for a washing machine:**

- The operation of the machine starts when a coin is deposited. Assume that the user will only deposit the exact amount of coins.
- It then sequences through the following stages: *soak, wash, rinse, and spin.*
- If the lid is raised during the spin cycle, the machine stops spinning until the lid is closed. Note that the machine is designed to stop when the lid is raised only during the spin cycle.
- There is a *double wash* switch, which if turned on, causes a second wash and rinse to occur after completing the first rinse. Assume that the double wash button is pressed before depositing the coins (if needed) and stays pressed till the job completes.
- The *wash* stage takes 3 minutes, whereas all other stages take 1 minute.
- The system includes a timer that begins ticking as soon as the coin is deposited. It suspends ticking while the lid is raised during the spin cycle and stops when the job is completed. This timer generates a 10-second pulse (signal) every 1 minute.

**You are required to:**

1. Write SystemVerilog code for the Finite State Machine => please make sure that the file can be compiled and simulated.
2. Write Test Bench to verify the FSM and try to cover all the possible scenarios.
3. Providing the steps to run the code on Modelsim is a plus.


Current_state
Soak
Wash
Current_state
Timer_on =1
N_timer =
Timer _on=0
Pulse =1 for 10s
Timer_on =1
N_timer =1
Pulse =1 for 10s
Timer_on =0
Current_state
Double_wash
=
my_double=1
Wait
Timer
Current_state
my_double
Timer_on =1
N_timer =1
Coin =1
Lid=0
Timer_on =0
Pulse =1 for 10s
Timer_on =0
Pulse =1 for 10s
1
timer_pause=1
N_timer =1
Lid=1
Timer =1
Rinse
my_double=??
0
Current_state
Spin
Current_state