计算机组成原理

第七讲

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容错与移动计算研究中心

第 4 章 存 储 器

4.1 概述

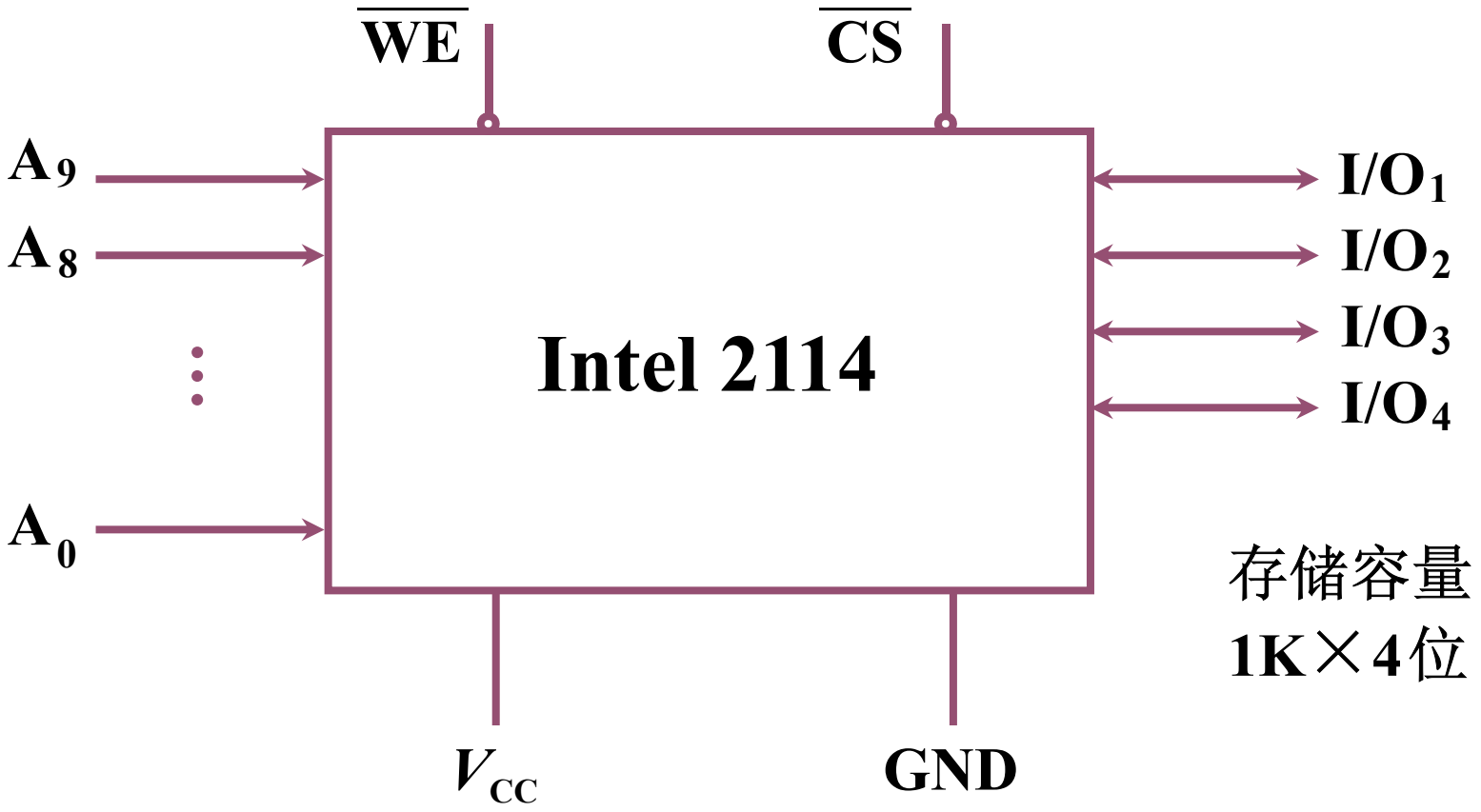
4.2 主存储器

4.3 高速缓冲存储器

4.4 辅助存储器

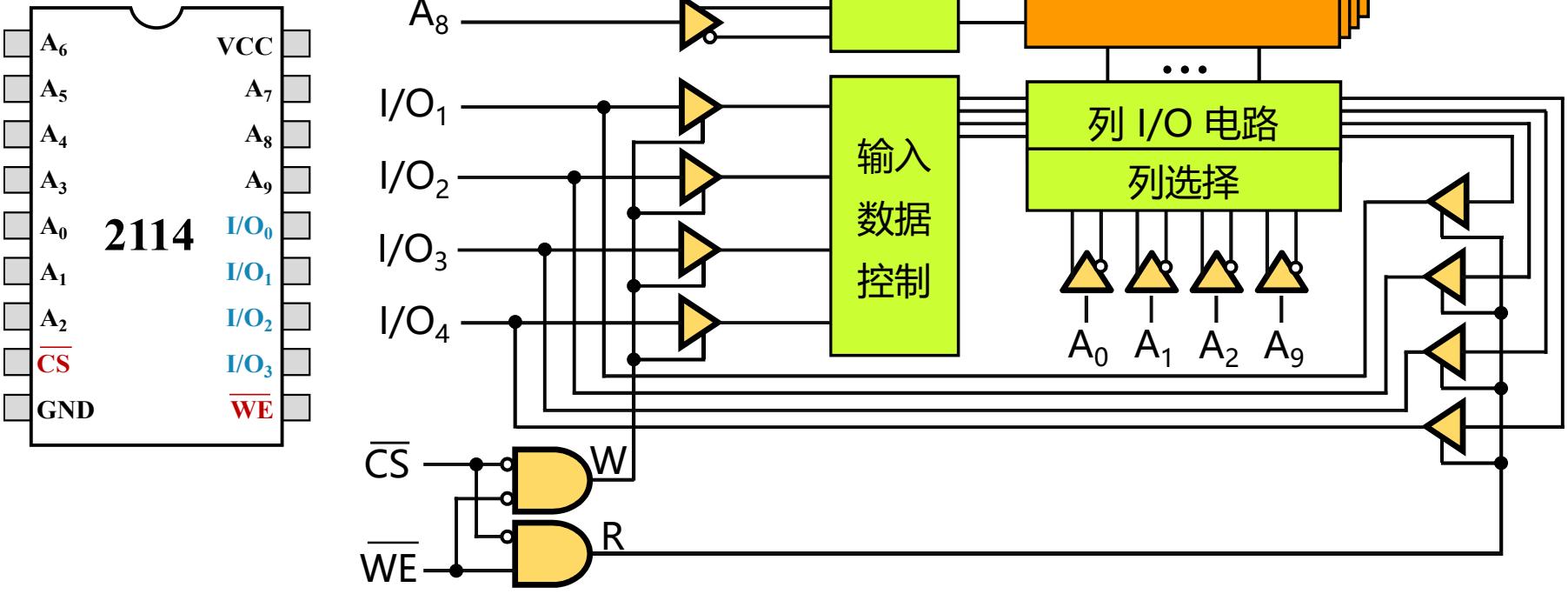
(2) 静态 RAM 芯片举例

① Intel 2114 外特性



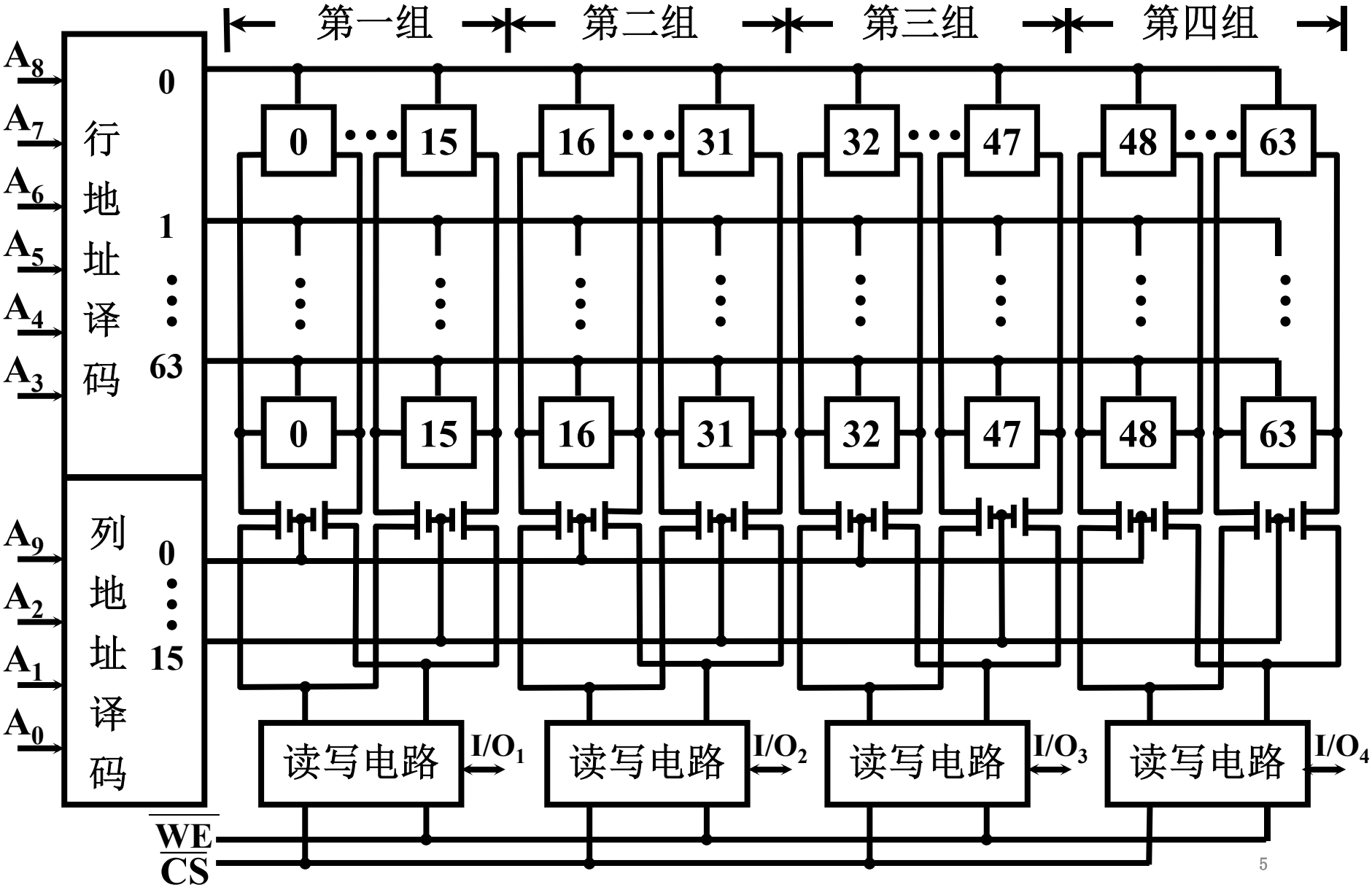
(2) 静态 RAM 芯片举例

① Intel 2114



② Intel 2114 RAM 矩阵 (64 × 64) 读

4.2



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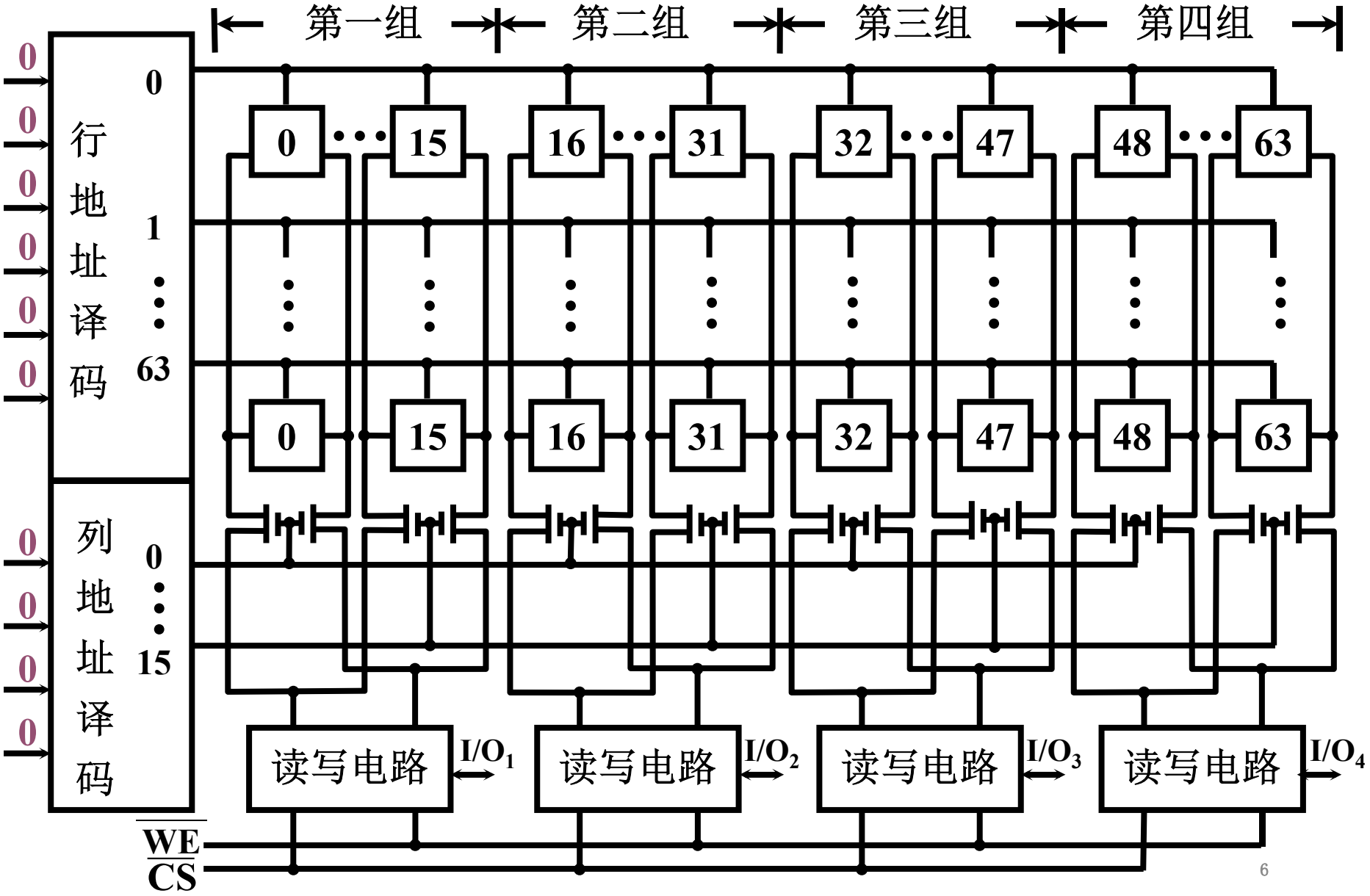

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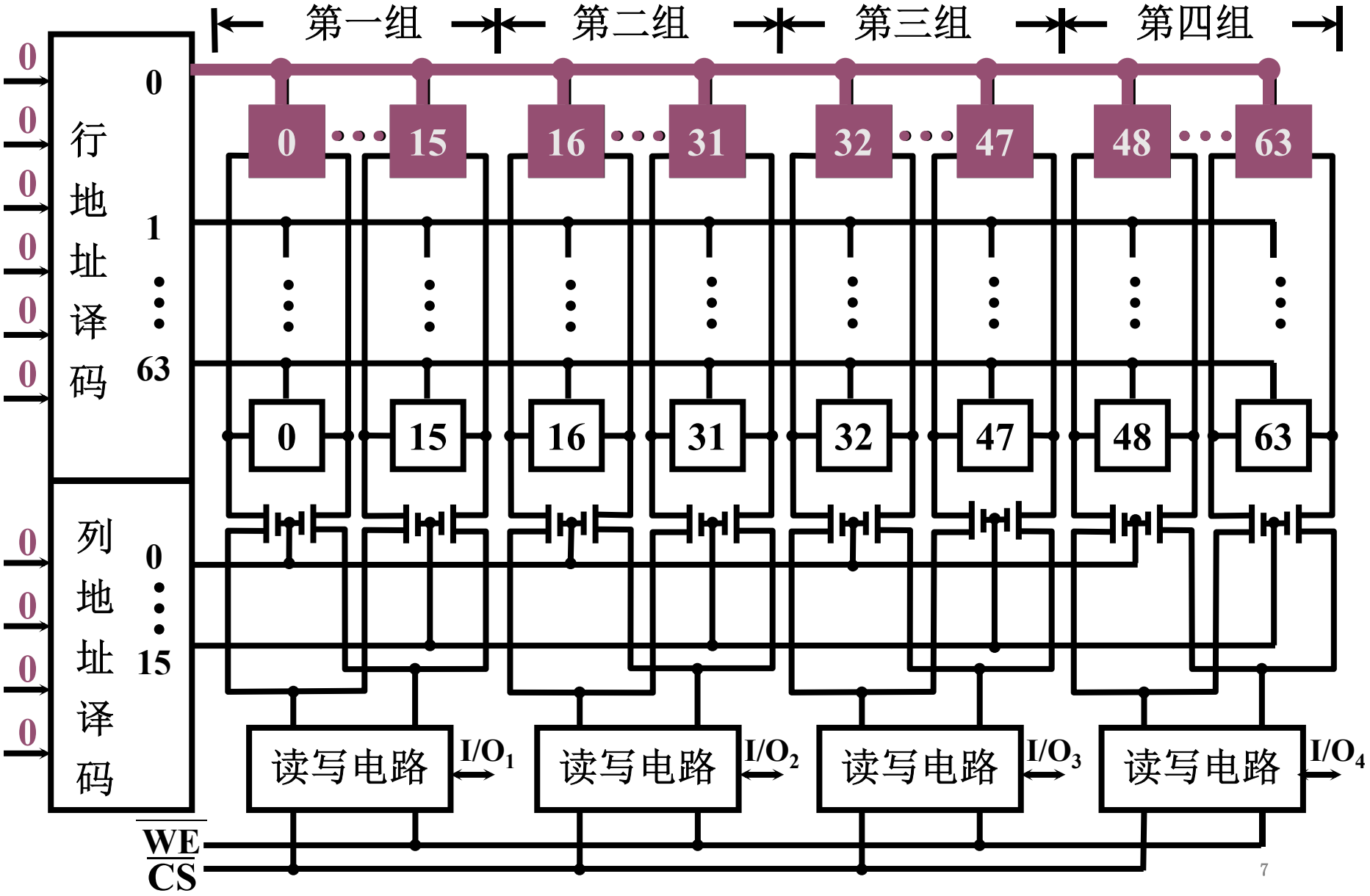

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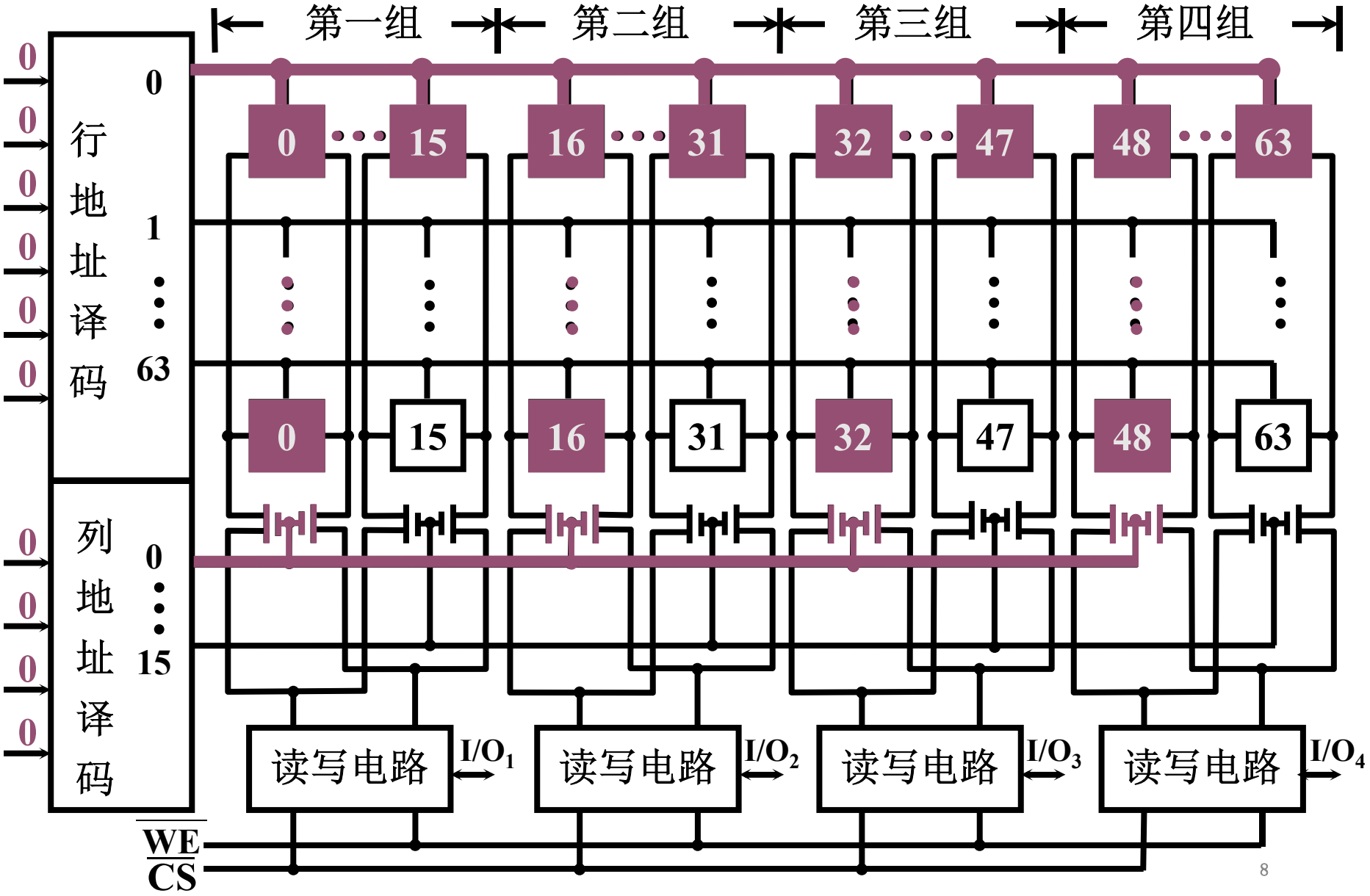

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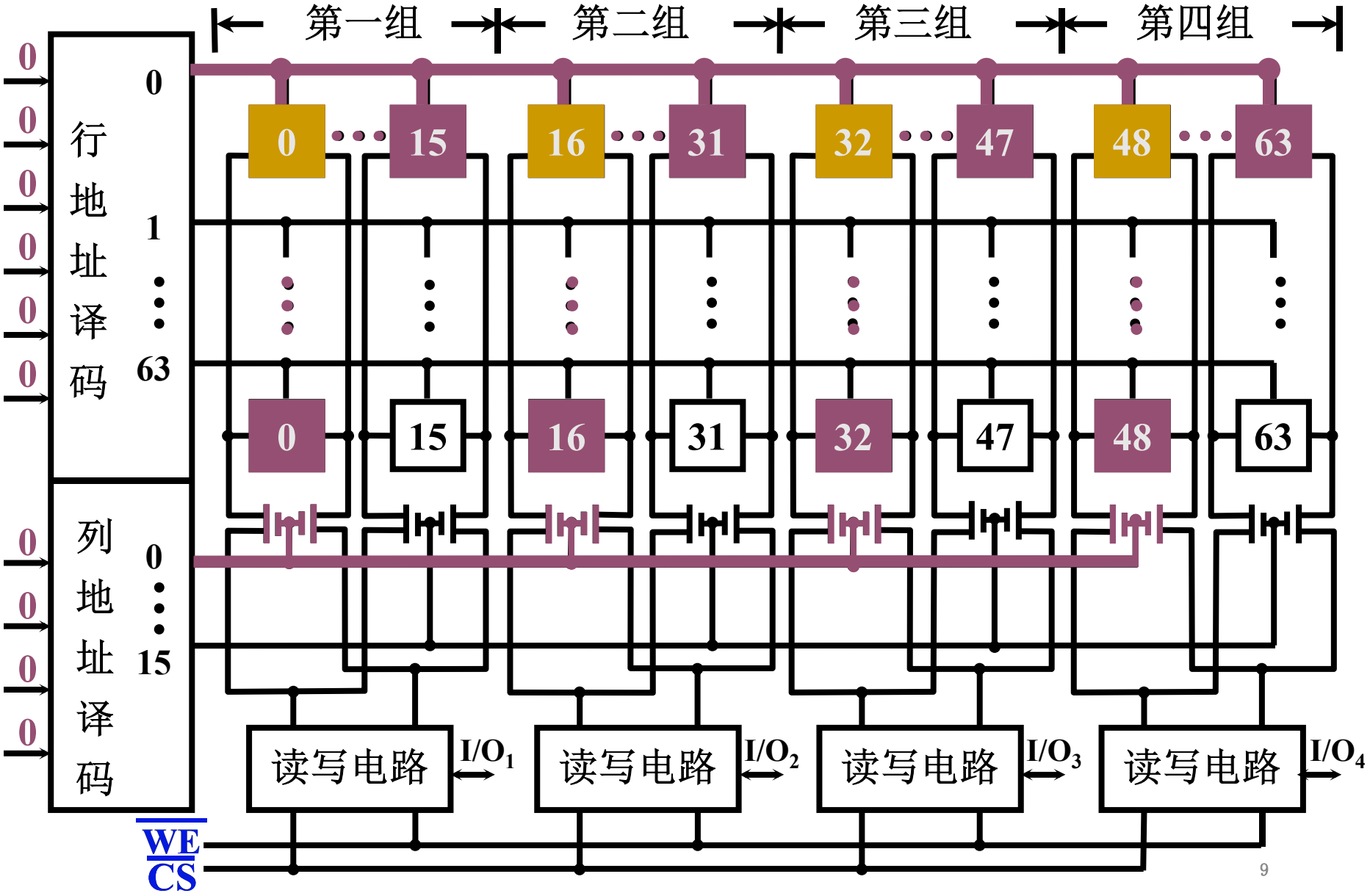

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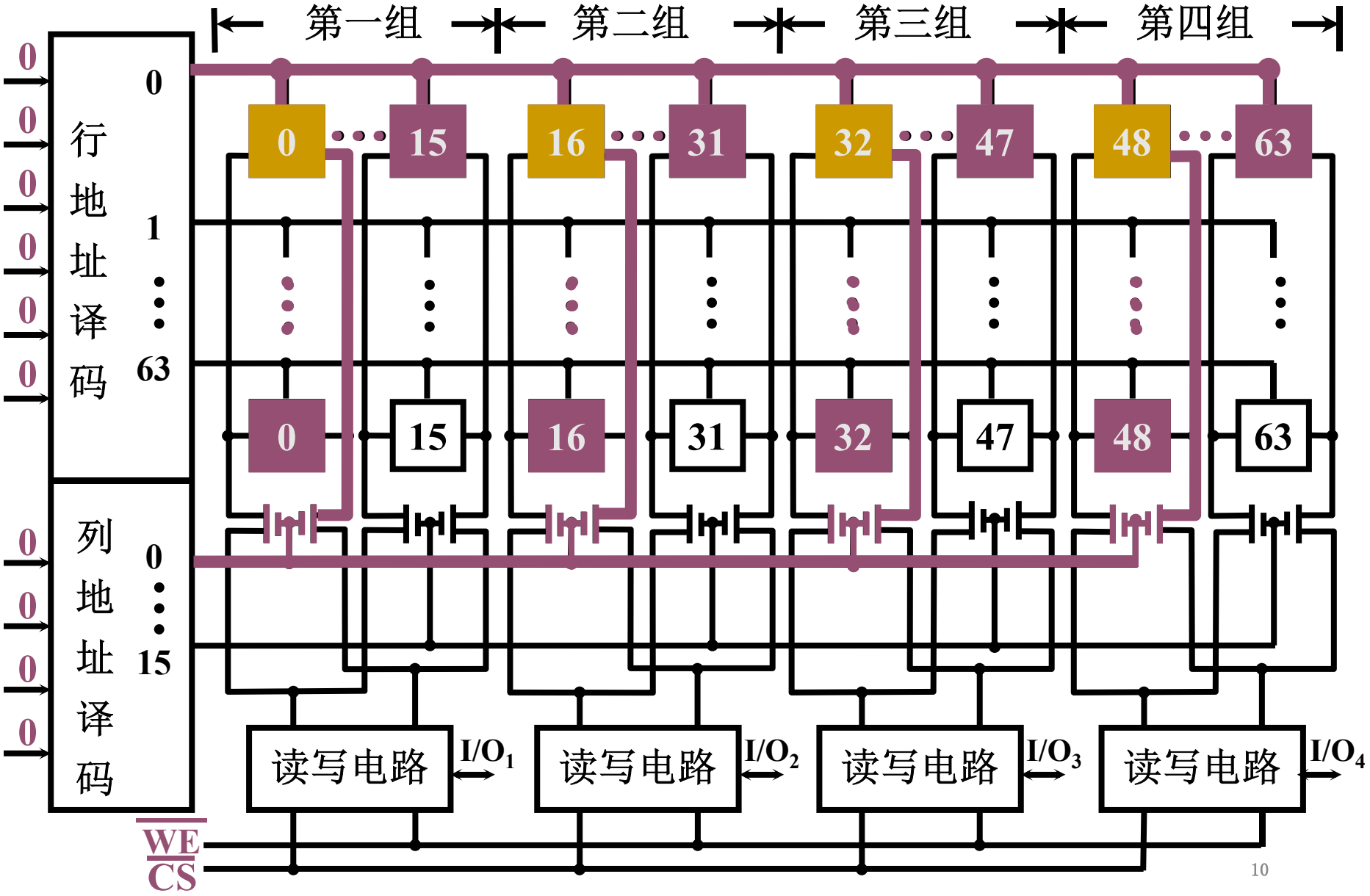

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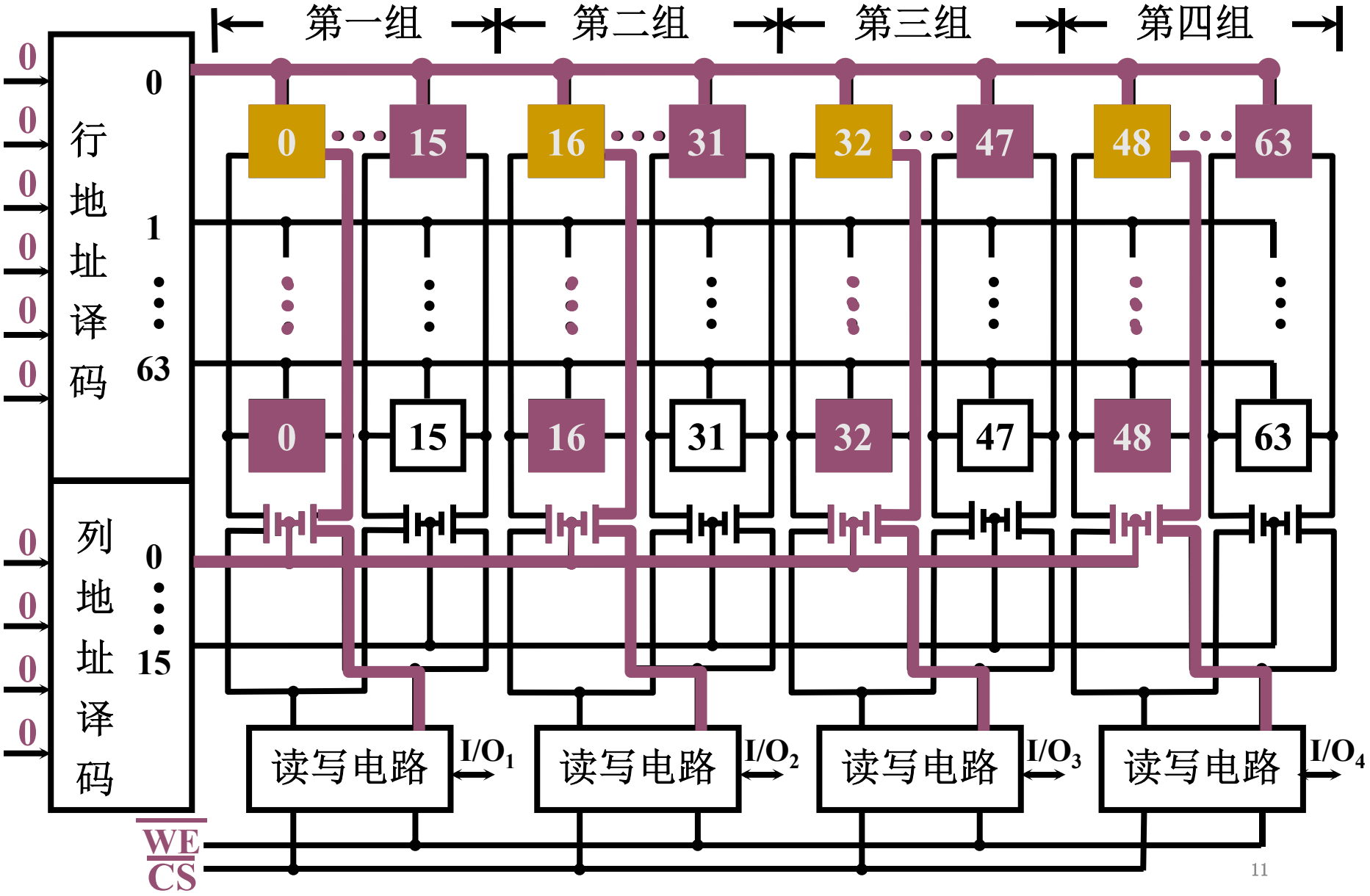

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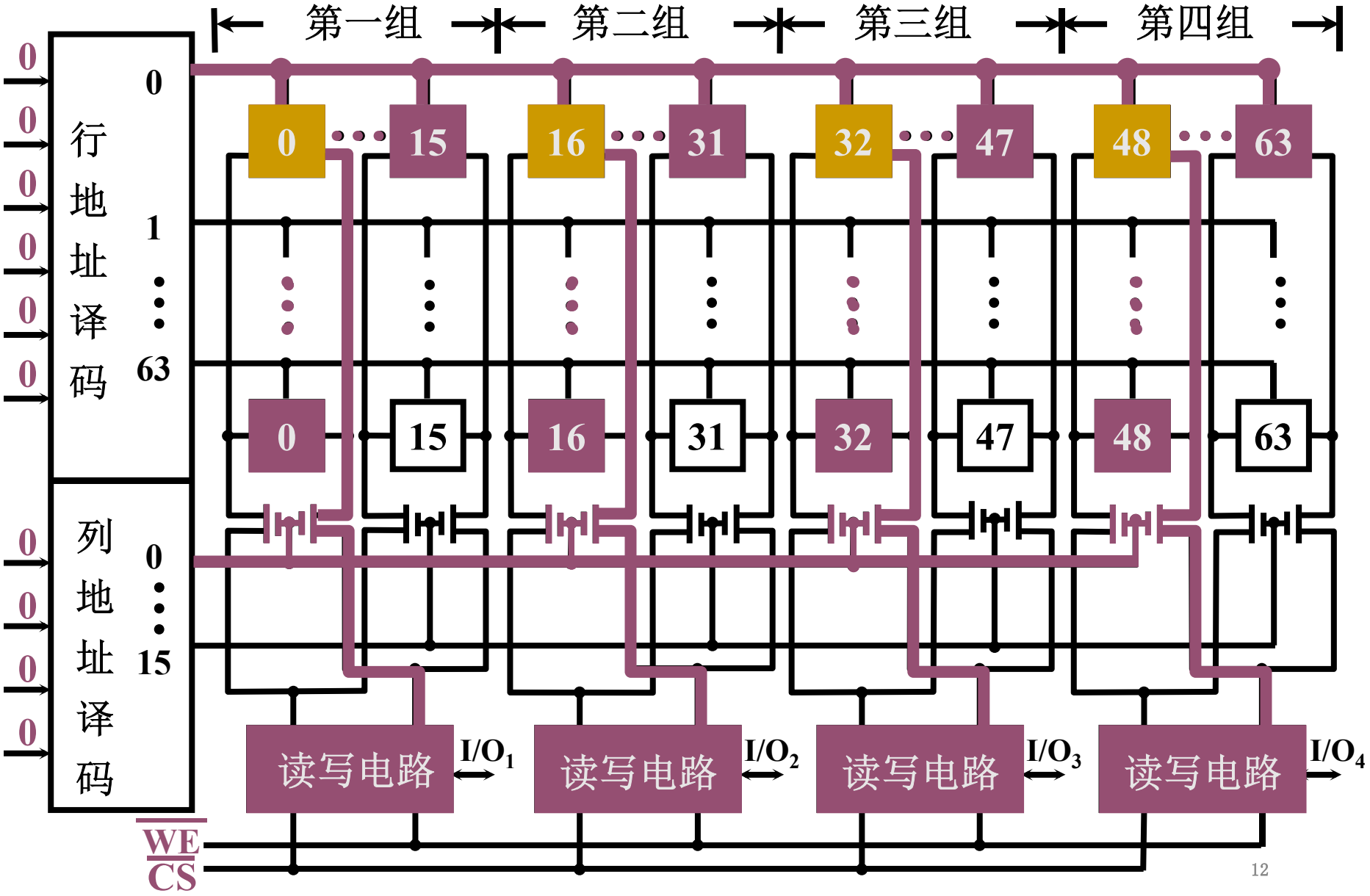

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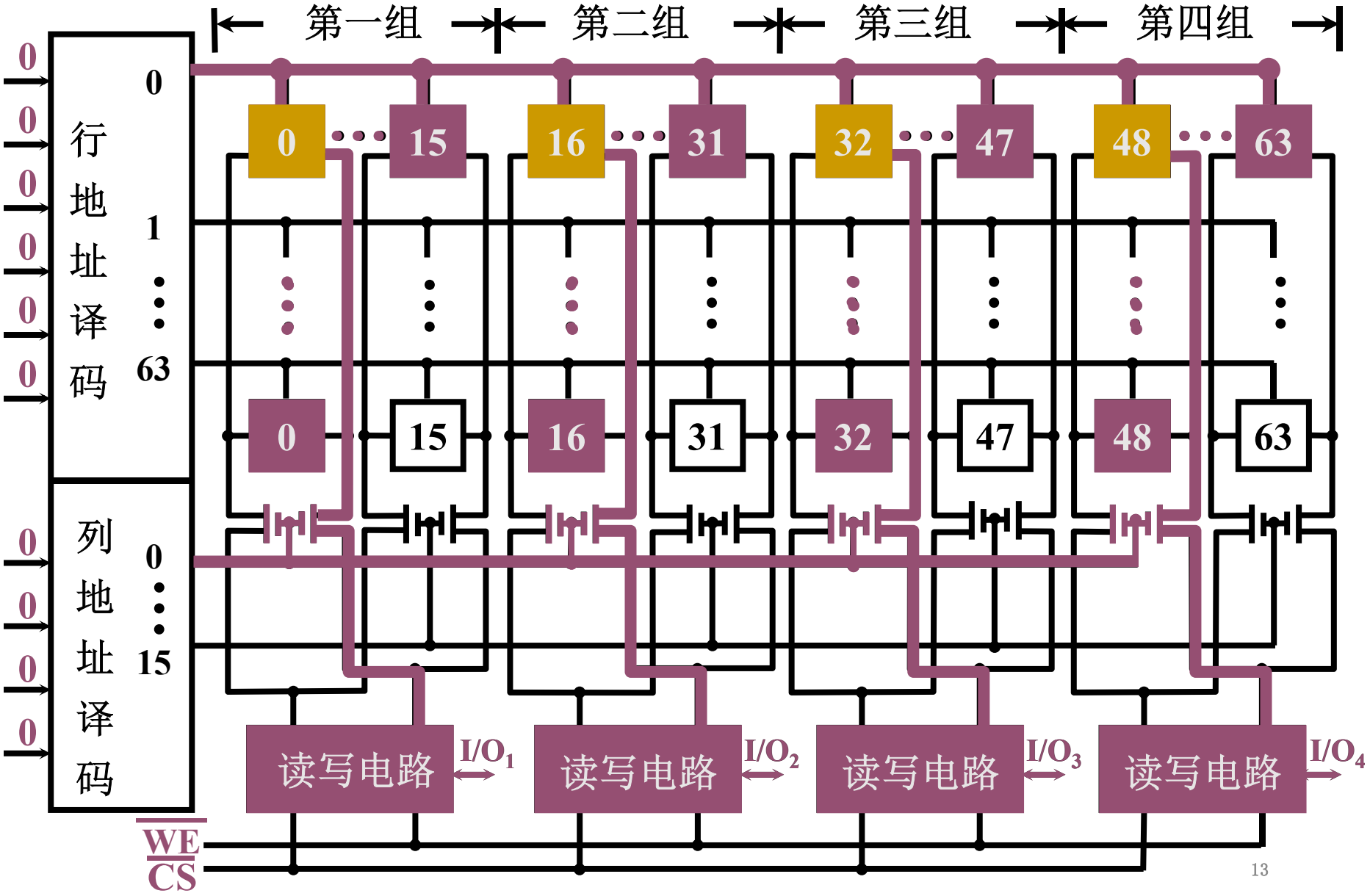

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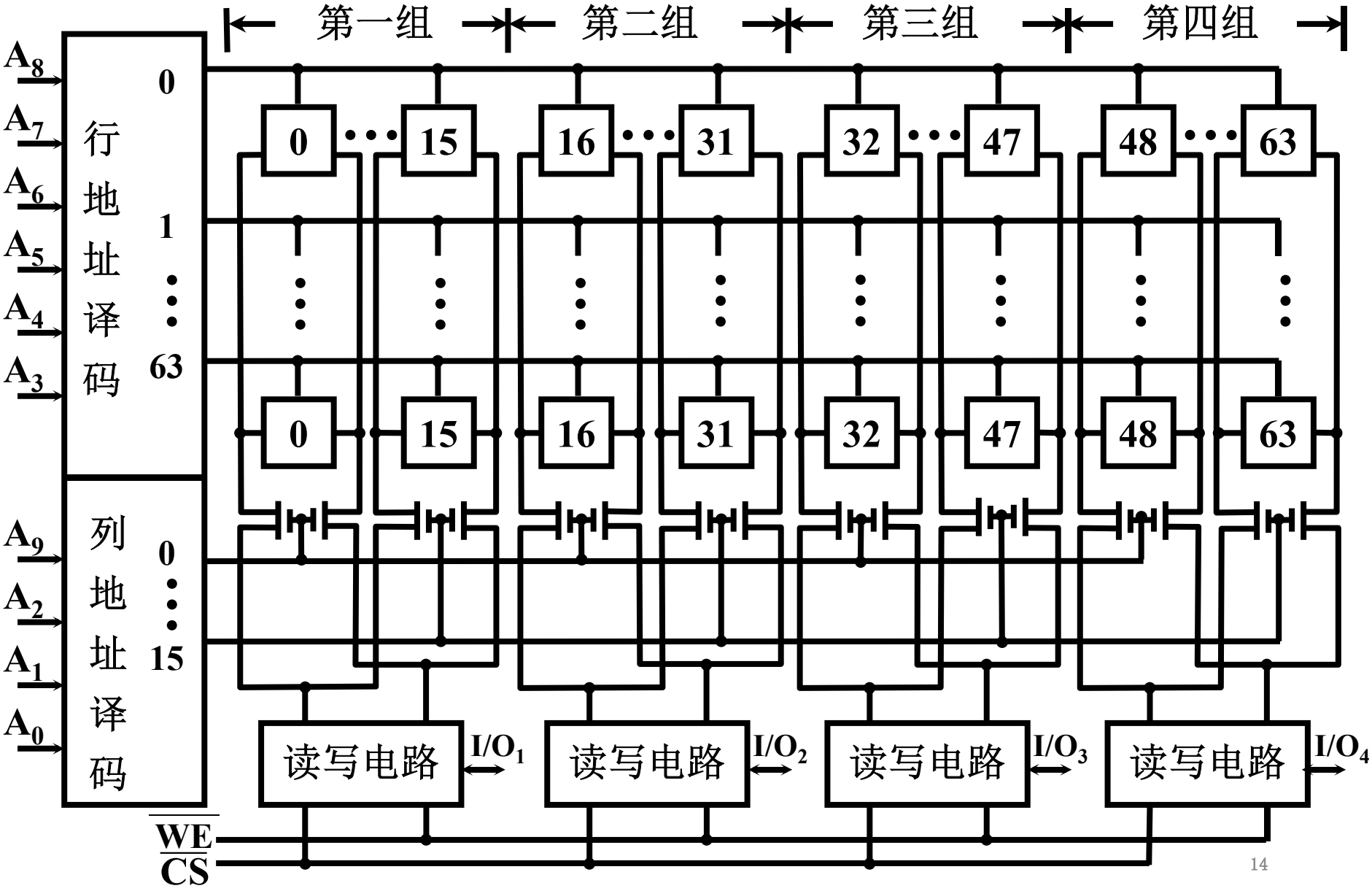

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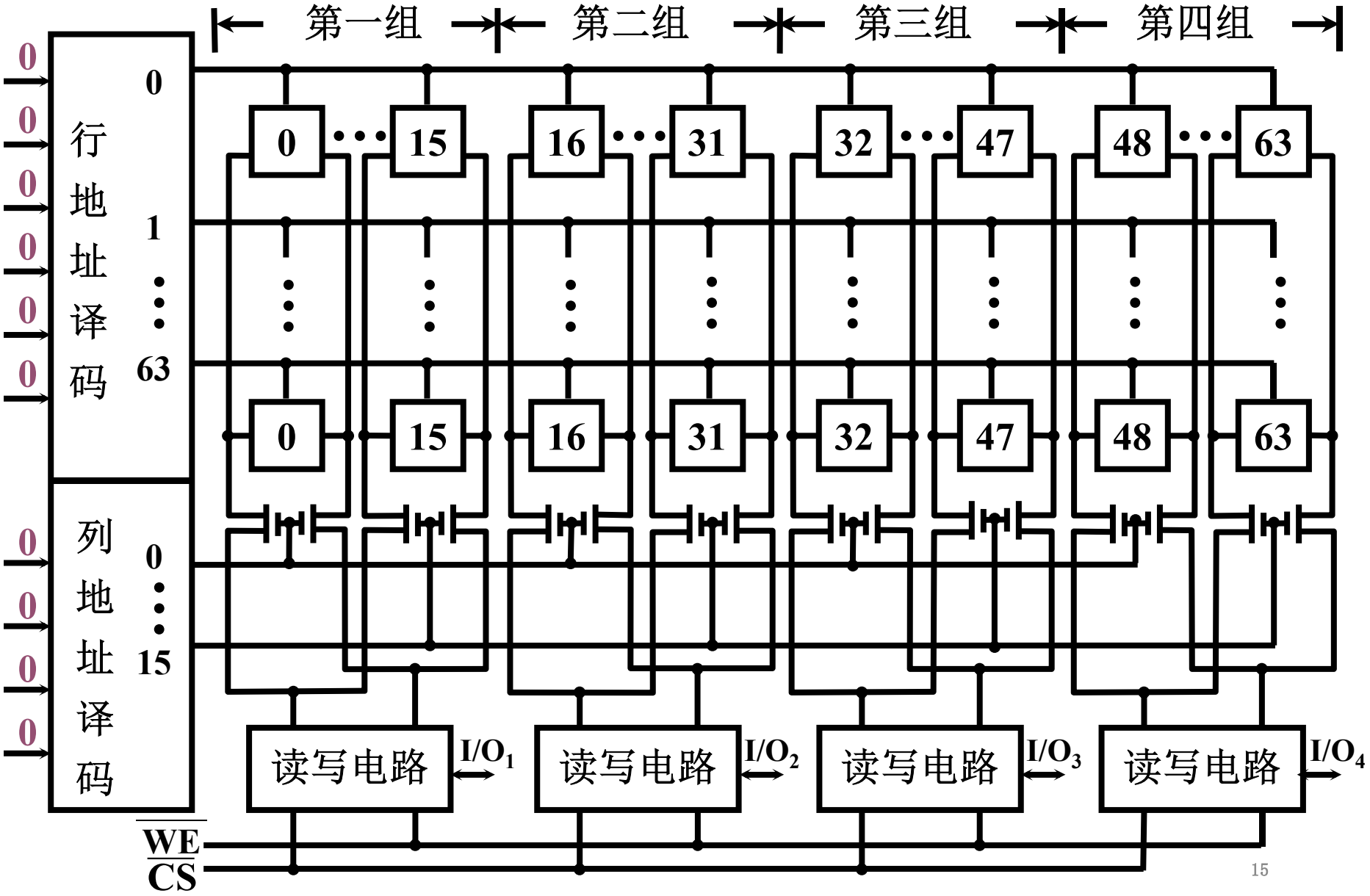

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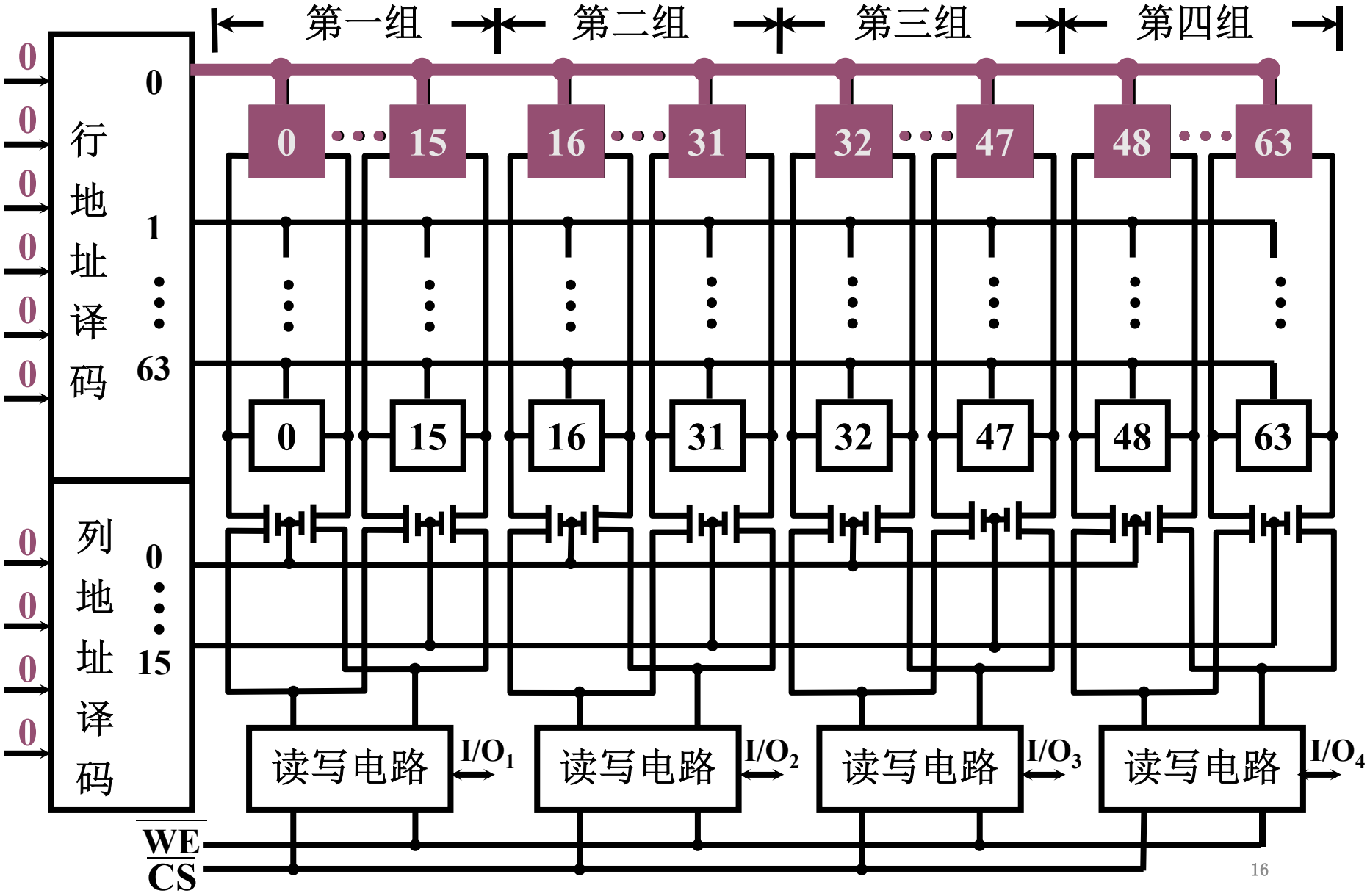

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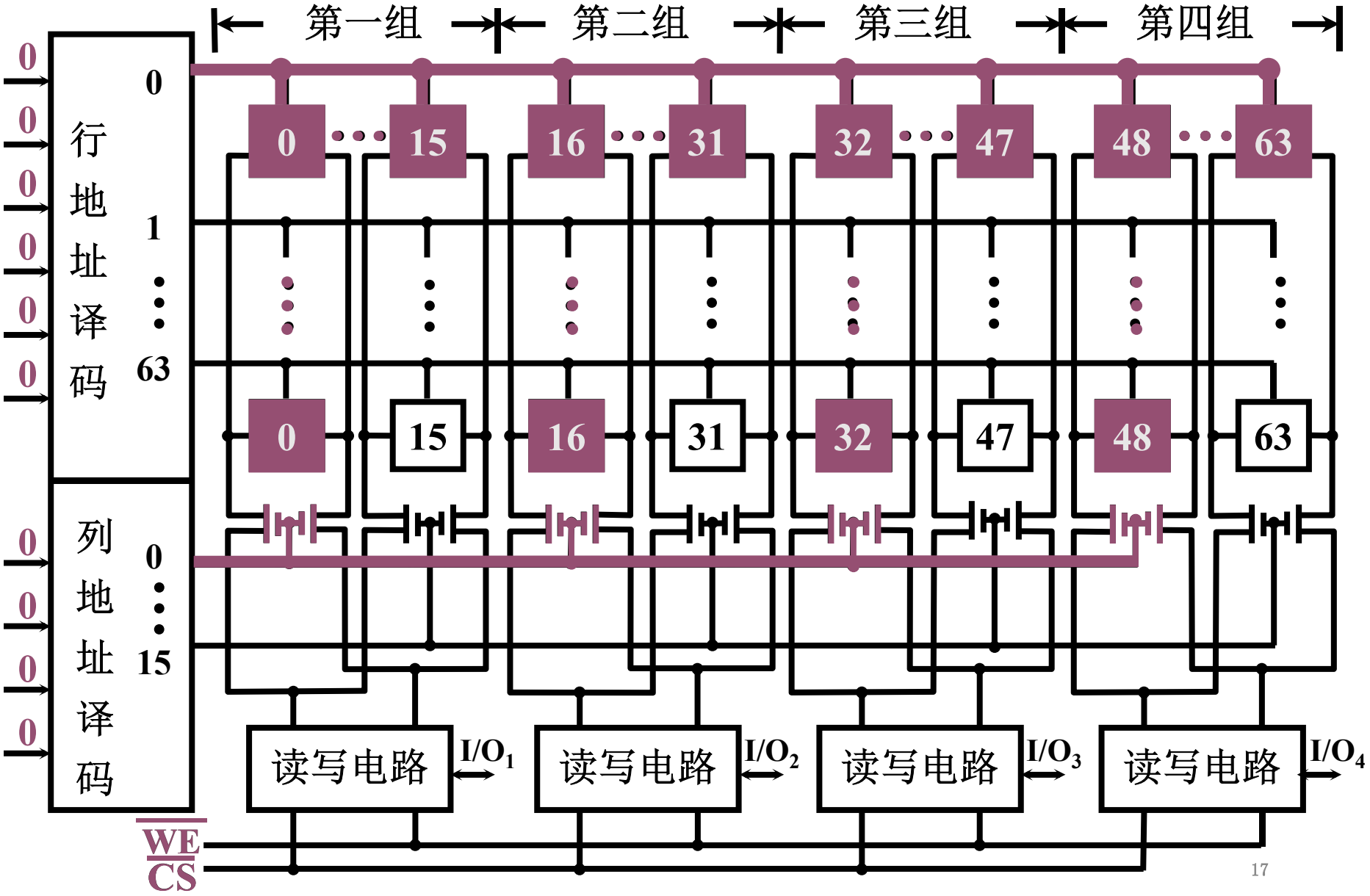

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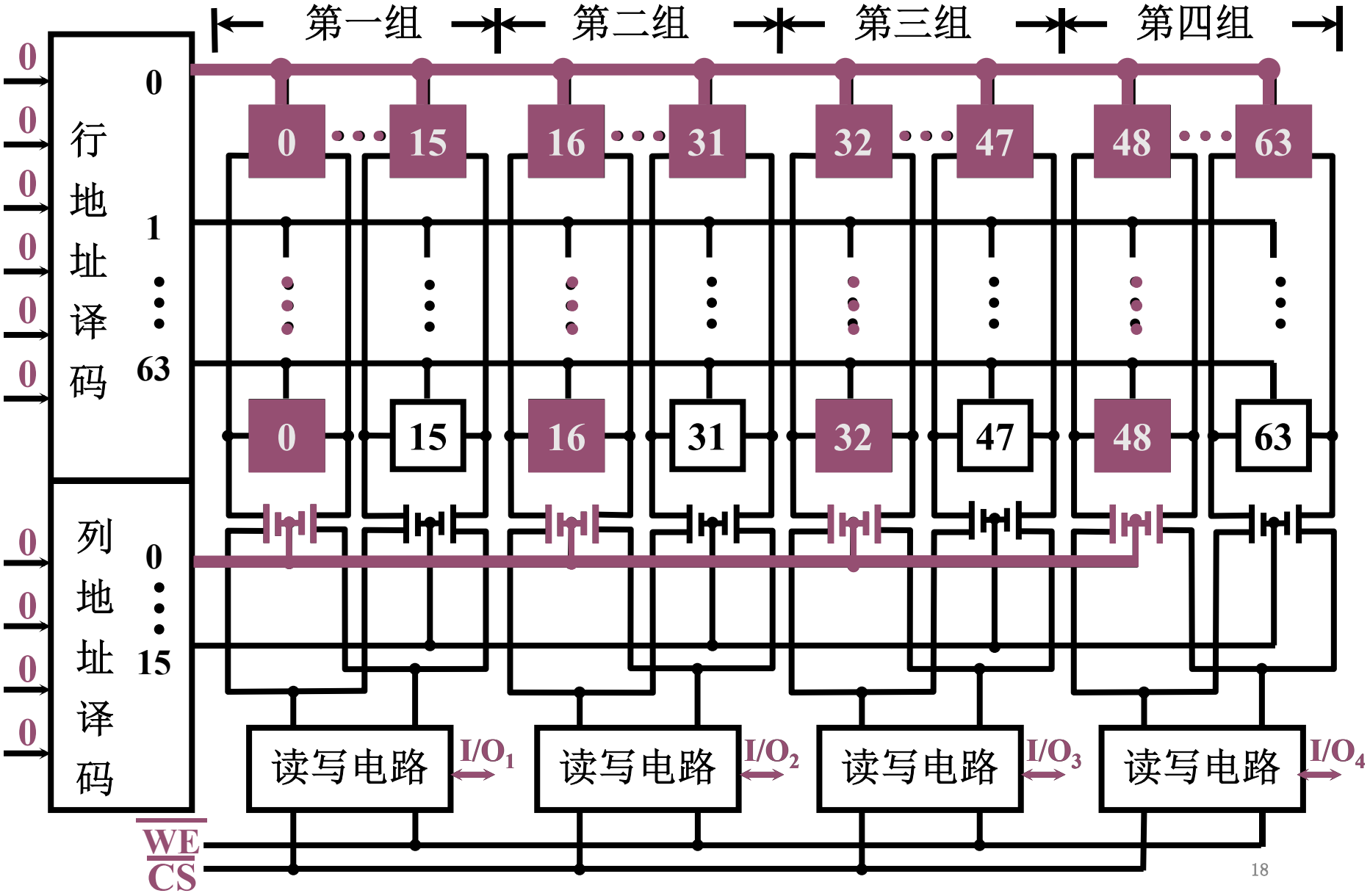

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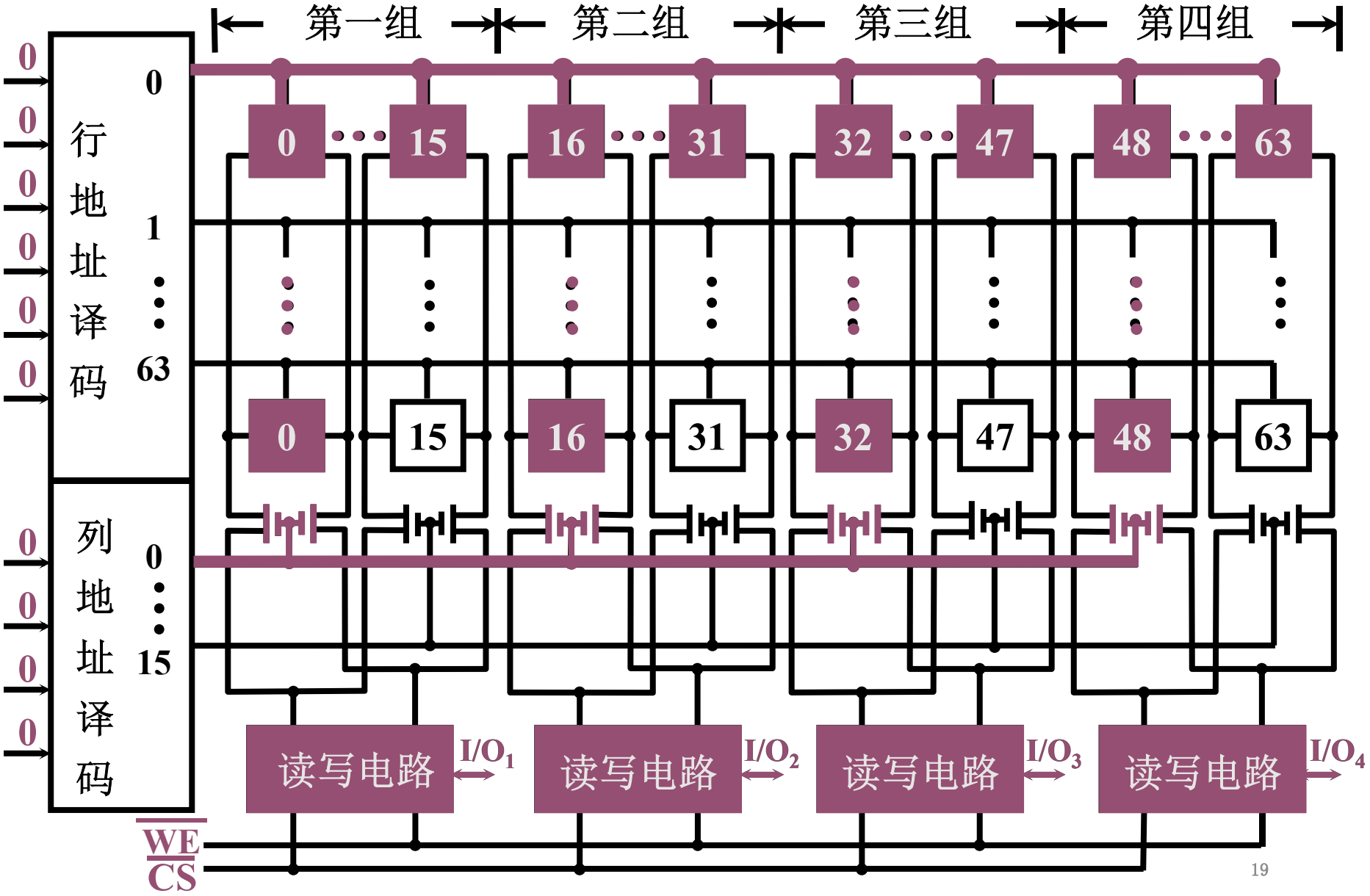

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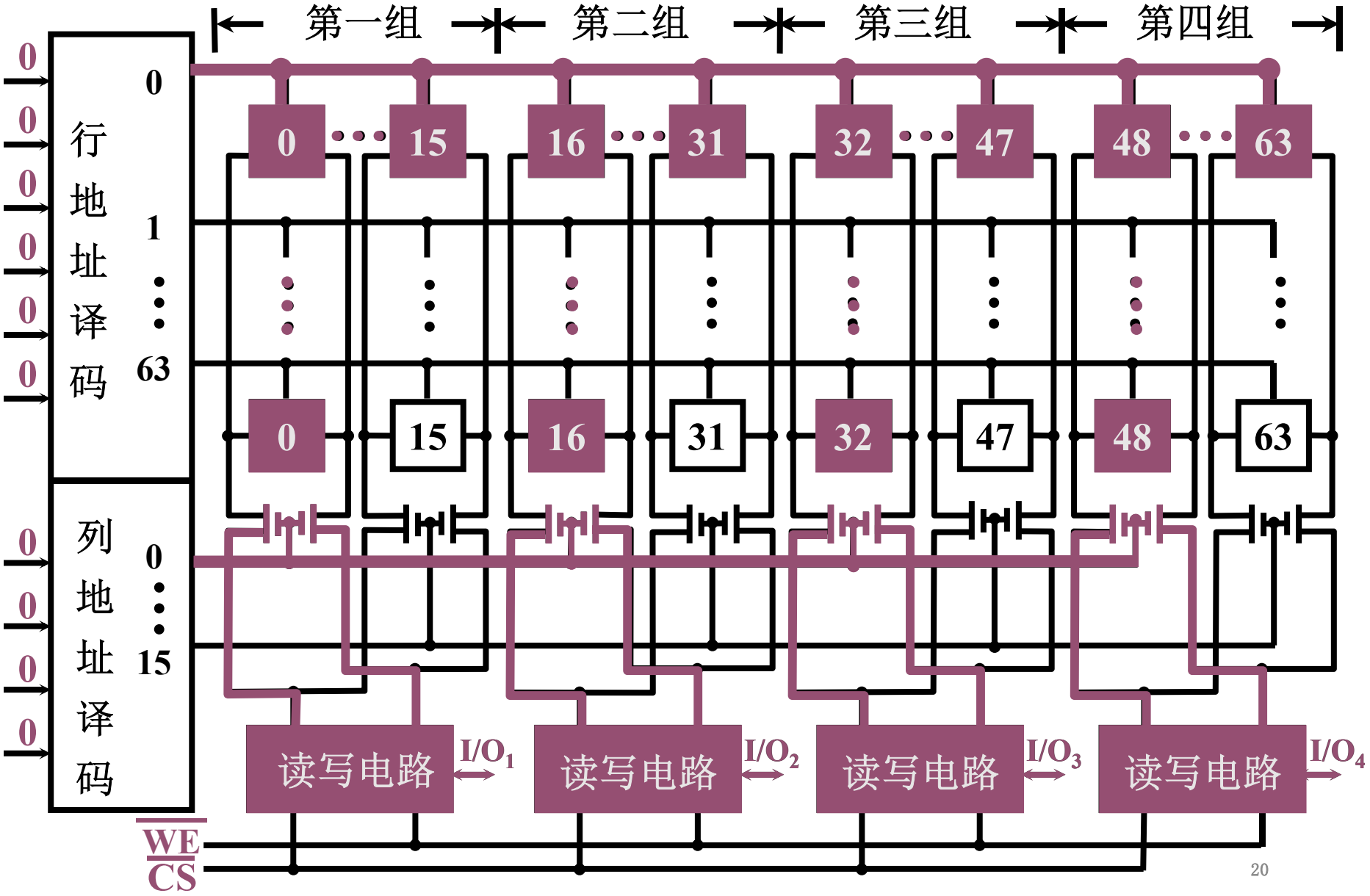

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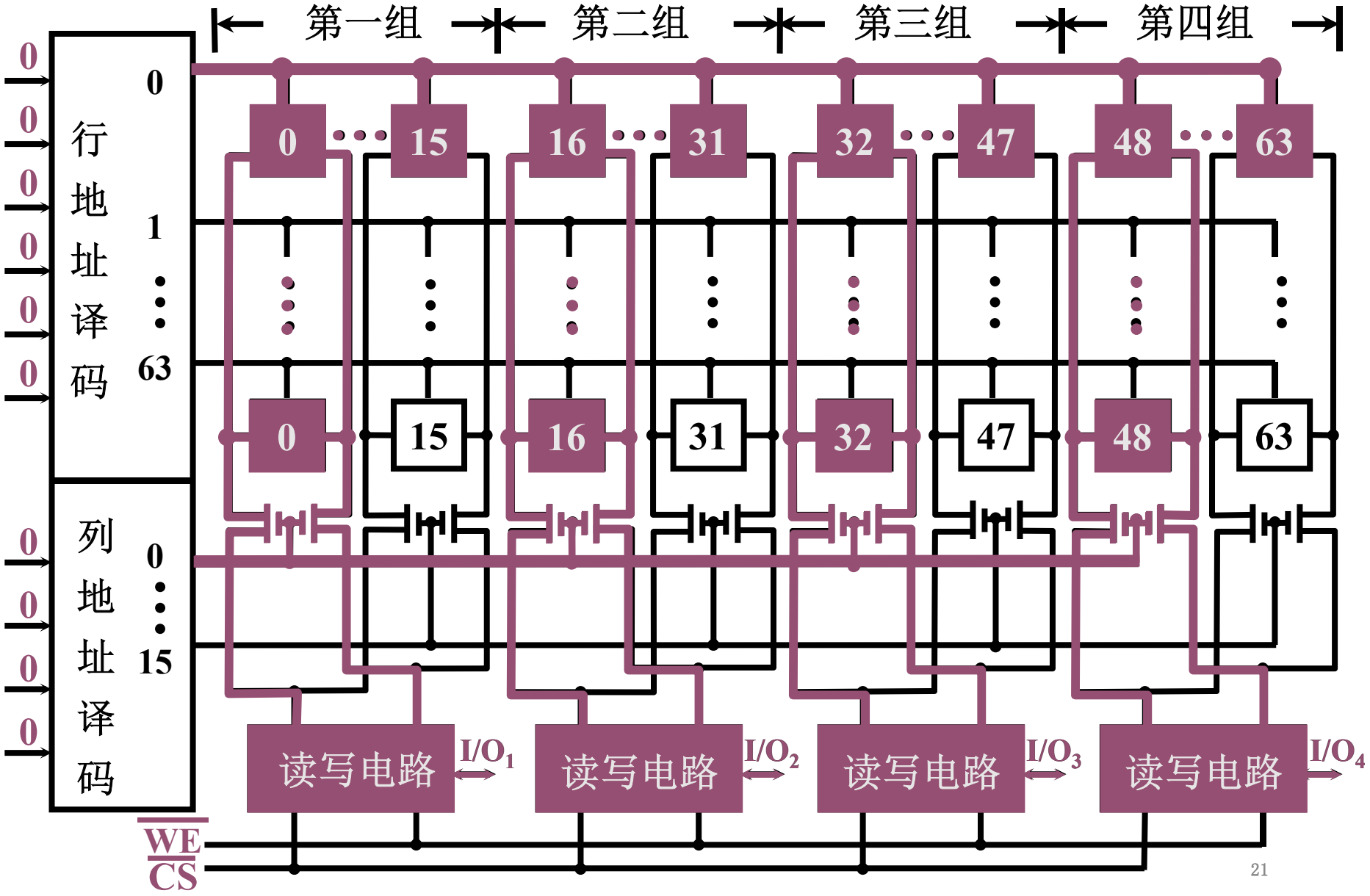

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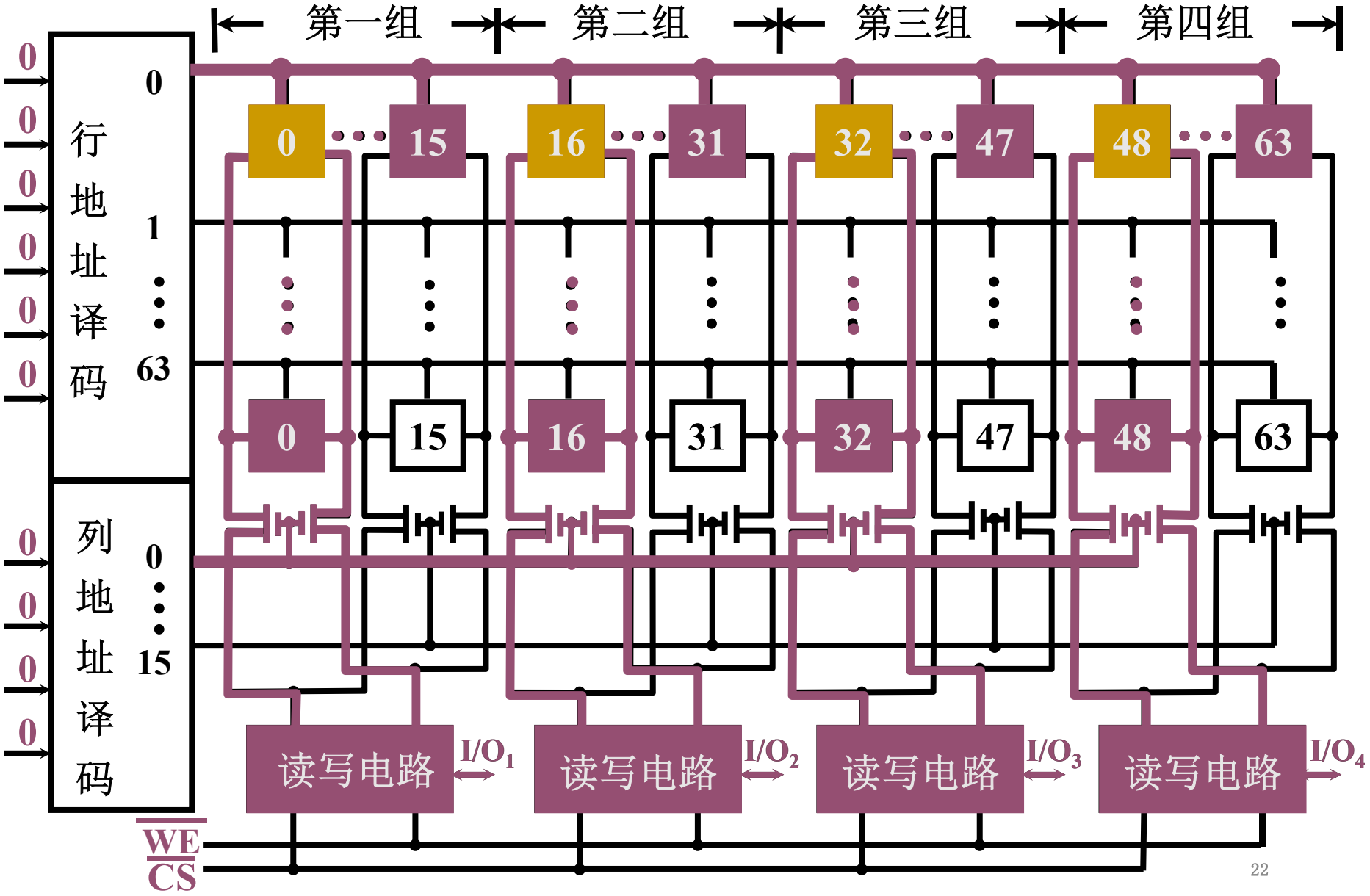
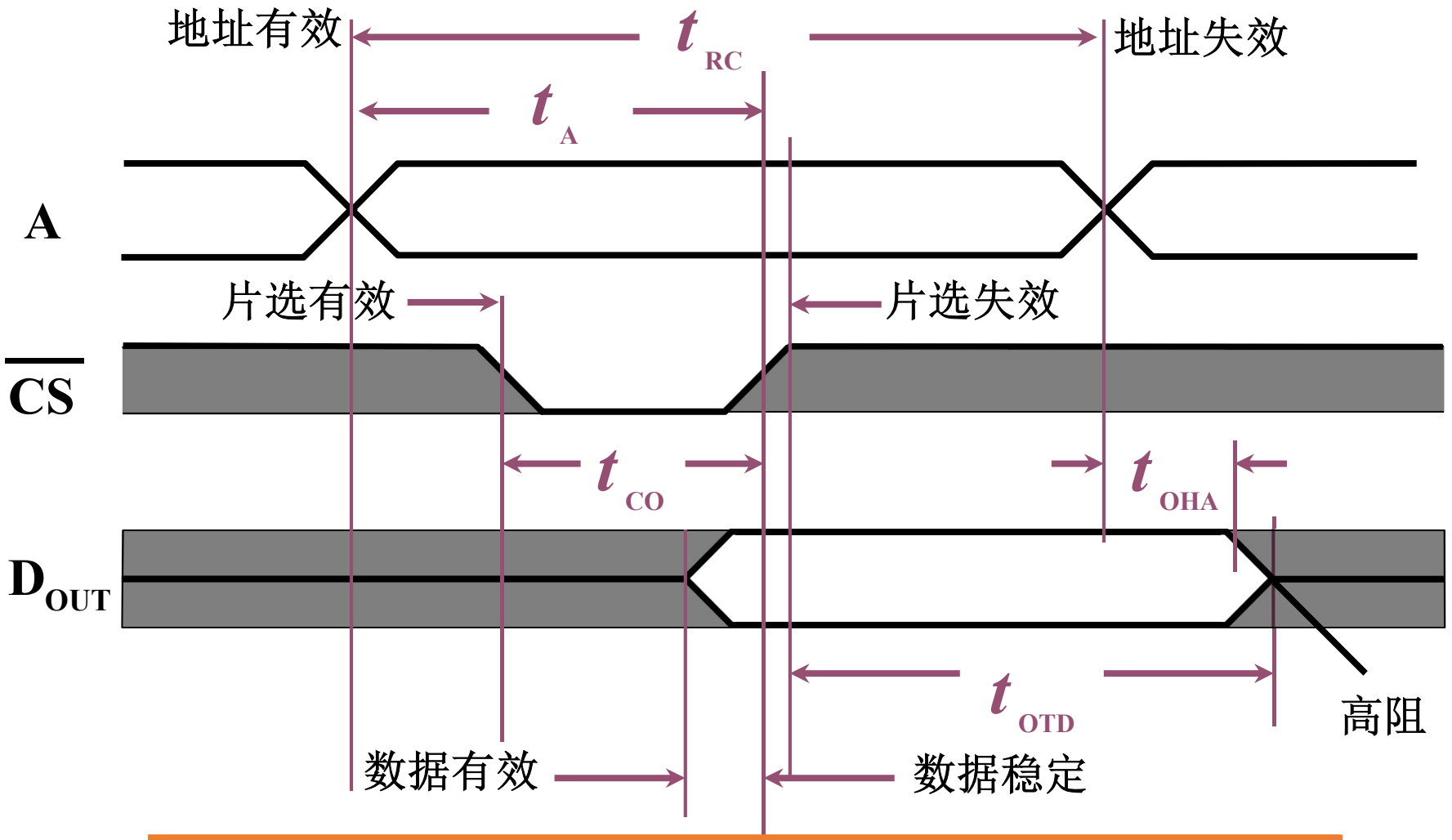


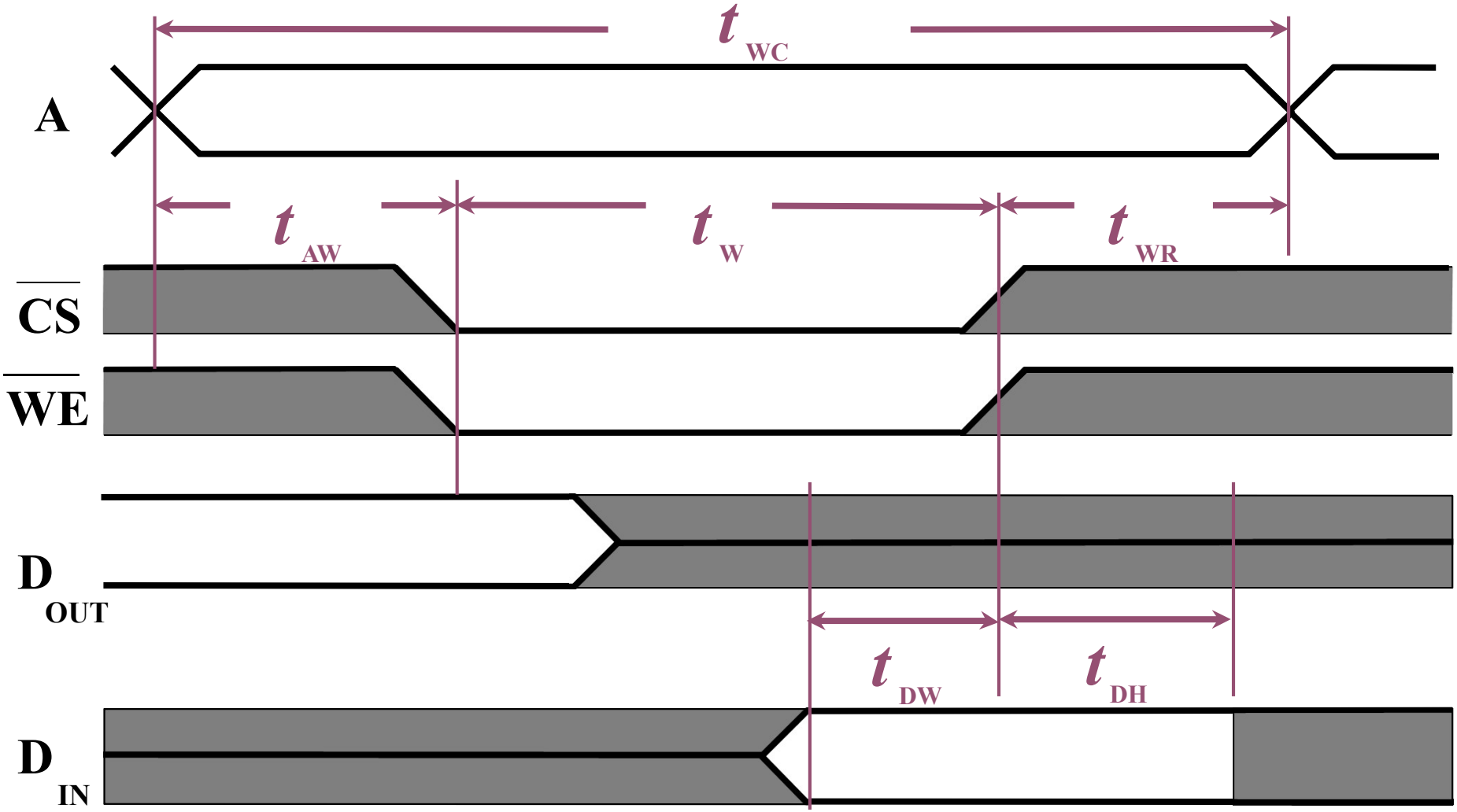
(3) 静态 RAM 读 时序



t_{OHA} 地址失效后的 数据维持时间

(4) 静态 RAM (2114) 写 时序

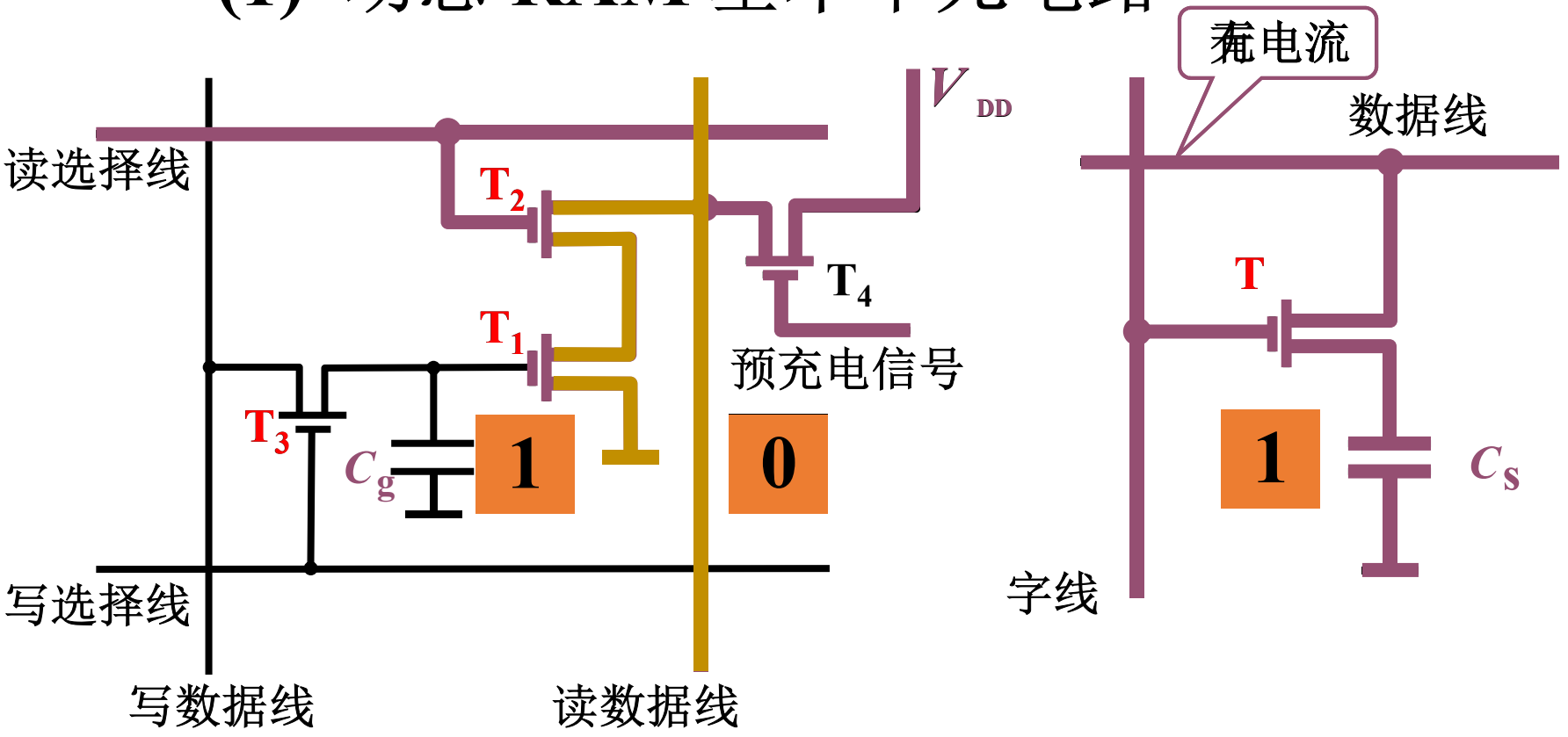
4.2



t_{DH} $\overline{WE}$ 失效后的数据维持时间

2. 动态 RAM (DRAM)

(1) 动态 RAM 基本单元电路



读出与原存信息相反

写入与输入信息相同

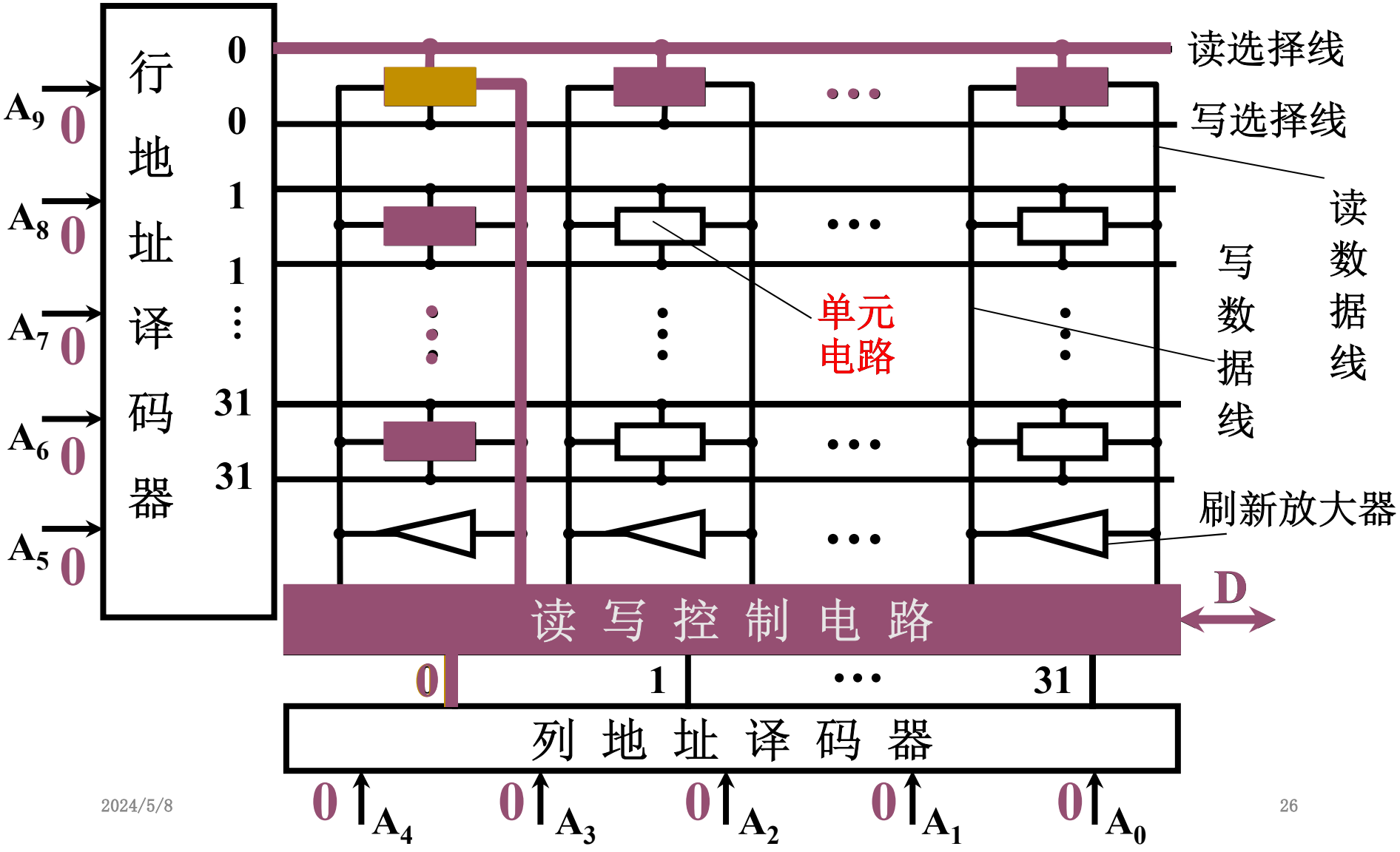
读出时数据线有电流 为 “1”

写入时 C_S 充电为 “1” 放电为 “0”

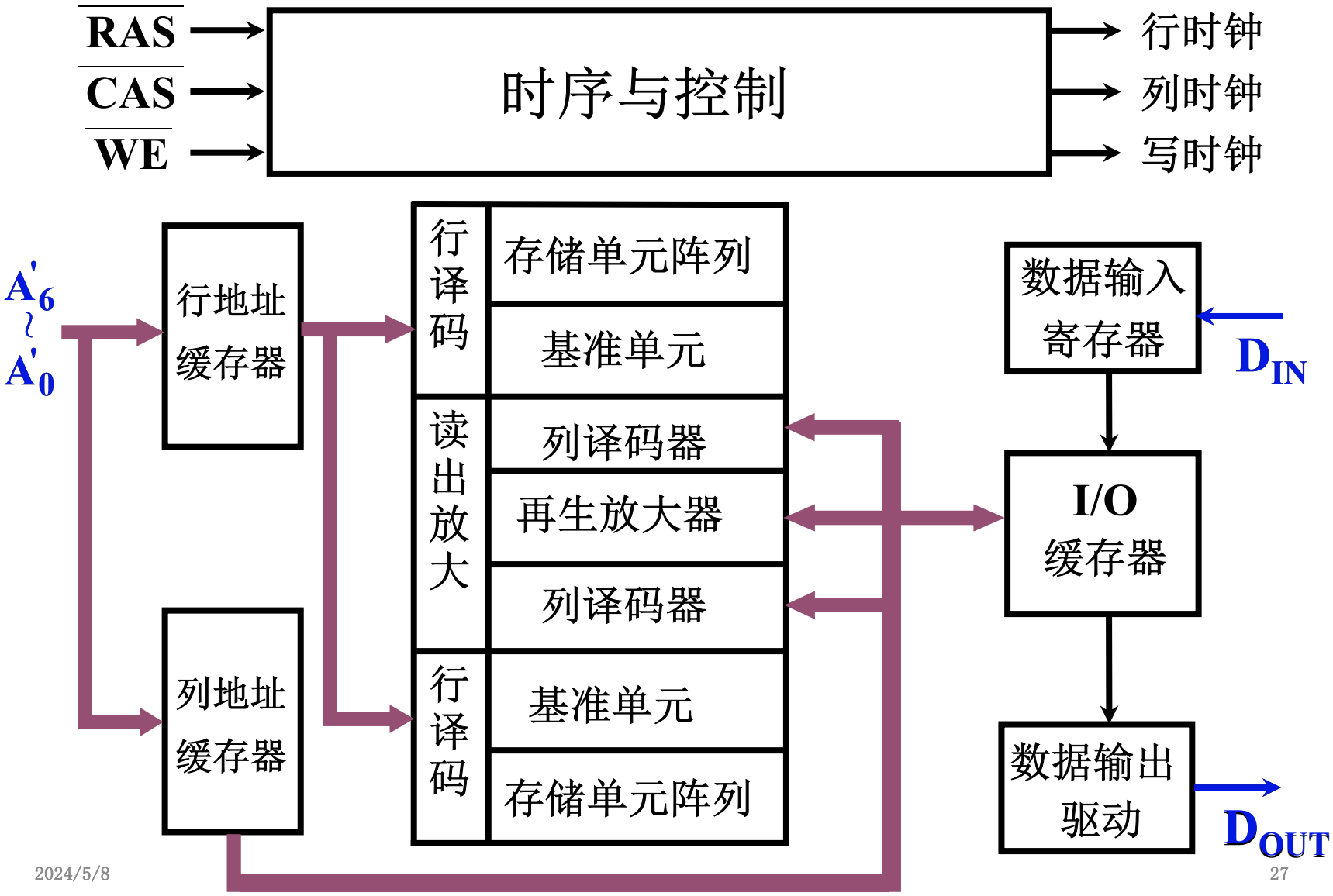
(2) 动态 RAM 芯片举例

三管动态 RAM 芯片 (Intel 1103)

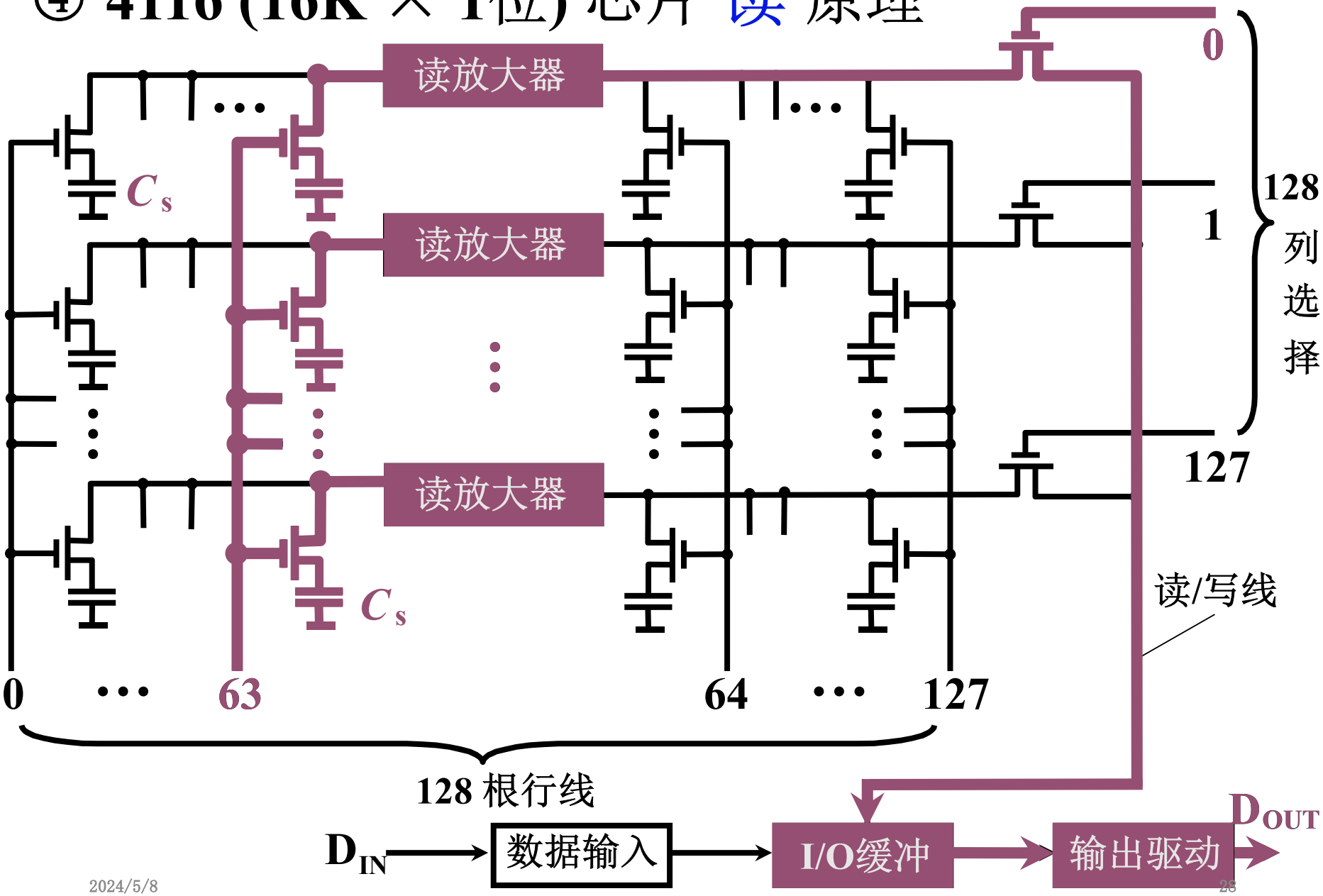
4.2



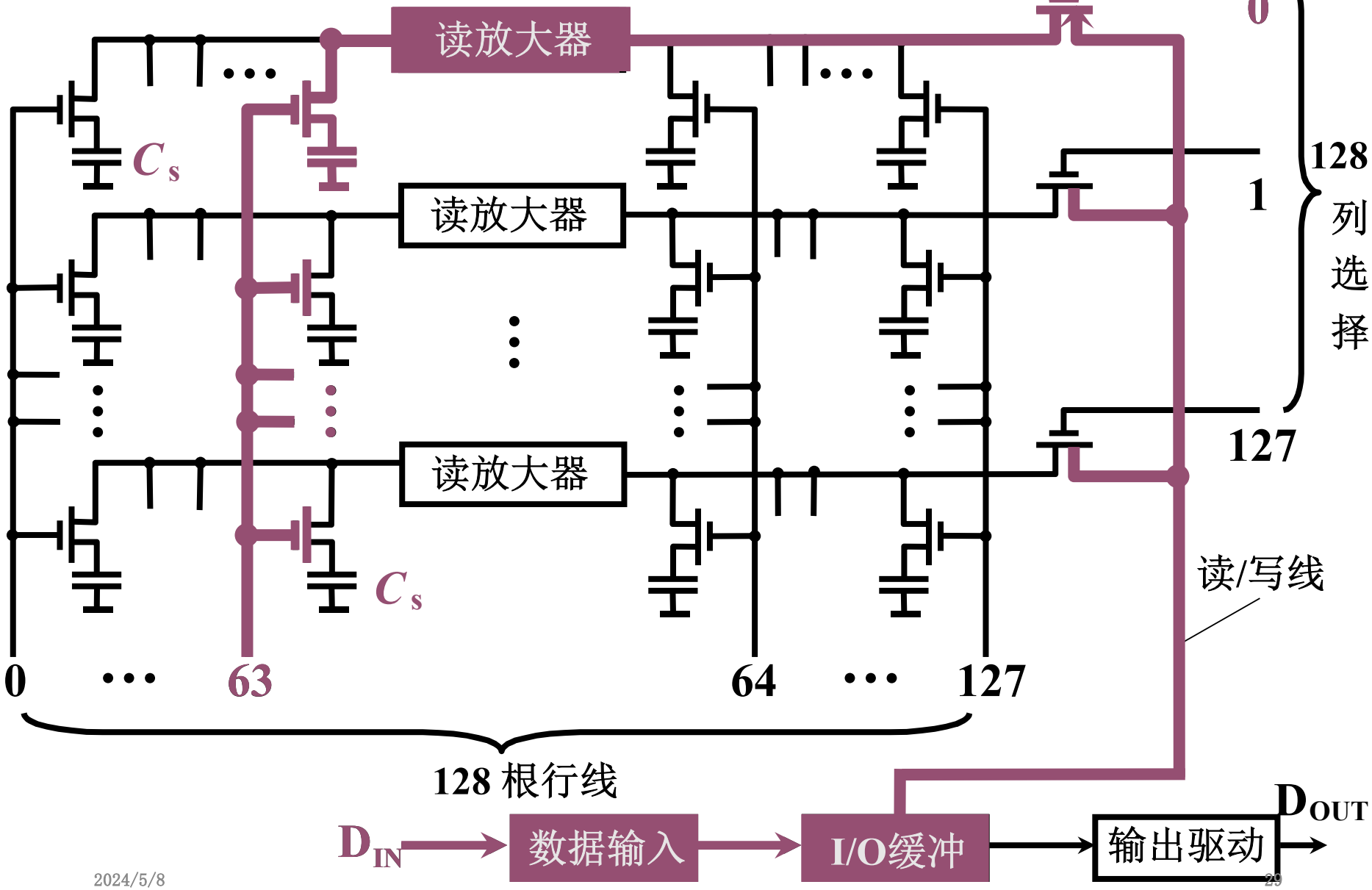
③ 单管动态 RAM 4116 (16K × 1位) 外特性 4.2



④ 4116 (16K × 1位) 芯片 读 原理



⑤ 4116 (16K×1位) 芯片 写 原理



(3) 动态 RAM 时序

行、列地址分开传送

读时序

行地址 $\overline{\text{RAS}}$ 有效

写允许 $\overline{\text{WE}}$ 有效(高)

列地址 $\overline{\text{CAS}}$ 有效

数据 D_{OUT} 有效

写时序

行地址 $\overline{\text{RAS}}$ 有效

写允许 $\overline{\text{WE}}$ 有效(低)

数据 D_{IN} 有效

列地址 $\overline{\text{CAS}}$ 有效

(4) 动态 RAM 刷新

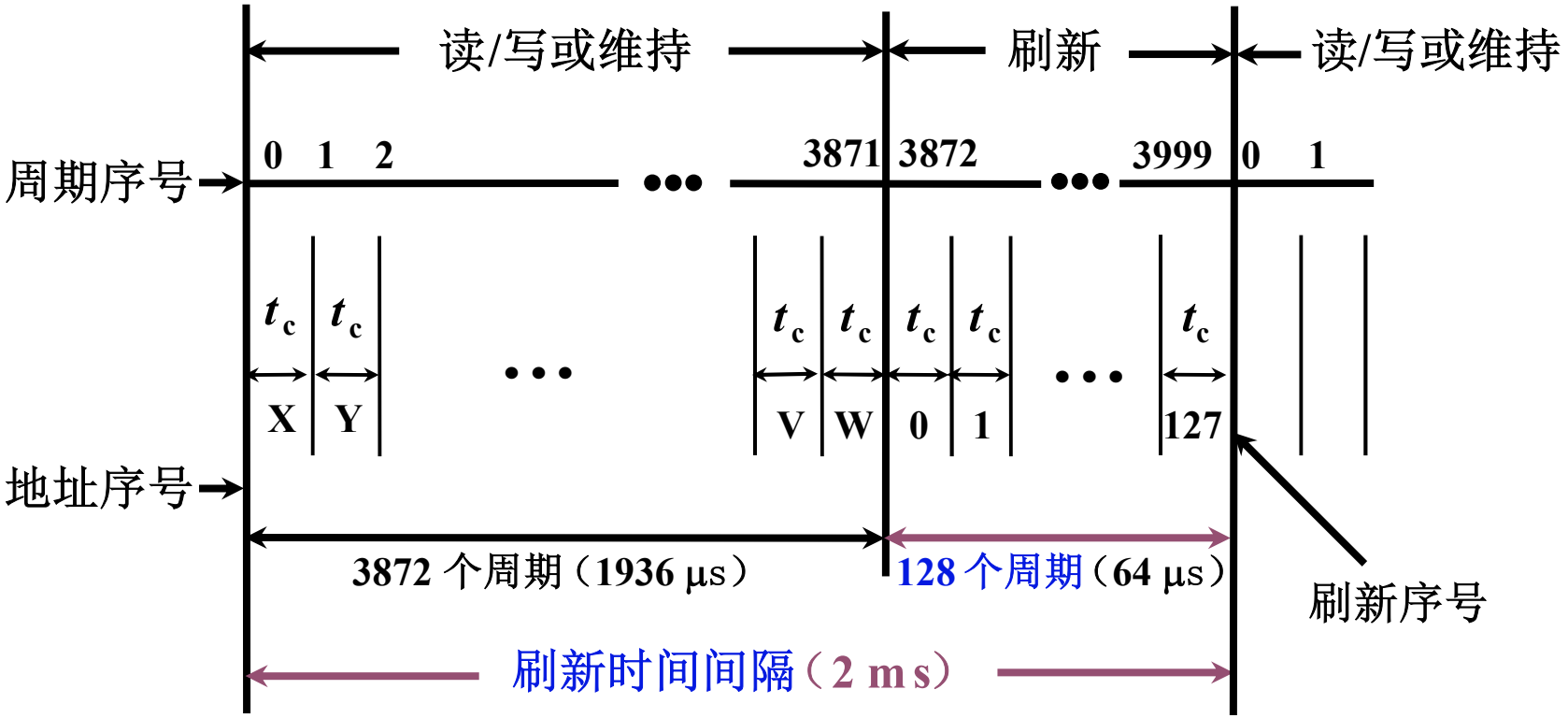
- 刷新：定期补充电荷以避免电荷泄露引起的信息丢失
  - 电容存在泄露电流
- 刷新周期：存储器两次完整刷新之间的时间间隔
  - 信息存储到泄漏之间必须完成刷新，称为最大刷新周期
- 按行刷新
  - 存储体采用双译码结构，刷新地址计数器给出刷新行地址
- 刷新方式
  - CPU与刷新控制器对DRAM的争用问题
  - 集中式、分散式、异步式

(4) 动态 RAM 刷新

4.2

刷新与行地址有关

① 集中刷新 （存取周期为0.5 μs ）以128 × 128 矩阵为例

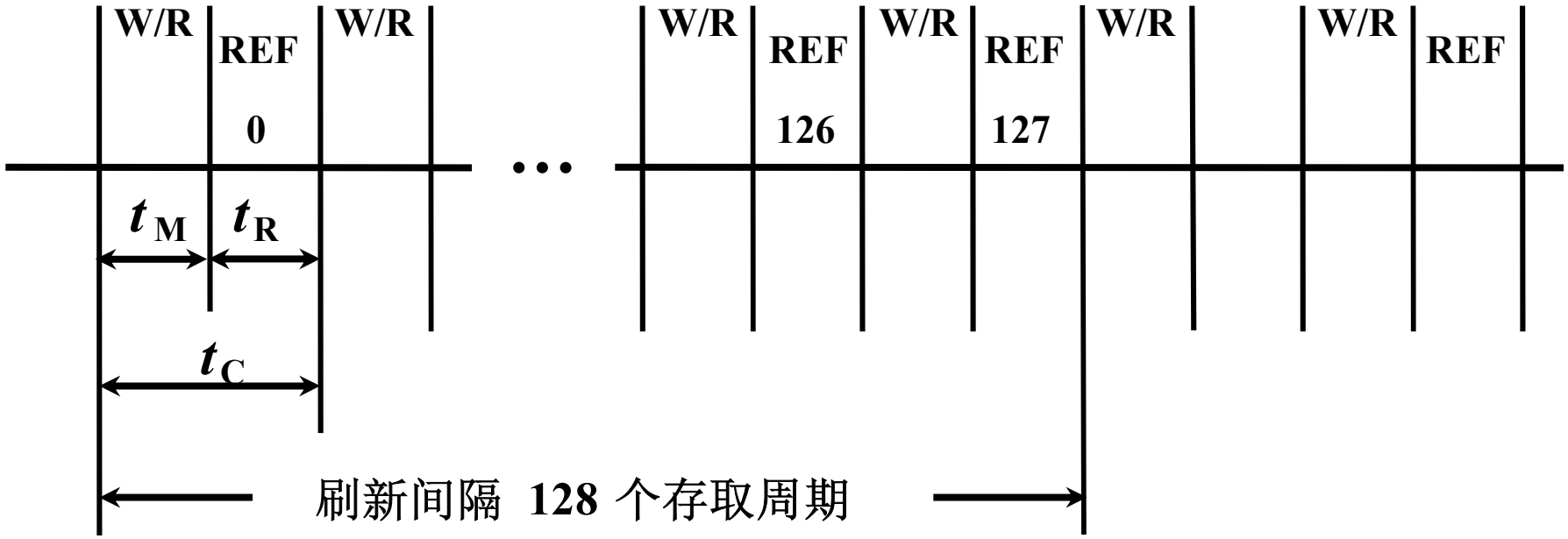


“死区” 为 0.5 μs ×128 = 64 μs

“死时间率” 为 128/4 000 ×100% = 3.2%

② 分散刷新（存取周期为1μs）

以 128 ×128 矩阵为例



$t_C = t_M + t_R$

读写　刷新

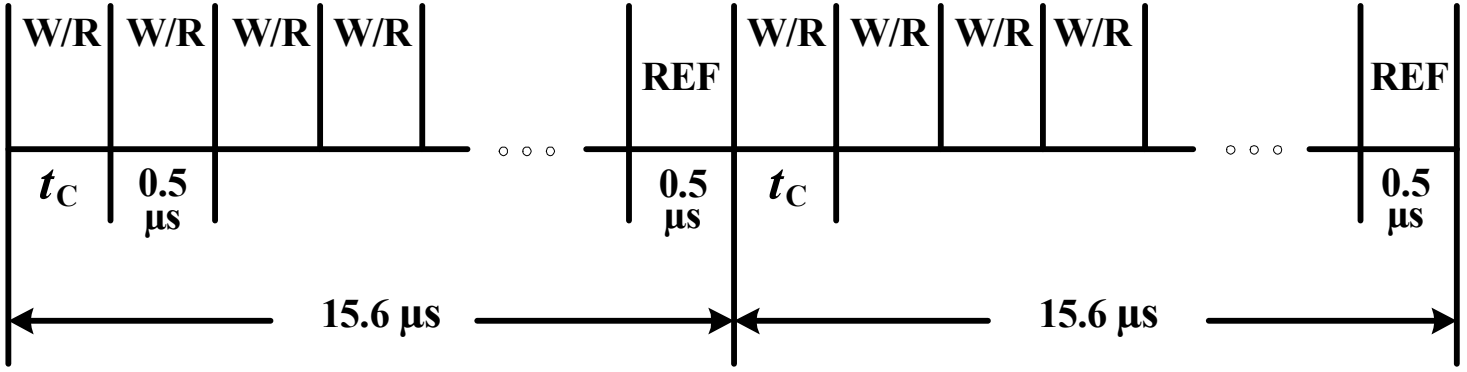
无“死区”

(存取周期为 0.5 μs + 0.5 μs)

③ 分散刷新与集中刷新相结合（异步刷新）

对于 **128 ×128** 的存储芯片（存取周期为 **0.5 μs**）

若每隔 **15.6 μs** 刷新一行



每行每隔 **2 ms** 刷新一次　　“死区”为 **0.5 μs**

将刷新安排在指令译码阶段，不会出现“死区”

3. 动态 RAM 和静态 RAM 的比较

主存

缓存

	DRAM	SRAM
存储原理	电容	触发器
集成度	高	低
芯片引脚	少	多
功耗	小	大
价格	低	高
速度	慢	快
刷新	有	无

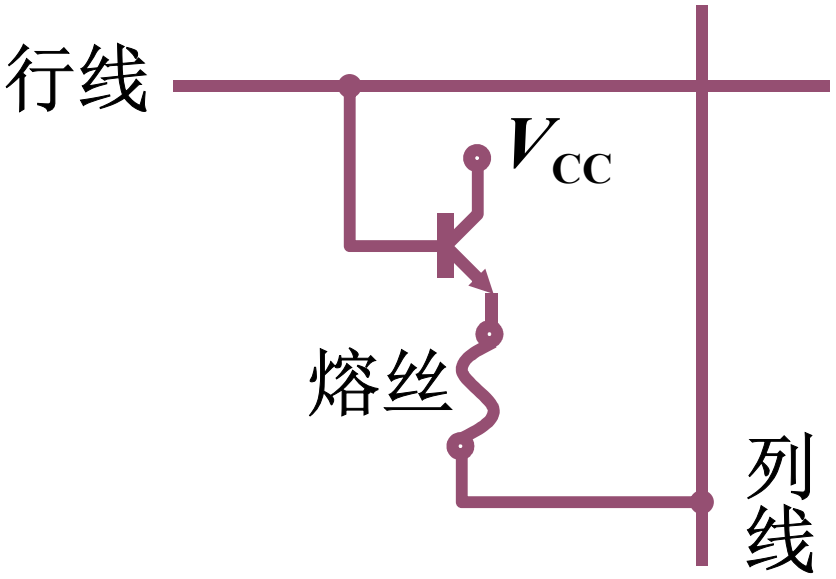
四、只读存储器（ROM）

1. 掩模 ROM (MROM)

行列选择线交叉处有 MOS 管为“1”

行列选择线交叉处无 MOS 管为“0”

2. PROM (一次性编程)

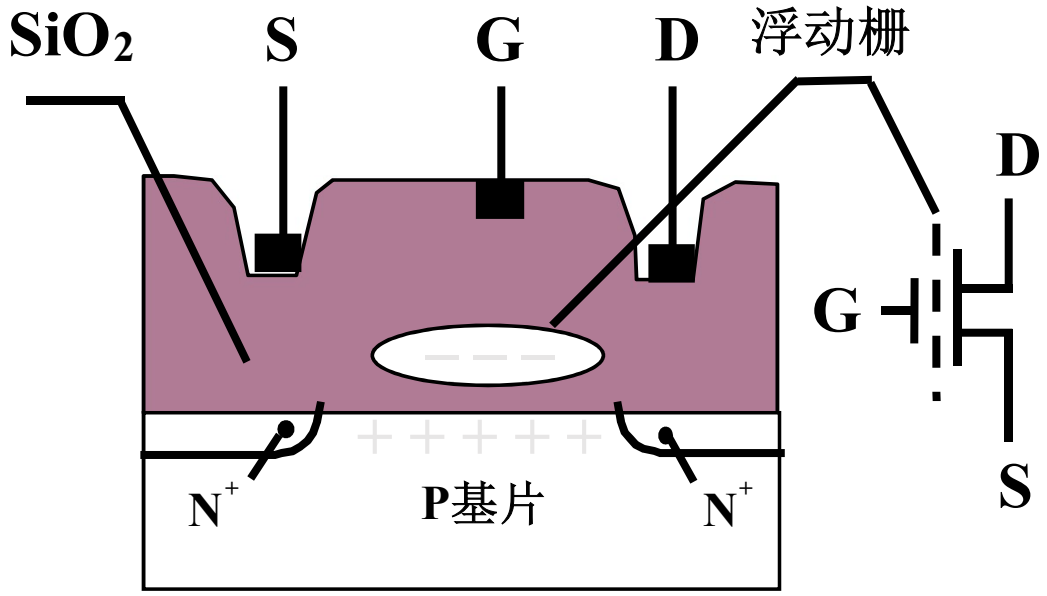


熔丝断　　为“0”

熔丝未断　为“1”

3. EPROM (多次性编程)

(1) N型沟道浮动栅 MOS 电路



G 栅极

S 源

D 漏

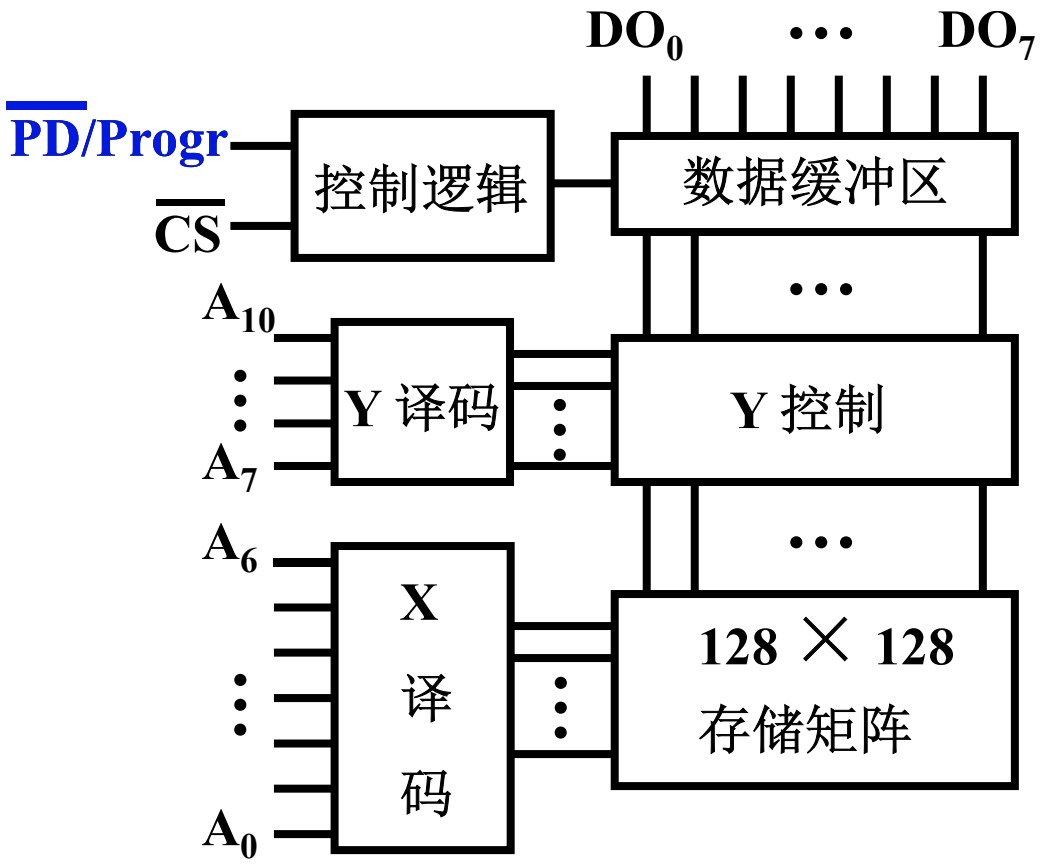
紫外线全部擦洗

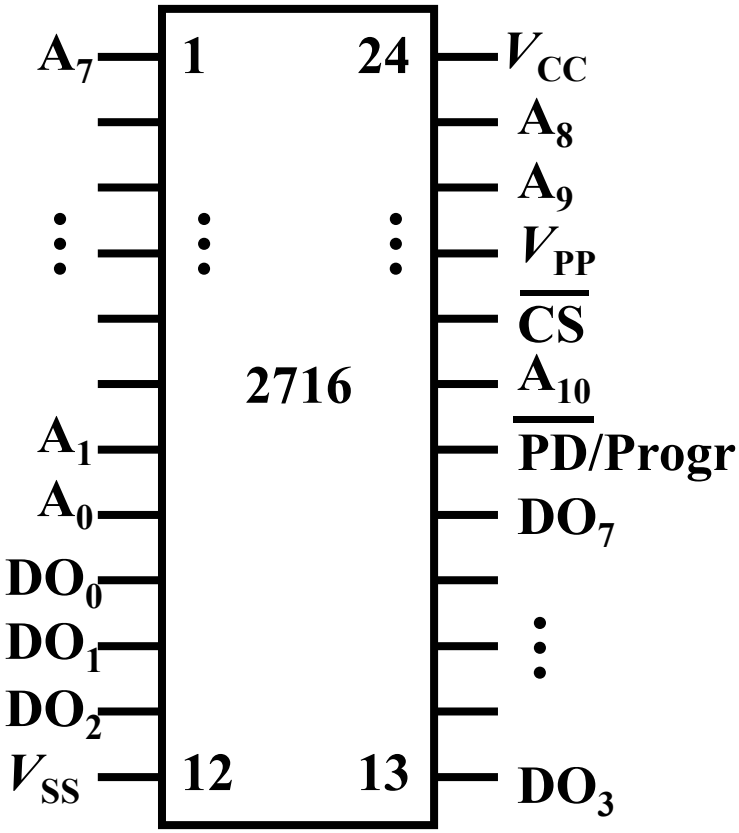
D 端加正电压　　形成浮动栅　　S 与 D 不导通为 “0”

D 端不加正电压　　不形成浮动栅　　S 与 D 导通为 “1”

(2) 2716 EPROM 的逻辑图和引脚

4.2





PD/Progr 功率下降 / 编程输入端　读出时 为 低电平

4. EEPROM (多次性编程)

电可擦写

局部擦写

全部擦写

5. Flash Memory (闪速型存储器)

EPROM 价格便宜 集成度高

EEPROM 电可擦洗重写

比 **EEPROM**快 具备 **RAM** 功能

五、存储器与 CPU 的连接

4.2

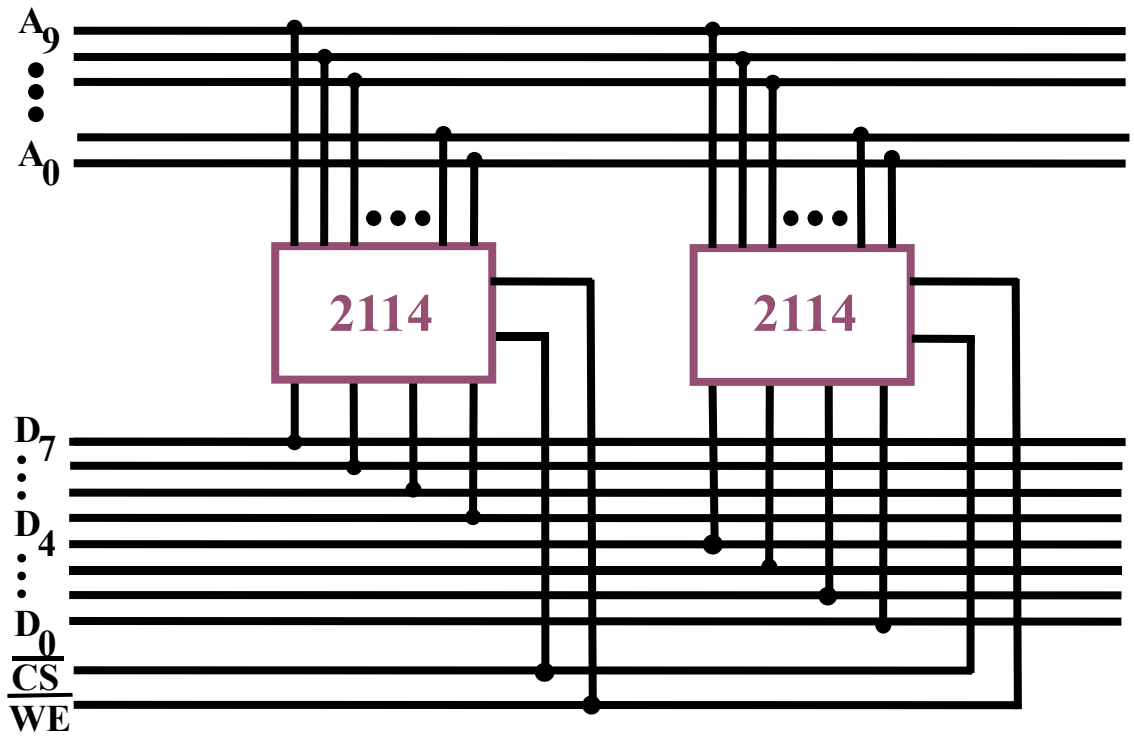
1. 存储器容量的扩展

(1) 位扩展（增加存储字长）

用 ?2片 1K×4位 存储芯片组成 1K×8位 的存储器

10根地址线

8根数据线

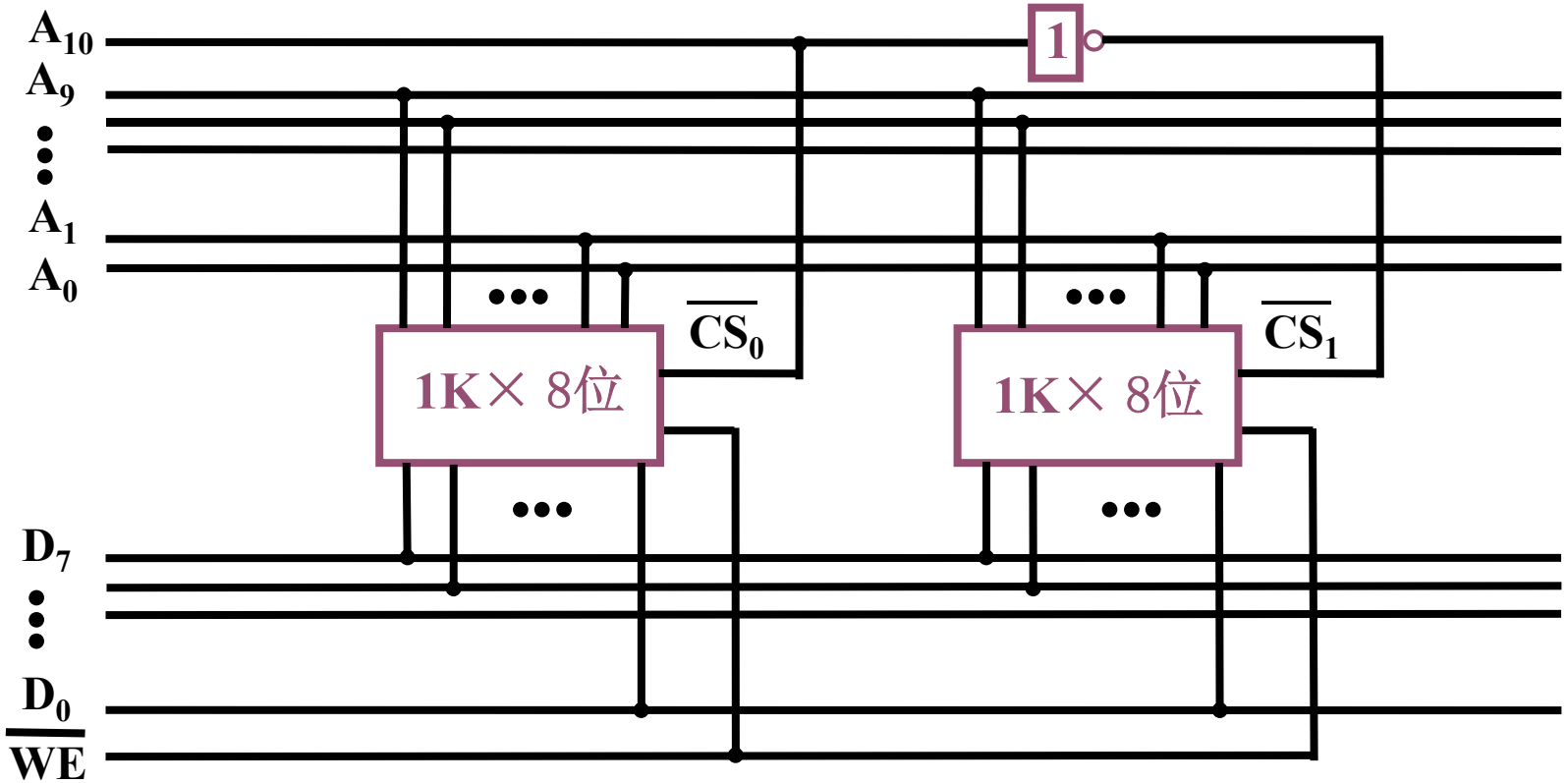


(2) 字扩展（增加存储字的数量）

11根地址线

用 2片 1K×8位 存储芯片组成 2K×8位 的存储器

8根数据线

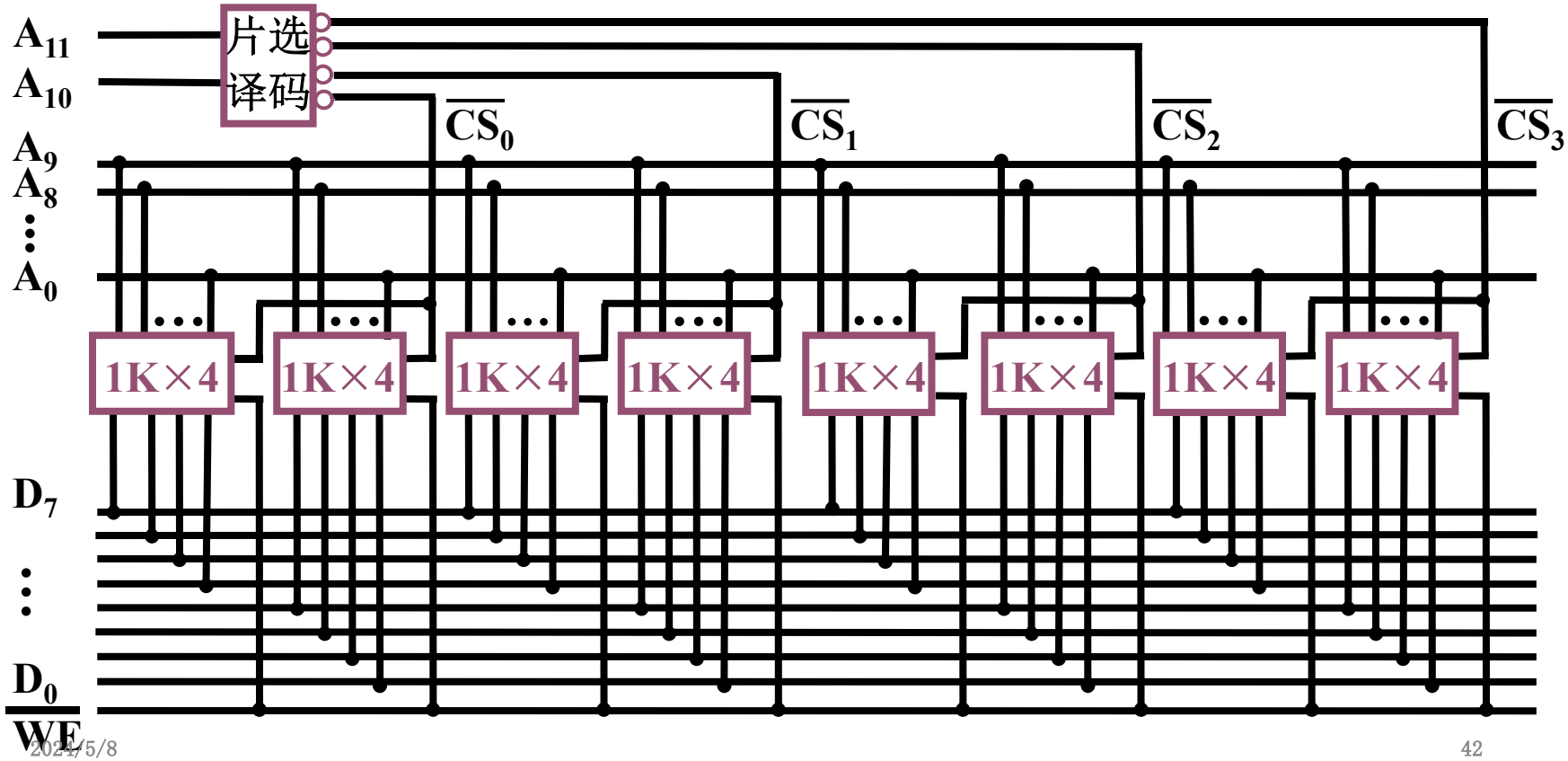


(3) 字、位扩展

用 ?8片 1K×4位 存储芯片组成 4K×8位 的存储器

12根地址线

8根数据线



2. 存储器与 CPU 的连接

(1) 地址线的连接

(2) 数据线的连接

(3) 读/写命令线的连接

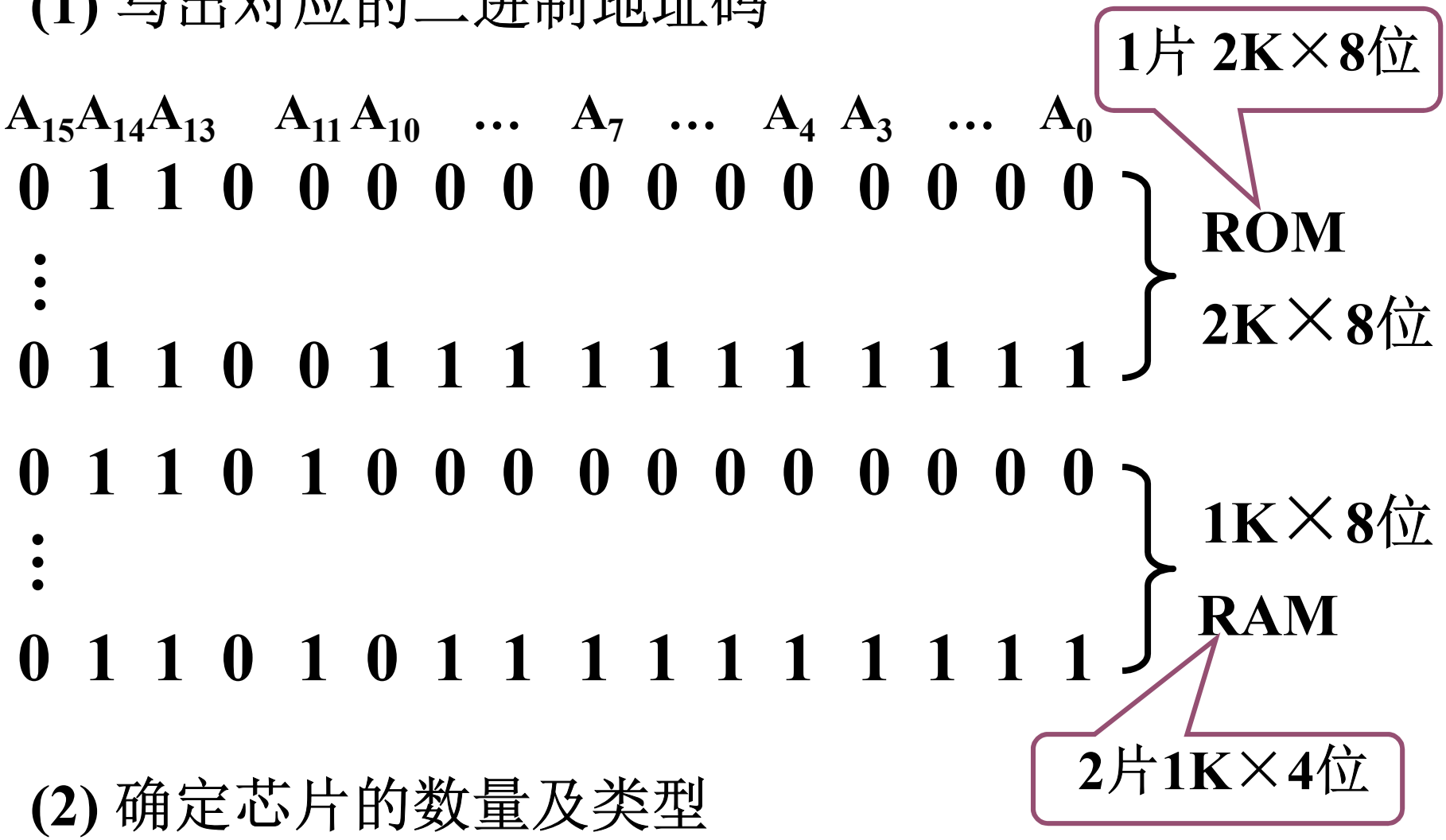
(4) 片选线的连接

(5) 合理选择存储芯片

(6) 其他　　时序、负载

例4.1 解：

(1) 写出对应的二进制地址码



(2) 确定芯片的数量及类型

(3) 分配地址线

A_{15}	A_{13}	A_{11}	A_{10}	…	A_7	…	A_4	A_3	…	A_0	
0 1	1	0	0	0	0 0	0	0	0	0	0	1片 ROM
⋮											2K×8位
0 1	1	0	0	1	1 1	1	1	1	1	1	
0 1	1	0	1	0	0 0	0	0	0	0	0	2片RAM
⋮											1K×4位
0 1	1	0	1	0	1 1	1	1	1	1	1	
	C	B	A								

A_{10}~A_0 接 2K×8位 ROM 的地址线

A_9 ~A_0 接 1K×4位 RAM 的地址线

(4) 确定片选信号

例 4.1 CPU 与存储器的连接图