ALC5651

Ultra-Low Power Two-Channel Audio CODEC
with SounzReal™ Digital Sound Effect
for Mobile Devices

Application Note

Rev. 0.1

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5651 Audio CODEC chip.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

.Revision History

Revision	Release Date	Summary
0.1	2012-9-26	preliminary

Table of Contents

1. Initial

1.1. Power on/off sequence

To avoid the unexpected issue, the power on/off sequence of ALC5651 is better to be as below:

i. The power on sequence：

(1) Power on DBVDD & AVDD & CPVDD & DACREF.
(2) Power on MICVDD
(3) Software initialize

ii. The power off sequence：

(1) Power down all codec power by software
(2) Power off MICVDD
(3) Power off the DBVDD & AVDD & CPVDD& DACREF.

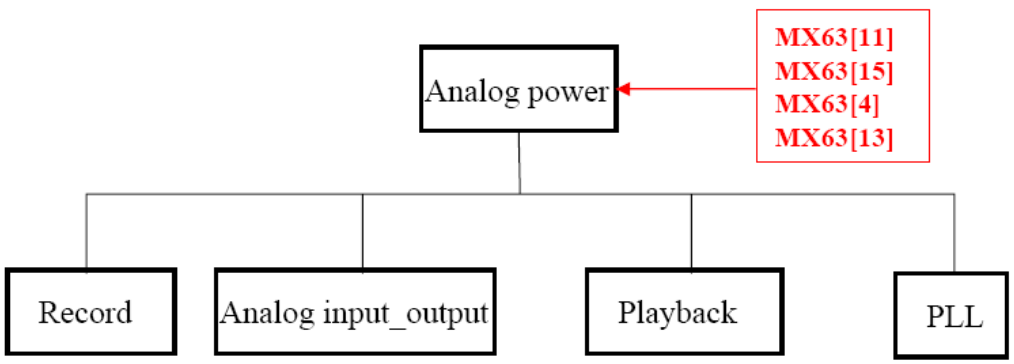
1.2. Power block diagram

When codec is initial power on, we suggest customer to enable the registers as below:

Control Register	Reg	Value	Description	Note
Pow_bg_bias	MX63[11]	1'b	Power On MBIAS Bandgap	
Pow_vref1	MX63[15]	1'b	Power On Vref1	
Pow_main_bias	MX63[13]	1'b	Power On Main Bias	
Pow_vref2	MX63[4]	1'b	Power On Vref2	
En_ fastb1	MX63[14]	0'b	Enable fast Vref1	
En_ fastb2	MX63[3]	0'b	Enable fast Vref2	
digital_gate_ctrl	MXFA[0]	1'b	Enable MCLK input	

Part of the analog can be used after enable **Pow_vref1 & Pow_vref2 (**with the fast Vref1& fast Vref2 enable) pass through 0.2 second. After Vref1 and Vref2 power is ready(0.2 sec) , the **En_ fastb1 & En_ fastb** can be disable(set to 1'b) for better audio performance.

After power on these registers, we will not disable them unless the system is power down.
The picture as below is the power block diagram of ALC5651 .The function just like Record ..etc. in this picture will be introduced one by one in later chapter.



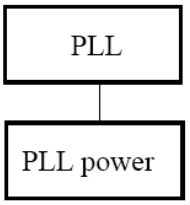
2. PLL

PLL is mainly used to generate I2S required clock for Audio CODEC by input an unrelated reference clock.

2.1. Power ON

For Enable PLL, the related block has to be power on and Register shown as below has to be enabled.

Control Register	Reg	Value	Description	Note
Pow_bg_bias	MX63[11]	1'b	Power On MBIAS Bandgap	
Pow_vref1	MX63[15]	1'b	Power On Vref1	
Pow_main_bias	MX63[13]	1'b	Power On Main Bias	
Pow_vref2	MX63[4]	1'b	Power On Vref2	
Pow_pll	MX64[9]	1'b	Power On PLL	



Note: MX63[11], MX63[15], MX63[4], MX63[13] should enable first

2.2. PLL Input Path

There are three sources that can be used as PLL input source: MCLK, BCLK1 and BCLK2 can be configured by **sel_pll_sour**. And there is a divider in front of PLL by setting **sel_pll_pre_div**.

Name	Bits	Default value	Function Description
sel_pll_sour	MX80 [13:12]	0'h	Pll Source Selection 00'b: From MCLK 01'b: From BCLK1 10'b: From BCLK2 11'b: Reserved
sel_pll_pre_div	MX80[3]	0'b	PLL Pre-Divider 0'b: ÷ 1 1'b: ÷ 2

2.3. PLL Output Path

The system clock of I2S Stereo DAC/ADC is SYSCLK which can source from **MCLK** or **PLL** by setting **sel_sysclk1**.

Name	Bits	Default value	Function Description
sel_sysclk	MX80 [15:14]	0'h	SYSCLK1 Source MUX Control 00'b: MCLK 01'b: PLL 10'b: Reserved 11'b: Reserved

2.4. PLL Parameter Setting

2.4.1. PLL Parameter

According to different PLL reference input clock frequency, different PLL parameters have to be set by Driver.

Name	Bits	Default value	Function Description
Pll_n_code	MX81 [15:7]	0'h	PLL N[8:0] Code 000000000'b: Div 2 000000001'b: Div 3 ~ 111111111'b: Div 513
Pll_k_code	MX81 [4:0]	0'h	PLL K[4:0] Code 000'b: ÷ 2 001'b: ÷ 3 ~ 111'b: ÷ 9
Pll_m_code	MX82 [15:12]	0'h	PLL M[3:0] Code 0000'b: Div 2 0001'b: Div 3 … 1111'b: Div 17
Pll_m_bypass	MX82 [11]	0'h	Bypass PLL M Code 0'b: No bypass 1'b: Bypass

The Function of PLL is as below:

$$F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) \{Typical\ K=2\}$$

For example 1:

48KHz sample rate:

(unit: MHz)

PLL IN	N	M	F_{VCO}	K	F_{OUT}	MX81	MX82
13	119	14	98.312	2	24.578	3B82	E000
3.6864	78	1	98.304	2	24.576	2702	1000
2.048	46	0	98.304	2	24.576	1702	0800
4.096	22	0	98.304	2	24.576	0B02	0800
12	129	14	98.25	2	24.562	4082	E000
15.36	30	3	98.304	2	24.576	0F02	3000
16	41	5	98.285	2	24.571	1482	5000
19.2	85	15	98.258	2	24.564	2A82	F000
19.68	3	0	98.4	2	24.6	0182	0800

For example 2:

44.1KHz sample rate

(unit: MHz)

PLL IN	N	M	F_{VCO}	K	F_{OUT}	MX81	MX82
13	116	15	90.235	2	22.558	3A02	F000
3.6864	47	0	90.316	2	22.5792	1782	0000
2.048	439	8	90.316	2	22.5792	DB82	8000
4.096	213	11	67.741	1	22.58	6A81	B000
12	126	15	90.352	2	22.588	3F02	F000
15.36	98	15	90.352	2	22.588	3102	F000
16	77	12	90.285	2	22.571	2682	C000
19.2	78	15	90.352	2	22.588	2702	F000
19.68	76	15	90.296	2	22.574	2602	F000

2.5. PLL Setting Example

For example : The input clock source from Samsung CPU is 12 MHz.

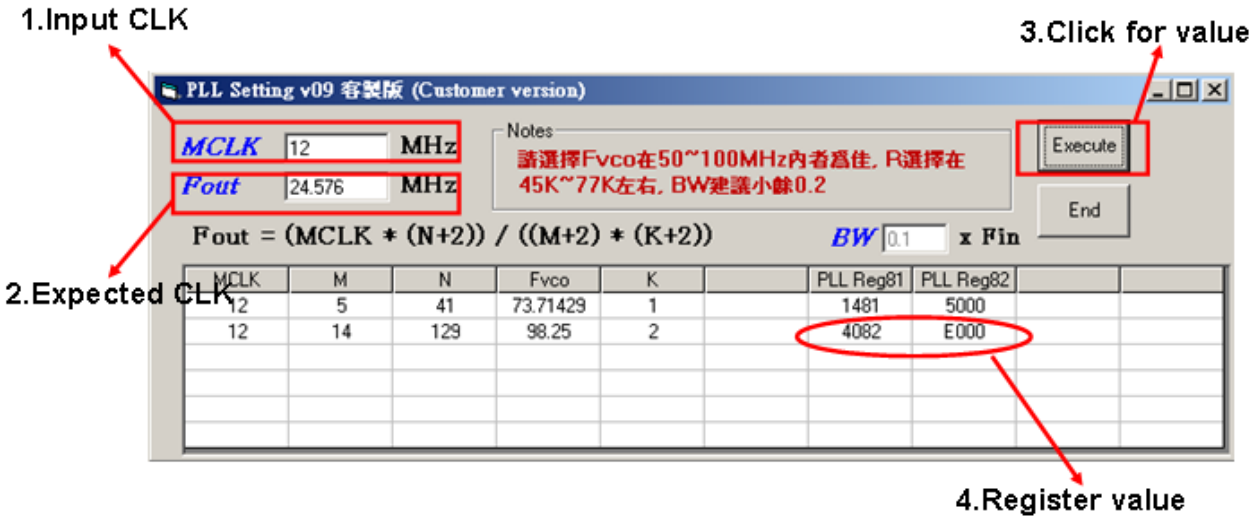
Step1: When the codec initialize. At first, we should enable the power for PLL**.** The setting is as below:

a. Set MX63[11] to 1'b
b. Set MX63 [15] to 1'b
c. Set MX63 [13] to 1'b
d. Set MX63 [4] to 1'b
e. Set MX64[9] to 1'b

Step2: Set the PLL divider to transform 12MHz to 24.576MHz

The user needs to set the value of MX81 & MX82 for clock transformation.

Note: Realtek has made a tool for customer to easily produce the MX81 & MX82 value. The using of PLL tool is in the picture as below:



a. Use the PLL tool to produce the value [4082] for MX81 and [E000] for MX82
b. Set MX81: 4082'h
c. Set MX82: E000'h

Step3: Set the system clock source from MCLK to PLL.
The original system clock source is from MCLK (MX80[15:14]: 00'b)
We have to change the clock source from MCLK to PLL.
So , we set MX80[15:14]:01'b and then delay 10m sec

Step4: After setting MX80[15:14] to change the clock source to PLL , the clock source change to PLL immediately. PLL starts using for system clock.

3. Playback

3.1. Power ON

The Register shown as below has to be set in order to enable DAC.

Control Register	Reg	Value	Description	Note
Pow_bg_bias	MX63[11]	1'b	Power On MBIAS Bandgap	
Pow_vref1	MX63[15]	1'b	Power On Vref1	
Pow_main_bias	MX63[13]	1'b	Power On Main Bias	
Pow_vref2	MX63[4]	1'b	Power On Vref2	
Pow_dac_l_1	MX61[12]	1'b	Power ON DACL1	Depends on path
Pow_dac_r_1	MX61[11]	1'b	Power ON DACR1	Depends on path
Pow_dac_stereo1_filter	MX62[11]	1'b	Power ON Stereo1 DAC Digital Filter	Depends on path
Pow_dac_stereo2_filter	MX62[10]	1'b	Power ON Stereo2 DAC Digital Filter	Depends on path
En_i2s1	MX61[15]	1'b	Enable I2S1 Digital interface	Depends on path
En_i2s2	MX61[14]	1'b	Enable I2S2 Digital interface	Depends on path
digital_gate_ctrl	MXFA[0]	1'b	Enable MCLK input	
En_detect_clk_sys	MXFA[3]	1'b	Enable MCLK detection and auto switch internal clock	Depends on application
Ckxen_dac	PR3D[10]	1'b	Enable DAC Clock1 Generator	
En_ckgen_dac	PR3D[9]	1'b	Enable DAC Clock2 Generator	

3.2. Mixer Control

3.2.1. Power

The power of each mixer can be individually power down in order to save power consumption. The following power management register should be enabled according to playback path.

Control Register	Reg	Value	Description	Note
Pow_outmixl	MX65[15]	1'b	Power On Left OUT Mixer	Depends On Path
Pow_outmixr	MX65[14]	1'b	Power On Right OUT Mixer	Depends On Path

3.2.2. Path Setup

3.2.2.1. OUT mixer

ALC5651 has a stereo OUT mixer which can input the signal from DAC or IN2…etc .The input source of Out mixer can be set by **MX4F** & **MX52**. Each input signal has an attenuate gain control before input OUT mixer.

Name	Bits	Default value	Function Description
Mu_bst2_outmixl	MX4F [6]	1'b	Mute Control for BST2 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst1_outmixl	MX4F [5]	1'b	Mute Control for BST1 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_inl_outmixl	MX4F [4]	1'b	Mute Control for INL to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_recmixl_outmixl	MX4F [3]	1'b	Mute Control for RECMIXL to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_dacl1_outmixl	MX4F [0]	1'b	Mute Control for DACL1 to OUTMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst2_outmixr	MX52 [6]	1'b	Mute Control for BST2 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_outmixr	MX52 [5]	1'b	Mute Control for BST1 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_inr_outmixr	MX52 [4]	1'b	Mute Control for INR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_recmixr_outmixr	MX52 [3]	1'b	Mute Control for RECMIXR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_dacr1_outmixr	MX52 [0]	1'b	Mute Control for DACR1 to OUTMIXR 0'b: Un-Mute

			1'b: Mute
Gain_bst2_outmixl	MX4D [12:10]	0'h	Gain Control for BST2 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_bst1_outmixl	MX4D [9:7]	0'h	Gain Control for BST1 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_inl_outmixl	MX4D [6:4]	0'h	Gain Control for INL to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_recmixl_outmixl	MX4D [3:1]	0'h	Gain Control for RECMIXL to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_dacl1_outmixl	MX4E [9:7]	0'h	Gain Control for DACL1 to OUTMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_bst2_outmixr	MX50 [12:10]	0'h	Gain Control for BST2 to OUTMIXR 000'b: 0dB

			001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_bst1_outmixr	MX50 [9:7]	0’h	Gain Control for BST1 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_inr_outmixr	MX50 [6:4]	0’h	Gain Control for INR to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_recmixr_outmixr	MX50 [3:1]	0’h	Gain Control for RECMIXR to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_dacr1_outmixr	MX51 [9:7]	0’h	Gain Control for DACR1 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved

3.2.3. HP Output Control

3.2.3.1. Power

The power management of Headphone out is shown as below:

Control Register	Reg	Value	Description	Note
en_out_hp	MX8E[4]	1'b	Enable Headphone output	
Pow_pump_hp	MX8E[3]	1'b	Power On Charge pump	
En_l_hp	MX63[7]	1'b	Power On Headphone Amplifier Left Channel	
En_r_hp	MX63[6]	1'b	Power On Headphone Amplifier Right Channel	
Pow_hpovoll	MX66[11]	1'b	Power On Left Headphone Output Volume	Depends On Path
Pow_hpovolr	MX66[10]	1'b	Power On Right Headphone Output Volume	Depends On Path
Pow_capless	MX8E[0]	1'b	HP Amp All Power On	

3.2.3.2. HP Volume

When HP output signal is from Out mixer, its volume can be controlled by HPOVOL L/R. It also has a mute/unmute before HPOVOL L/R.

Name	Bits	Default value	Function Description
Mu_hpovoll_in	MX02 [14]	1'h	Mute Control for Left Headphone Volume Channel(HPOVOLL) 0'b: Un-Mute 1'b: Mute
vol_hpol	MX02 [13:8]	8'h	Left Headphone Channel Volume Control (HPOVOLL) 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step
Mu_hpovolr_in	MX02 [6]	1'h	Mute Control for Right Headphone Volume Channel(HPOVOLR) 0'b: Un-Mute 1'b: Mute
vol_hpor	MX02 [5:0]	8'h	Right Headphone Channel Volume Control (HPOVOLR) 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

3.2.3.3. HP Out control

HP Output can select its source to HPOMIX, and the source can be selected from Out mixer or just direct form DAC1.

When using direct path from DAC1, the HPO Volume will be useless. HPOMIX also has gain control on it.

After selecting the source of input, HP Out also has a mute function which can be set by register. Customer can use it to mute the sound which output to HPO.

Name	Bits	Default value	Function Description
mu_dac1_hpomix	MX45 [14]	1'h	Mute Control for DAC1 to HPOMIX 0'b: Un-Mute 1'b: Mute
mu_hpovol_hpomix	MX45 [13]	1'h	Mute Control for HPOVOL to HPOMIX 0'b: Un-Mute 1'b: Mute
Gain_hpomix	MX45 [12]	0'h	Gain Control for HPOMIX 0'b: 0dB 1'b: -6dB

3.2.3.4. HP Out depop control

ALC5651 supports depop mode which can use to decrease pop noise.ALC5651 also has a DC calibration function to shorten the delay time of depop.

HP OUT initial DC calibration for De-pop				
Step	Procedure	Register	Set	Remark
1	Enable I2S clock	MX-FA[0]	1'b	
2	Enable depop function	MX-8F	3100'h	
3	Enable charge pump & HPO power	MX-8E	0009'h	
4	Enable DC calibration	PR-77	9F00'h	

HP OUT initial Power on + Un-mute De-pop				
Step	Procedure	Register	Set	Remark
1	Enable power on depop	MX-8F	1140'h	
2	Power On Vref & Main Bias	MX-63	A8F0'h	
3	Delay >80m Sec			
4	Disable fast Vref	MX-63	E8F8'h	
5	Select depop timing	MX-90	0636'h	
6	Enable HPO amp power	MX-8E	0005'h	
7	HPO Un-Mute	MX-02[15][7]	00'b	
8	Delay >100m Sec			

HP OUT Mute + Power off De-pop				
Step	Procedure	Register	Set	Remark
1	HPO Mute	MX-02[15][7]	11'b	
2	Delay >100m Sec			
3	Disable HPO amp power	MX-8E	0004'h	
4	Delay >50m Sec			
5	Power Off Vref & Main Bias	MX-63	0000'h	

3.2.4. LOUT Output Control

3.2.4.1. Power

The power management of LOUT out is shown as below:

Control Register	Reg	Value	Description	Note
Pow_lout	MX63[12]	1'b	Power On LOUT mixer	
Pow_pump_hp	MX8E[3]	1'b	Power On Charge pump	
Pow_outvoll	MX66[13]	1'b	Power On Left Output Volume	Depends On Path
Pow_outvolr	MX66[12]	1'b	Power On Right Output Volume	Depends On Path

3.2.4.2. LOUT Out Volume

When LOUT output signal is from Out mixer, its volume can be controlled by OUTVOL L/R. It also has a mute/unmute before OUTVOL L/R.

Name	Bits	Default value	Function Description
Mu_outvoll_in	MX03 [14]	1'h	Mute Control for Left Output Volume Channel (OUTVOLL) 0'b: Un-Mute 1'b: Mute
Vol_outl	MX03 [13:8]	08'h	Left Output Volume Control (OUTVOLL) 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step
Mu_outvolr_in	MX03 [6]	1'h	Mute Control for Right Output Volume Channel (OUTVOLR) 0'b: Un-Mute 1'b: Mute
Vol_outr	MX03 [5:0]	8'h	Right Output Volume Control 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

3.2.4.3.LOUT Out control

LOUT Output has a LOUT mixer which can select its source, and the source can be selected from Out mixer or just direct form DAC1.

When using direct path from DAC1, the OUT Volume will be useless. LOUT mixer also has gain control on it.

After selecting the source of input, LOUT also has a mute function which can be set by register. Customer can use it to mute the sound which output to LOUT.

Name	Bits	Default value	Function Description
Mu_dacl1_lout	MX53 [15]	1'h	Mute Control for DACL1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_dacr1_lout	MX53 [14]	1'h	Mute Control for DACR1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_outvoll_lout	MX53 [13]	1'h	Mute Control for OUTVOLL to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_outvolr_lout	MX53 [12]	1'h	Mute Control for OUTVOLR to LOUTMIX 0'b: Un-Mute 1'b: Mute
Gain_lout	MX53 [11]	0'h	Gain Control for LOUTMIX 0'b: 0dB 1'b: -6dB
Mu_lout_l	MX03 [15]	1'h	Mute Control for Left Line Output Port(LOUTL) 0'b: Un-Mute 1'b: Mute
Mu_lout_r	MX03 [7]	1'h	Mute Control for Right Line Output Port (LOUTR) 0'b: Un-Mute 1'b: Mute

LOUT Output also supports differential mode function which is set by register to invert the R channel to minus 180 degree.

Name	Bits	Default value	Function Description
En_ dfo	MX05 [15]	0'h	Enable Differential Line Output 0'b: Disable 1'b: Enable (LP / RN)

3.2.4.4. PDM Out control

ALC5651 support a PDM output which can be connected to the PDM type external SPK amplifier. User can choose the PDM data source and mute/unmute the PDM data by register setting. The PDM output also has a gain control -6dB for selection.

Name	Bits	Default value	Function Description
sel_pdm_l	MX30 [15]	0'h	Select PDM Left channel source 0'b: DD_MIXL 1'b: Stereo_DAC_MIXL
sel_pdm_r	MX30 [13]	0'h	Select PDM Right channel source 0'b: DD_MIXR 1'b: Stereo_DAC_MIXR
mu_pdm_l	MX30 [14]	1'h	Mute PDM Left channel data 0'b: UnMute 1'b: Mute
mu_pdm_r	MX30 [12]	1'h	Mute PDM Right channel data 0'b: UnMute 1'b: Mute
Gain_pdm_in	MX30 [4]	0'h	PDM Gain Selection 0'b: -6dB 1'b: 0dB

ALC5651 PDM interface support the command sending from PDM interface to control the external SPK amp.User can set the data in MX-32[7:0] and set MX-31[11] to 1 to transmit the command. When the commend is transmitting , MX-30[6] will show busy .

The PDM clock can also be set by setting the divider register as below:

Name	Bits	Default value	Function Description
Sel_pdm_pattern_ctrl	MX30 [5]	0'h	Select Into PDM Pattern Control Repeat Count Number 0'b: Repeat 64 times (For ALC9010) 1'b: Repeat 128times (For SSM2517 and TFA9881)
pdm_cmd_pattern	MX32 [7:0]	0'h	PDM Pattern Command
pdm_cmd_exe	MX31 [11]	0'h	Write "1" to Execute
Pdm_cmd_busy	MX30 [6]	0'h	Pattern Controller Busy Flag 0'b: Normal 1'b: Busy
Sel_pdm_div	MX30 [1:0]	0'h	System Clock to PDM Filter Divider 00'b: Div 1 01'b: Div 2 10'b: Div 3 11'b: Div 4

3.2.5. Digital Interface Format Setting

3.2.5.1. TDM Format Setting

The first Digital Interface of ALC5651 can support TDM(Time Division Multiplexing) mode which can transmit/receive up to 8 channels data. The TDM mode selection is controlled by the register .
Its data length and channel decision is also set by the register.

Name	Bits	Default value	Function Description
mode_sel	MX77 [14]	0'h	I2S / TDM Mode Control 0'b: Normal I2S Mode 1'b: TDM Mode
Tdmslot_sel	MX77 [13:12]	0'h	TDM Channel Number Select 00'b: 2ch 01'b: 4ch 10'b: 6ch 11'b: 8ch
channel_length	MX77 [11:10]	3'h	TDM Channel Length 00'b: 16bit (For Slave Mode and Master Mode) 01'b: 20bit (For Slave Mode) 10'b: 24bit (For Slave Mode) 11'b: 32bit (For Slave Mode and Master Mode)

When interface is under master mode, the LRCK clock format can also be set .The relative register is list as below:

Name	Bits	Default value	Function Description
sel_i2s_lrck_polarity	MX78 [15]	0'h	LRCK Polarity Inverter 0'b: Normal 1'b: Invert
lrck_pulse_sel	MX78 [11]	0'h	LRCK Pulse Width Select (Master Mode Only) 0'b: One BCLK width 1'b: One channel slot width

3.2.5.2. I2S/PCM Format Setting

Two Digital Interface of ALC5651 can be configured as Master mode or Slave mode, and three different audio data formats are supported: I2S, Left Justify and PCM. In addition, PCM interface can support mode-A and mode-B. Each kind of audio data format supports different data length, and polarity of LRCK and BCLK can be inverted depends on audio data format.

ALC5651 also support A law, u law format, and customer can also set these two format by register control.

Name	Bits	Default value	Function Description
Sel_i2s1_ms	MX70 [15]	1'h	I2S1 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode
en_i2s1_out_comp	MX70 [11:10]	0'h	I2S1 Output Data Compress (For ADCDAT1 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s1_in_comp	MX70 [9:8]	0'h	I2S1 Input Data Compress (For DACDAT1 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
Inv_i2s1_bclk	MX70 [7]	0'h	I2S1 BCLK Polarity Control 0'b: Normal 1'b: Invert
sel_i2s1_len	MX70 [3:2]	0'h	I2S1 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
sel_i2s1_format	MX70 [1:0]	0'h	I2S1 PCM Data Format Selection 00'b: I2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

Name	Bits	Default value	Function Description
sel_i2s2_ms	MX71 [15]	1'h	I2S2 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode
en_i2s2_out_comp	MX71 [11:10]	0'h	I2S2 Output Data Compress (For ADCDAT2 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s2_in_comp	MX71 [9:8]	0'h	I2S2 Input Data Compress (For DACDAT2 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
inv_i2s2_bclk	MX71 [7]	0'h	I2S2 BCLK Polarity Control 0'b: Normal 1'b: Invert
sel_i2s2_len	MX71 [3:2]	0'h	I2S2 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
sel_i2s2_format	MX71 [1:0]	0'h	I2S2 PCM Data Format Selection 00'b: I2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

3.2.5.3. Stereo DAC Sample Rate Relative Setting

The sample rate Relative setting of DAC1 can be set in the register shown below:

Name	Bits	Default value	Function Description
sel_i2s_pre_div1	MX73 [14:12]	1'h	I2S Clock Pre-Divider 1 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
sel_dac_osr	MX73 [3:2]	0'h	Stereo DAC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 128Fs/3
sel_adc_osr	MX73 [1:0]	0'h	Stereo ADC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 128Fs/3
sel_i2s_pre_div2	MX73 [10:8]	1'h	I2S Pre-Divider 2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
sel_i2s_bclk_ms2	MX73 [11]	0'h	I2S2 Master Mode Clock Relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)

In I2S/PCM mode, sample rate is setting by **sel_i2s_pre_div1** & **sel_i2s_pre_div2**. About the register setting, please refer to the table in page31~32.

Master Mode:

Clock source		I2S1 Clock		MX73	MX70 [15]	MX80 [15:14]
MCLK	PLL	LRCLK	BCLK			
24576000 (3072Fs)	X	Fs=8000	64Fs	6110	0'b	00'b
24576000 (1536Fs)	X	Fs=16000	64Fs	4110	0'b	00'b
24576000 (1024Fs)	X	Fs=24000	64Fs	3110	0'b	00'b
24576000 (768Fs)	X	Fs=32000	64Fs	2110	0'b	00'b
24576000 (512Fs)	X	Fs=48000	64Fs	1110	0'b	00'b
22579200 (2048Fs)	X	Fs=11025	64Fs	5110	0'b	00'b
22579200 (1024Fs)	X	Fs=22050	64Fs	3110	0'b	00'b
22579200 (512Fs)	X	Fs=44100	64Fs	1110	0'b	00'b
●	24576000 (3072Fs)	Fs=8000	64Fs	6110	0'b	01'b
●	24576000 (1536Fs)	Fs=16000	64Fs	4110	0'b	01'b
●	24576000 (1024Fs)	Fs=24000	64Fs	3110	0'b	01'b
●	24576000 (768Fs)	Fs=32000	64Fs	2110	0'b	01'b
●	24576000 (512Fs)	Fs=48000	64Fs	1110	0'b	01'b
●	22579200 (2048Fs)	Fs=11025	64Fs	5110	0'b	01'b
●	22579200 (1024Fs)	Fs=22050	64Fs	3110	0'b	01'b
●	22579200 (512Fs)	Fs=44100	64Fs	1110	0'b	01'b

Slave Mode:

Clock source		I2S1 Clock		MX73	MX70 [15]	MX80 [15:14]
MCLK	PLL	LRCLK	BCLK			
2048000 (256Fs)	X	Fs=8000	X	0110	1'b	00'b
4096000 (256Fs)	X	Fs=16000	X	0110	1'b	00'b
6144000 (256Fs)	X	Fs=24000	X	0110	1'b	00'b
8192000 (256Fs)	X	Fs=32000	X	0110	1'b	00'b
12288000 (256Fs)	X	Fs=48000	X	0110	1'b	00'b
2822400 (256Fs)	X	Fs=11025	X	0110	1'b	00'b
5644800 (256Fs)	X	Fs=22050	X	0110	1'b	00'b
11289600 (256Fs)	X	Fs=44100	X	0110	1'b	00'b
4096000 (512Fs)	X	Fs=8000	X	1110	1'b	00'b
8192000 (512Fs)	X	Fs=16000	X	1110	1'b	00'b
6144000 (512Fs)	X	Fs=24000	X	1110	1'b	00'b
16384000 (512Fs)	X	Fs=32000	X	1110	1'b	00'b
24576000 (512Fs)	X	Fs=48000	X	1110	1'b	00'b
5644800 (512Fs)	X	Fs=11025	X	1110	1'b	00'b
11289600 (512Fs)	X	Fs=22050	X	1110	1'b	00'b
22579200 (512Fs)	X	Fs=44100	X	1110	1'b	00'b

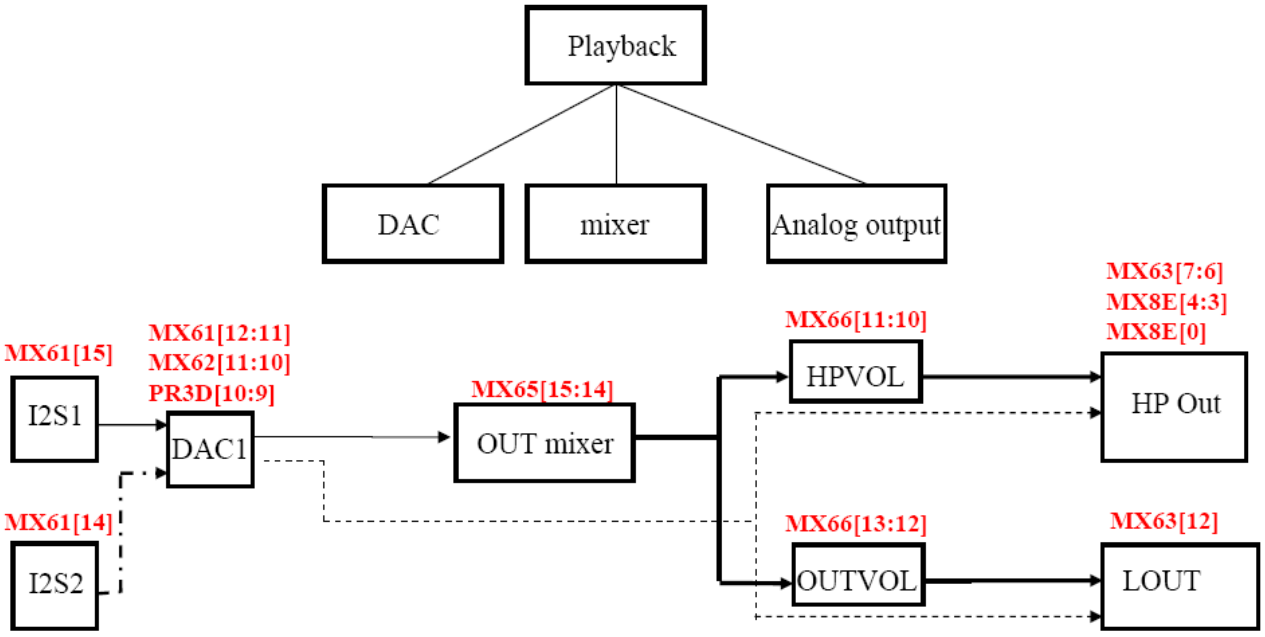
X **:** Don't care

●**:** MCLK does't use 24576000Hz clock , and using PLL changing clock to 24576000Hz .

Note : PLL output as System Clock only support Master Mode.

3.3. Power block of playback

The picture as below is the power block diagram of playback, the relative power register is marked red in this picture. It is easy for customer to setting the power register by checking this picture.



Note:MX63[11], MX63[15], MX63[4], MX63[13] should enable first

3.4. Playback setting example

For example1: The playback path is I2S1➔DAC1➔OUT mixer➔HPOL/R out

Step1: At first, we should enable the analog power for codec**.** The setting is as below:

a. Set MX63[11] to 1'b
b. Set MX63[15] to 1'b
c. Set MX63[4] to 1'b
d. Set MX63[13] to 1'b

Step2:Then refer to the power block of playback, the relative power as below need to be power on

a. MX61[15]
b. PR3D[10:9]
c. MX61[12:11]
d. MX62[11:10]
e. MX65[15:14]
f. MX66[11:10]
g. MX63[7:6]
h. MX8E[4:3]
i. MX8E[0]

Step3:Refer to the audio mixer path in ALC5651 datasheet to enable the path register

Step4:Finally , the setting register will be as below

Register	Value
MXFA	0011
MX63	E8D8
MX61	9800
MX62	0800
MX65	C000
MX66	0C00
PR3D	2E00
MX8E	0019
MX8F	3100
MX2A	1212
MX4F	0278
MX52	0278
MX45	4000
MX02	0808

For example2: The playback path is I2S1➔DAC1➔ HPOL/R out

Step1: At first, we should enable the analog power for codec**.** The setting is as below:

a. Set MX63[11] to 1'b
b. Set MX63[15] to 1'b
c. Set MX63[4] to 1'b
d. Set MX63[13] to 1'b

Step2:Then refer to the power block of playback, the relative power as below need to be power on

a. MX61[15]
b. PR3D[10:9]
c. MX61[12:11]
d. MX62[11:10]
e. MX63[7:6]
f. MX8E[4:3]
g. MX8E[0]

Step3:Refer to the audio mixer path in ALC5651 datasheet to enable the path register

Step4:Finally , the setting register will be as below

Register	Value
MXFA	0011
MX63	E8D8
MX61	9800
MX62	0800
PR3D	2E00
MX8E	0019
MX8F	3100
MX45	2000
MX02	4848

4. Record

4.1. Power

The Register shown as below has to be set in order to enable ADC.

Control Register	Reg	Value	Description	Note
Pow_bg_bias	MX63[11]	1'b	Power On MBIAS Bandgap	
Pow_vref1	MX63[15]	1'b	Power On Vref1	
Pow_main_bias	MX63[13]	1'b	Power On Main Bias	
Pow_vref2	MX63[4]	1'b	Power On Vref2	
Pow_adc_l	MX61[2]	1'b	Power On left ADC	
Pow_adc_r	MX61[1]	1'b	Power On right ADC	
Pow_adc_stereo1_filter	MX62[15]	1'b	Power on stereo1 ADC digital filter	Depends on path
Pow_adc_stereo2_filter	MX62[14]	1'b	Power on stereo2 ADC digital filter	Depends on path
En_i2s1	MX61[15]	1'b	Enable I2S1 Digital interface	Depends on path
En_i2s2	MX61[14]	1'b	Enable I2S2 Digital interface	Depends on path
digital_gate_ctrl	MXFA[0]	1'b	Enable MCLK input	
en_ckgen_adc	PR3D[12]	1'b	Enable ADC clock input	

4.2. Mixer Control

4.2.1. Power

The power of each mixer can be individually power down in order to save power consumption. The following power management register should be enabled according to Record path.

Control Register	Reg	Value	Description	Note
Pow_recmixl	MX65[11]	1'b	Power On left REC mixer	
Pow_recmixr	MX65[10]	1'b	Power On right REC mixer	

4.2.2. REC Mixer Control

REC mixer is used to select the record source of ADC. There are two channels REC mixer which can be configured separately by **MX3C** & **MX3E**. Each input source of REC mixer also has each gain control.

Name	Bits	Default value	Function Description
Mu_inl_rexmixl	MX3C [5]	1'h	Mute Control for INL to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst3_recmixl	MX3C [3]	1'h	Mute Control for BST3 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixl	MX3C [2]	1'h	Mute Control for BST2 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixl	MX3C [1]	1'h	Mute Control for BST1 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_outmixl_recmixl	MX3C [0]	1'h	Mute Control for OUTMIXL to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_inr_rexmixr	MX3E [5]	1'h	Mute Control for INR to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst3_recmixr	MX3E [3]	1'h	Mute Control for BST3 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixr	MX3E [2]	1'h	Mute Control for BST2 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixr	MX3E [1]	1'h	Mute Control for BST1 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_outmixr_recmixr	MX3E [0]	1'h	Mute Control for OUTMIXR to RECMIXR 0'b: Un-Mute 1'b: Mute
Gain_inl_recmixl	MX3B [12:10]	0'h	Gain Control for INL to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved

Gain_bst3_ recmixl	MX3B [6:4]	0'h	Gain Control for BST3 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_bst2_ recmixl	MX3B [3:1]	0'h	Gain Control for BST2 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_bst1_ recmixl	MX3C [15:13]	0'h	Gain Control for BST1 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_outm ixl_recmix l	MX3C [12:10]	0'h	Gain Control for OUTMIXL to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_inr_r ecmixr	MX3D [12:10]	0'h	Gain Control for INR to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_bst3_ recmixr	MX3D [6:4]	0'h	Gain Control for BST3 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB

			011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved
Gain_bst2_recmixr	MX3D [3:1]	0’h	Gain Control for BST2 to RECMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved
Gain_bst1_recmixr	MX3E [15:13]	0’h	Gain Control for BST1 to RECMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved
Gain_outmixr_recmixr	MX3E [12:10]	0’h	Gain Control for OUTMIXR to RECMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved

4.3. Input Control

4.3.1. Stereo Input Control

4.3.1.1 Power

The analog IN2 can be a stereo single end input (linein function) .The power management of stereo input is shown as below, each channel can be enable/disable individually.

Control Register	Reg	Value	Description	Note
Pow_inlvol	MX66[9]	1'b	Power On INL Input Volume	Depends on Application
Pow_inrvol	MX66[8]	1'b	Power On INR Input Volume	Depends on Application

4.3.1.2 Stereo Input Volume Control

The volume gain of different channel of stereo input can be adjusted individually by following register.

Name	Bits	Default value	Function Description
Vol_inl	MX0F [12:8]	8'h	INL Channel Volume Control 00'h: +12dB … 08'h: 0dB … 1F'h: -34.5dB, with 1.5dB/step
Vol_inr	MX0F [4:0]	8'h	INR Channel Volume Control 00'h: +12dB … 08'h: 0dB … 1F'h: -34.5dB, with 1.5dB/step

4.3.2. IN1/2/3(MIC) In Control

4.3.2.1 Power

ALC5651 can be configured as one differential microphone or three single end microphone. The power management of Microphone can be disable/enable individually and shown as below.

Control Register	Reg	Value	Description	Note
Pow_bst1	MX64[15]	1'b	Power On MIC BST1 Boost Gain	Depends on Application
Pow_bst2	MX64[14]	1'b	Power On MIC BST2 Boost Gain	Depends on Application
Pow_bst3	MX64[13]	1'b	Power On MIC BST3 Boost Gain	Depends on Application
Pow_bst2_op2	MX64[4]	1'b	Power On MIC BST2 Single End Mode	Depends on Application
pow_micbias1	MX64[11]	1'b	Power On MICBIAS1	Depends on Application

4.3.2.2 IN1/2_In Boost Control

ALC5651 IN2_In can be configured as Differential mode or Single Ended mode. The boost gain of BST1 & BST2 &BST3 can be adjusted individually by following register.

Name	Bits	Default value	Function Description
En_in2_df	MX0E [6]	0'h	IN2 Input Mode Control 0'b: Single Ended Mode 1'b: Differential Mode
Sel_bst1	MX0D [15:12]	0'h	IN1 Boost Control (BST1) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
Sel_bst2	MX0D [11:8]	0'h	IN2 Boost Control (BST2) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved

Sel_bst3	MX0E [15:12]	0'h	IN3 Boost Control (BST3) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved

4.3.2.3 MICBIAS function

ALC5651 provide two kind of MICBIAS voltage for user selection. User can choose 0.9*MICVDD or 0.75*MICVDD for different microphone sensitivity.

ALC5651 also provides short current detect for each microphone bias which is configured by **Pow_mic1_ovcd .** Different short current threshold is set by register setting, and the short current status is shown on MXBE [3].User can use sticky function to hold the short current status when short current happens.

Name	Bits	Default value	Function Description
Sel_micbias1	MX93 [15]	0'h	MICBIAS1 Output Voltage Control 0'b: 0.9 * MICVDD 1'b: 0.75 * MICVDD
Pow_mic1_ovcd	MX93 [11]	0'h	MICBIAS1 Short Current Detector Control 0'b: Disable 1'b: Enable
Mic1_ovcd_th_sel	MX93 [10:9]	0'h	MICBIAS1 Short Current Detector Threshold 00'b: 600uA 01'b: 1500uA 1x'b: 2000uA Note: tolerance is 200uA
en_micbias1_ovcd_sticky	MXBE [11]	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable
inv_micbias1_ovcd	MXBE [7]	0'h	MICBIAS1 over current status polarity 0'b: Normal 1'b: Output Invert
Ovc_micbias1	MXBE [3]	0'h	MICBIAS1 Over Current Status Read: return status of each status pin Write: Write '0' to clear stick bit

4.4. ADC Control

4.4.1. TDM ADC Relative Setting

The TDM relative setting of ADC is similar as DAC TDM setting, and user can refer to chapter 3.2.5.1.

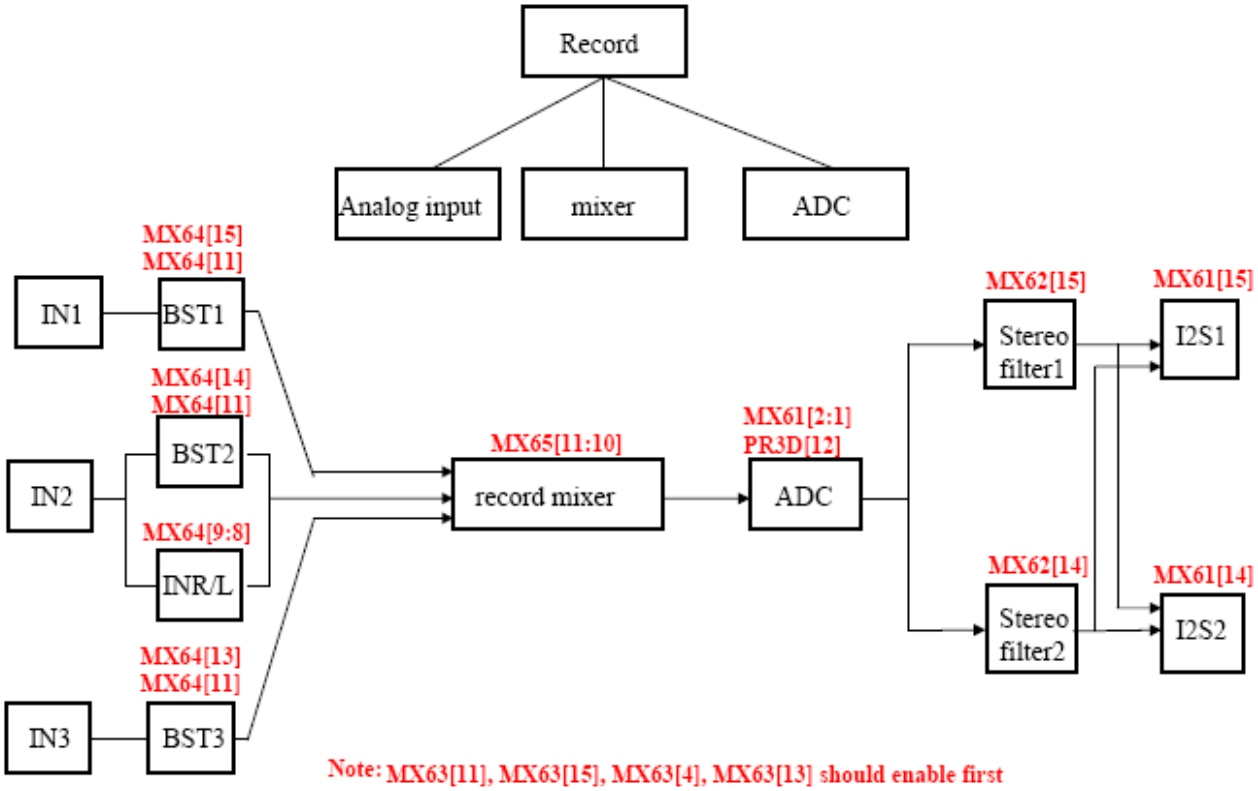
4.4.2. Stereo ADC Format & Sample Rate Relative Setting

The sample rate relative setting of ADC is same as DAC sample rate setting, and user can also refer to the sample rate register setting table in chapter 3.2.5.2 ~ 3.2.5.3.

4.5. Power block of record

The picture as below are the power block diagram of record, the relative power register is marked red in these pictures. It is easy for customer to setting the power register by checking these pictures.

Record path



4.6. Record setting example

Example1: Record path is IN2(differential 40dB) ➔ADC Record mixer➔ ADC ➔ I2S1

Step1: At first, we should enable the analog power for codec **.** The setting is as below:

a. Set MX63[11] to 1'b
b. Set MX63[15] to 1'b
c. Set MX63[4] to 1'b
d. Set MX63[13] to 1'b

Step2:Then refer to the power block of Record path 1, the relative power as below need to be power on

a. MX64[14][11]
b. MX65[11:10]
c. MX61[2:1]
d. PR3D[12]
e. MX62[15]
f. MX61[15]

Step3:Refer to the audio mixer path in ALC5651 datasheet to enable the path register

Step4:Finally , the setting register will be as below

Register	Value
PR3D	3800
MXFA	0011
MX63	E818
MX64	4800
MX65	0C00
MX61	8006
MX62	8000
MX0D	0540
MX3C	006B
MX3E	006B

5. Digital Mixer

ALC5651 supports several digital mixers. The digital mixer can mix the data which comes from different digital interface. Customer can refer to the digital mixer path to implement many kinds of complicate application path.

5.1. Digital Audio Interface

ALC5651 has two digital audio interfaces Digital audio interface-1(IF1) and Digital audio interface-2(IF2). IF1 support TDM multi-channel data, and it is mainly used for main input signal from CPU. IF1 also can pass the data to the Realtek audio sound effect block diagram. IF2 is mainly for other voice signal like BT module or 3G module.

5.1.1. Digital to DAC

The digital interface1 of ALC5651 can support TDM format , so user can set the register to choose the data should pass from which slot. There are two digital palyback path IF1_DAC1 & IF1_DAC2 which can be used by the user in codec.

Name	Bits	Default value	Function Description
sel_i2s_tx_l_ch2	MX79 [14:12]	0'h	IF1_DAC1_L Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
sel_i2s_tx_r_ch2	MX79 [10:8]	1'h	IF1_DAC1_R Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
sel_i2s_tx_l_ch4	MX79 [6:4]	2'h	IF1_DAC2_L Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7
sel_i2s_tx_r_ch4	MX79 [6:4]	2'h	IF1_DAC2_R Data Selection 000'b: Slot0 001'b: Slot1 010'b: Slot2 011'b: Slot3 100'b: Slot4 101'b: Slot5 110'b: Slot6 111'b: Slot7

When digital data comes from digital interface1 (IF1_DAC1), the data will pass to a mixer which is before audio sound effect block. And there is a mute/unmute control and digital volume control before that mixer.

Name	Bits	Default value	Function Description
mu_ dac_l	MX29 [14]	0'h	Mute Control for I2S-1 to DAC Left Channel 0'b: Un-Mute 1'b: Mute
mu_ dac_r	MX29 [6]	0'h	Mute Control for I2S-1 to DAC Right Channel 0'b: Un-Mute 1'b: Mute
vol_dac1_l	MX19 [15:8]	AF'h	DAC1 Left Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac1_r	MX19 [7:0]	AF'h	DAC1 Right Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

The data of DAC2(second DAC path) can select the data pass from digital interface1 or digital interface2 by **Sel_dacl2** & **Sel_dacr2**. After that , there is also a volume control and mute function which can be set by register.

Name	Bits	Default value	Function Description
Sel_dacl2	MX1B [11]	1'h	Select IF1 or IF2 Data to DACL2 0'b: IF1_DAC_L 1'b: IF2_DAC_L
Sel_dacr2	MX1B [10]	1'h	Select IF1 or IF2 Data to DACL2 0'b: IF1_DAC_L 1'b: IF2_DAC_L
vol_dac2_l	MX1A [15:8]	AF'h	DAC2 Left Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac2_r	MX1A [7:0]	AF'h	DAC2 Right Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

Mu_dac2_l	MX1B [13]	0'h	Mute Control for Left DAC2 Volume 0'b: Un-Mute 1'b: Mute
Mu_dac2_r	MX1B [12]	0'h	Mute Control for Right DAC2 Volume 0'b: Un-Mute 1'b: Mute

ALC5651 DACL1 & DACR1 has each mixer which can mix the signal from IF1 & IF2. Each input of the mixer also has a gain control which can attenuate -6dB at the input signal.

Name	Bits	Default value	Function Description
mu_stereo_dacl1_mixl	MX2A [14]	1'h	Mute Control for DACL1 to Stereo DAC Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dacl2_mixl	MX2A [12]	1'h	Mute Control for DACL2 to Stereo DAC Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dacr1_mixl	MX2A [9]	1'h	Mute Control for DACR1 to Stereo DAC Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dacr1_mixl	MX2A [6]	1'h	Mute Control for DACR1 to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dacr2_mixl	MX2A [4]	1'h	Mute Control for DACR2 to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dacl1_mixl	MX2A [1]	1'h	Mute Control for DACL1 to Stereo DAC Right Mixer 0'b: Un-Mute 1'b: Mute
gain_dacl1_to_stereo_l	MX2A [13]	0'h	Gain Control for DACL1 to Stereo DAC Left Mixer 0'b: 0dB 1'b: -6dB

gain_dacl2_to_stereo_l	MX2A [11]	0'h	Gain Control for DACL2 to Stereo DAC Left Mixer 0'b: 0dB 1'b: -6dB
gain_dacr1_to_stereo_l	MX2A [8]	0'h	Gain Control for DACR1 to Stereo DAC Left Mixer 0'b: 0dB 1'b: -6dB
gain_dacr1_to_stereo_r	MX2A [5]	0'h	Gain Control for DACR1 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB
gain_dacr2_to_stereo_r	MX2A [3]	0'h	Gain Control for DACR2 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB
gain_dacl1_to_stereo_r	MX2A [0]	0'h	Gain Control for DACL1 to Stereo DAC Right Mixer 0'b: 0dB 1'b: -6dB

ALC5651 also has DD_MIXL & DD_MIXR mixer which can mix the signal from IF1 & IF2 and transmit the data to ADC1/2 or PDM interface. Each input of the mixer also has a gain control which can attenuate -6dB at the input signal.

Name	Bits	Default value	Function Description
mu_stereo_dd_l1	MX2B [14]	1'h	Mute Control for DACL1 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dd_l2	MX2B [12]	1'h	Mute Control for DACL2 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dd_r2_l	MX2B [10]	1'h	Mute Control for DACR2 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dd_r1	MX2B [6]	1'h	Mute Control for DACR1 to DD Right Mixer 0'b: Un-Mute 1'b: Mute
mu_stereo_dd_r2	MX2B [4]	1'h	Mute Control for DACR2 to DD Right Mixer 0'b: Un-Mute 1'b: Mute

mu_stereo_dd_l2_r	MX2B [2]	1'h	Mute Control for DACL2 to DD Right Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_l1	MX2B [13]	0'h	Gain Control for DACL1 to DD Left Mixer 0'b: 0dB 1'b: -6dB
gain_stereo_dd_l2	MX2B [11]	0'h	Gain Control for DACL2 to DD Left Mixer 0'b: 0dB 1'b: -6dB
gain_stereo_dd_r2_l	MX2B [9]	0'h	Gain Control for DACR2 to DD Left Mixer 0'b: 0dB 1'b: -6dB
gain_stereo_dd_r1	MX2B [5]	0'h	Gain Control for DACR1 to DD Right Mixer 0'b: 0dB 1'b: -6dB
gain_stereo_dd_r2	MX2B [3]	0'h	Gain Control for DACR2 to DD Right Mixer 0'b: 0dB 1'b: -6dB
gain_stereo_dd_l2_r	MX2B [1]	0'h	Gain Control for DACL2 to DD Right Mixer 0'b: 0dB 1'b: -6dB

5.1.2. ADC to digital

The ADC path has two stereo mixer Stereo1_ADC_mixer_L/R & Stereo2_ADC_mixer_L/R. And each mixer can mix the DMIC1/2, DD_MIX or ADC signal which is selected by multiplexer. Between the mixer and multiplexer, it also has a mute function which can disconnect the signal.

Name	Bits	Default value	Function Description
sel_stereo1 _adc1	MX27 [12]	1'h	Select Control for Stereo1 ADC1 Source 0'b: DD_MIXL/ DD_MIXR 1'b: ADCL/ADCR
sel_stereo1 _adc2	MX27 [11]	1'h	Select Control for Stereo1 ADC2 Source 0'b: DMIC_L/ DMIC_R 1'b: DD_MIXL/ DD_MIXR
mu_stereo1 _adcl1	MX27 [14]	1'h	Mute Control for Stereo1 ADC1 Left Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1 _adcl2	MX27 [13]	1'h	Mute Control for Stereo1 ADC2 Left Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1 _adcr1	MX27 [6]	1'h	Mute Control for Stereo1 ADC1 Right Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1 _adcr2	MX27 [5]	1'h	Mute Control for Stereo1 ADC2 Right Channel 0'b: Un-Mute 1'b: Mute

Name	Bits	Default value	Function Description
sel_stereo2 _adcl1	MX28 [12]	1'h	Select Control for Stereo2 ADC1 Left Channel Source 0'b: DD_MIXL 1'b: ADCL
sel_stereo2 _adcl2	MX28 [11]	0'h	Select Control for Stereo2 ADC2 Left Channel Source 0'b: DMIC_L 1'b: DD_MIXL
sel_stereo2 _adcr1	MX28 [4]	1'h	Select Control for Stereo2 ADC1 Right Channel Source 0'b: DD_MIXR 1'b: ADCR
sel_stereo2 _adcr2	MX28 [3]	0'h	Select Control for Stereo2 ADC2 Right Channel Source 0'b: DMIC_R 1'b: DD_MIXR
mu_stereo2	MX28	1'h	Mute Control for Stereo2 ADC1 Left Channel

_adcl1	[14]		0’b: Un-Mute 1’b: Mute
mu_stereo2_adcl2	MX28 [13]	1’h	Mute Control for Stereo2 ADC2 Left Channel 0’b: Un-Mute 1’b: Mute
mu_stereo2_adcr1	MX28 [6]	1’h	Mute Control for Stereo2 ADC1 Right Channel 0’b: Un-Mute 1’b: Mute
mu_stereo2_adcr2	MX28 [5]	1’h	Mute Control for Stereo2 ADC2 Right Channel 0’b: Un-Mute 1’b: Mute

After the signal mix in Stereo1_ADC_L/R mixer, there is a gain and a volume control which can be set before the signal pass through EQ or AGC functions. At the last, the signal can pass to IF1_ADC1 interface or the mixer in DAC path.

Name	Bits	Default value	Function Description
Ad_boost_gain_l	MX1E [15:14]	0’h	ADC Left Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Ad_boost_gain_r	MX1E [13:12]	0’h	ADC Right Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Vol_adc1_l	MX1C [14:8]	2F’h	Stereo1 ADC Left Channel Volume Control 00’h: -17.625dB …

			2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Vol_adc1_r	MX1C [6:0]	2F'h	Stereo1 ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc_vol_l	MX1C [15]	0'h	Mute Control for Stereo1 ADC Left Volume Channel 0'b: Un-Mute 1'b: Mute
Mu_adc_vol_r	MX1C [7]	0'h	Mute Control for Stereo1 ADC Right Volume Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1_adc_mixer_l	MX29 [15]	1'h	Mute Control for Stereo1 ADC Left Channel to DAC 0'b: Un-Mute 1'b: Mute
mu_stereo1_adc_mixer_r	MX29 [15]	1'h	Mute Control for Stereo1 ADC Right Channel to DAC 0'b: Un-Mute 1'b: Mute

After the signal mix in Stereo2_ADC_L/R mixer, there is a volume and mute control which can be set before the signal pass to IF2_ADC interface.

Name	Bits	Default value	Function Description
Vol_adc2_l	MX1D [14:8]	2F'h	Stereo2 ADC Left Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Vol_adc2_r	MX1D [6:0]	2F'h	Stereo2 ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

Mu_adc2_vol_l	MX1D [15]	0'h	Digital Mute For Stereo2 ADC Left Channel Digital Mixer 0'b: Un-Mute 1'b: Mute
Mu_adc2_vol_r	MX1D [7]	0'h	Digital Mute For Stereo2 ADC Right Channel Digital Mixer 0'b: Un-Mute 1'b: Mute

Due to the digital interface1 support TDM mode, the data of IF_ADC1 and IF_ADC2 can select the slot(channel) to transmit when ender TDM mode by the register setting.

Name	Bits	Default value	Function Description
rx_adc_start	MX77 [8]	0'h	ADC1/2 to ADCDAT Data Start Location 0'b: slot0 start 1'b: slot4 start
rx_adc_data_sel	MX77 [9]	0'h	ADC1/2 to ADCDAT Data Location 0'b: normal(adc1→slot0/1) If rx_adc_start=0'b =>Slot0/1/2/3 is ADC1_L/ADC1_R/ADC2_L/ADC2_R If rx_adc_start=1'b =>Slot4/5/6/7 is ADC1_L/ADC1_R/ADC2_L/ADC2_R 1'b: adc data swap(adc2→slot0/1) If rx_adc_start=0'b =>Slot0/1/2/3 is ADC2_L/ADC2_R/ADC1_L/ADC1_R

			If rx_adc_start=1'b =>Slot4/5/6/7 is ADC2_L/ADC2_R/ADC1_L/ADC1_R
sel_i2s_rx_ch2	MX77 [7:6]	0'h	Data Swap for Slot0/1 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_ch4	MX77 [5:4]	0'h	Data Swap for Slot2/3 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_ch6	MX77 [3:2]	0'h	Data Swap for Slot4/5 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R
sel_i2s_rx_ch8	MX77 [1:0]	0'h	Data Swap for Slot6/7 in ADCDAT1 00'b: L/R 01'b: R/L 10'b: L/L 11'b: R/R

6. DMIC

6.1. Initial

ALC5651 supports digital microphone interface. When customer wants to use DMIC function, the register should be set as below:

Control Register	Reg	Value	Description	Note
sel_gpio2_type	MXC0[14]	1'b	Enable DMIC clock output	
en_dmic1	MX75[15]	1'b	Enable DMIC1 interface	

6.2. DMIC Clock setting

The clock frequency which provide from codec to DMIC is better to offer from 1MHz to 3MHz. Due to different sample

rate, the register setting shown as below should set to meet the range of clock frequency.

Name	Bits	Default value	Function Description
sel_dmic_clk	MX75 [7:5]	0'h	DMIC Clock Rate Control 000'b: 256*fs/2 001'b: 256*fs/3 010'b: 256*fs/4 011'b: 256*fs/6 100'b: 256*fs/8 101'b: 256*fs/12 Others: Reserved

6.2.1. DMIC clock setting example

Example 1 :

When recording sample rate(Fs) is 48k Hz , the clock should be set to 256*fs/8. So , the DMIC clock will be

256 * fs/8 = 32 * 48kHz = 1.536 MHz

Example 2 :

When recording sample rate(Fs) is 8k Hz , the clock should be set to 256*fs/2. So , the DMIC clock will be

256 * fs/2 = 128 * 8kHz = 1.024 MHz

6.3. DMIC other relative setting

ALC5651 DMIC1 data are pin share with different pins which are ADCDAT2(pin26) , IN1P(pin4 default) and PDM_SCL(pin25).For mapping to different pins , the DMIC data source need to be set by register. And the DMIC1 can also select the falling edge or rising edge data for left channel or right channel .

Name	Bits	Default value	Function Description
Dmic1_data_pin_share	MX75 [11:10]	1'h	DMIC1 Data Pin Share Selection 00'b: ADCDAT2 01'b: IN1P 10'b: PDM_SCL 11'b: Reserved
sel_dmic1_l_edge	MX75 [13]	0'h	DMIC1 Left Channel Source Control 0'b: Latch from falling edge 1'b: Latch from rising edge
sel_dmic1_r_edge	MX75 [12]	1'h	DMIC1 Right Channel Source Control 0'b: Latch from falling edge 1'b: Latch from rising edge

7. ASRC

ALC5651 support ASRC(Asynchronous Sample Rate Converter) function under I2S slave mode. Normally, the MCLK and BCLK clock should be synchronous(MCLK should be 8 or 16 times of BCLK).The ASRC allows the clock sources from MCLK and BCLK1 (or BCLK2) to be asynchronous.

7.1. Path setting

When using different path, the different setting should be implement .The relative setting is as below:

1. I2S1➔DAC1

The register as below should be enable, and the register setting will be MX-83 : 8000'h , MX-84 : A000'h

Name	Bits	Default value	Function Description
sel_if1_asrc	MX83 [15]	0'h	Mode Select Control for I2S1 0'b : Normal Mode 1'b : ASRC Mode

en_if1_asrc	MX84 [15]	0'h	Enable Control for I2S1 0'b: Normal Mode 1'b: ASRC Mode
sel_stereo1 _dac_mode	MX84 [13]	0'h	Select Control for Stereo1 DAC Filter 0'b: Normal Mode 1'b: ASRC Mode

2. I2S2➔DAC2

The register as below should be enable, and the register setting will be MX-83 : 1000'h , MX-84 : 5000'h

Name	Bits	Default value	Function Description
sel_if2_asrc	MX83 [12]	0'h	Mode Select Control for I2S2 0'b : Normal Mode 1'b : ASRC Mode
en_if2_asrc	MX84 [14]	0'h	Enable Control for I2S2 0'b: Normal Mode 1'b: ASRC Mode
sel_stereo2 _dac_mode	MX84 [12]	0'h	Select Control for Stereo2 DAC Filter 0'b: Normal Mode 1'b: ASRC Mode

3. Analog In➔Stereo1 ADC➔I2S1

The register as below should be enable, and the register setting will be MX-83 : 8000'h , MX-84 : 8800'h

Name	Bits	Default value	Function Description
sel_if1_asrc	MX83 [15]	0'h	Mode Select Control for I2S1 0'b : Normal Mode 1'b : ASRC Mode
en_if1_asrc	MX84 [15]	0'h	Enable Control for I2S1 0'b: Normal Mode 1'b: ASRC Mode
sel_adc_mo de	MX84 [11]	0'h	Select Control for ADC Stereo Filter 0'b: Normal Mode 1'b: ASRC Mode

4. Analog In➔ Stereo2 ADC➔I2S2

The register as below should be enable, and the register setting will be MX-83 : 1000'h , MX-84 : 4800'h

Name	Bits	Default value	Function Description

sel_if2_asrc	MX83 [12]	0'h	Mode Select Control for I2S2 0'b : Normal Mode 1'b : ASRC Mode
en_if2_asrc	MX84 [14]	0'h	Enable Control for I2S2 0'b: Normal Mode 1'b: ASRC Mode
sel_adc_mode	MX84 [11]	0'h	Select Control for ADC Stereo Filter 0'b: Normal Mode 1'b: ASRC Mode

5. DMIC1 In➔Stereo1 ADC➔I2S1

The register as below should be enable, and the register setting will be MX-83 : 8200'h ,MX-84 : 8000'h

Name	Bits	Default value	Function Description
sel_if1_asrc	MX83 [15]	0'h	Mode Select Control for I2S1 0'b : Normal Mode 1'b : ASRC Mode
en_if1_asrc	MX84 [15]	0'h	Enable Control for I2S1 0'b: Normal Mode 1'b: ASRC Mode
sel_dmic1_mode	MX83 [9]	0'h	Select Control for ASRC Mode in DMIC1 Function 0'b : Normal Mode 1'b : ASRC Mode

6. DMIC1 In➔ Stereo2 ADC➔I2S2

The register as below should be enable, and the register setting will be MX-83 : 4200'h ,MX-84 : 8000'h

Name	Bits	Default value	Function Description
sel_if2_asrc	MX83 [12]	0'h	Mode Select Control for I2S2 0'b : Normal Mode 1'b : ASRC Mode
en_if2_asrc	MX84 [14]	0'h	Enable Control for I2S2 0'b: Normal Mode 1'b: ASRC Mode
sel_dmic1_mode	MX83 [9]	0'h	Select Control for ASRC Mode in DMIC1 Function 0'b : Normal Mode 1'b : ASRC Mode

7.2. Clock setting

Although ASRC support asynchronous MCLK , it still need to be limited at a clock range about 384Fs~768Fs (Fs =

sample rate) . If the MCLK is too fast for system clock, customer can use the divider to let the system clock meet the ASRC support clock range.

Name	Bits	Default value	Function Description
i2s1_track_prediv	MX89 [14:12]	0'h	Set I2S1 Clock Division for Stereo Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16
i2s2_track_prediv	MX89 [10:8]	0'h	Set I2S2 Clock Division for Mono Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16

8. Audio H/W Processing

ALC5651 provides 7 band EQ for DAC or ADC, 1 wind filter for ADC and SounzReal Sound effect as Audio H/W Processing.

8.1. Power

The Register shown as below has to be set in order to enable H/W Processing.

Control Register	Reg	Value	Description	Note
Pow_bg_bias	MX63[11]	1'b	Power On MBIAS Bandgap	
Pow_vref1	MX63[15]	1'b	Power On Vref1	
Pow_main_bias	MX63[13]	1'b	Power On Main Bias	
Pow_vref2	MX63[4]	1'b	Power On Vref2	
Pow_dac_l_1	MX61[12]	1'b	Power On left DAC1	Depend on path
Pow_dac_r_1	MX61[11]	1'b	Power On right DAC1	Depend on path
Pow_adc_l	MX61[2]	1'b	Power On left ADC	Depend on path
Pow_adc_r	MX61[1]	1'b	Power On right ADC	Depend on path
En_i2s1	MX61[15]	1'b	Enable I2S1 Digital interface	

digital_gate_ctrl	MXFA[0]	1'b	Enable MCLK input	
Ckxen_dac	PR3D[10]	1'b	Enable DAC Clock1 Generator	Depend on path
En_ckgen_dac	PR3D[9]	1'b	Enable DAC Clock2 Generator	Depend on path
en_ckgen_adc	PR3D[12]	1'b	Enable ADC clock input	Depend on path

8.2.7-band EQ Control

ALC5651 has 7 band EQ which can be applied both on DAC or ADC. The 7 band EQ contains LPF, BPF1, BPF2, BPF3, BPF4, HPF1 and HPF2. Each band can be disabled separately. In addition, there is a Max. -66dB attenuator in front of EQ block and a Max. +24dB gain in rear of EQ block to avoid clamping during EQ processing. Realtek provides **EQ Tool.exe** to our customer in order to generate customized EQ parameter. The following register can be fully set according to the parameter that suggested by **EQ Tool.exe**. After setting the EQ parameter, customer need to load the parameter to each filter by setting MXB0[14] to 1. Customer can load the EQ parameter to filter dynamically.

Name	Bits	Default value	Function Description
eq_sour	MXB0 [15]	0'b	EQ Path Control 0'b: DAC path 1'b: ADC path
reg_typ_hpf_en	MXB1 [8]	0'b	EQ High Pass Filter 1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
reg_typ_lpf_en	MXB1 [7]	0'b	EQ Low Pass Filter Mode Control 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
en_hpf2	MXB1 [6]	0'b	EQ High Pass 2nd Butterworth Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_hpf1	MXB1 [5]	0'b	EQ High Pass Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_bpf4	MXB1 [4]	0'b	EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.

en_bpf3	MXB1 [3]	0'b	EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf2	MXB1 [2]	0'b	EQ Band-2 (BP2) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf1	MXB1 [1]	0'b	EQ Band-1 (BP1) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_lpf	MXB1 [0]	0'b	EQ Low Pass Filter (LPF) Filter Control. 0'b: Disabled and reset 1'b: Enabled.
Eq_pre_vol	PrivateB3 [15:0]	0800'h	2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~15.99 [+24dB ~ -66dB]
Eq_post_vol	PrivateB4 [15:0]	0800'h	2's Complement in 5.11 Format. (Default is 0dB) The range is from -16 ~ 15.99, pre-gain should be in 0 ~15.99 [+24dB ~ -66dB]

8.2.1. LP0

Name	Bits	Default value	Function Description
lpf_a1	PrivateA0 [15:0]	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
lpf_h0	PrivateA1 [15:0]	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.2. BP1

Name	Bits	Default value	Function Description
Bpf1_a1	PrivateA2 [15:0]	C5E9'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf1_a2	PrivateA3	1A98'h	2's complement in 3.13 format. (The range is

	[15:0]		from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf1_h0	PrivateA4 [15:0]	1D2C'h	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.3. BP2

Name	Bits	Default value	Function Description
Bpf2_a1	PrivateA5 [15:0]	C882'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf2_a2	PrivateA6 [15:0]	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf2_h0	PrivateA7 [15:0]	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.4. BP3

Name	Bits	Default value	Function Description
Bpf3_a1	PrivateA8 [15:0]	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf3_a2	PrivateA9 [15:0]	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf3_h0	PrivateAA [15:0]	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.5. BP4

Name	Bits	Default value	Function Description
Bpf4_a1	PrivateAB	E904'h	2's complement in 3.13 format. (The range is

	[15:0]		from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf4_a2	PrivateAC [15:0]	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Bpf4_h0	PrivateAD [15:0]	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.6. HPF1

Name	Bits	Default value	Function Description
Hpf1_a1	PrivateAE [15:0]	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Hpf1_h0	PrivateAF [15:0]	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.7. HPF2

Name	Bits	Default value	Function Description
Hpf2_a1	PrivateB0 [15:0]	C01E’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Hpf2_a2	PrivateB1 [15:0]	1FE2’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)
Hpf2_h0	PrivateB2 [15:0]	1FF1’h	2’s complement in 3.13 format. (The range is from –4~3.99, the Ho should be in -4 ~ 3.99)

8.2.8. EQ volume

Name	Bits	Default	Function Description

		value	
Eq_pre_vol	PrivateB3 [15:0]	0800'h	2's Complement in 5.11 Format. (Default is 0dB)The range is from -16 ~ 15.99, pre-gain should be in 0 ~15.99 [+24dB ~ -66dB]
Eq_post_vol	PrivateB4 [15:0]	0800'h	2's Complement in 5.11 Format. (Default is 0dB)The range is from -16 ~ 15.99, pre-gain should be in 0 ~15.99 [+24dB ~ -66dB]

8.3. EQ setting example

For setting the EQ parameter , there is a register setting sequence of ALC5651.
The setting sequence should be as below:

Step1: Power on main bias , MX63[11][13] : 11'b

Step2: Power on I2S interface , MX61[15] : 1'b

Step3: Power on left/right DAC , MX61[12:11] : 11'b
(or left/right ADC , MX61[2:1] : 11'b)

Step4:set the EQ parameter to register , PR-A0~ PR-B4

Step5: Enable EQ block , MX-B1[8:0]

Step6: Update EQ parameter , MX-B0[14] : 1'b

Step7:EQ parameter setting finish

8.4. Wind Filter

The wind filter is implemented by a high pass filter equalizer. The wind filter is mainly for ADC recording used. The cut-off frequency of wind filter is programmable and is varied according to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode.

The following table is shown the Fc with sample rate selection.

For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
Sample rate = 8K/12K/16K (MX-D3[14:12] & [10:8]), $a = 2^{-6} + n * 2^{-6}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 24K/32K (MX-D3[14:12] & [10:8]), $a = 2^{-7} + n * 2^{-7}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 44.1K/48L (MX-D3[14:12] & [10:8]), $a = 2^{-8} + n * 2^{-8}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 88.2K/96L (MX-D3[14:12] & [10:8]), $a = 2^{-9} + n * 2^{-9}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 176.4K/192L (MX-D3[14:12] & [10:8]), $a = 2^{-10} + n * 2^{-10}$ (n is MX-D4[13:8] & [5:0])

Name	Bits	Default value	Function Description

adj_hpf_2nd_en	MXD3 [15]	0’h	Enable Adjustable 2nd Wind Filter 0'b : Disable (bypass mode) 1'b : Enable
adj_hpf_coef_l_sel	MXD3 [14:12]	3’h	Left Channel Coefficient Sample Rate Selection 000'b: 8K/12K/16K Hz 001'b: 24K/32K Hz 010'b: 48K/44.1K Hz 011'b: 96K/88.2K Hz 100'b: 192K/176.4K Hz Others: Reserved
adj_hpf_coef_r_sel	MXD3 [10:8]	2’h	Right Channel Coefficient Sample Rate Selection 000'b: 8K/12K/16K Hz 001'b: 24K/32K Hz 010'b: 48K/44.1K Hz 011'b: 96K/88.2K Hz 100'b: 192K/176.4K Hz Others: Reserved
adj_hpf_coef_l_num	MXD4 [13:8]	0’h	Left Channel Coefficient Fine Parameter Selection (0 ~ 63)
adj_hpf_coef_r_num	MXD4 [13:8]	0’h	Right Channel Coefficient Fine Parameter Selection (0 ~ 63)

MX-D4n	**L & R Channel Sample Rate Setting**				
	8K	**16K**	**32K**	**44.1K**	**48K**
000000’b, 0	20.0	40.1	39.9	27.4	29.8
000001’b, 1	40.4	80.8	80.2	55.0	59.9
000010’b, 2	61.1	122.2	120.7	82.7	90.0
000011’b, 3	82.1	164.2	161.6	110.5	120.3
000100’b, 4	103.4	206.9	202.8	138.4	150.6
000101’b, 5	125.1	250.2	244.4	166.4	181.1
000110’b, 6	147.1	294.3	286.2	194.5	211.7
000111’b, 7	169.5	339.0	328.4	222.7	242.5
001000’b, 8	192.2	384.4	371.0	251.1	273.3
001001’b, 9	215.2	430.5	413.8	279.5	304.3
001010’b, 10	238.7	477.4	457.0	308.1	335.4
001011’b, 11	262.4	524.9	500.5	336.8	366.6
001100’b, 12	286.6	573.2	544.4	365.6	397.9
001101’b, 13	311.1	622.3	588.6	394.5	429.4
001110’b, 14	336.0	672.1	633.2	423.5	460.9
001111’b, 15	361.3	722.6	678.1	452.6	492.6
010000’b, 16	386.9	773.9	723.3	481.9	524.5
010001’b, 17	413.0	826.0	768.9	511.2	556.4

MX-D4	L & R Channel Sample Rate Setting				
n	8K	16K	32K	44.1K	48K
010010’b, 18	439.4	878.9	814.9	540.7	588.5
010011’b, 19	466.2	932.5	861.2	570.3	620.7
010100’b, 20	493.5	987.0	907.8	600.0	653.0
010101’b, 21	521.1	1042.2	954.9	629.8	685.5
010110’b, 22	549.1	1098.2	1002.2	659.7	718.1
010111’b, 23	577.5	1155.0	1050.0	689.8	750.8
011000’b, 24	606.3	1212.7	1098.1	719.9	783.6
011001’b, 25	635.5	1271.1	1146.6	750.2	816.6
011010’b, 26	665.1	1330.3	1195.5	780.6	849.6
011011’b, 27	695.2	1390.4	1244.7	811.1	882.9
011100’b, 28	725.6	1451.2	1294.3	841.8	916.2
011101’b, 29	756.4	1512.9	1344.3	872.5	949.7
011110’b, 30	787.6	1575.3	1394.7	903.4	983.3
011111’b, 31	819.3	1638.6	1445.4	934.4	1017.0
100000’b, 32	851.3	1702.7	1496.5	965.5	1050.9
100001’b, 33	883.7	1767.5	1548.0	996.8	1084.9
100010’b, 34	916.6	1822.3	1599.9	1028.1	1119.0
100011’b, 35	949.8	1899.6	1652.2	1059.6	1153.3
100100’b, 36	983.3	1966.7	1704.9	1091.2	1187.7
100101’b, 37	1017.3	2034.7	1757.9	1122.9	1222.2
100110’b, 38	1051.6	2103.3	1811.4	1154.8	1256.9
100111’b, 39	1086.3	2172.7	1865.2	1186.7	1291.7
101000’b, 40	1121.4	2242.9	1919.5	1218.8	1326.6
101001’b, 41	1156.8	2313.7	1974.1	1251.0	1361.7
101010’b, 42	1192.6	2385.2	2029.1	1283.4	1396.9
101011’b, 43	1228.7	2457.4	2084.6	1315.8	1432.2
101100’b, 44	1265.1	2530.2	2140.4	1348.4	1467.7
101101’b, 45	1301.8	2603.6	2196.6	1381.1	1503.3
101110’b, 46	1338.8	2677.7	2253.3	1414.0	1539.0
101111’b, 47	1376.1	2752.3	2310.3	1447.0	1574.9
110000’b, 48	1413.7	2827.5	2367.7	1480.0	1610.9
110001’b, 49	1451.5	2903.1	2425.5	1513.3	1647.1
110010’b, 50	1489.6	2979.3	2483.8	1546.6	1683.4
110011’b, 51	1528.0	3056.0	2542.4	1580.1	1719.8
110100’b, 52	1566.5	3133.1	2601.5	1613.7	1756.4
110101’b, 53	1605.3	3210.6	2660.9	1647.4	1793.1
110110’b, 54	1644.2	3288.4	2720.8	1681.3	1830.0
110111’b, 55	1683.3	3366.6	2781.0	1715.3	1867.0
111000’b, 56	1722.5	3445.1	2841.7	1749.4	1904.1

MX-D4 n	L & R Channel Sample Rate Setting				
	8K	16K	32K	44.1K	48K
111001'b, 57	1761.9	3523.9	2902.7	1783.6	1941.4
111010'b, 58	1801.4	3602.9	2964.2	1818.0	1978.8
111011'b, 59	1841.0	3682.1	3026.1	1852.5	2016.3
111100'b, 60	1880.7	3761.4	3088.3	1887.1	2054.0
111101'b, 61	1920.4	3840.8	3151.0	1921.9	2091.9
111110'b, 62	1960.2	3920.4	3214.1	1956.8	2129.9
111111'b, 63	2000.0	4000.0	3277.5	1991.8	2168.0

8.5. Wind Filter setting procedure

Step1: Disable wind filter – MX-D3[15]

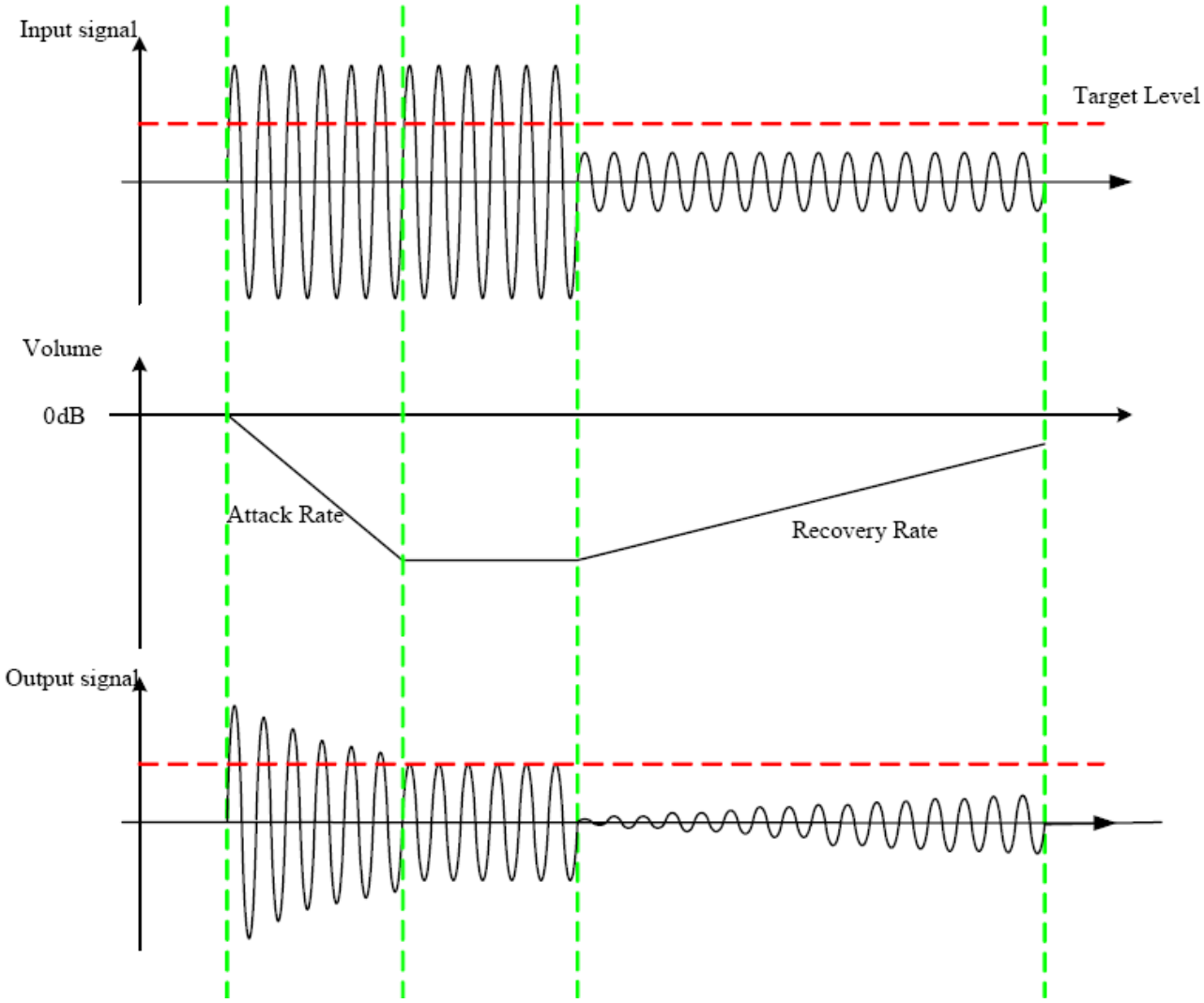
Step2: Select target sample rate – MX-D3[14:12] and MX-D3[10:8]

Step3: Fine tune wind filter Fc – MX-D4[13:8] and MX-D4[5:0]

Step4: Enable wind filter – MX-D3[15]

9. DRC/AGC

The behavior of DRC/AGC function is shown in the picture as bellow:



9.1. DRC/AGC relative parameter register setting

DRC/AGC can be disabled and enabled by register control. And the noise gate function in AGC can also be disabled or enabled individually. The DRC/AGC function also needs to change the register setting when using different sampling rate.

The default setting is for 48k Hz sampling rate.

Name	Bits	Default value	Function Description
sel_drc_agc	MXB4 [15:14]	0'h	DRC/AGC Enable 00'b: Disable DRC/AGC 01'b: Enable DRC to DAC Path 10'b: Disable DRC/AGC 11'b: Enable AGC to ADC Path
Drc_agc_rate_sel	MXB4 [7:5]	0'h	DRC/AGC Rate Control for Sample Rate Change 001'b: 48kHz 010'b: 96kHz 011'b: 192kHz 101'b: 44.1kHz 110'b: 88.2kHz 111'b: 176.4kHz Others: Reserved

9.1.1. Limit level

AGC/DRC has a target level which can be controlled by register setting. For DAC playback or ADC recording mode, when the input signal exceeds target threshold, the signal will decrease "DRC/AGC Digital Volume" (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up "DRC/AGC Digital Volume" (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

Name	Bits	Default value	Function Description
sel_drc_agc_thmax	MXB6 [11:7]	0'h	DRC/AGC Limiter Level (1.5dB/step) 00'h= 0dBFS 01'h= -1.5dBFS 02'h= -3dBFS 03'h= -4.5dBFS … 1F'h= -46.5dBFS
sel_drc_agc_pre_bst	MXB5 [4:0]	0'h	DRC/AGC Digital Pre-Boost GAin (1.5dB/step) 00'h= 0dB 01'h= 1.5dB 02'h= 3dB

			03’h= 4.5dB …….. 13’h= 28.5dBFS Others: Reserved
sel_drc_agc_post_bst	MXB5 [13:8]	1f’h	DRC/AGC Digital Post-Boost Gain (0.375dB/step) 00’h= -11.625dB …….. 3F’h= 12dB Others: Reserved

9.1.2. Noise gate

When input signal is below noise gate, the input signal will be reduced and to suppress the background noise. The reducing level can be set by register. And when input signal is above noise gate, the input signal will be boosted to target level.

The noise gate function is only suggested to use in record AGC function, and customer can disable it when playback DRC.

Name	Bits	Default value	Function Description
en_drc_agc_noise_gate	MXB6 [6]	0’h	Enable Noise Gate function 0’b: Diaable 1’b: Enable
sel_drc_agc_noise_th	MXB6 [4:0]	0’h	Noise Gate Threshold (-1.5dB/step) 00’h: -36dBFS 01’h: -37.5 dBFS …….. 1F’h: -82.5 dBFS
Noise_gate_boost	MXB6 [15:12]	0’h	Select Compensation Gain When Signal is Below Noise Gate 0’h: 0dB 1’h: 3dB 2’h: 6dB … E’h: 42dB F’h: 45dB

9.1.3. Attack and Recovery Time

The AGC/DRC function can modify the attack and recovery time by register setting. The attack time is for speed of the decreasing gain, and the recovery time is for the speed of the increasing gain.

The attack and recovery time are relative to the sampling rate, and the formula is shown as below:

Name	Bits	Default value	Function Description
sel_drc_agc_atk	MXB4 [12:8]	2'h	Select DRC/AGC attack rate (0.375dB/TU) ❶ 00'h: 83 uSec 01'h: 0.167 mSec … 10'h: 5.46 Sec Others: Reserved
sel_rc_rate	MXB4 [4:0]	6'h	Select DRC/AGC recovery rate (0.375dB/TU)❷ 00'h: 83 uSec 01'h: 0.167 mSec … 10'h: 5.46 Sec Others: Reserved

Note: ❶Attack time = (4*2^n)/Sample Rate, n = Reg64[12:8], default=0.33mS, Sample Rate = 48kHz

❷Recovery time = (4*2^n)/Sample Rate, n = Reg64[4:0], default=5.3mS, Sample Rate = 48kHz

9.1.4. DRC Compressor

For the Noise Gate function is used to make sound smooth and comfortable when transition from normal mode into Limiter mode. The ALC5651 has four segments Compressor ratio for tuning.

The ratio 1:1 is mean:

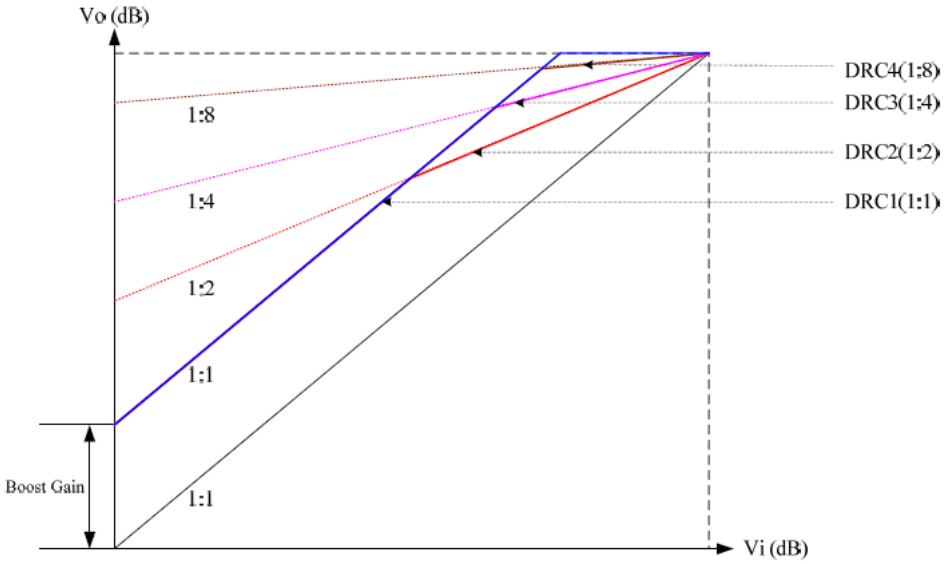
output level = input level * speaker ratio gain

The output level is equal to input level multiply by speaker ratio gain. That is no compression in DRC1

The ratio 1:2 is mean:

output level = input level/2 * speaker ratio gain

The output level is equal to input level divide by 2 then multiply by speaker ratio gain. So the output with input has 2 multiples compression in DRC2.



Name	Bits	Default value	Function Description
En_drc_agc_compress	MXB5 [7]	0'h	DRC Compression Function Control 0'b: Disable 1'b: Enable
Sel_ratio	MXB5 [6:5]	0'h	DRC Compression Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:3 11'b: 1:4

9.1.5. Parameter update

After setting the DRC/AGC parameter, user need to set MXB4 [13]:1'b to update all the DRC/AGC parameter.

Name	Bits	Default value	Function Description
update_drc_agc_param	MXB4 [13]	1'h	Update DRC/AGC Parameter Write 1'b to update all DRC/AGC parameter

10. Jack Detection

ALC5651 supports Jack detect function to switch ON/OFF the analog Output and PDM Output (Headphone Out...etc) by setting MX-BB Jack Detect Control Register. The Jack detect source can be GPIO1~GPIO6 , JD1 or JD2. JD2 is pin shared from IN2N.

User should decide the JD pin source from GPIO or JD1 JD2 first by setting **Sel_jd_trigger** .If user decide to use GPIO pin for jack detection , please select the GPIO by **sel_gpio_jd** .

Name	Bits	Default value	Function Description
Sel_jd_trigger	MXBC [11:9]	0'h	JD Trigger Source Selection 000'b: From sta_gpio_jd 001'b: From sta_jd1_1 010'b: From sta_jd1_2 011'b: From sta_jd2 Others: Reserved
sel_gpio_jd	MXBB [15:13]	0'h	Jack Detect Selection 000'b: OFF 001'b: GPIO1 010'b: GPIO2 011'b: GPIO3 100'b: GPIO4 101'b: GPIO5 110'b: GPIO6 Others: Reserved
en_jd_hpo	MXBB [11]	0'h	Enable Jack Detect Trigger HPOUT 0'b: Disable 1'b: Enable
polarity_jd_tri_hpo	MXBB [10]	0'h	Select Jack Detect Polarity Trigger HPOUT 0'b: Low trigger 1'b: High trigger
en_jd_pdm_l	MXBB [9]	0'h	Enable Jack Detect Trigger PDM_L 0'b: Disable 1'b: Enable
polarity_jd_tri_pdm_l	MXBB [8]	0'h	Select Jack Detect Polarity Trigger PDM_L 0'b: Low trigger 1'b: High trigger
en_jd_pdm_r	MXBB [7]	0'h	Enable Jack Detect for Trigger S PDM_ R 0'b: Disable 1'b: Enable
polarity_jd_tri_pdm_r	MXBB [6]	0'h	Select Jack Detect Polarity Trigger PDM_ R 0'b: Low trigger 1'b: High trigger

en_jd_lout	MXBB [3]	0'h	Enable Jack Detect Trigger LOUT 0'b: Disable 1'b: Enable
polarity_jd_tri_lout	MXBB [2]	0'h	Select Jack Detect Polarity Trigger LOUT 0'b: Low trigger 1'b: High trigger

10.1. JD setting example

For example, HP and LOUT auto switch when JD is trigger **.**

Setting procedure:

1. **Select JD source: use sta_jd1_1 as JD status. MX-BC[11:9] = 001'b**
2. **Set target behavior by JD active – HP & LOUT auto switch when JD is triggered.**
   MX-BB[11:10] = 11'b & MX-BB[3:2] = 10'b
3. **When JD status is low, HP_OUT is mute and LOUT is un-mute.**
   When JD status is low go high, HP is un-mute and LOUT is mute.

Note: For HP and SPK jack switch function, driver need to turn-on DAC to HP path and DAC to LOUT path first. The register control of MX-BB is only do mute/un-mute function for HP and SPK.

11. GPIO & IRQ

Pin 24~29&37,38 of ALC5651 can be pin share to DMIC_SCL, DMIC_SDA, GPIO ,PDM and IRQ.

11.1. Initial

When **sel_gpio1_type** =”0’b”, Pin 37 is assigned to GPIO1

sel_gpio1_type =”1’b”, Pin 37 is assigned to IRQ

Control Register	Reg	Value	Description	Note
sel_gpio1_type	MXC0[15]	0’b	As GPIO1	
sel_gpio1_type	MXC0[15]	1’b	As IRQ	

When **sel_gpio2_type** =”0’b”, Pin 38 is assigned to GPIO2

sel_gpio2_type =”1’b”, Pin 38 is assigned to DMIC_SCL

Control Register	Reg	Value	Description	Note
sel_gpio2_type	MXC0[14]	0’b	As GPIO2	
sel_gpio2_type	MXC0[14]	1’b	As DMIC_SCL	

When **Sel_i2s_pin** =”1’b”, Pin 29 is assigned to GPIO3 , Pin 28 is assigned to GPIO4

Sel_ i2s_pin =”0’b”, Pin 29 28 is assigned to I2S2 signal

Control Register	Reg	Value	Description	Note
Sel_i2s_pin	MXC0[8]	0’b	As I2S2	
Sel_i2s_pin	MXC0[8]	1’b	As GPIO3 GPIO4	

When **Sel_i2s_pin** =”1’b” & **sel_gpio5_type** =”0’b”, Pin 27 is assigned to GPIO5

Sel_ i2s_pin =”1’b” & **sel_gpio5_type** =”1’b”, Pin 27 is assigned to IRQ

Sel_ i2s_pin =”0’b”, Pin 27 is assigned to I2S2 signal

Control Register	Reg	Value	Description	Note
Sel_i2s_pin & sel_gpio5_type	MXC0[8:7]	10’b	As GPIO5	
Sel_i2s_pin & sel_gpio5_type	MXC0[8:7]	11’b	As IRQ	
Sel_i2s_pin	MXC0[8]	0’b	As I2S2	

When **Sel_i2s_pin** =”1’b” & **sel_gpio6_type** =”0’b”, Pin 26 is assigned to GPIO6

Sel_ i2s_pin =”1’b” & **sel_gpio6_type** =”1’b”, Pin 26 is assigned to DMIC_SDA

Sel_ i2s_pin =”0’b”, Pin 26 is assigned to I2S2 signal

Control Register	Reg	Value	Description	Note
Sel_i2s_pin & sel_gpio6_type	MXC0[8][6]	[1’b][0’b]	As GPIO6	
Sel_i2s_pin & sel_gpio6_type	MXC0[8][6]	[1’b][1’b]	As DMIC_SDA	
Sel_i2s_pin	MXC0[8]	0’b	As I2S2	

When **sel_gpio_pdm** =”1’b” & **sel_gpio7_type** =”0’b”, Pin 24 is assigned to GPIO7

sel_gpio_pdm =”1’b” & **sel_gpio7_type** =”1’b”, Pin 24 is assigned to IRQ

sel_gpio_pdm =”0’b”, Pin 24 is assigned to PDM_SDA signal

Control Register	Reg	Value	Description	Note
sel_gpio_pdm & sel_gpio7_type	MXC0[3][5]	[1’b][0’b]	As GPIO7	
sel_gpio_pdm & sel_gpio7_type	MXC0[3][5]	[1’b][1’b]	As IRQ	
sel_gpio_pdm	MXC0[3]	0’b	As PDM_SDA	

When **sel_gpio_pdm** =”1’b” & **sel_gpio8_type** =”0’b”, Pin 25 is assigned to GPIO8

sel_gpio_pdm =”1’b” & **sel_gpio8_type** =”1’b”, Pin 25 is assigned to DMIC_SDA

sel_gpio_pdm =”0’b”, Pin 25 is assigned to PDM_SCL signal

Control Register	Reg	Value	Description	Note
sel_gpio_pdm & sel_gpio8_type	MXC0[3][4]	[1’b][0’b]	As GPIO8	
sel_gpio_pdm & sel_gpio8_type	MXC0[3][4]	[1’b][1’b]	As DMIC_SDA	
sel_gpio_pdm	MXC0[3]	0’b	As PDM_SCL	

11.2. GPIO & IRQ Control

ALC5651 GPIO can be configured As Input/ Output by MXC1 & MXC2. When GPIO is configured as Output, MXC1&MXC2 can also used to Drive GPIO to High (1'b) or Low (0'b). The status can be read in MXBF[11:4]. Independent to GPIO, there are some Internal Event Signals (Jack Detection, Over temperature and MICBIAS short detect) which is the same as GPIO input and can be treat as Interrupts source. The application of Internal Event Signal is the same as GPIO and located in MXBD MXBE MXBF.

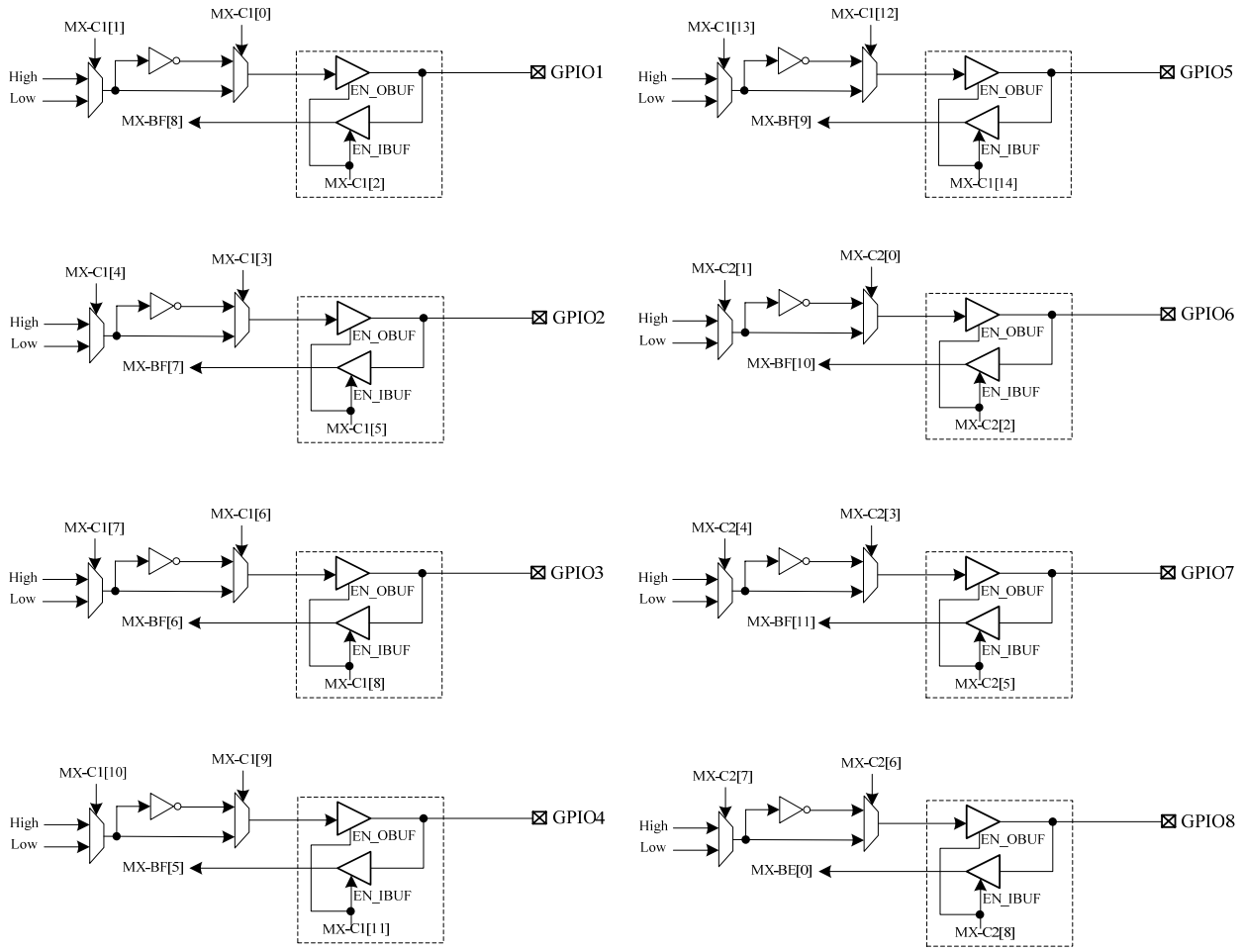


Figure1.GPIO function block

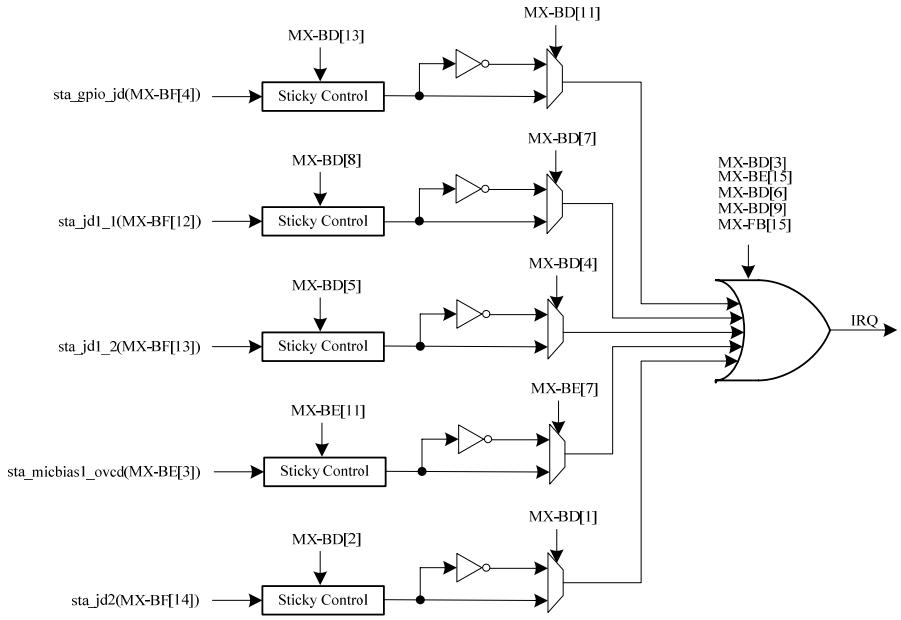


Figure2.IRQ function block

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