1. Description

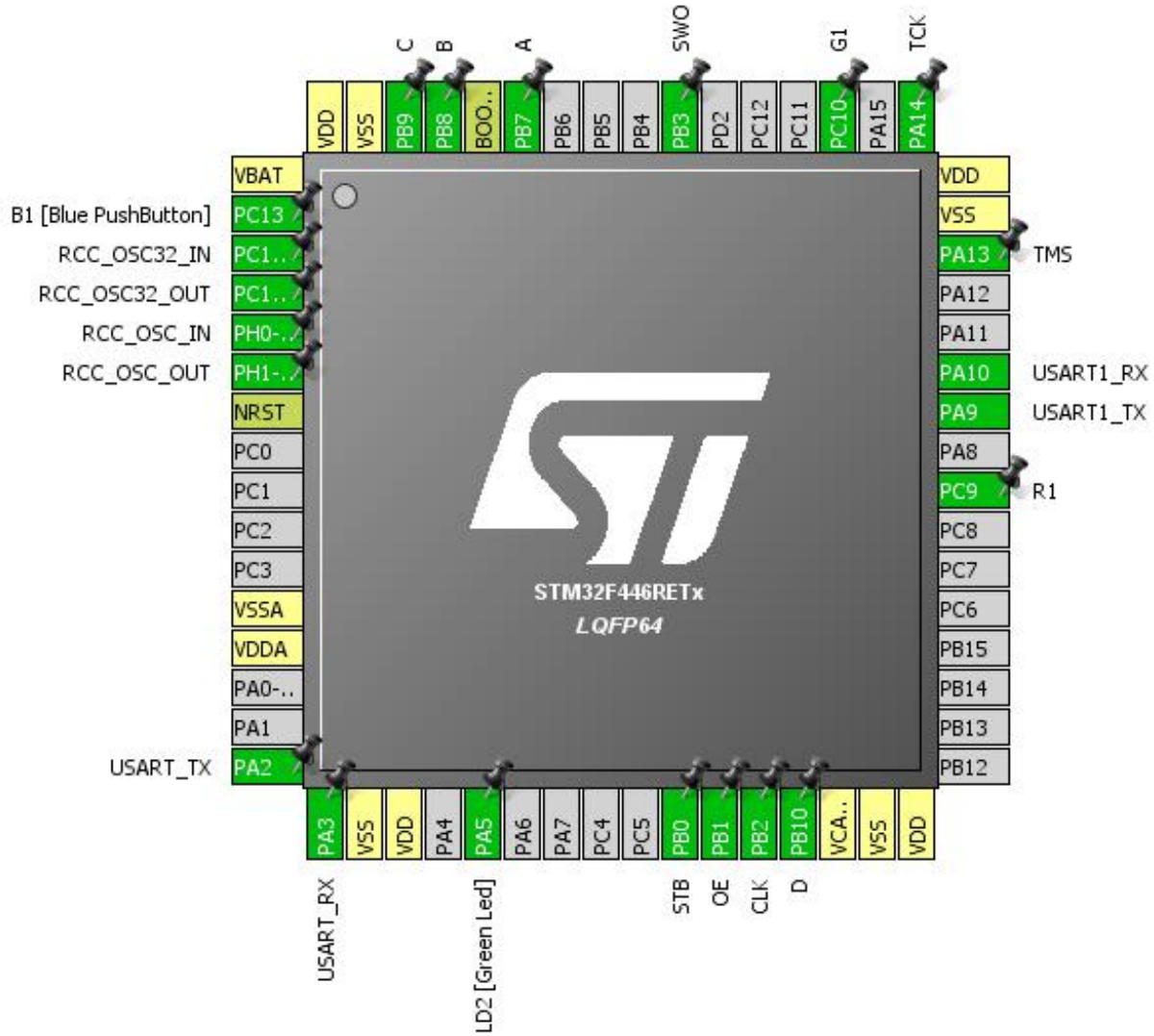
1.1. Project

Project Name	MatrixF446_rtos
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 4.25.1
Date	05/30/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration

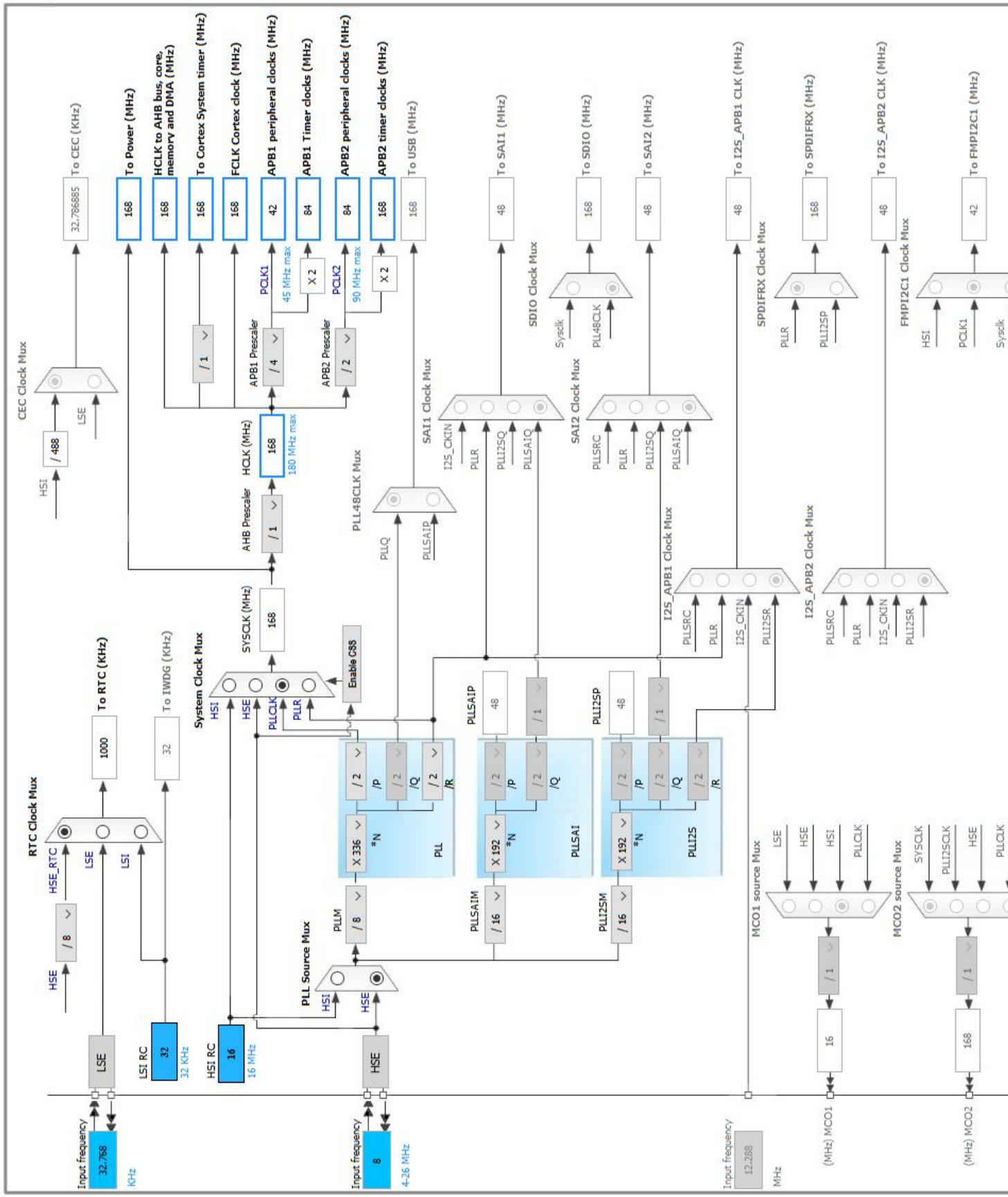


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
26	PB0 *	I/O	GPIO_Output	STB
27	PB1 *	I/O	GPIO_Output	OE
28	PB2 *	I/O	GPIO_Output	CLK
29	PB10 *	I/O	GPIO_Output	D
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
40	PC9 *	I/O	GPIO_Output	R1
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10 *	I/O	GPIO_Output	G1
55	PB3	I/O	SYS_JTDO-SWO	SWO
59	PB7 *	I/O	GPIO_Output	A
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Output	B
62	PB9 *	I/O	GPIO_Output	C
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: Temperature Sensor Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel Temperature Sensor
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.3. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm

5.3.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	**63 ***
Synchronous Predivider value	**15624 ***

Calendar Time:

Data Format	BCD data format
Hours	**12 ***
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1

Year	**18 ***

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

5.4. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM1

5.5. TIM3

Clock Source : Internal Clock

Channel1: Output Compare No Output

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**42 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High

5.6. TIM8

Clock Source : Internal Clock

Channel1: Output Compare No Output

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	**Down ***
Counter Period (AutoReload Register - 16 bits value)	**42 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare No Output Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.7. USART1

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.8. USART2

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. FREERTOS

mode: Enabled

5.9.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	**Disabled ***
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	**Enabled ***
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	USART_RX
GPIO	PC13	GPIO_EXTI13	**External Event Mode with Falling edge trigger detection ***	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	STB
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	OE
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CLK
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	D

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	R1
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	G1
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	A
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	B
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	C

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable

Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
RCC global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
TIM3 global interrupt	true	5	0
USART1 global interrupt	true	5	0
RTC alarms A and B interrupt through EXTI line 17	true	5	0
TIM8 capture compare interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
USART2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	027107_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	MatrixF446_rtos
Project Folder	C:\Users\fzs\Documents\git\MatrixF446_rtos
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.21.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report